LP2989LV Micropower 500 mA Low Noise Low Dropout Regulator for Applications with Output Voltages < 2V

Designed for Use with Very Low ESR Output Capacitors

Check for Samples: LP2989LV

FEATURES

- **Ultra Low Dropout Voltage**
- **Ensured 500 mA Continuous Output Current**
- **Very Low Output Noise with External Capacitor**
- **SOIC-8, VSSOP, 8 Lead WSON Surface Mount Packages**
- **<0.8 µA Quiescent Current when Shut Down**
- **Low Ground Pin Current at All Loads**
- **0.75% Output Voltage Accuracy ("A" Grade)**
- **High Peak Current Capability (800 mA Typical)**
- **Wide Supply Voltage Range (16V Max)**
- **Overtemperature/Overcurrent Protection**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **Notebook/Desktop PC**
- **PDA/Palmtop Computer**
- **Wireless Communication Terminals**
- **SMPS Post-Regulator**

DESCRIPTION

The LP2989LV is a 500 mA fixed-output voltage regulator designed to provide high performance and low noise in applications requiring output voltages < 2V.

Output noise can be reduced to 18µV (typical) by connecting an external 10 nF capacitor to the bypass pin.

Using an optimized VIP (Vertically Integrated PNP) process, the LP2989LV delivers superior performance:

Ground Pin Current: Typically 3 mA @ 500 mA load, and 110 µA @ 100 µA load.

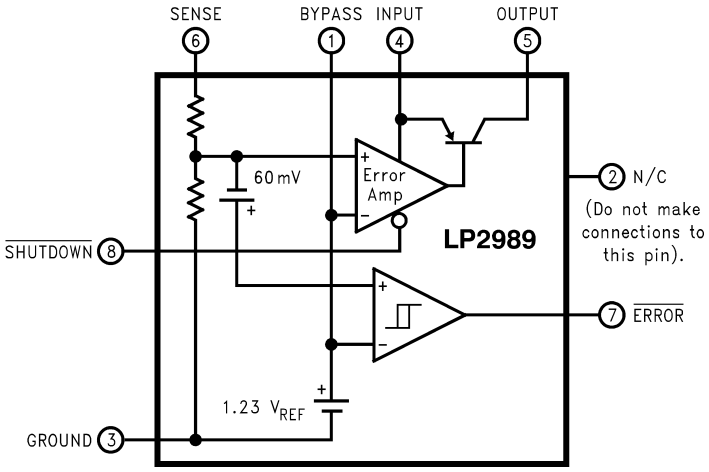
Sleep Mode: The LP2989LV draws less than 0.8 µA quiescent current when shutdown pin is pulled low.

Error Flag: The built-in error flag goes low when the output drops approximately 5% below nominal.

Precision Output: Ensured output voltage accuracy is 0.75% ("A" grade) and 1.25% (standard grade) at room temperature.

For output voltages ≥ 2V, see LP2989 data sheet.

Block Diagram



Connection Diagrams

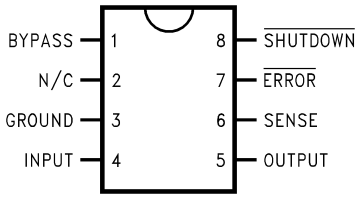


Figure 1. SOIC-8/ VSSOP Package
Surface Mount Packages
See Package Drawing Numbers D0008A/DGK0008A

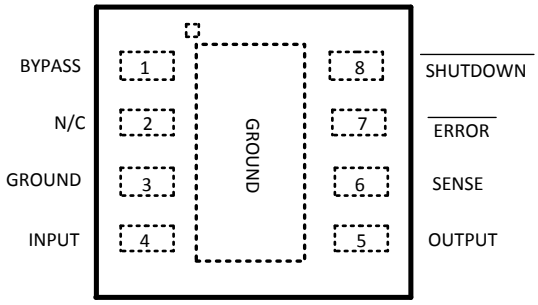
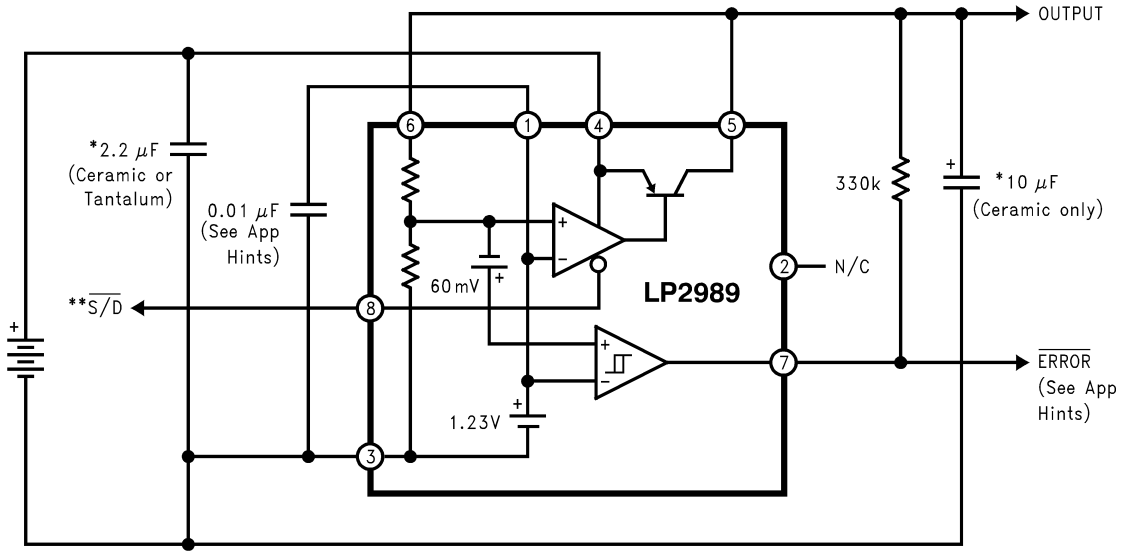


Figure 2. 8 Lead WSON Surface Mount Package
(Top View)
See Package Number NGN0008A

Basic Application Circuit



*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.
**Shutdown must be actively terminated (see APPLICATION HINTS). Tie to INPUT (Pin4) if not used.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating(3)	2 kV
Power Dissipation(4)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
Sense Pin	−0.3V to +6V
Output Voltage (Survival)(5)	−0.3V to +16V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival)(6)	−0.3V to +16V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ESD testing was performed using Human Body Model, a 100 pF capacitor discharged through a 1.5 kΩ resistor.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

The value of θ_{J-A} for the SOIC-8 (D) package is 160°C/W and the VSSOP (DGK) package is 200°C/W. The value θ_{J-A} for the WSON (NGN) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (SNOA401Q). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2989LV output must be diode-clamped to ground.
(6) The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see APPLICATION HINTS).

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_{OUT} = 10 µF, C_{IN} = 2.2 µF, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typical	LP2989AI-X.X (1)		LP2989I-X.X (1)		Units
				Min	Max	Min	Max	
V_O	Output Voltage Tolerance			−0.75	0.75	−1.25	1.25	%V_{NOM}
		1 mA < I_L < 500 mA $V_O(NOM) + 1V \le V_{IN} \le 16V$		−1.5	1.5	−2.5	2.5	
				−4.0	**2.5**	**−5.0**	**3.5**	
		1 mA < I_L < 500 mA $V_O(NOM) + 1V \le V_{IN} \le 16V$ −25°C ≤ T_J ≤ 125°C		**−3.5**	**2.5**	**−4.5**	**3.5**	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output Voltage Line Regulation	$V_O(NOM) + 1V \le V_{IN} \le 16V$	0.005		0.014		0.014	%/V
					0.032		**0.032**	
$\frac{\Delta V_O}{\Delta I_L}$	Load Regulation	1 mA < I_L < 500 mA	0.4					%V_{NOM}
V_{IN} (min)	Minimum Input Voltage Required To Maintain Output Regulation	V_{OUT} = 1.8 $I_L \le 50$ mA	1.96					V
		V_{OUT} = 1.8 I_L = 250 mA	1.98					
		V_{OUT} = 1.8 I_L = 500 mA	2.11					

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_{OUT} = 10 µF, C_{IN} = 2.2 µF, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typical	LP2989AI-X.X (1)		LP2989I-X.X (1)		Units
				Min	Max	Min	Max	
I_{GND}	Ground Pin Current	I_L = 100 µA	110		175		175	µA
					200		**200**	
		I_L = 200 mA	1		2		2	mA
					3.5		**3.5**	
		I_L = 500 mA	3		6		6	
					9		**9**	
		$V_{S/D}$ < 0.18V	**0.5**		**2**		**2**	µA
		$V_{S/D}$ < 0.4V	0.05		0.8		0.8	
$I_O(PK)$	Peak Output Current	$V_{OUT} \geq V_O(NOM) - 5\%$	800	600		600		mA
$I_O(MAX)$	Short Circuit Current	R_L = 0 (Steady State) (2)	1000					
e_n	Output Noise Voltage (RMS)	BW = 100 Hz to 100 kHz, C_{BYPASS} = .01 µF	18					µV(RMS)
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	f = 1 kHz	60					dB
$\frac{\Delta V_{OUT}}{\Delta T}$	Output Voltage Temperature Coefficient	See (3)	**20**					ppm/°C
SHUTDOWN INPUT								
$V_{S/D}$	S/D Input Voltage	V_H = O/P ON	1.4	**1.6**		**1.6**		V
		V_L = O/P OFF $I_{IN} \leq 2$ µA	0.50		**0.18**		**0.18**	
$I_{S/D}$	S/D Input Current	$V_{S/D}$ = 0	0.001		**−1**		**−1**	µA
		$V_{S/D}$ = 5V	5		**15**		**15**	
ERROR COMPARATOR								
I_{OH}	Output “HIGH” Leakage	V_{OH} = 16V	0.001		1		1	µA
					2		**2**	
V_{OL}	Output “LOW” Voltage	$V_{OUT} = V_O(NOM) - 0.5V$ $I_O(COMP)$ = 150 µA	150		220		220	mV
					350		**350**	
V_{THR} (MAX)	Upper Threshold Voltage		−4.8	−6.0	−3.5	−6.0	−3.5	$\%V_{OUT}$
				−8.3	**−2.5**	**−8.3**	**−2.5**	
V_{THR} (MIN)	Lower Threshold Voltage		−6.6	−8.9	−4.9	−8.9	−4.9	
				−13.0	**−3.0**	**−13.0**	**−3.0**	
HYST	Hysteresis		2.0					

(2) See TYPICAL PERFORMANCE CHARACTERISTICS curves.
(3) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_A = 25°C, C_{OUT} = 10 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, V_{OUT} = 1.8V.

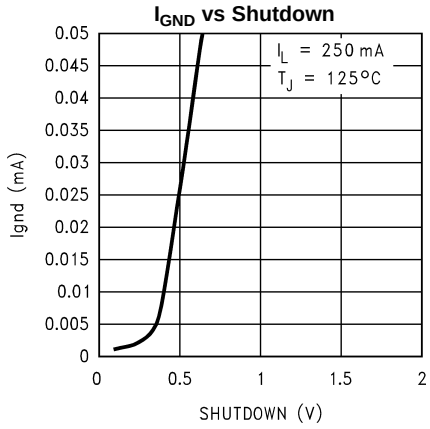


Figure 3.

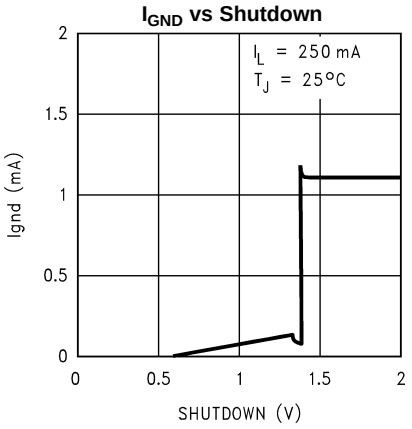


Figure 4.

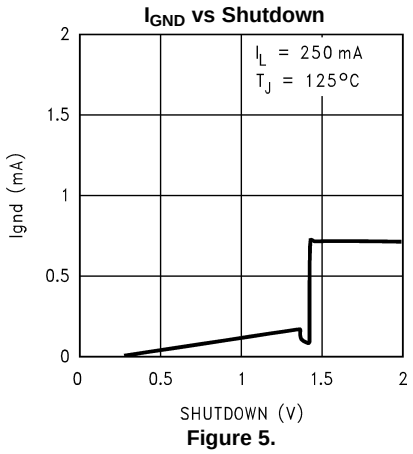


Figure 5.

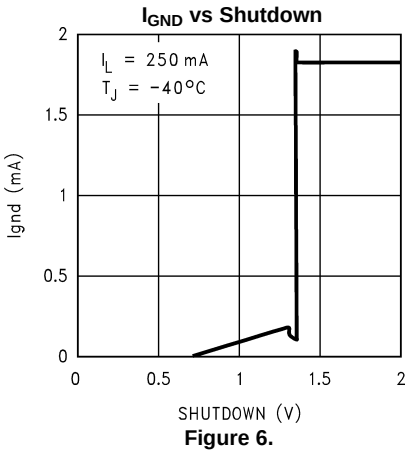


Figure 6.

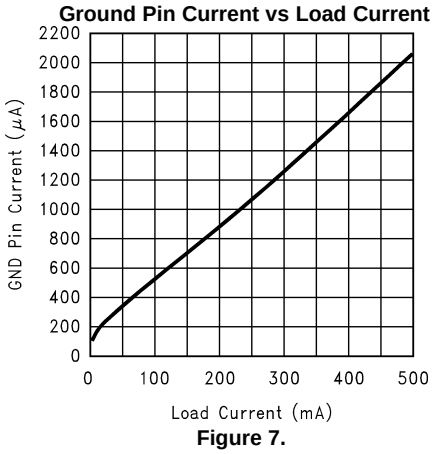


Figure 7.

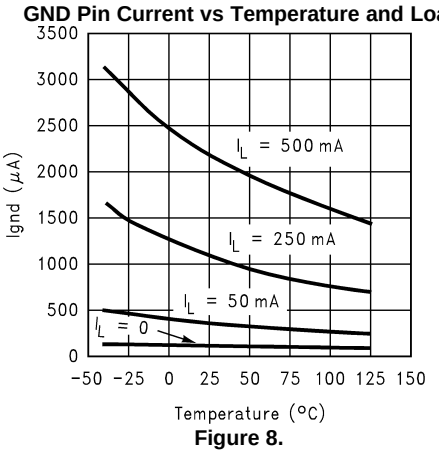


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C, C_{OUT} = 10 µF, C_{IN} = 2.2 µF, S/D is tied to V_{IN}, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, V_{OUT} = 1.8V.

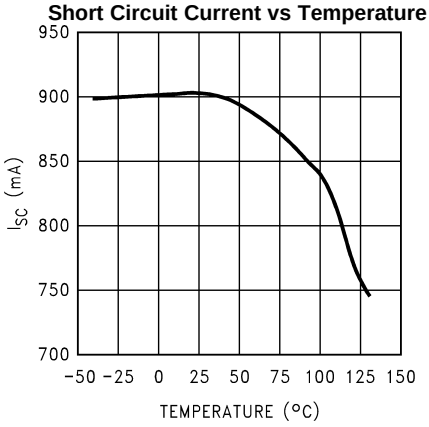


Figure 9.

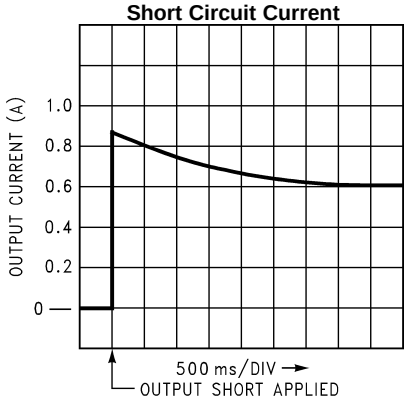


Figure 10.

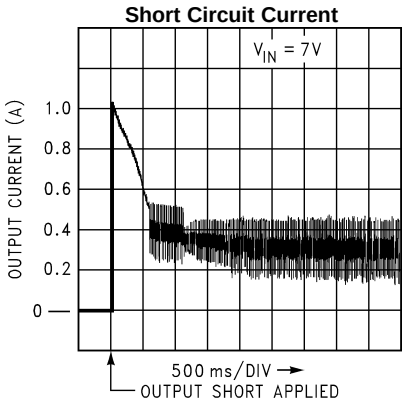


Figure 11.

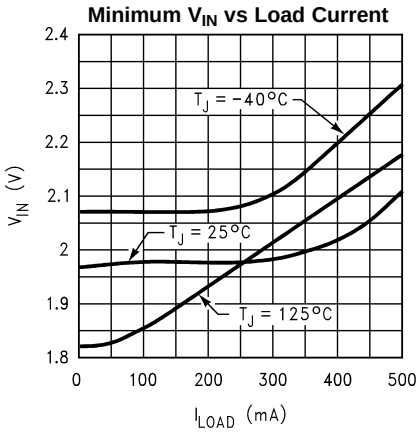


Figure 12.

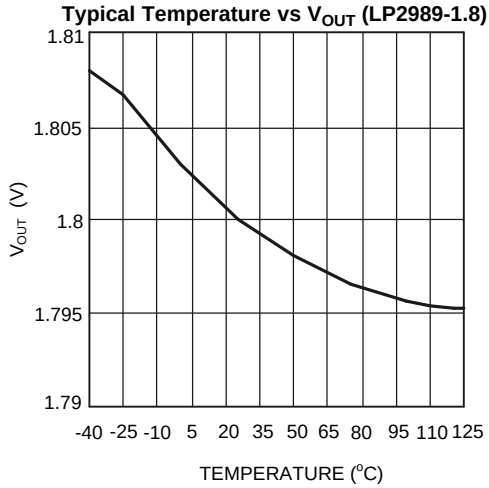


Figure 13.

APPLICATION HINTS

WSON Package Devices

The LP2989LV is offered in the 8 lead WSON surface mount package to allow for increased power dissipation compared to the SOIC-8 and VSSOP. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187 (SNOA401Q).

For output voltages ≥ 2V, see LP2989 data sheet.

External Capacitors

Like any low-dropout regulator, the LP2989LV requires external capacitors for regulator stability.These capacitors must be correctly selected for good performance.

Input Capacitor: An input capacitor whose capacitance is at least 2.2 µF is required between the LP2989LV input and ground (the amount of capacitance may be increased without limit).

Characterization testing performed on the LP2989LV has shown that if the amount of actual input capacitance drops below about 1.5 µF, an unstable operating condition may result. Therefore, the next larger standard size (2.2 µF) is specified as the minimum required input capacitance. Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see Capacitor Characteristics section) to assure the minimum requirement of 1.5 µF is met over all operating conditions.

The input capacitor must be located at a distance of not more than 0.5" from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor, assuming the minimum capacitance requirement is met.

Output Capacitor: The LP2989LV requires a ceramic output capacitor whose size is at least 10 µF. The actual amount of capacitance on the output must never drop below about 7 µF or unstable operation may result. For this reason, capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor

The LP2989LV is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 4 mΩ. It may also be possible to use Tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see Capacitor Characteristics section).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (equivalent series resistance) value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see Figure 14).

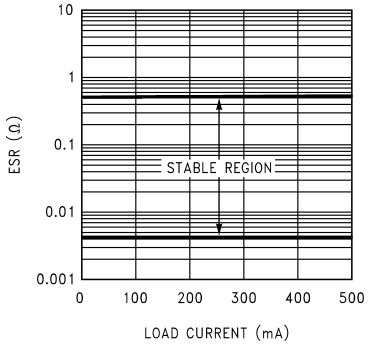


Figure 14. Stable Region For Output Capacitor ESR

Important: The output capacitor must maintain its ESR within the stable region *over the full operating temperature range of the application* to assure stability.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. (See Capacitor Characteristics section.)

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground.

Noise Bypass Capacitor: Connecting a 10 nF capacitor to the Bypass pin significantly reduces noise on the regulator output. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10 nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Capacitor Characteristics

Ceramic: The LP2989LV was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 10 µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 10 µF ceramic capacitor is in the range of 5 mΩ to 10 mΩ, which meets the ESR limits required for stability by the LP2989LV.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 10 µF Y5V capacitor were used on the output since it will drop down to approximately 5 µF at high ambient temperatures (which could cause the LP2989LV to oscillate).

Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP2989LV.

Tantalum: Tantalum output capacitors are not recommended for use with the LP2989LV because:

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are typically more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 10 µF range.

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

Most 10 µF Tantalum capacitors have ESR values higher than the 0.5Ω maximum limit required to make the LP2989LV stable.

It should also be noted that the ESR of a typical Tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

Film: Polycarbonate and polypropelene film capacitors have excellent electrical performance: their ESR is the lowest of the three types listed, their capacitance is very stable with temperature, and DC leakage currrent is extremely low.

One disadvantage is that film capacitors are larger in physical size than ceramic or tantalum which makes film a poor choice for either input or output capacitors.

However, their low leakage makes them a good choice for the noise bypass capacitor. Since the required amount of capacitance is only .01 µF, small surface-mount film capacitors are avalable in this size.

Shutdown Input Operation

The LP2989LV is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the ELECTRICAL CHARACTERISTICS section under $V_{ON/OFF}$.

Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2989LV has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP2989LV to 0.3V (see ABSOLUTE MAXIMUM RATINGS).

REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2989AILD-1.8/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	L01EA	Samples
LP2989AILDX-1.8/NOPB	ACTIVE	WSON	NGN	8	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR		L01EA	Samples
LP2989AIM-1.8	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2989A IM1.8	
LP2989AIM-1.8/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2989A IM1.8	Samples
LP2989AIMX-1.8/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2989A IM1.8	Samples
LP2989ILD-1.8/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	L01EA B	Samples
LP2989ILDX-1.8/NOPB	ACTIVE	WSON	NGN	8	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR		L01EA B	Samples
LP2989IM-1.8	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2989 IM1.8	
LP2989IM-1.8/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2989 IM1.8	Samples
LP2989IMX-1.8/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2989 IM1.8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

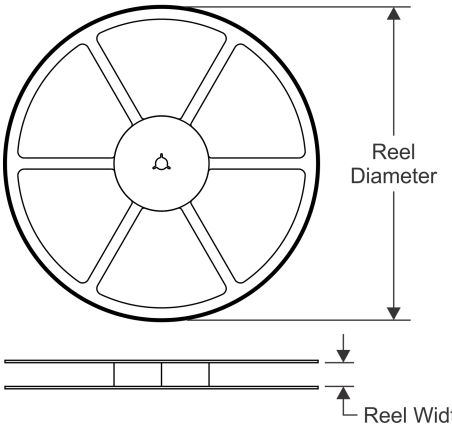
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

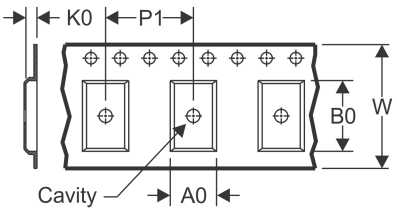
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

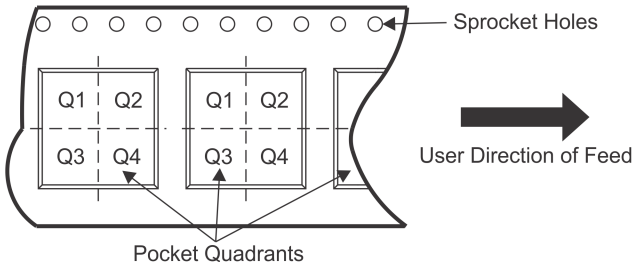


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

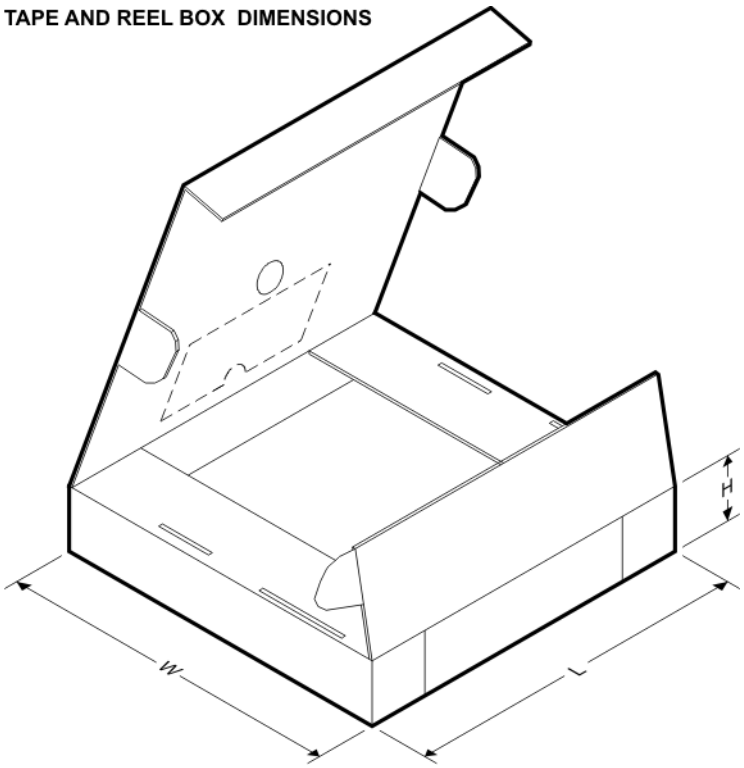
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2989AILD-1.8/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2989AILDX-1.8/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2989AIMX-1.8/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2989ILD-1.8/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2989ILDX-1.8/NOPB	WSON	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2989IMX-1.8/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

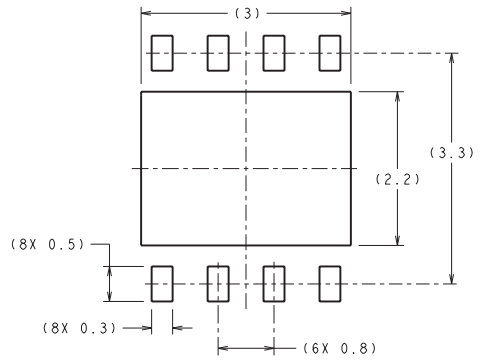
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

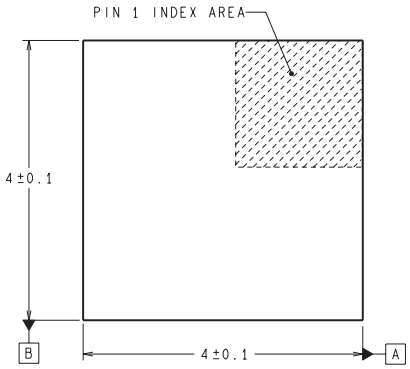
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2989AILD-1.8/NOPB	WSON	NGN	8	1000	213.0	191.0	55.0
LP2989AILDX-1.8/NOPB	WSON	NGN	8	4500	367.0	367.0	35.0
LP2989AIMX-1.8/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2989ILD-1.8/NOPB	WSON	NGN	8	1000	213.0	191.0	55.0
LP2989ILDX-1.8/NOPB	WSON	NGN	8	4500	367.0	367.0	35.0
LP2989IMX-1.8/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

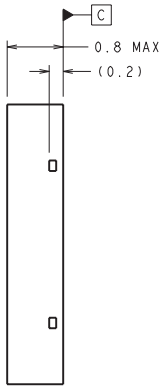
NGN0008A

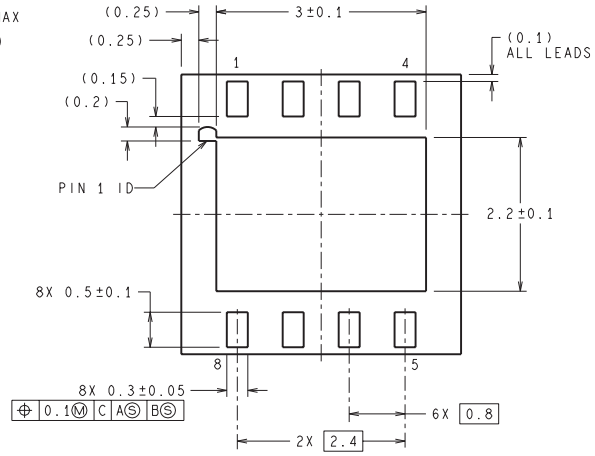


RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

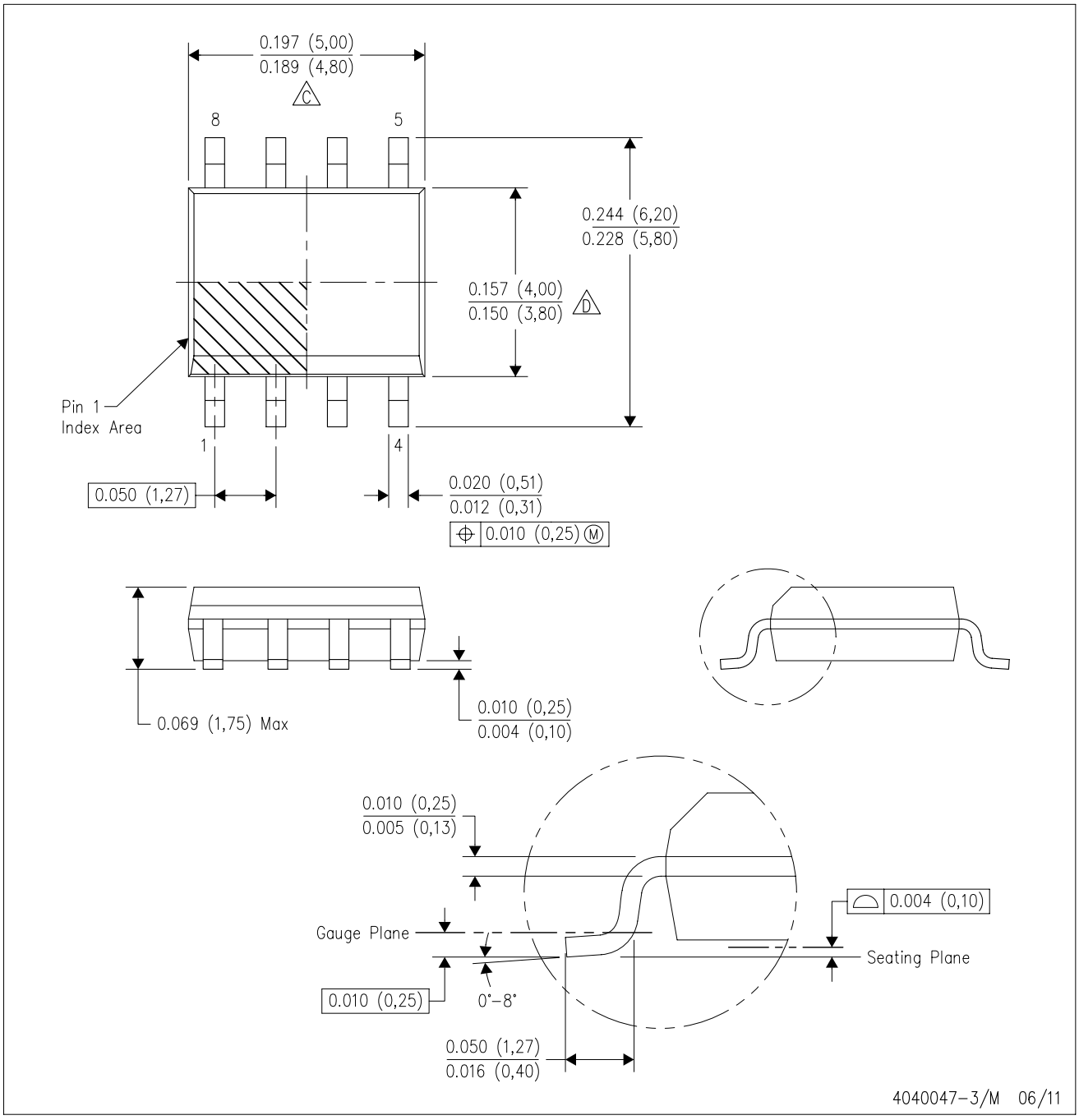






LDC08A (Rev B)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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