DDR Termination Regulator

Check for Samples: LP2994

FEATURES

- **Source and Sink Current**
- **Low External Component Count**
- **Independent Analog and Power Rails**
- **Linear Topology**
- **Small Package SOIC-8**
- **Low Cost and Easy to Use**
- **Shutdown Pin**

APPLICATIONS

- **SSTL-2**
- **SSTL-3**
- **DDR-SDRAM Termination**
- **DDR-II Termination**

DESCRIPTION

The LP2994 regulator is designed to provide a linear solution to meet the JEDEC SSTL-2 and SSTL-3 specifications (Series Stub Termination Logic) for active termination of DDR-SDRAM. The device utilizes an internal operational amplifier to provide linear regulation of V_{TT} without the need for expensive external components. The output stage prevents shoot through while delivering 1.5A continuous current and maintaining excellent load regulation. The LP2994 also incorporates an active low shutdown pin to tri-state the output during Suspend To Ram (STR) states.

Patents Pending

Typical Application Circuit

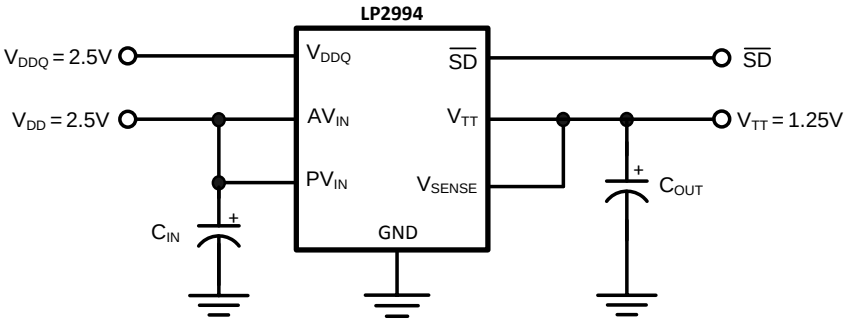


Figure 1. SSTL-2 V_{TT} Termination

Connection Diagram

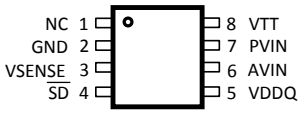


Figure 2. SOIC-8 (D) Package - Top View

PIN DESCRIPTIONS

SOIC-8 Pin	Name	Function
1	NC	No internal connection
2	GND	Ground
3	VSENSE	Feedback pin for regulating VTT
4	$\overline{SD}$	Active low shutdown pin
5	VDDQ	Input for internal reference equal to VDDQ/2
6	AVIN	Analog input pin
7	PVIN	Power input pin
8	VTT	Output voltage for connection to termination resistors

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

AVIN, VTT, SD to GND	−0.3V to +6V
PVIN to GND	−0.3V to AVIN
VDDQ(3)	−0.3V to +6V
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating(4)	2kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) VDDQ voltage must be less than 2 x (AVIN - 1) or 6V, whichever is smaller.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

OPERATING RANGE

Junction Temp. Range(1)	0°C to +125°C
AVIN Supply Voltage	2.2V to 5.5V
PVIN Supply Voltage	-0.3V to (AVIN + 0.3V)
SD Input Voltage	-0.3V to (AVIN + 0.3V)
VTT Output Voltage	-0.3V to (PVIN + 0.3V)
SOIC-8 Thermal Resistance (θ_{JA})	151°C/W

(1) At elevated temperatures, devices must be derated based on thermal resistance. The device in the SOIC-8 package must be derated at θ_{JA} = 151.2° C/W junction to ambient with no heat sink.

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for T_J = 25°C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0°C to +125°C). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TT}	V_{TT} Output Voltage I_{OUT} = 0A(2)	VIN=VDDQ = 2.3V	**1.108**	1.138	**1.168**	V
		VIN=VDDQ = 2.5V	**1.210**	1.236	**1.260**	
		VIN=VDDQ = 2.7V	**1.305**	1.334	**1.360**	
I_q	Quiescent Current	I_{OUT} = 0A(3)		272	**400**	µA
Z_{VDDQ}	VDDQ Input Impedance		**86**	100		kΩ
I_{QSD}	Quiescent current in shutdown			21	**45**	µA
I_{SD}	Shutdown Leakage Current	SD = 0V SD = 2.5V		2 2	**5**	µA nA
V_{IH}	Minimum Shutdown High Level		**1.9**			V
V_{IL}	Maximum Shutdown Low Level				**0.8**	V
$\Delta V_{TT}/V_{TT}$	Load Regulation(4)	I_{OUT} = 0 to 1.5A		-0.4		%
		I_{OUT} = 0 to −1.5A		+0.4		
I_{SENSE}	SENSE Input Current			100		pA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) VIN is defined as the VIN = AVIN = PVIN
(3) Quiescent current defined as the current flow into AVIN.
(4) Load regulation is tested by using a 10ms current pulse and measuring V_{TT}.

TYPICAL PERFORMANCE CHARACTERISTICS

Iq vs V_{IN} (25°C)

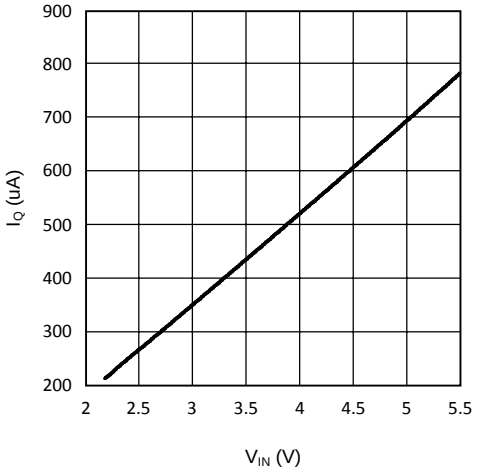


Figure 3.

Iq vs V_{IN} (0, 25, and 125°C)

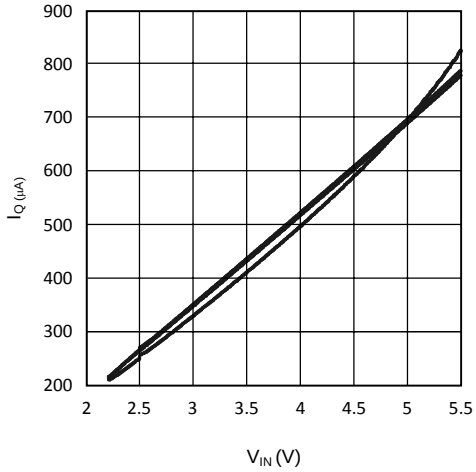


Figure 4.

Iq vs Temperature (V_{IN} = 2.5V)

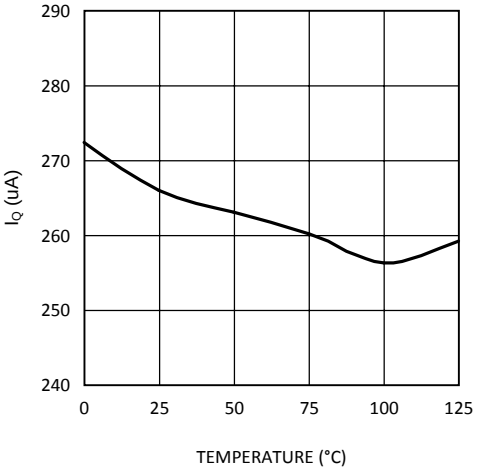


Figure 5.

I_{SD} vs V_{IN} (25°C)

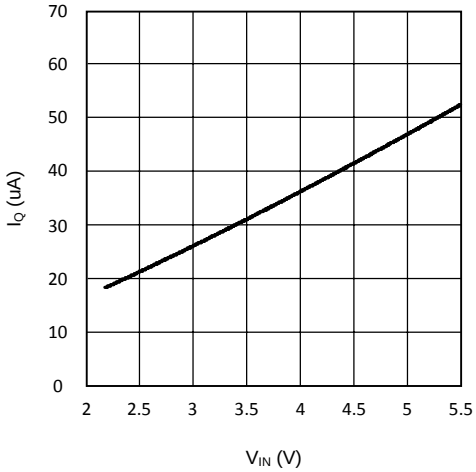


Figure 6.

I_{SD} vs V_{IN} (0, 25, and 125°C)

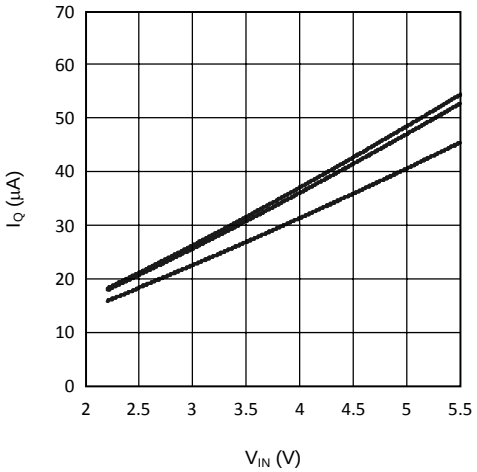


Figure 7.

I_{SD} vs Temperature (V_{IN} = 2.5V)

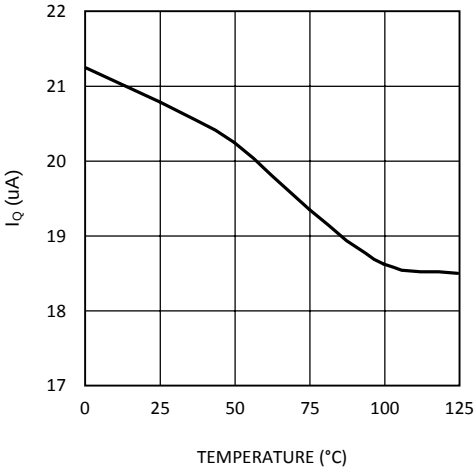


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IL} and V_{IH} vs AV_{IN} (25°C)

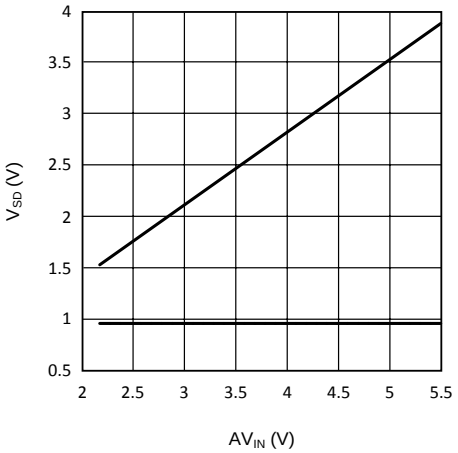


Figure 9.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5V, PV_{IN} = 1.8V)

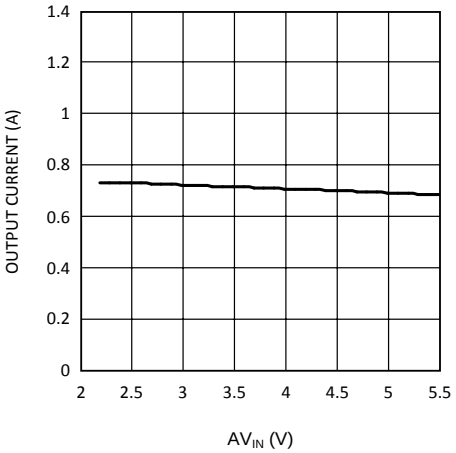


Figure 10.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5V, PV_{IN} = 2.5V)

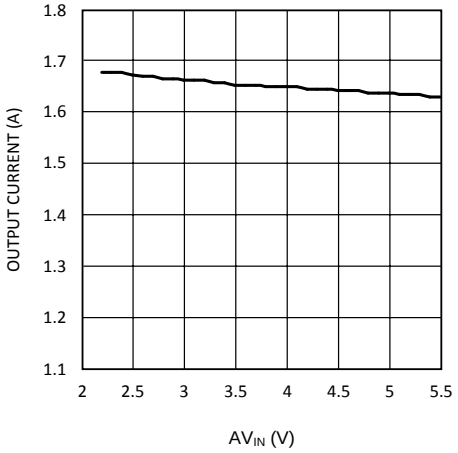


Figure 11.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 2.5V, PV_{IN} = 3.3V)

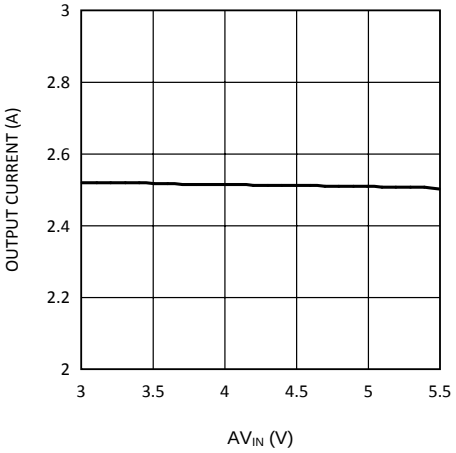


Figure 12.

Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 2.5V)

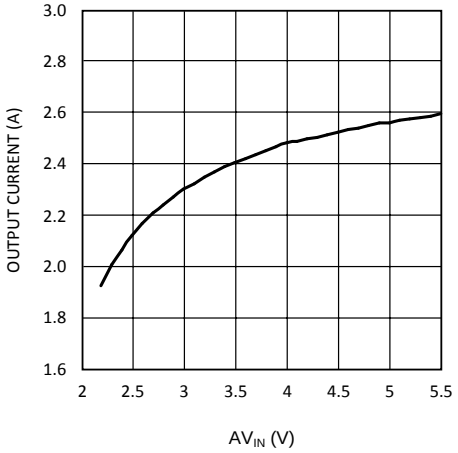


Figure 13.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8V, PV_{IN} = 1.8V)

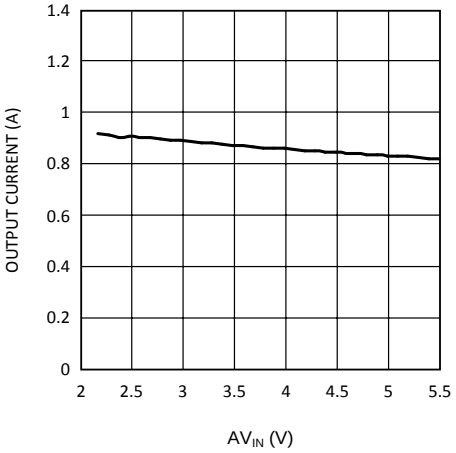


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Maximum Sinking Current vs AV_{IN} (V_{DDQ} = 1.8V)

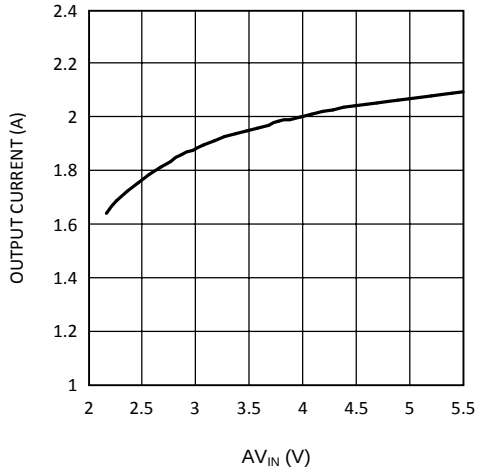


Figure 15.

Maximum Sourcing Current vs AV_{IN} (V_{DDQ} = 1.8V, PV_{IN} = 3.3V)

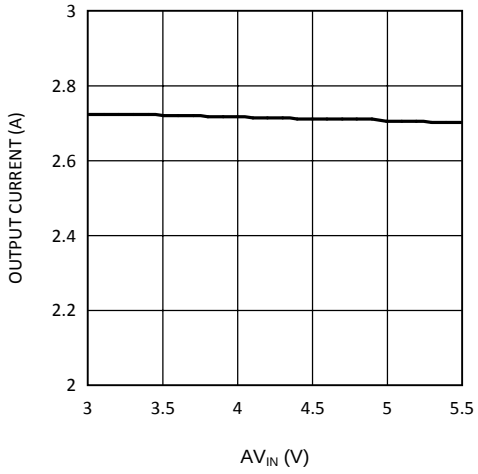


Figure 16.

V_{TT} vs I_{OUT} (0, 25, 85, and 125°C)

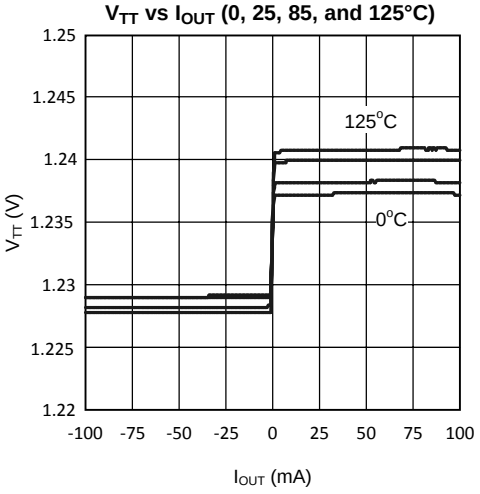


Figure 17.

V_{TT} vs I_{OUT}

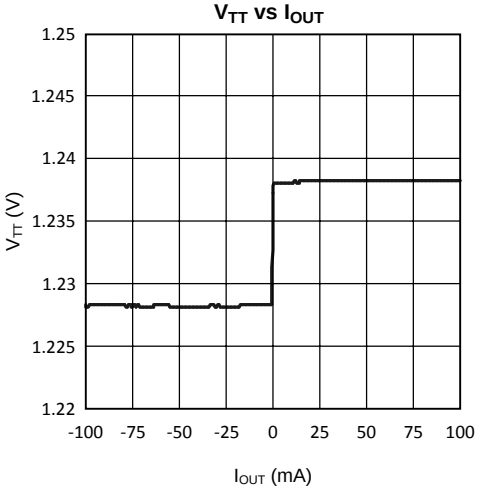
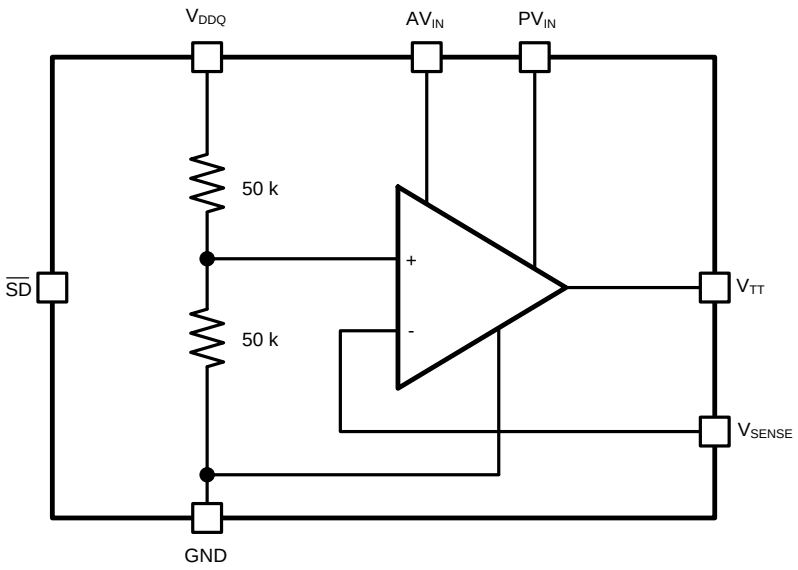


Figure 18.

BLOCK DIAGRAM



DESCRIPTION

The LP2994 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2 and SSTL-3. The output, V_{TT} is capable of sinking and sourcing current while regulating the output voltage equal to V_{DDQ} / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2994 also incorporates two distinct power rails which separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2994 to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII).

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ohms, although these can be changed to scale the current requirements from the LP2994. This implementation can be seen below in Figure 19.

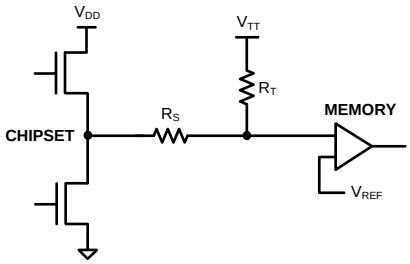


Figure 19. SSTL Termination Scheme

Pin Descriptions

AVIN and PVIN

AVIN and PVIN are the input supply pins for the LP2994. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create V_{TT}. These pins have the capability to work off separate supplies depending on the application. Higher voltages on PVIN will increase the maximum continuous output current because of output RDSON limitations at voltages close to V_{TT}. The disadvantage of high values of PVIN is that the internal power loss will also increase, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5V. This eliminates the need for bypassing the two supply pins separately. The only limitation on input voltage selection is that PVIN must be equal to or lower than AVIN.

V_{DDQ}

V_{DDQ} is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This ensures that V_{TT} will track V_{DDQ} / 2 precisely. The optimal implementation of V_{DDQ} is as a remote sense. This can be achieved by connecting V_{DDQ} directly to the 2.5V rail at the DIMM instead of AVIN and PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications V_{DDQ} will be a 2.5V signal, which will create a 1.25V termination voltage at V_{TT} (See ELECTRICAL CHARACTERISTICS Table for exact values of V_{TT} over temperature).

V_{SENSE}

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the LP2994 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1uF ceramic capacitor placed next to the V_{SENSE} pin can help filter any high frequency signals and preventing errors.

Shutdown

The LP2994 contains an active low shutdown pin that can be used to tri-state VTT. During shutdown V_{TT} should not be exposed to voltages that exceed PVIN. With the shutdown pin asserted low the quiescent current of the LP2994 will drop, however, V_{DDQ} will always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section. The shutdown pin also has an internal pull-up current, therefore to turn the part on the shutdown pin can either be connected to AVIN or left open.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to V_{DDQ} / 2. The LP2994 is designed to handle peak transient currents of up to +/- 3A with excellent load regulation. The maximum continuous current is a function of AVIN and PVIN and several curves can be seen in the TYPICAL PERFORMANCE CHARACTERISTICS section. If a transient is expected to last above the maximum continuous current rating for a significant amount of time, then the bulk output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the LP2994 is designed to handle large transient output currents it is not capable of handling these for long durations under all conditions. The reason for this is that the SOIC-8 package is not able to thermally dissipate an infinite amount of heat as a result of internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal de-rating should always be used (Please refer to the Thermal Dissipation section).

Component Selections

INPUT CAPACITOR

The LP2994 does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 47uF. Ceramic capacitors can also be used, a value in the range of 10uF with X5R dielectric or better would be an ideal choice. The input capacitance can be reduced if the LP2994 is placed close to the bulk capacitance from the output of the 2.5V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47uF capacitor should be placed as close to possible to the PVIN rail. An additional 0.1uF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

OUTPUT CAPACITOR

The LP2994 has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of VTT. As a general recommendation, the output capacitor should be sized above 100uF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (approximately 100kHz) should be used for the LP2994. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100uF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10mOhm). However, some dielectric types have poor capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than other capacitors.

Thermal Dissipation

Since the LP2994 is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (1)$$

From this equation, the maximum power dissipation (P_D) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA} \quad (2)$$

The θ_{JA} of the LP2994 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SOIC-8 is 163°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. Figure 20 shows how the θ_{JA} varies with airflow for the two boards mentioned.

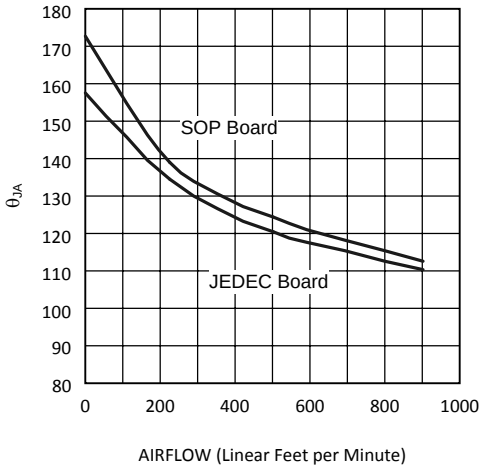


Figure 20. θ_{JA} vs Airflow

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout, it is possible to reduce the θ_{JA} further than the nominal values shown in Figure 20.

Optimizing the θ_{JA} and placing the LP2994 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AVIN and V_{DDQ}. During the active state (when Shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT} \quad (3)$$

where,

$$P_{AVIN} = I_{AVIN} \times V_{AVIN} \quad (4)$$

$$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ}^2 \times R_{VDDQ} \quad (5)$$

To calculate the maximum power dissipation at V_{TT}, both sinking and sourcing current conditions at V_{TT} need to be examined. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \text{ (Sinking)} \quad (6)$$

or

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD} \text{ (Sourcing)} \quad (7)$$

The power dissipation of the LP2994 can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the V_{DDQ} pin.

$$P_D = P_{AVIN} + P_{VDDQ} \quad (8)$$

Where,

$$P_{AVIN} = I_{AVIN} \times V_{AVIN} \quad (9)$$

$$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ}^2 \times R_{VDDQ} \quad (10)$$

Typical Application Circuits

Several different application circuits have been shown in Figure 21 through Figure 30 to illustrate some of the options that are possible in configuring the LP2994. Graphs of the individual circuit performance can be found in the TYPICAL PERFORMANCE CHARACTERISTICS section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

SSTL-2 APPLICATIONS

For the majority of applications that implement the SSTL-2 termination scheme, it is recommended to connect all the input rails to the 2.5V rail. This provides an optimal trade-off between power dissipation and component count and selection. An example of this circuit can be seen in Figure 21.

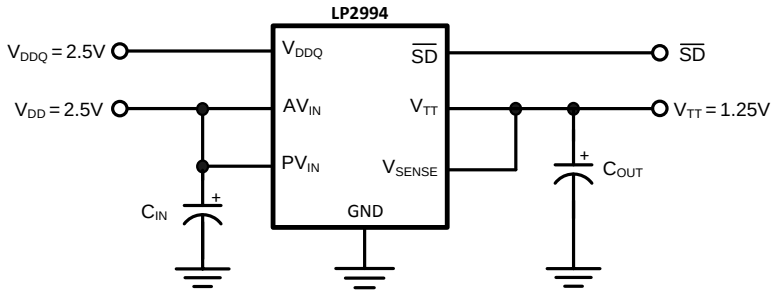


Figure 21. Recommended SSTL-2 Implementation

If power dissipation or efficiency is a major concern then the LP2994 has the ability to operate on split power rails. The output stage (PVIN) can be operated on a lower rail such as 1.8V and the analog circuitry (AVIN) can be connected to a higher rail such as 2.5V, 3.3V or 5V. This allows the internal power dissipation to be lowered when sourcing current from VTT. The disadvantage of this circuit is that the maximum continuous current is reduced because of the lower rail voltage, although it is adequate for all motherboard SSTL-2 applications. Increasing the output capacitance can also help if periods of large load transients will be encountered.

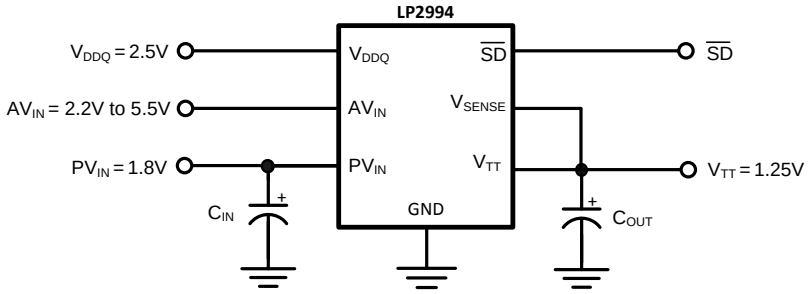


Figure 22. Lower Power Dissipation SSTL-2 Implementation

The third option for SSTL-2 applications in the situation that a 1.8V rail is not available and it is not desirable to use 2.5V, is to connect the LP2994 power rail to 3.3V. In this situation AVIN will be limited to operation on the 3.3V or 5V rail as PVIN can never exceed AVIN. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. Care should be taken to prevent the LP2994 from experiencing large current levels which cause the junction temperature to exceed the maximum. Because of this risk it is not recommended to supply the output stage with a voltage higher than a nominal 3.3V rail.

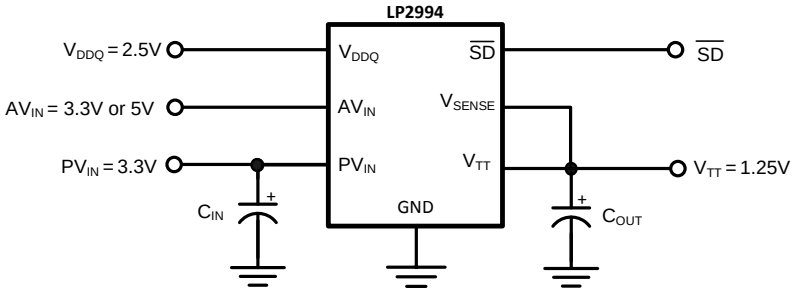


Figure 23. SSTL-2 Implementation with higher voltage rails

DDR-II APPLICATIONS

With the separate V_{DDQ} pin and an internal resistor divider it is possible to use the LP2994 in applications utilizing DDR-II memory. Figure 24 and Figure 25 show several implementations of recommended circuits with output curves displayed in the Typical Performance Characteristics. Figure 24 shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 3.3V or 5V rail.

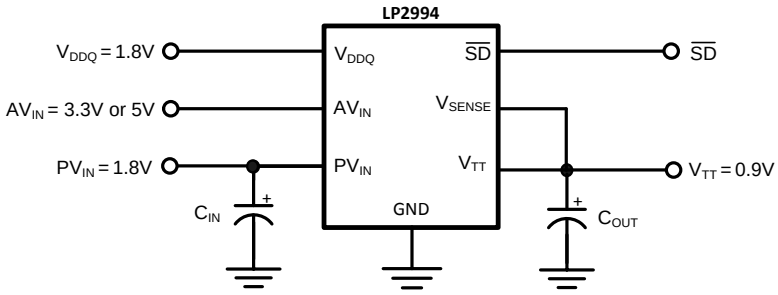


Figure 24. Recommended DDR-II Termination

If it is not desirable to use the 1.8V rail it is possible to connect the output stage to a 3.3V rail. Care should be taken to not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason, it is not recommended to power PVIN off a rail higher than the nominal 3.3V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

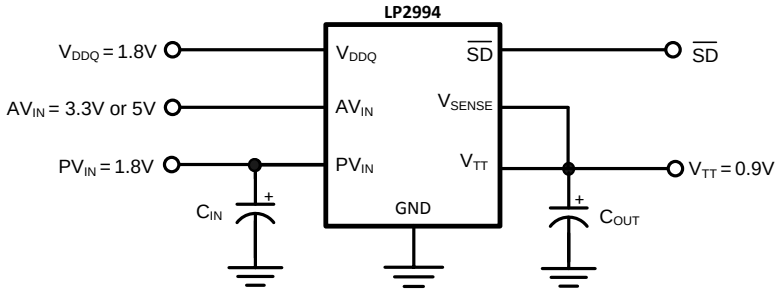


Figure 25. DDR-II Termination with higher voltage rails

If standards other than SSTL-2 are required, such as SSTL-3, it may be necessary to use a different scaling factor than 0.5 times V_{DDQ} for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from V_{TT} to the V_{SENSE} pin. This has been illustrated in Figure 26 and Figure 27. Figure 26 shows how to use two resistors to level shift V_{TT} above the internal reference voltage of $V_{DDQ}/2$. To calculate the exact voltage at V_{TT} the following equation can be used.

$$V_{TT} = (V_{DDQ}/2) \times (1 + R1/R2) \quad (11)$$

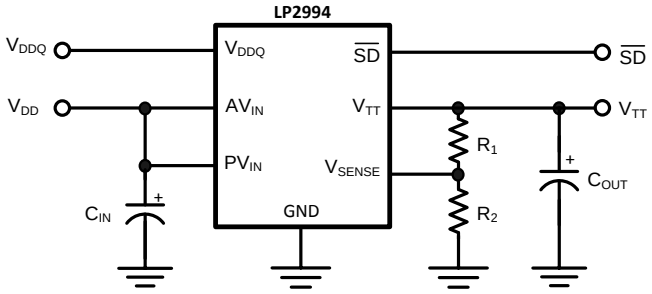


Figure 26. Increasing V_{TT} by Level Shifting

Conversely, the R2 resistor can be placed between V_{SENSE} and V_{DDQ} to shift the V_{TT} output lower than the internal reference voltage of $V_{DDQ}/2$. The equations relating V_{TT} and the resistors can be seen below:

$$V_{TT} = (V_{DDQ}/2) \times (1 - R1/R2) \quad (12)$$

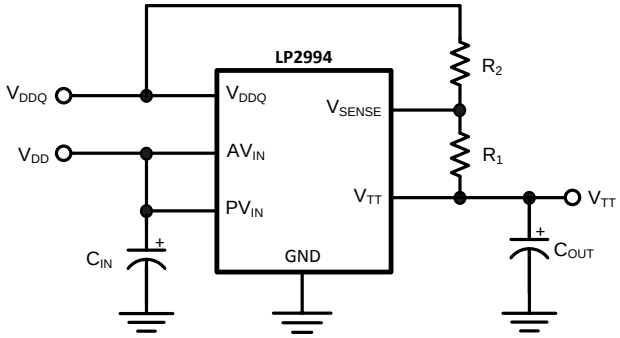


Figure 27. Decreasing V_{TT} by Level Shifting

REFERENCE VOLTAGE

DDR-SDRAM and the motherboard chipsets usually require a reference voltage which tracks V_{TT}. To implement this feature in most applications it is advisable to use two equal resistors as a resistor divider. This prevents long V_{REF} traces from running across the motherboard picking up noise which can interfere with performance. However, in a few applications it may be desirable to use the V_{TT} output on the LP2994 to generate the V_{REF} signal. The can be accomplished by using an RC filter on the output of V_{TT} to create a V_{REF} signal. Typically, the reference voltage required by chipsets and memory is well under 1µA combined, therefore, a fairly large resistor such as 1kΩ or larger can be used. A recommended capacitor would be a 1uF X7R ceramic capacitor.

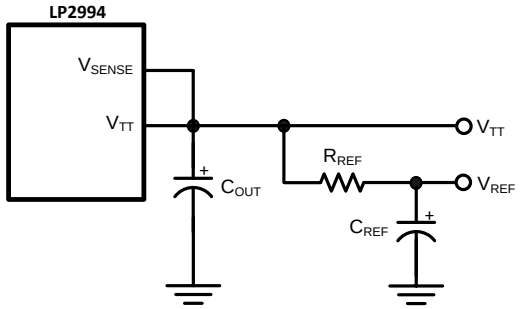


Figure 28. Creating a Reference Voltage for Memory and Chipsets

OUTPUT CAPACITOR SELECTION

For applications utilizing the LP2994 to terminate SSTL-2 I/O signals the typical application circuit shown in Figure 29 can be implemented.

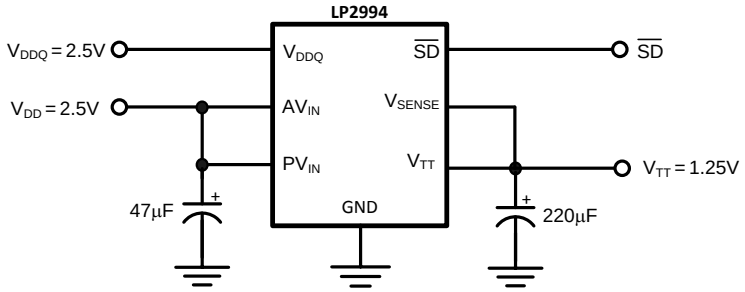


Figure 29. Typical SSTL-2 Application Circuit

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. Figure 30 shown below depicts an example circuit where 2 bulk output capacitors could be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

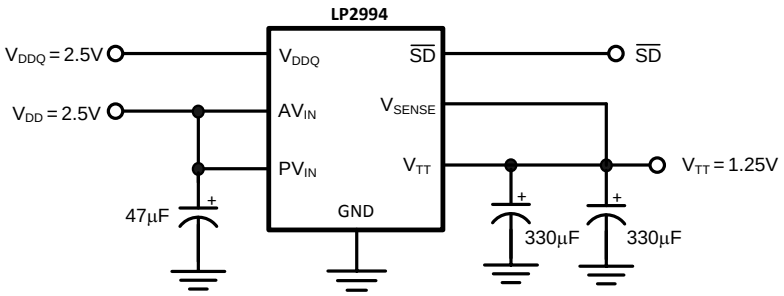


Figure 30. Typical SSTL-2 Application Circuit for Motherboards

In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result bulk aluminum electrolytic capacitors in the range of 1000uF are typically used.

PCB Layout Considerations

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the V_{SENSE} can also be used to filter any unwanted high frequency signal. This can be an issue especially if long V_{SENSE} traces are used.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	15

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