LP38798-ADJ High PSRR, Ultra Low Noise, 800 mA Linear Voltage Regulator for RF/Analog Circuits

FEATURES

- **Ultra-Low Output Noise: 5 μV_{RMS} (10Hz to 100 kHz)**
- **High PSRR: 90 dB at 10 kHz, 60 dB at 100 kHz**
- **Wide Operating Input Voltage Range: 3.0V to 20V**
- **±1.0% Output Voltage Initial Accuracy (T_J = 25°C)**
- **Very Low Dropout : 200 mV (Typical) at 800mA**
- **Stable with Ceramic or Tantalum Output Capacitors**
- **Excellent Line and Load Transient Response**
- **Current Limit and Over-Temperature Protection**

APPLICATIONS

- **RF and VCO Power**
- **Wireless LAN Devices**
- **Wireless Cable Modems**
- **Low Noise Post-Regulation**

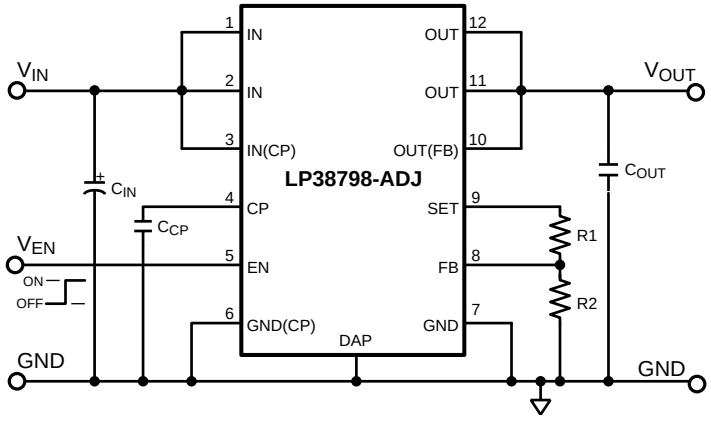
DESCRIPTION

The LP38798-ADJ is a high performance linear regulator capable of supplying 800 mA output current. Designed to meet the requirements of sensitive RF/Analog circuitry, the LP38798-ADJ implements a novel linear topology on an advanced CMOS process to deliver ultra-low output noise and high PSRR at switching power supply frequencies. The LP38798SD-ADJ is stable with both ceramic and tantalum output capacitors and requires a minimum output capacitance of only 1 µF for stability.

The LP38798-ADJ can operate over a wide input voltage range (3.0V to 20V) making it well suited for many post-regulation applications.

The LP38798-ADJ is available in a 12-Lead WSON package (4.0 x 4.0 x 0.8 mm) with Thermal Pad.

Typical Application Circuit



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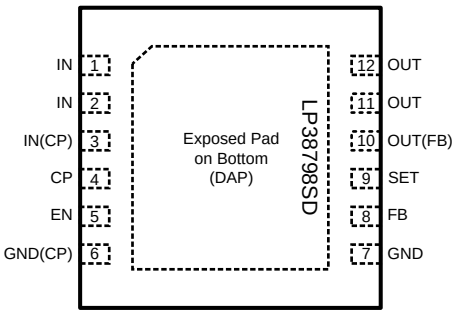
Connection Diagram

Top View



Connect WSON DAP to GND at Pins 6 and 7

Figure 1. LP38798SD-ADJ
12-Lead WSON Package (Top View)

PIN DESCRIPTIONS

Pin	Name	Function
1, 2	IN	Device unregulated input voltage pins. Connect pins together at the package.
3	IN(CP)	Charge pump input voltage pin. Connect directly to pins 1 and 2 at the package.
4	CP	Charge pump output. See Charge Pump section in the Applications Information for more information.
5	EN	Enable pin. A Logic high level is required on this pin to enable the LDO output. A Logic low level will turn the output off and reduce the operating current of the device. See Enable Input Operation section in the Applications Information for more information.
6	GND	Device charge pump ground pin.
7	GND	Device analog ground pin.
8	FB	Feedback pin for programming the output voltage.
9	SET	Internally filtered pre-buffered output. A feedback resistor divider network from this pin to FB and GND will set the output voltage of the device.
10	OUT(FB)	OUT buffer feedback pin. Connect directly to pins 11 and 12 at the package.
11, 12	OUT	Device regulated output voltage pins. Connect pins together at the package.
Exposed Pad	DAP	The exposed die attach pad on the bottom of the package should be connected to a thermal pad at ground potential. See 12-Lead WSON Package Thermal Considerations section in the APPLICATIONS INFORMATION for more information.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

IN	–0.3V to 22V
OUT	–0.3V to V_{IN} +0.3V
FB, EN	–0.3V to 6.0V
Storage Temperature Range	–65°C to +150°C
Soldering(2)	260°C, 10 sec
ESD Rating (HBM)(3)	2 kV
Power Dissipation(4)	Internally Limited
I_{OUT} (Survival)	Internally Limited

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) Peak Reflow Temperatures for Surface Mount devices are defined in “Absolute Maximum Ratings for Soldering,” Literature Number: SNOA549C
(3) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ; resistor into each pin. Applicable test standard is JESD-22-A114-C.
(4) The value of θ_{J-A} for the WSON package is dependent on PCB copper area, copper thickness, the number of copper layers in the PCB, and the number of thermal vias under the exposed thermal pad (DAP). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator may go into thermal shutdown. See 12-Lead WSON Package Thermal Considerations in the Applications Information.

OPERATING RATINGS(1)

Input Voltage, V_{IN}	3.0V to 20.0V
Output Voltage, V_{OUT}	1.2V to (V_{IN} – V_{DO})
Enable Voltage, V_{EN}	0.0V to 5.0V
Junction Temperature, T_J	–40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of –40°C to +125°C. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Minimum and Maximum limits are specified through test, design, or statistical correlation. Unless otherwise stated the following conditions apply: V_{IN} = 5.5 V, V_{SET} = 5.0 V, C_{CP}= 10 nF X7R, C_{IN} = 10 µF 50 mΩ Tantalum, C_{OUT} = 10 µF X7R MLCC, I_{OUT} = 10 mA, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{FB}	Feedback Voltage		1.188	1.2	1.212	V
		5.5 V ≤ V_{IN} ≤ 20.0 V	**1.176**		**1.224**	
V_{OS}	V_{OUT} – V_{SET}		0	3.5	**16.0**	mV
I_{FB}	Feedback Pin Current	V_{FB} = 1.2 V	-	0	**1**	µA
I_{SET}	SET Pin Internal Current Sink	V_{IN} = 3.0 V, V_{SET} = 2.5 V	-	46	-	µA
		V_{IN} = 5.5 V, V_{SET} = 5.0 V	**25.2**	52	**67.8**	
		V_{IN} = 12.5 V, V_{SET} = 12.0 V	-	71	-	
ΔV_{OUT} / ΔV_{IN}	Line Regulation(1)	5.5 V ≤ V_{IN} ≤ 20.0 V I_{OUT} = 10 mA	-	0.005	-	%/V
ΔV_{OUT} / ΔI_{OUT}	Load Regulation(2)	V_{IN} = 5.5 V 10 mA ≤ I_{OUT} ≤ 800 mA	-	-0.2	-	%/A
V_{DO}	Dropout Voltage(3)	I_{OUT} = 800 mA	-	200	**420**	mV
UVLO	Undervoltage Lock-Out	V_{IN} Rising until output is on	**2.47**	2.65	**2.83**	V
ΔUVLO	UVLO Hysteresis	V_{IN} Falling from > UVLO threshold until output is off	-	180	-	mV
I_{GND}	Ground Pin Current(4)	I_{OUT} = 800 mA	-	1.4	**2.25**	mA
		V_{IN} = 20.0 V, I_{OUT} = 800 mA	-	1.6	**2.51**	
I_Q	Ground Pin Current, Quiescent(4)	I_{OUT} = 0 mA	-	1.4	**2.1**	mA
		V_{IN} = 20.0 V, I_{OUT} = 0 mA	-	1.5	**2.2**	
I_{SD}	Ground Pin Current, Shutdown(4)	V_{EN} = 0.0 V	-	9	**20**	µA
		V_{IN} = 20.0 V, V_{EN} = 0.0 V	-	12	**40**	
I_{SC}	Short Circuit Current	R_{LOAD} = 0Ω	**850**	1200	**1600**	mA
ΔV_{CP}	V_{CP} – V_{IN}		-	2.8	-	V
		V_{IN} = 20.0V	-	2.3	-	
t_{START}	Start-up Time	From V_{EN} > $V_{EN(ON)}$ to V_{OUT} ≥ 98% of $V_{OUT(NOM)}$	-	155	**300**	µs
PSRR	Power Supply Rejection Ratio	V_{OUT} = 1.2 V, f = 10 kHz	-	110	-	dB
		V_{OUT} = 5.0 V, f = 10 kHz	-	90	-	
		V_{OUT} = 1.2 V, f = 100 kHz	-	90	-	
		V_{OUT} = 5.0 V, f = 100 kHz	-	60	-	
		V_{OUT} = 1.2 V, f = 1 MHz	-	70	-	
		V_{OUT} = 5.0 V, f = 1 MHz	-	60	-	

(1) Line Regulation: % change in $V_{OUT(NOM)}$ for every 1V change in V_{IN}= ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔV_{IN}) x 100%
(2) Load Regulation: % change in $V_{OUT(NOM)}$ for every 1A change in I_{OUT} = ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔI_{OUT}) x 100%
(3) Dropout voltage (V_{DO}) is defined as the differential voltage measured between V_{OUT} and V_{IN} when V_{IN}, falling from V_{IN} = V_{OUT} + 1V, causes V_{OUT} to drop 2% below the value measured with V_{IN} = V_{OUT} + 1V. Dropout voltage specification does not apply when the programmed output voltage is below the Minimum Operating Input Voltage.
(4) Ground pin current is the sum of the current in both GND pins (Pin 4 + Pin 5) only, and does not include current from the SET pin.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of –40°C to +125°C. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Minimum and Maximum limits are specified through test, design, or statistical correlation. Unless otherwise stated the following conditions apply: V_{IN} = 5.5 V, V_{SET} = 5.0 V, C_{CP}= 10 nF X7R, C_{IN} = 10 µF 50 mΩ Tantalum, C_{OUT} = 10 µF X7R MLCC, I_{OUT} = 10 mA, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
e_N	Output Noise Voltage (RMS)	V_{IN} = 3.0 V, V_{OUT} = 1.2 V C_{OUT} = 1 µF X7R BW = 10 Hz to 100 kHz	-	4.96	-	$\mu V_{(RMS)}$
		V_{IN} = 3.0 V, V_{OUT} = 1.2 V BW = 10 Hz to 100 kHz	-	5.21	-	
		V_{IN} = 3.0 V, V_{OUT} = 1.2 V BW = 10 Hz to 10 MHz	-	11.53	-	
		V_{IN} = 6.0 V, V_{OUT} = 5.0 V C_{OUT} = 1 µF X7R BW = 10 Hz to 100 kHz	-	5.38	-	
		V_{IN} = 6.0 V, V_{OUT} = 5.0 V BW = 10 Hz to 100 kHz	-	5.43	-	
		V_{IN} = 6.0 V, V_{OUT} = 5.0 V BW = 10 Hz to 10 MHz	-	11.58	-	
ENABLE INPUT						
$V_{EN(ON)}$	Enable ON Threshold Voltage	V_{EN} rising from 500 mV until Output is ON	**1.14**	1.24	**1.34**	V
ΔV_{EN}	Enable Threshold Voltage Hysteresis	V_{EN} Falling from $V_{EN(ON)}$	-	110	-	mV
$I_{EN(IL)}$	EN Pin Pull-up Current	V_{EN} = 500 mV	-	2	**3.0**	µA
$I_{EN(IH)}$	EN Pin Pull-up Current	V_{EN} = 2.0 V	-	2	**3.0**	µA
$V_{EN(CLAMP)}$	Enable Pin Clamp Voltage	EN pin = Open	-	5.0	-	V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Junction Temperature (T_J) Rising	-	170	-	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	Junction Temperature (T_J) Falling from T_{SD}	-	12	-	

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

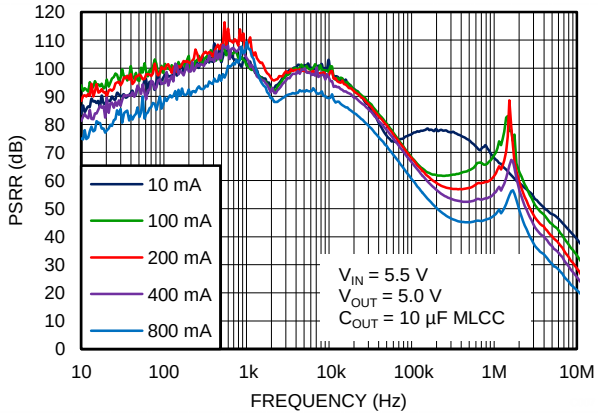


Figure 2. PSRR, V_{IN} = 5.5V, V_{OUT} = 5.0V

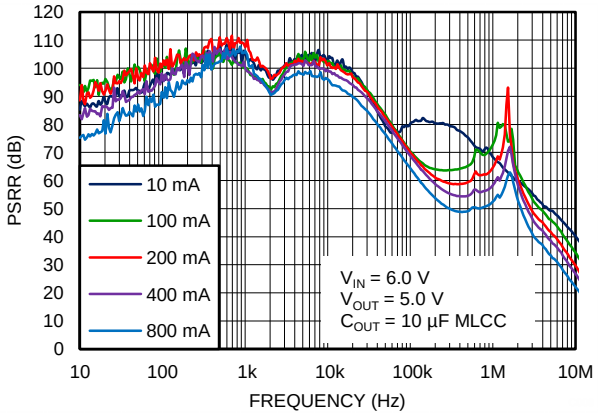


Figure 3. PSRR, V_{IN} = 6.0 V, V_{OUT} = 5.0 V

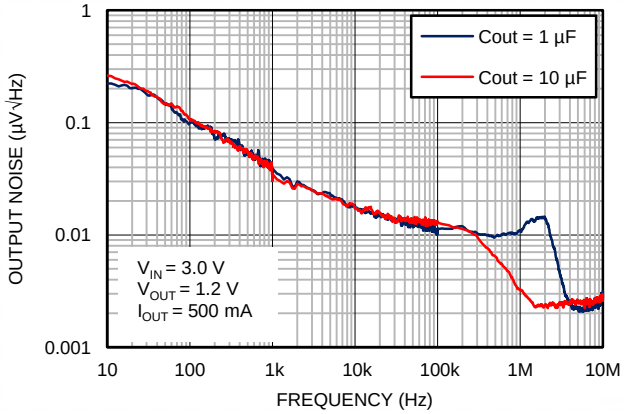


Figure 4. Noise Density, V_{OUT} = 1.2 V

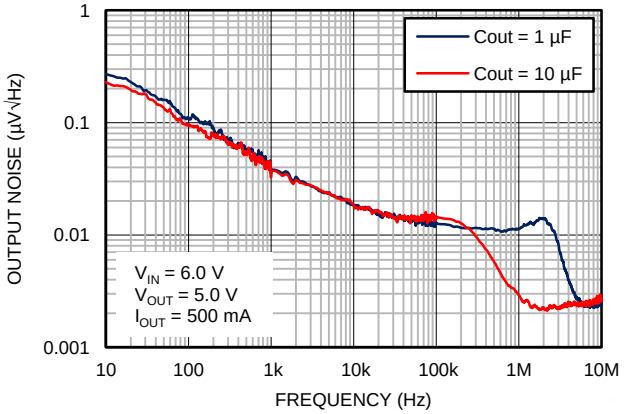


Figure 5. Noise Density, V_{OUT} = 5.0 V

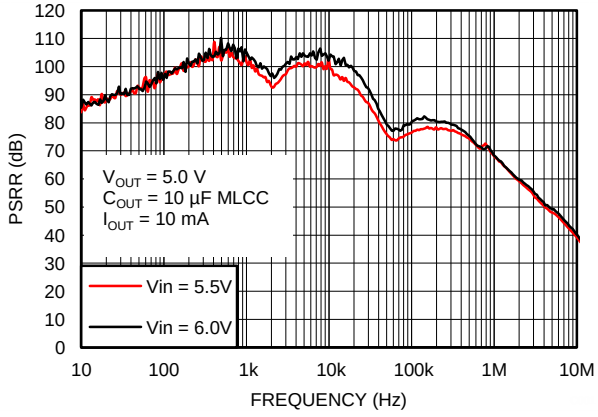


Figure 6. PSRR, V_{OUT} = 5.0 V, I_{OUT} = 10 mA

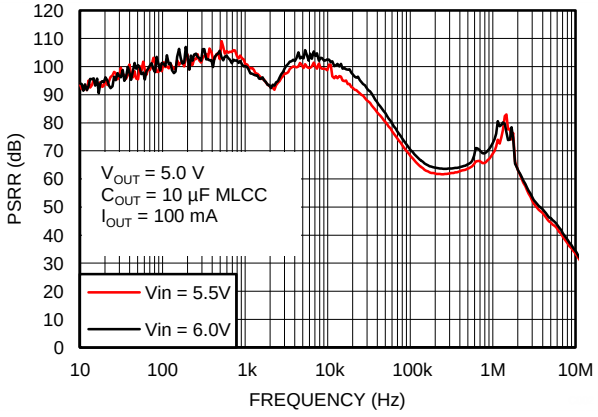


Figure 7. PSRR, V_{OUT} = 5.0 V, I_{OUT} = 100 mA

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

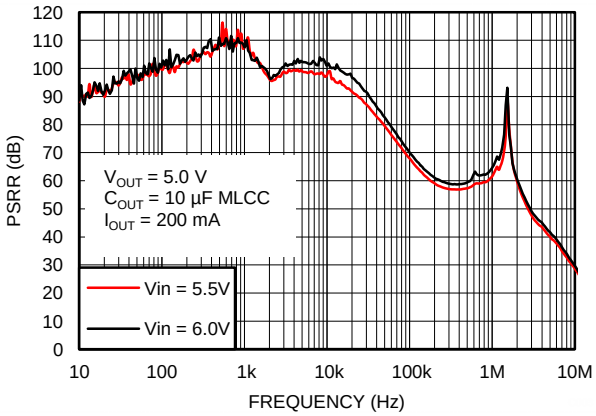


Figure 8. PSRR, V_{OUT} = 5.0 V, I_{OUT} = 200 mA

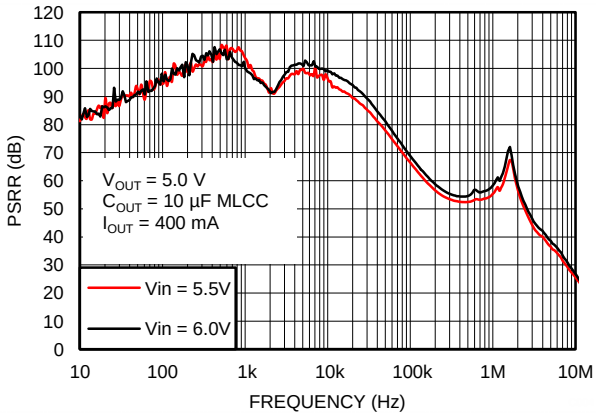


Figure 9. PSRR, V_{OUT} = 5.0 V, I_{OUT} = 400 mA

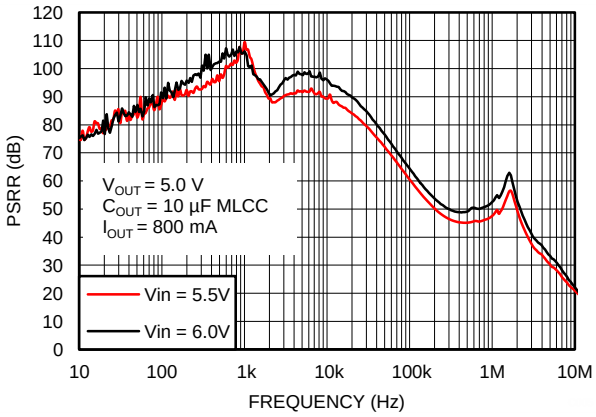


Figure 10. PSRR, V_{OUT} = 5.0 V, I_{OUT} = 800 mA

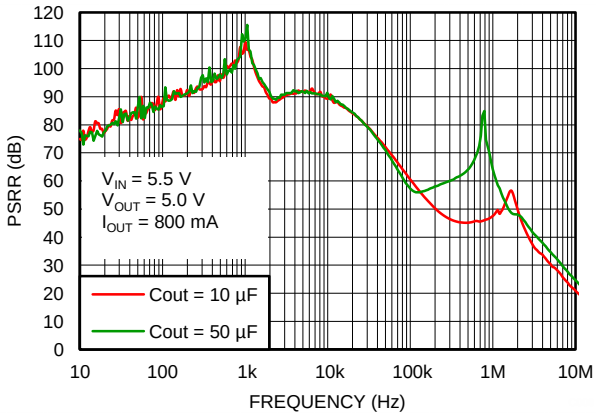


Figure 11. PSRR, V_{OUT} = 5.0 V, I_{OUT}= 800mA

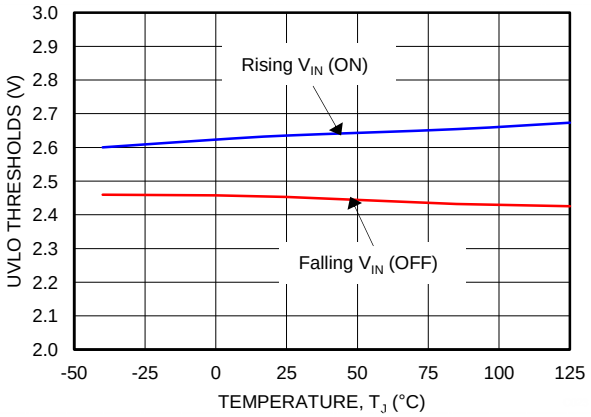


Figure 12. UVLO Thresholds vs. T_J

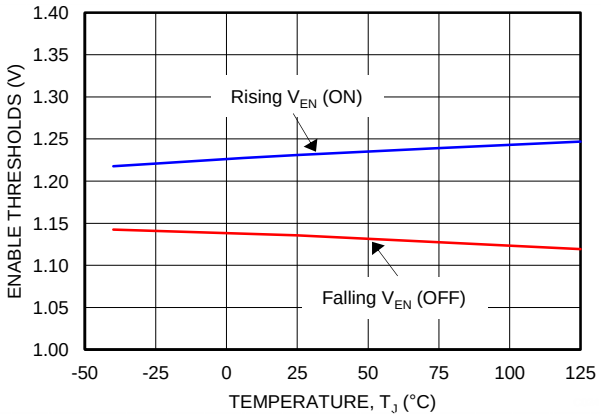


Figure 13. Enable Thresholds vs. T_J

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

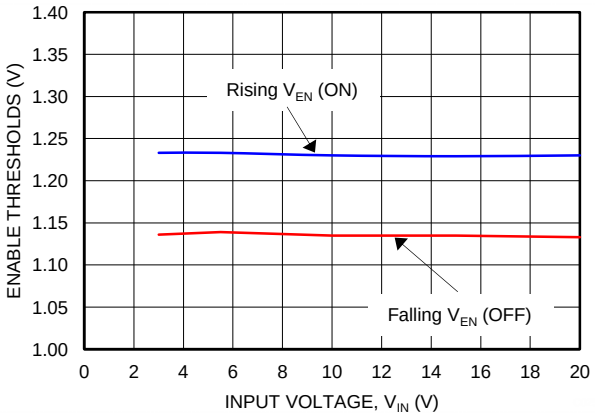


Figure 14. Enable Thresholds vs V_{IN}

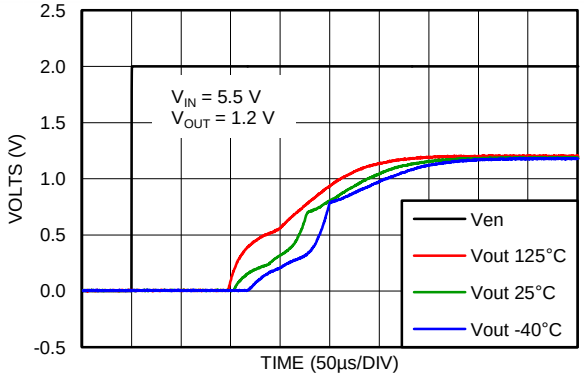


Figure 15. Start-up Time, V_{OUT} = 1.2 V

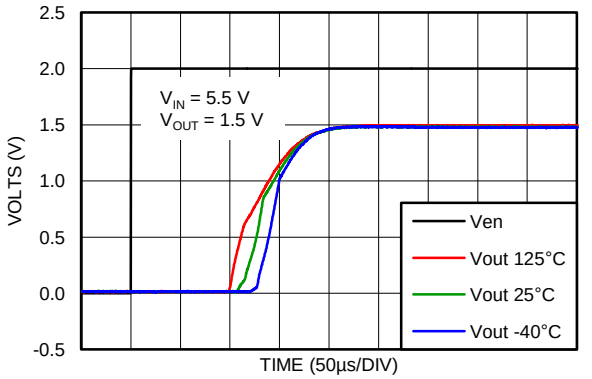


Figure 16. Start-up Time, V_{OUT} = 1.5V

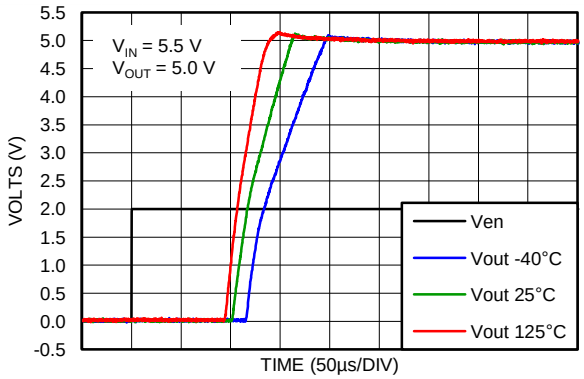


Figure 17. Start-up Time, V_{OUT} = 5.0 V

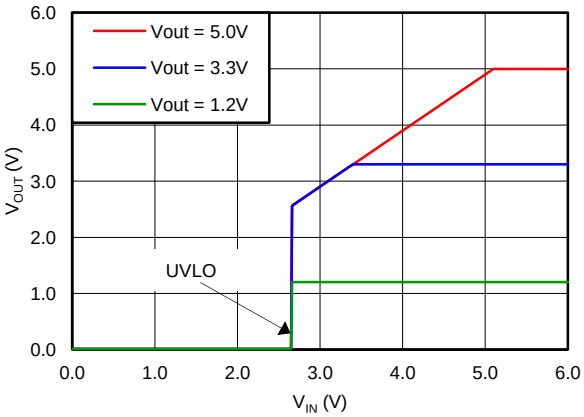


Figure 18. V_{OUT} vs. Rising V_{IN}

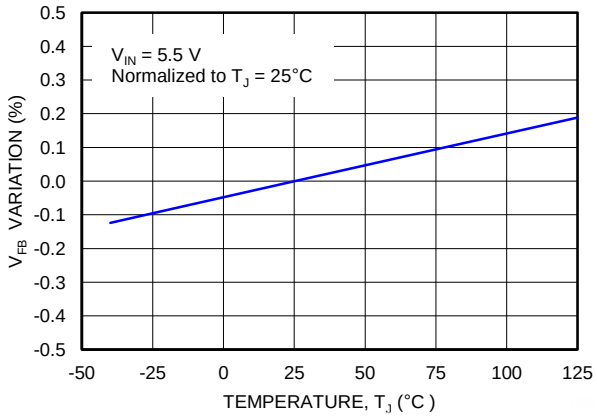


Figure 19. V_{FB} Variation vs. T_J

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

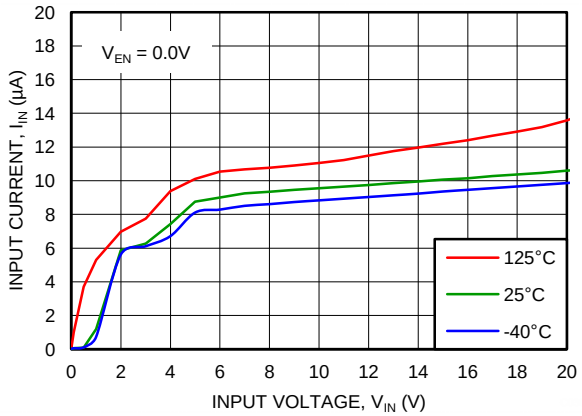


Figure 20. IN pin Current vs. V_{IN}

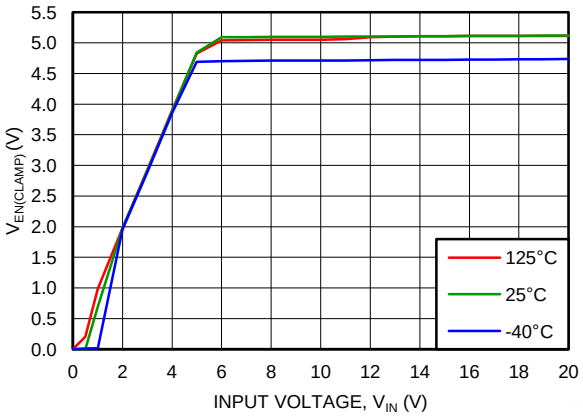


Figure 21. $V_{EN(CLAMP)}$ vs. V_{IN}

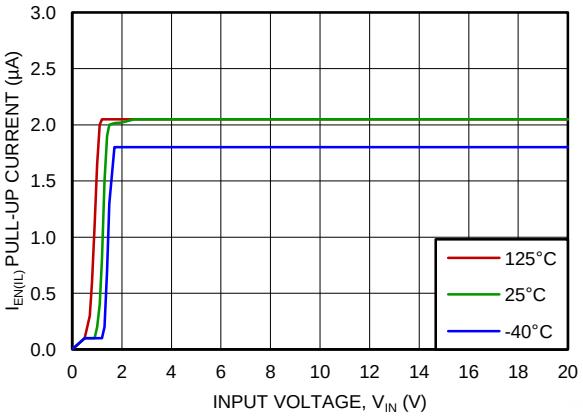


Figure 22. Enable pin Pull-up Current vs V_{IN}

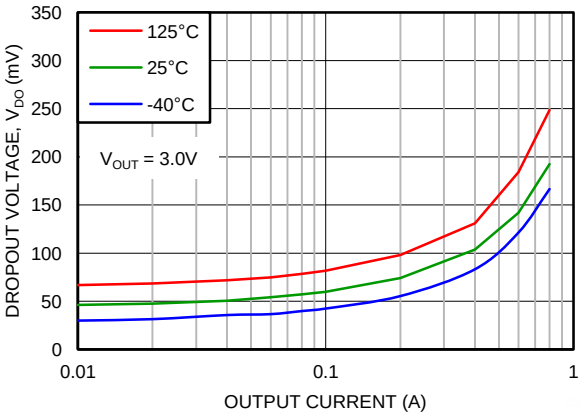


Figure 23. Dropout Voltage vs. Output Current

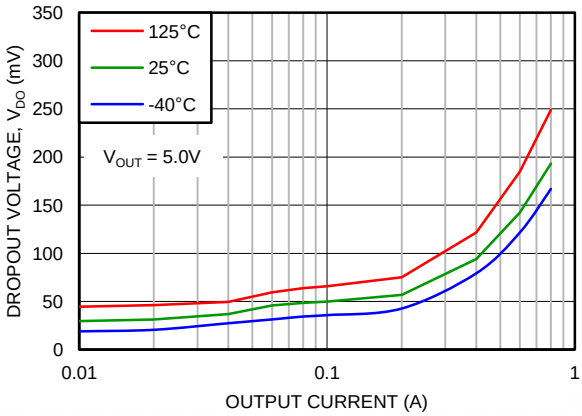


Figure 24. Dropout Voltage vs. Output Current

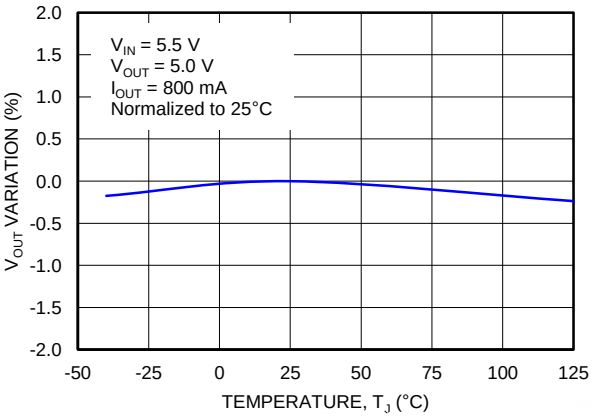


Figure 25. V_{OUT} Variation vs. T_J

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

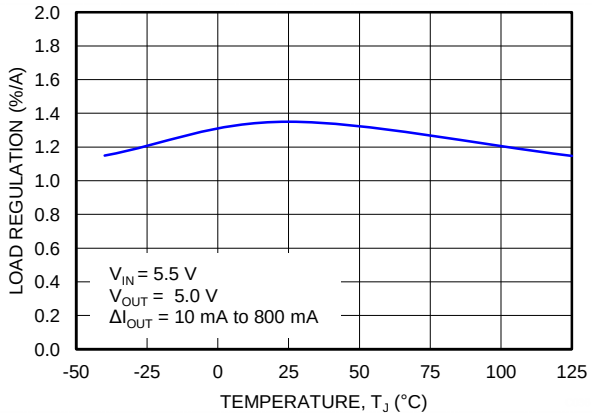


Figure 26. Load Regulation vs. T_J

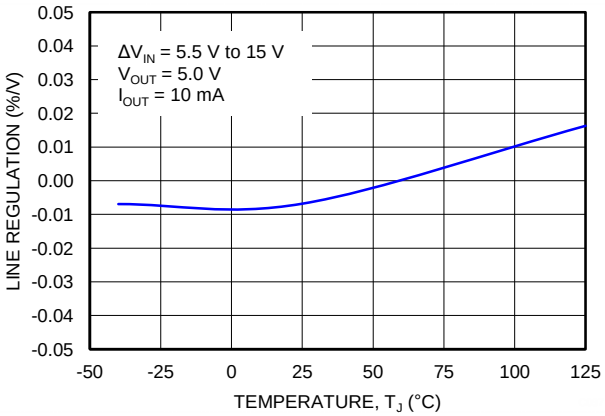


Figure 27. Line Regulation vs. T_J

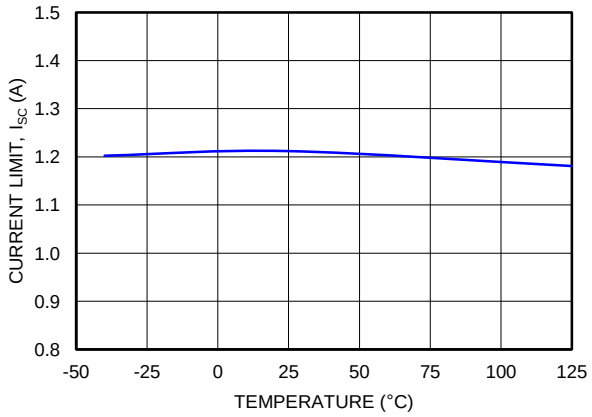


Figure 28. Current Limit, I_{SC} vs. T_J

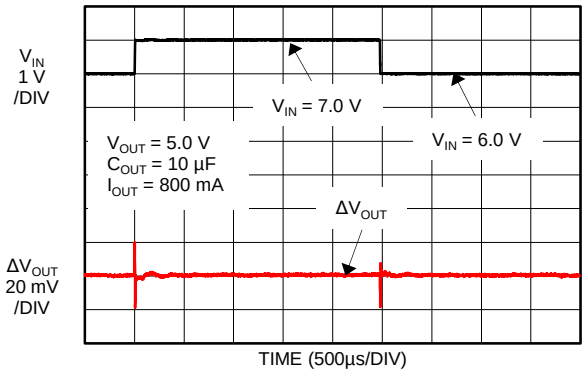


Figure 29. Line Transient, V_{OUT} = 5.0 V, I_{OUT} = 800 mA

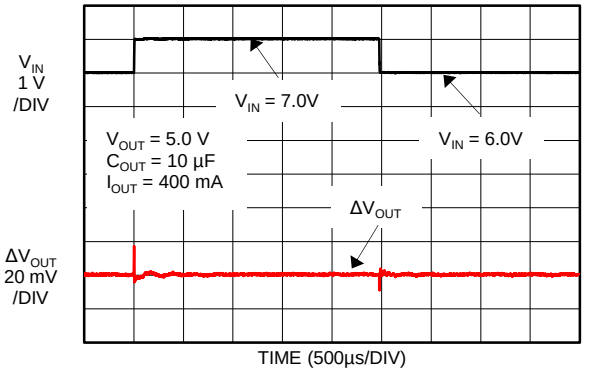


Figure 30. Line Transient, V_{OUT} = 5.0 V, I_{OUT} = 400 mA

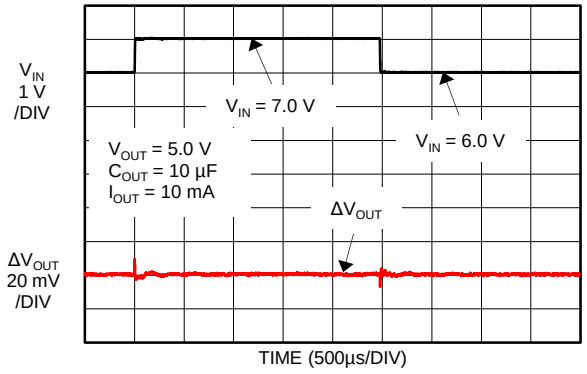


Figure 31. Line Transient, V_{OUT} = 5.0 V, I_{OUT} = 10 mA

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

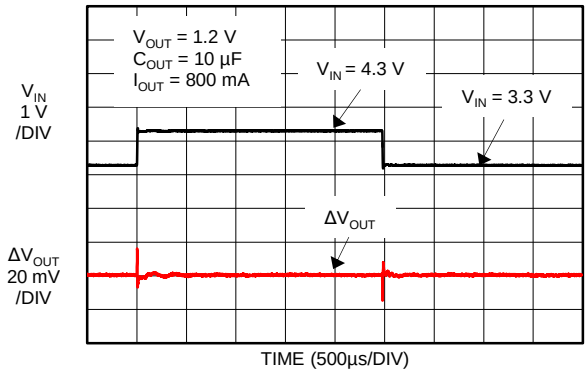


Figure 32. Line Transient, V_{OUT} = 1.2 V, I_{OUT} = 800 mA

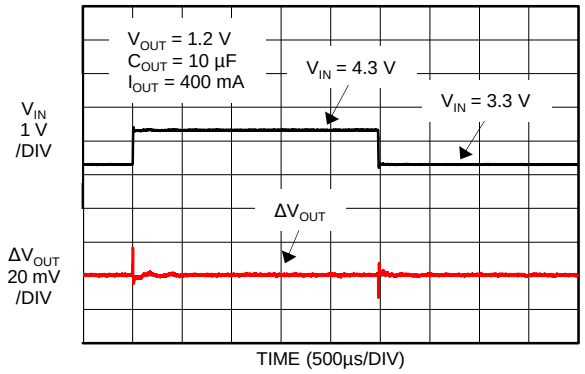


Figure 33. Line Transient, V_{OUT} = 1.2 V, I_{OUT}= 400 mA

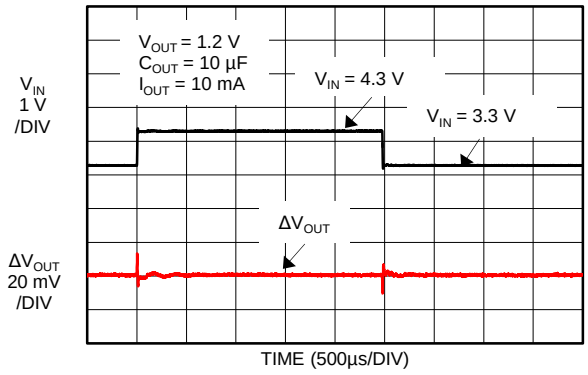


Figure 34. Line Transient, V_{OUT} = 1.2 V, I_{OUT}= 10 mA

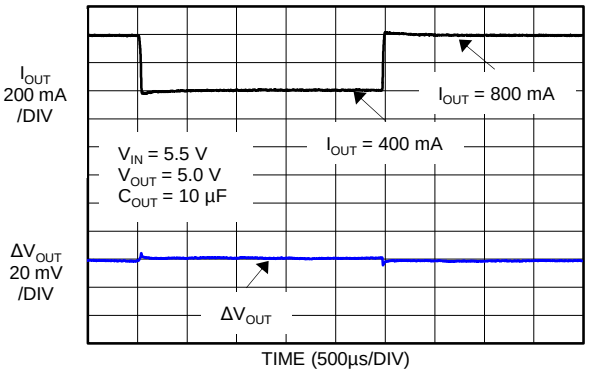


Figure 35. Load Transient, V_{OUT} = 5.0 V, I_{OUT} = 400 mA to 800 mA

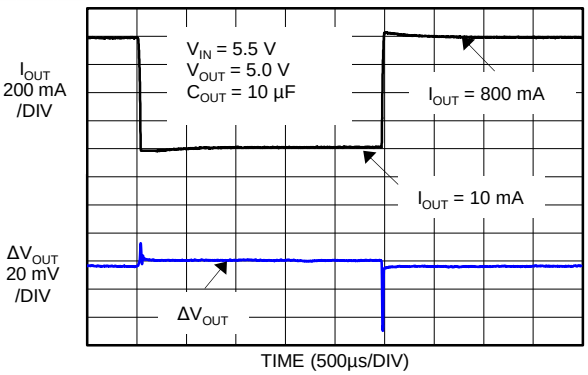


Figure 36. Load Transient, V_{OUT} = 5.0 V, I_{OUT} = 10 mA to 800 mA

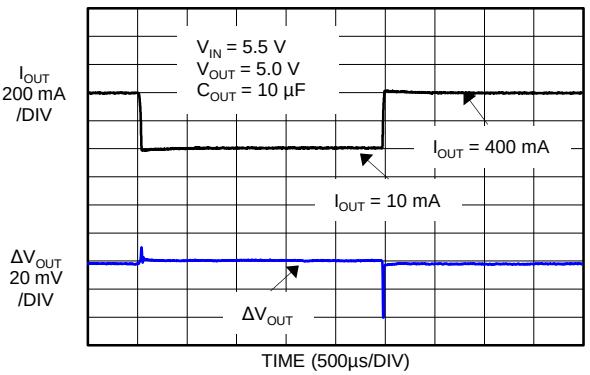


Figure 37. Load Transient, V_{OUT} = 5.0 V, I_{OUT} = 10 mA to 400 mA

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 5.5V, V_{OUT} = 5.0 V, I_{OUT} = 10 mA, C_{OUT} = 10 µF MLCC 16V X7R, T_J = 25°C.

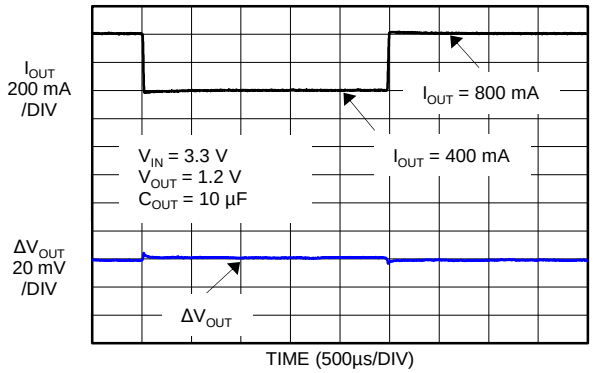


Figure 38. Load Transient, V_{OUT} = 1.2 V, I_{OUT} = 400 mA to 800 mA

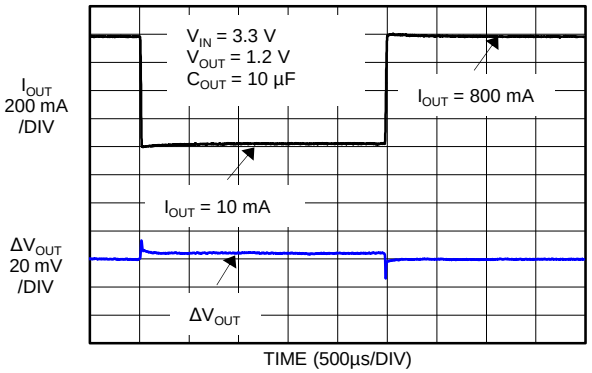


Figure 39. Load Transient, V_{OUT} = 1.2 V, I_{OUT} = 10 mA to 800 mA

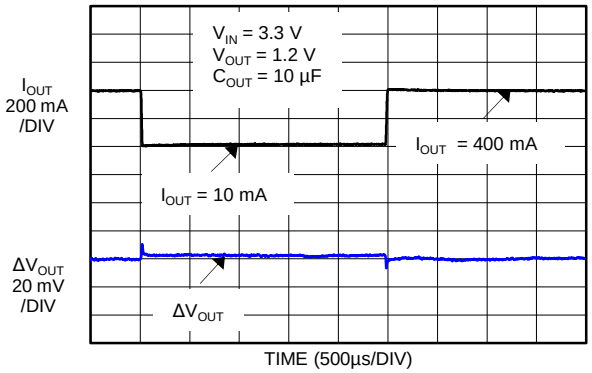
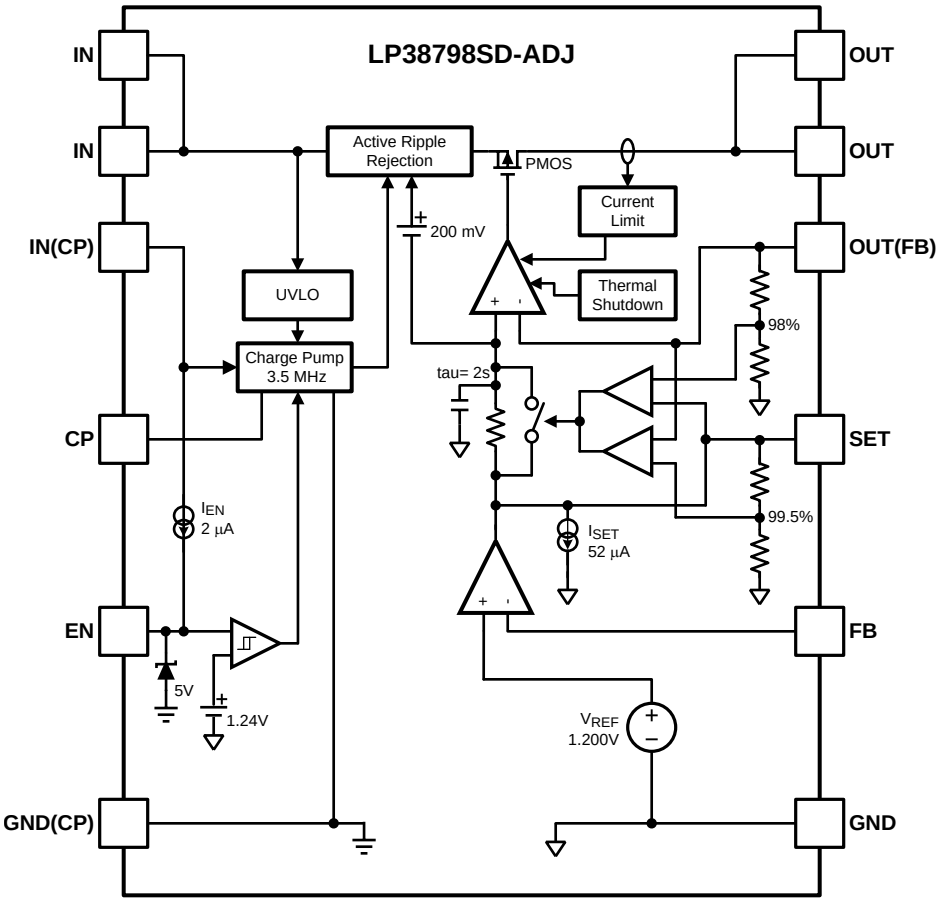


Figure 40. Load Transient, V_{OUT} = 1.2 V, I_{OUT}= 10 mA to 400 mA

APPLICATIONS INFORMATION

Functional Block Diagram



Package Information

The LP38798-ADJ is available in the 12-Lead WSON surface mount package that allows for increased power dissipation compared to the standard PSOP-8 and WQFN-8 packages.

External Capacitors

Like any low-dropout regulator, the LP38798-ADJ requires external capacitors for regulator stability. These capacitors must be correctly selected for optimum performance.

INPUT CAPACITOR: The minimum recommended input capacitance is 1 µF, ceramic or tantalum. However, if the LP38798 is operating in conditions where input ripple, fast changes in the input voltage, or large changes in the load current demand are expected, a minimum input capacitance of 10 µF is strongly recommended.

Ceramic capacitor tolerance and variations due temperature and applied voltage must be considered when selecting a capacitor to assure the minimum input capacitance requirement is met over the intended operating range.

The input capacitor must be located as close as physically possible to the input pin and returned to a clean analog ground. Any good quality tantalum capacitor may be used, while a ceramic capacitor should be X5R or X7R rated with appropriate adjustments due to the loss of capacitance value from the applied DC voltage.

Larger input capacitance values are encouraged if fast output current steps are expected, as this will minimize voltage drops at the input pin. However, if there is any PCB trace inductance between the bulk supply and the input pin it is recommended that a tantalum capacitor be placed in parallel with the ceramic input capacitor. This will help to damp out undesired ringing that may occur during input transient conditions.

OUTPUT CAPACITOR: The LP38798 requires an output capacitance of at least 1 µF, ceramic or tantalum, however a minimum output capacitance of 10 µF is strongly recommended if fast load transient conditions are expected. While the LP38798 is designed to work with Ceramic output capacitors, the output capacitor can be Ceramic, Tantalum, or a combination. The total output capacitance should be sized appropriately to handle any fast load current steps. Capacitance type, tolerance, ESR, as well as temperature and voltage characteristics, must be considered when selecting an output capacitor for the application.

Even though the LP38798 is stable with an output capacitance of 1 µF to 10 µF, a single output capacitor will generally not be able to provide the best PSRR performance across a wide frequency range. Multiple parallel capacitors, each with a different self-resonance frequency will provide better performance over a wider frequency range.

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground to the LP38798 GND pin.

Charge Pump

The charge pump is running when both the input voltage is above the UVLO threshold (2.65 V typical) and the EN pin voltage is above the $V_{EN(ON)}$ threshold (1.24 V typical). The typical charge pump operating frequency is 3.5 MHz.

A low leakage 10 nF X7R storage capacitor is required between the CP pin and ground to store the energy required for gate drive of the internal NMOS pass device.

Do not make any other connection to the CP pin. Loading this pin in any manner will degrade regulator performance. No external biasing may be applied to, or derived from, this pin, as permanent damage to the internal charge pump circuitry may occur.

Programming the Output Voltage

Current sourced from the SET pin, through R1 and R2, must be kept to less than 100 µA. The minimum allowed value for R2 is 12.9 kΩ;

$$I_{SET} = V_{FB} / R2 \quad (1)$$

$$R2_{MIN} = V_{FB(MAX)} / 100\ \mu A \quad (2)$$

$$R2_{MIN} = 12.9\ k\Omega; \quad (3)$$

The values for R1 and R2 may be adjusted as needed to achieve the desired output voltage as long as the value for R2 is no less than 12.9 kΩ. The maximum recommended value for R2 is 100 kΩ.

The following equation is used to determine the output voltage:

$$V_{OUT} = (V_{FB} \times (1 + (R1 / R2))) + V_{OS} \quad (4)$$

Alternately, the following formula can be used to determine the appropriate R1 value for a given R2 value:

$$R1 = R2 \times (((V_{OUT}) / V_{FB}) - 1) \quad (5)$$

The following table suggests some ±1% values for R1 and R2 for a range of output voltages using the typical V_{FB} value of 1.200V. This is not a definitive list, as other combinations exist that will provide similar, possibly better, performance.

Target V_{OUT}	R1	R2	Typical V_{OUT}
1.5 V	4.22 kΩ	16.9 kΩ	1.5 V
1.8 V	10.5 kΩ	21.0 kΩ	1.8 V
2.0 V	10.0 kΩ	15.0 kΩ	2.0 V
2.5 V	16.2 kΩ	15.0 kΩ	2.496 V
3.0 V	21.0 kΩ	14.0 kΩ	3.0 V
3.3 V	23.2 kΩ	13.3 kΩ	3.293 V
5.0 V	47.5 kΩ	15.0 kΩ	5.0 V

Noise Filter

Any noise at LP38798 SET pin is reduced by an internal passive, first order low-pass RC filter before it is passed to the output buffer stage. The low-pass filter has a -3dB cut-off frequency of approximately 0.08Hz.

To keep the low-pass filter from interfering with the output voltage rise time at start-up, a voltage comparator keeps the filter in a fast-charge mode while the output voltage (V_{OUT}) is less than 99.5% of the SET pin voltage (V_{SET}) . When the rising V_{OUT} is within 0.5% of V_{SET} the fast-charge mode ends, and V_{OUT} will rise the final 0.5% based on the RC time constant (τ = 2s) of the filter.

Should V_{OUT} be more than 2% above the V_{SET} voltage, a voltage comparator will put the filter into the fast-charge mode to allow the filter to discharge and V_{OUT} to fall a value closer to V_{SET}. When the falling V_{OUT} is within 2% of V_{SET} the fast-charge mode ends, and V_{OUT} will fall the final 2% based on the RC time constant (τ = 2s) of the filter.

If the input voltage has an extended rise time, the output voltage may exhibit a stair-case waveform as the fast-charge mode is activated and de-activated as V_{SET} rises with V_{IN}, and V_{OUT} follows. Once the V_{IN} has risen above the programmed V_{SET} voltage, and V_{OUT} is within 0.5% of V_{SET}, the stair-case behavior will end.

Enable Input Operation

The Enable pin (EN) is pulled high internally by a 2 µA (typical) current source from the IN pin, and internally clamped at 5V (typical) by a zener. Pulling the EN pin low, by sinking the I_{EN} current to ground, will turn the output off.

If the EN function is not needed the EN pin should be left open (floating). Do not connect the EN pin directly to V_{IN} if there is any possibility that V_{IN} might exceed 5.5V (i.e. EN pin AbsMax). If external pull-up is required, the external current into the EN pin should be limited to no more than 10 µA.

$$R_{PULL\text{-}UP} > (V_{PULL\text{-}UP} - 5V) / 10\ \mu A) \quad (6)$$

Thermal Shutdown

The LP38798 includes thermal protection that will shut-off the output current when activated by excessive device dissipation. Thermal shutdown (T_{SD}) will occur when the junction temperature has risen to 170°C. The junction temperature must fall typically 12°C for the output current to be restored. Junction temperature is calculated from the following formula:

$$T_J = (T_A + (P_D \times \theta_{J\text{-}A})) \quad (7)$$

Where the power being dissipated, P_D, is defined as:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) \quad (8)$$

Note that Thermal Shutdown is provided as a safety feature and is outside the specified Operating Ratings temperature range. Operation with a junction temperature (T_J) above 125°C is not recommended as the device behavior is not specified.

12-Lead WSON Package Thermal Considerations

The value of θ_{J-A} for the 12-lead WSON package is specifically dependent on PCB copper area, copper thickness, the number of layers, and thermal vias under the exposed thermal pad (DAP). Please refer to AN-1520 (Literature Number: SNVA183A) for general guidelines for mounting packages with exposed thermal pads.

Exceeding the maximum allowable power dissipation defined by the final θ_{J-A} will cause excessive die temperature, and the regulator may go into thermal shutdown.

Mounting the 12-lead WSON Package

The 12-Lead WSON package requires specific mounting techniques that are detailed in Texas Instruments Application Note # 1187 (Literature Number: SNOA401Q). Referring to the section ***PCB Design Recommendations*** in AN-1187, it should be noted that the pad style that should be used with the WSON DNT0012B package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the 12-lead WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the 12-lead WSON DNT0012B package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the twelve pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device leads 6 and 7 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP38798SD in the 12-Lead WSON DNT0012B package, the junction-to-case thermal resistance rating, θ_{JC}, is 5°C/W, where the case is defined as being on the bottom of the package at the center of the DAP.

The junction-to-ambient thermal performance, θ_{JA}, for the LP38798SD in the 12-lead WSON DNT0012B package, using the JEDEC JESD51 standards, is summarized in the following table:

LP38798SD-ADJ (12-lead WSON DNT0012B) Thermal Performance				
Board Type	**Thermal Vias**	**θ_{JA}**	**Ψ_{JB}**	**θ_{JC}**
JEDEC 2-Layer JESD 51-3	None	138°C/W	45.9°C/W	5°C/W
JEDEC 4-Layer JESD 51-7	1	51°C/W	26.1°C/W	5°C/W
	2	45°C/W	24.7°C/W	
	4	39°C/W	18.0°C/W	
	6	36°C/W	14.9°C/W	
	8	34°C/W	13.2°C/W	

Estimating the Junction Temperature

The EIA/JEDEC standard (JESD51-2) provides methodologies to estimate the junction temperature from external measurements (Ψ_{JB} references the temperature at the PCB, and Ψ_{JT} references the temperature at the top surface of the package) when operating under steady-state power dissipation conditions. These methodologies have been determined to be relatively independent of the copper thermal spreading area that may be attached to the package DAP when compared to the more typical θ_{JA}. Refer to ' Application Report : Semiconductor and IC Package Thermal Metrics' , Literature Number SPRA953B, for specifics.

Board Layout

The dynamic performance of the LP38798 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDO's may degrade the PSRR, noise, or transient performance of the LP38798.

Best performance is achieved by placing all of the components on the same side of the PCB as the LP38798, and as close as is practical to the LP38798 package. All component ground connections should be back to the LP38798 analog ground connection using as wide, and as short, of a copper trace as is practical. The connection from the FB pin to the V_{SET} resistors must be as short as possible as the FB pin is a high impedance input. Any trace length on the FB pin will act as an antenna.

Connections using long trace lengths, narrow trace widths, and connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A Ground Plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane serves two purposes : 1) Provide a circuit reference plane to assure accuracy, and 2) provides a thermal plane to remove heat from the LP38798 through thermal vias under the package DAP.

Typical Applications

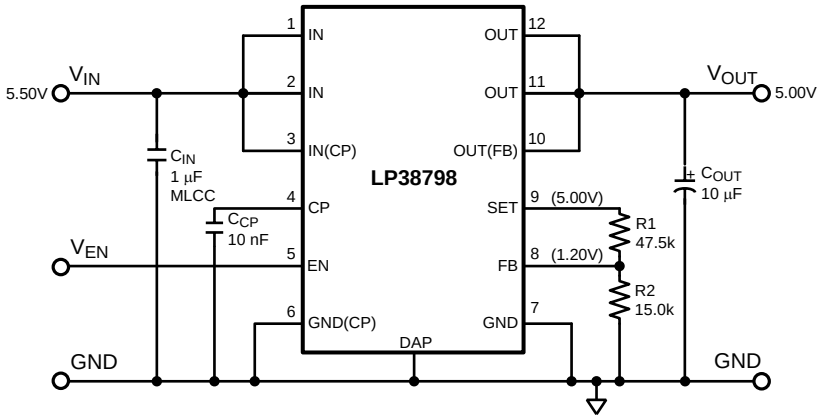


Figure 41. Typical Application, V_{OUT} = 5.0V

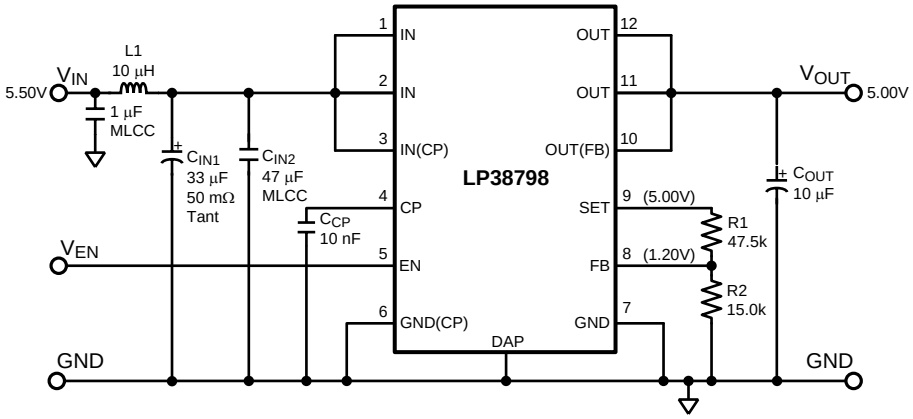


Figure 42. Improving PSRR at High Frequencies

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38798SD-ADJ/NOPB	ACTIVE	WSON	DNT	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00075B	Samples
LP38798SDE-ADJ/NOPB	ACTIVE	WSON	DNT	12	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00075B	Samples
LP38798SDX-ADJ/NOPB	ACTIVE	WSON	DNT	12	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00075B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

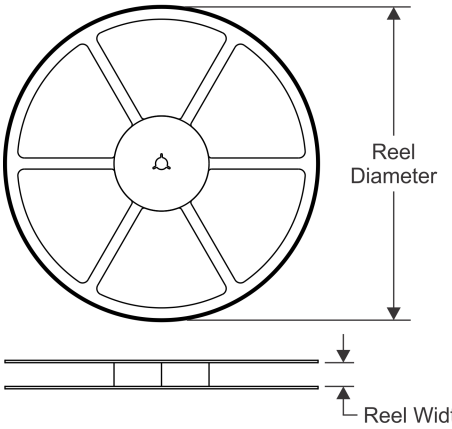
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

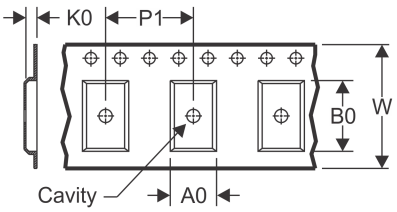
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

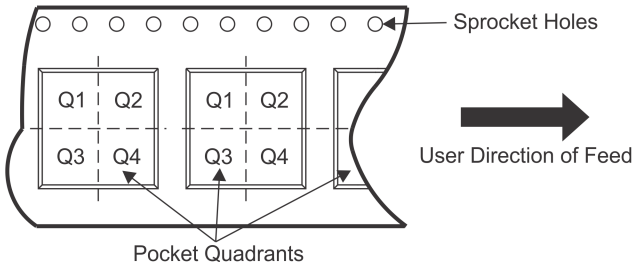


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

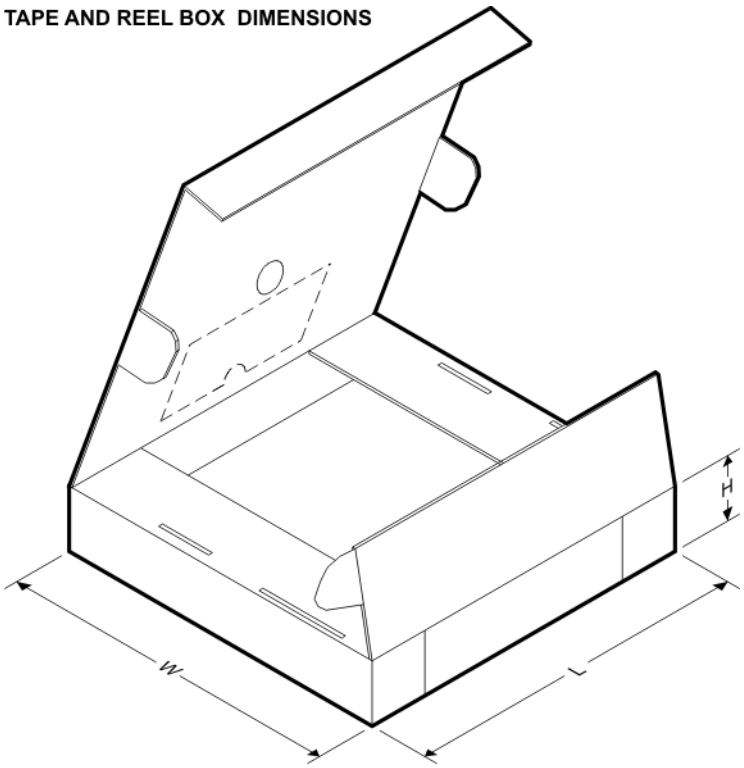
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38798SD-ADJ/NOPB	WSON	DNT	12	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP38798SDE-ADJ/NOPB	WSON	DNT	12	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP38798SDX-ADJ/NOPB	WSON	DNT	12	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



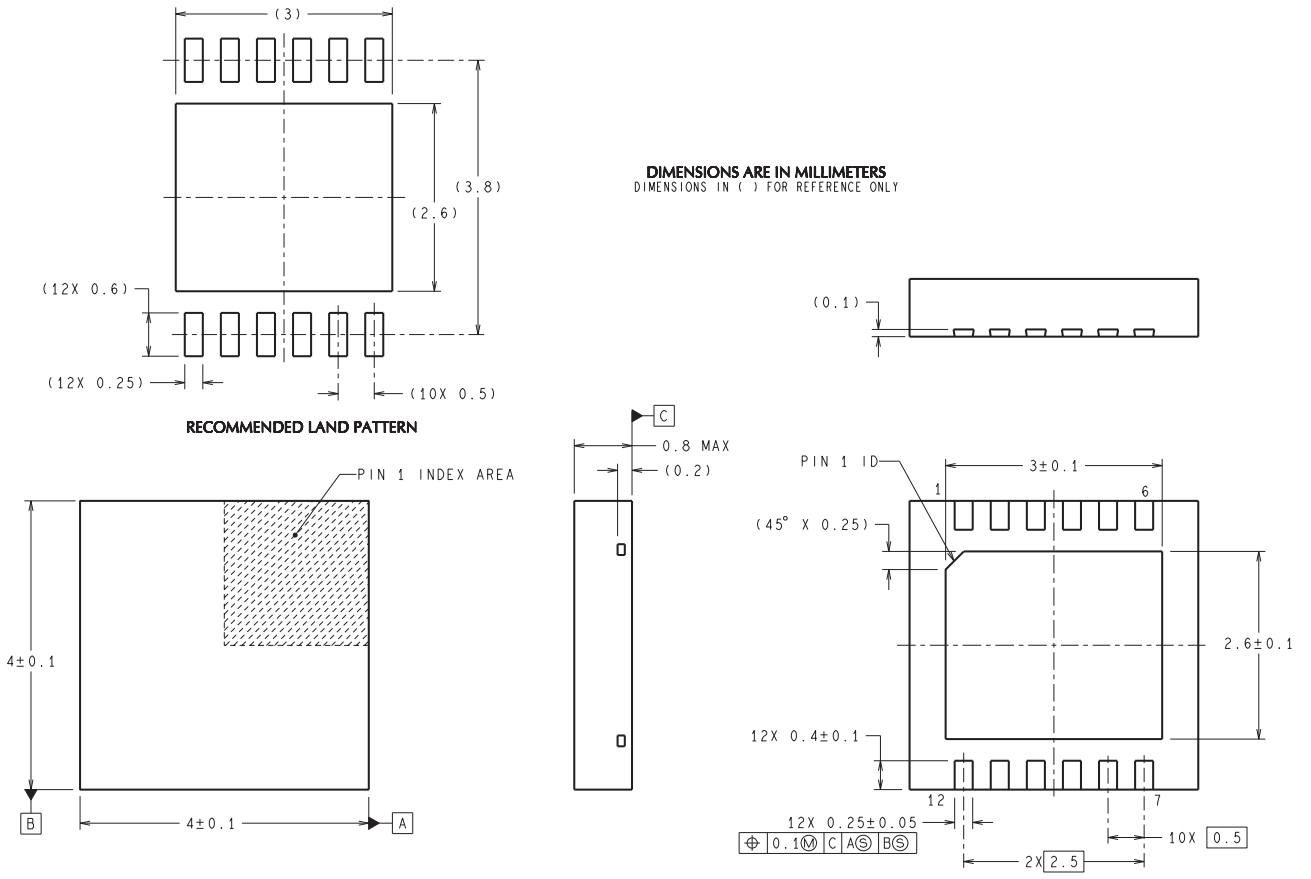
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38798SD-ADJ/NOPB	WSON	DNT	12	1000	210.0	185.0	35.0
LP38798SDE-ADJ/NOPB	WSON	DNT	12	250	210.0	185.0	35.0
LP38798SDX-ADJ/NOPB	WSON	DNT	12	4500	367.0	367.0	35.0

DNT0012B

WSON - 0.8mm max height

SON (PLASTIC SMALL OUTLINE - NO LEAD)



NOTES:
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to a thermal pad on the board for thermal and mechanical performance. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

IMPORTANT NOTICE

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