LP3952 6-Channel Color LED Driver with Audio Synchronization

Check for Samples: LP3952

FEATURES

- **Constant current and PWM controlled color LED drivers**
- **Maximum current 40mA / output in constant current mode, supports also switch mode control with 50 mA maximum current / output**
- **Complete audio synchronization for color/RGB LEDs with amplitude, frequency and speed optimization**
- **Command based lighting pattern generator for RGB LEDs**
- **Programmable ON/OFF blinking sequences for RGB1 outputs**
- **High efficiency Boost DC-DC converter with programmable V_{OUT} and f_{SW}**
- **I^2C compatible interface**
- **Possibility for external PWM dimming control**
- **Small package – 36-bump DSBGA, 3.0 x 3.0 x 0.65 mm**

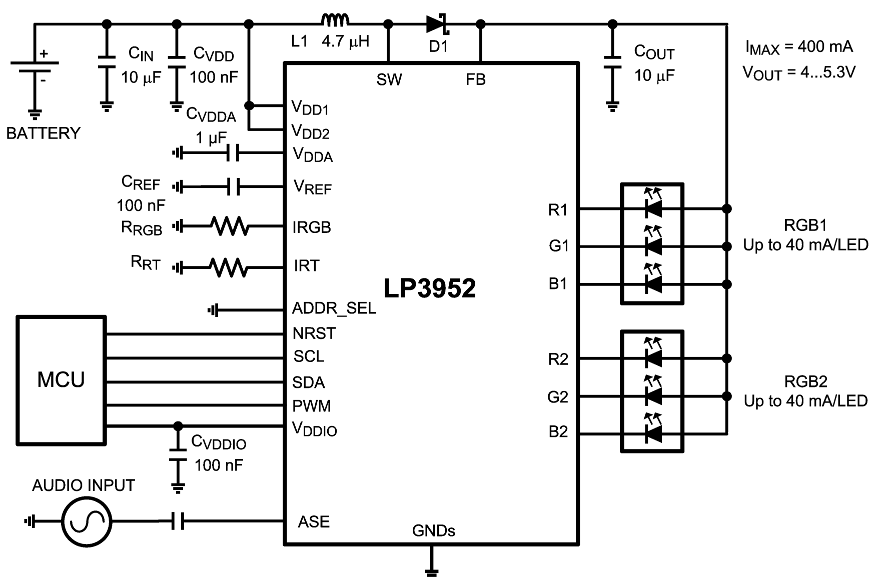
APPLICATIONS

- **Cellular Phones**
- **PDAs, MP3 players**

DESCRIPTION

LP3952 is a color LED driver for battery powered handheld devices. It drives any color LEDs including RGB LEDs, indicator LEDs and keypad backlight LEDs. The boost DC-DC converter drives high current loads with high efficiency. The stand-alone command based RGB controller is feature rich and easy to configure. Different lighting patterns and blinking sequences can be programmed to driver registers. Built-in audio synchronization feature allows user to synchronize the color LEDs to audio signal. LED lighting can be controlled either by audio signal amplitude or frequency. There are many controls available for audio synchronization to get desired lighting effect, including gain, speed, and different filter settings. The flexible I^2C interface allows easy control of LP3952. LED outputs can be also controlled with external PWM signal. Small DSBGA package together with minimum number of external components is a best fit for handheld devices.

Typical Application



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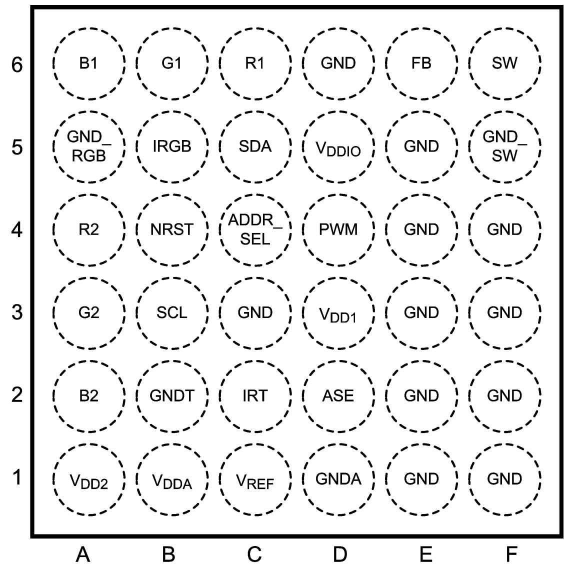
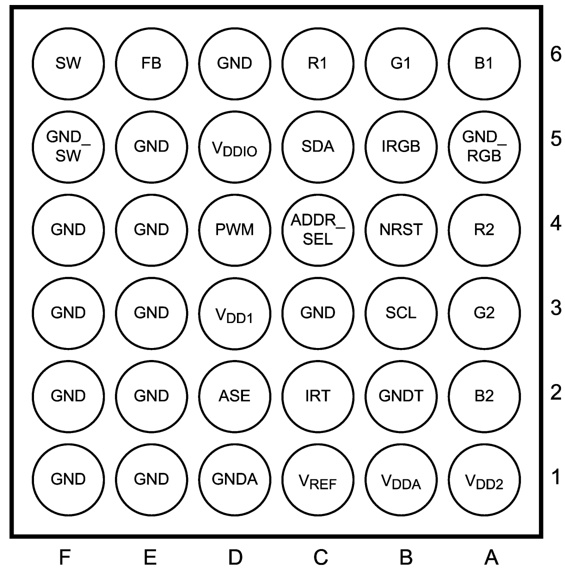
CONNECTION DIAGRAMS

36-bump DSBGA Package, 3.0 x 3.0 x 0.65 mm, 0.5 mm pitch
See Package Number YPG0036AAA



TOP VIEW



BOTTOM VIEW

PIN DESCRIPTIONS

Name	Pin No.	Type	Description
SW	6F	Output	Boost Converter Power Switch
FB	6E	Input	Boost Converter Feedback
GND	6D	Ground	Ground
R1	6C	Output	Red LED 1 Output
G1	6B	Output	Green LED 1 Output
B1	6A	Output	Blue LED 1 Output
GND_SW	5F	Ground	Power Switch Ground
GND	5E	Ground	Ground
V_{DDIO}	5D	Power	Supply Voltage for Logic Input/Output Buffers and Drivers
SDA	5C	Logic Input/Output	Serial Data In/Out (I^2C)
IRGB	5B	Input	Bias Current Set Resistor for RGB Drivers
GND_RGB	5A	Ground	Ground for RGB Currents
GND	4F	Ground	Ground
GND	4E	Ground	Ground
PWM	4D	Logic Input	External PWM Control for LEDs. Connect to GND if not used.
ADDR_SEL	4C	Logic Input	Address Select (I^2C)
NRST	4B	Logic Input	Reset Pin
R2	4A	Output	Red LED 2 Output
GND	3F	Ground	Ground
GND	3E	Ground	Ground
V_{DD1}	3D	Power	Supply Voltage
GND	3C	Ground	Ground
SCL	3B	Logic Input	Clock (I^2C)
G2	3A	Output	Green LED 2 Output
GND	2F	Ground	Ground

PIN DESCRIPTIONS (continued)

Name	Pin No.	Type	Description
GND	2E	Ground	Ground
ASE	2D	Input	Audio Synchronization Input
IRT	2C	Input	Oscillator Frequency Resistor
GNDT	2B	Ground	Ground
B2	2A	Output	Blue LED 2 Output
GND	1F	Ground	Ground
GND	1E	Ground	Ground
GNDA	1D	Ground	Ground for Analog Circuitry
VREF	1C	Output	Reference Voltage
V_{DDA}	1B	Power	Internal LDO Output
V_{DD2}	1A	Power	Supply Voltage

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)(3)

V (SW, FB, R1-2, G1-2, B1-2) (4) (5)	-0.3V to +7.2V
V_{DD1}, V_{DD2}, V_{DDIO}, V_{DDA}	-0.3V to +6.0V
Voltage on ASE, IRT, IRGB, VREF	-0.3V to V_{DD1}+0.3V with 6.0V max
Voltage on Logic Pins	-0.3V to V_{DDIO} +0.3V with 6.0V max
V(all other pins): Voltage to GND	-0.3V to 6.0V
I (V_{REF})	10 µA
I(R1, G1, B1, R2, G2, B2)	100 mA
Continuous Power Dissipation (6)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering) (7)	260°C
ESD Rating (8)	
Human Body Model:	2 kV

(1) All voltages are with respect to the potential at the GND pins.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(4) Battery/Charger voltage should be above 6V no more than 10% of the operational lifetime.
(5) Voltage tolerance of LP3952 above 6.0V relies on fact that V_{DD1} and V_{DD2} (2.8V) are available (ON) at all conditions. If V_{DD1} and V_{DD2} are not available (ON) at all conditions, Texas Instruments does not guarantee any parameters or reliability for this device.
(6) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typ.) and disengages at T_J=140°C (typ.).
(7) For detailed soldering specifications and information, please refer to Application Note AN1412 : DSBGA Wafer Level Chip Scale Package
(8) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings (1) (2)

V (SW, FB, R1-2, G1-2, B1-2)	0 to 6.0V
$V_{DD1,2}$ with external LDO	2.7 to 5.5V
$V_{DD1,2}$ with internal LDO	3.0 to 5.5V
V_{DDA}	2.7 to 2.9V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.

Operating Ratings [1] [2] (continued)

V_{DDIO}	1.65V to V_{DD1}
Voltage on ASE	0.1V to V_{DDA} –0.1V
Recommended Load Current	0 to 300 mA
Junction Temperature (T_J) Range	-30°C to +125°C
Ambient Temperature (T_A) Range [3]	-30°C to +85°C

(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance(θ_{JA}), YPG0036AAA Package [1]	60°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

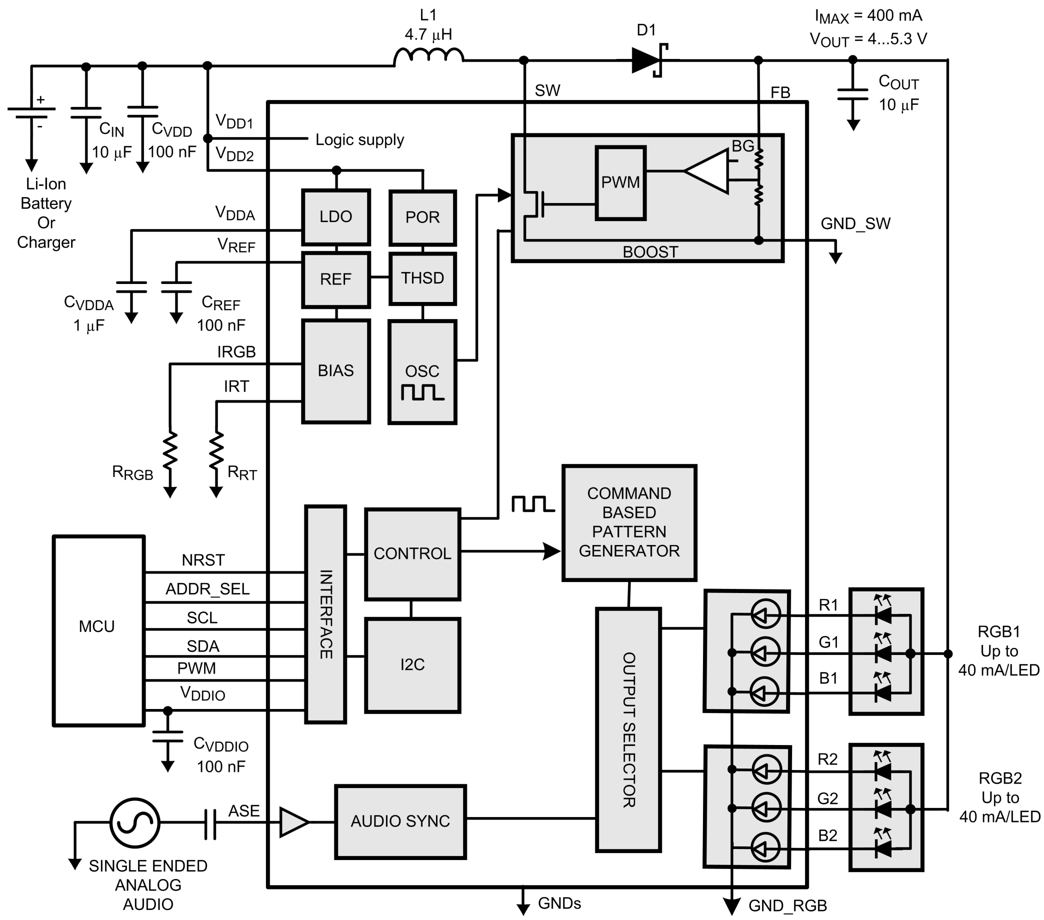
Electrical Characteristics [1] [2]

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (-30°C < T_A < +85°C). Unless otherwise noted, specifications apply to the LP3952 Block Diagram with: $V_{DD1} = V_{DD2}$ = 3.6V, V_{DDIO} = 2.8V, $C_{VDD} = C_{VDDIO}$ = 100 nF, $C_{OUT} = C_{IN}$ = 10 µF, C_{VDDA} = 1 µF, C_{REF} = 100 nF, L_1 = 4.7 µH, R_{RGB} = 5.6 kΩ and R_{RT} = 82 kΩ [3].

Parameter		Test Conditions	Min	Typ	Max	Units
I_{VDD}	Standby supply current ($V_{DD1} + V_{DD2}$)	NSTBY (bit) = L, NRST (pin) = H SCL=H, SDA = H		1	**8**	µA
	No-boost supply current ($V_{DD1} + V_{DD2}$)	NSTBY (bit) = H, EN_BOOST(bit) = L SCL = H, SDA = H Audio sync and LEDs OFF			**450**	µA
	No-load supply current ($V_{DD1} + V_{DD2}$)	NSTBY (bit) = H, EN_BOOST (bit) = H SCL = H, SDA = H Audio sync and LEDs OFF Autoload OFF			**1**	mA
	RGB drivers ($V_{DD1} + V_{DD2}$)	CC mode at R1, G1, B1 and R2, G2, B2 set to 15 mA		150		µA
		SW mode		150		
I_{VDD}	Audio synchronization ($V_{DD1} + V_{DD2}$)	Audio sync ON				µA
		$V_{DD1,2}$ = 2.8V		390		
		$V_{DD1,2}$ = 3.6V		700		
I_{VDDIO}	V_{DDIO} Standby Supply current	NSTBY (bit)=L SCL = H, SDA = H			**1**	µA
I_{EXT_LDO}	External LDO output current (V_{DD1}, V_{DD2}, V_{DDA})	7V tolerant application only I_{BOOST} = 300 mA			**6.5**	mA
V_{DDA}	Output voltage of internal LDO for analog parts	[4]	**2.72**	2.80	**2.88**	V
			-3		**+3**	%

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) V_{DDA} output is not recommended for external use.

BLOCK DIAGRAM



MODES OF OPERATION

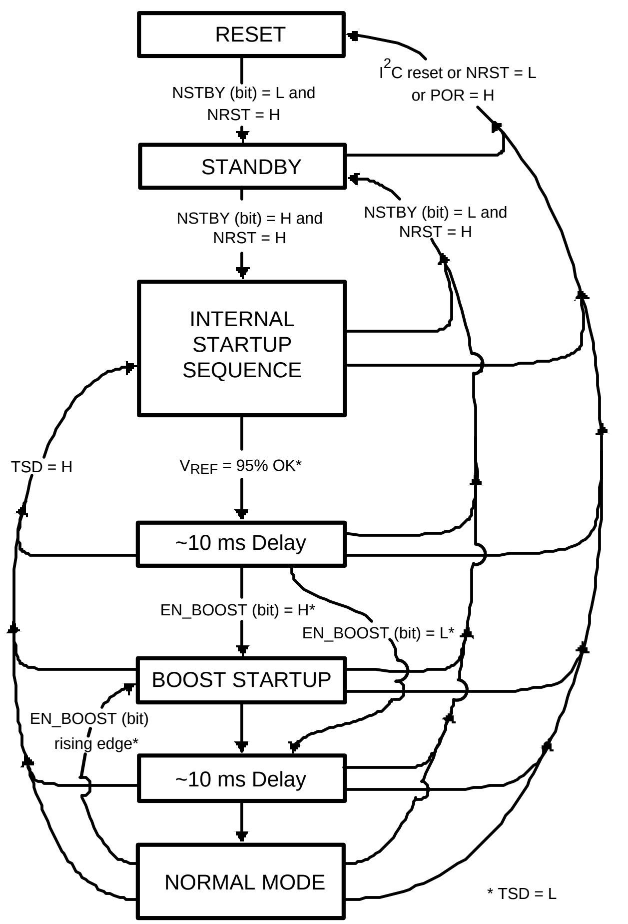
RESET: In the RESET mode all the internal registers are reset to the default values and the chip goes to STANDBY mode after reset. NSTBY control bit is low after reset by default. Reset is active always if NRST input pin is low or internal Power On Reset is active. LP3952 can be also reset by writing any data to Reset Register in address 60H. Power On Reset (POR) will activate during the chip startup or when the supply voltage V_{DD2} falls below 1.5V. Once V_{DD2} rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode.

STANDBY: The STANDBY mode is entered if the register bit NSTBY is LOW. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after power up.

STARTUP: When NSTBY bit is written high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (Vref, Bias, Oscillator etc..). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in PFM mode during the 10 ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH or from Normal mode when EN_BOOST is written HIGH. During the 10 ms Boost Startup time all LED outputs are switched off to ensure smooth start-up.

NORMAL: During NORMAL mode the user controls the chip using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write



Magnetic Boost DC/DC Converter

The LP3952 Boost DC/DC Converter generates a 4.0 – 5.3V voltage for the LEDs from single Li-Ion battery (3V…4.5V). The output voltage is controlled with an 8-bit register in 9 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter has three options for switching frequency, 1 MHz, 1.67 MHz and 2 MHz (default), when timing resistor RT is 82 kΩ. Timing resistor defines the internal oscillator frequency and thus directly affects boost frequency and all circuit's internally generated timing (RGB patterns).

The LP3952 Boost Converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An active load is used to remove the excess charge from the output capacitor at very light loads. At very light load and when input and output voltages are very close to each other, the pulse skipping is not completely eliminated. Output voltage should be at least 0.5V higher than input voltage to avoid pulse skipping. Reducing the switching frequency will also reduce the required voltage difference.

Active load can be disabled with the en_autoload bit. Disabling will increase the efficiency at light loads, but the downside is that pulse skipping will occur. The Boost Converter should be stopped when there is no load to minimise the current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop.

The following figure shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
   - Keeps the output below breakdown voltage.
   - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
   - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection. Prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.

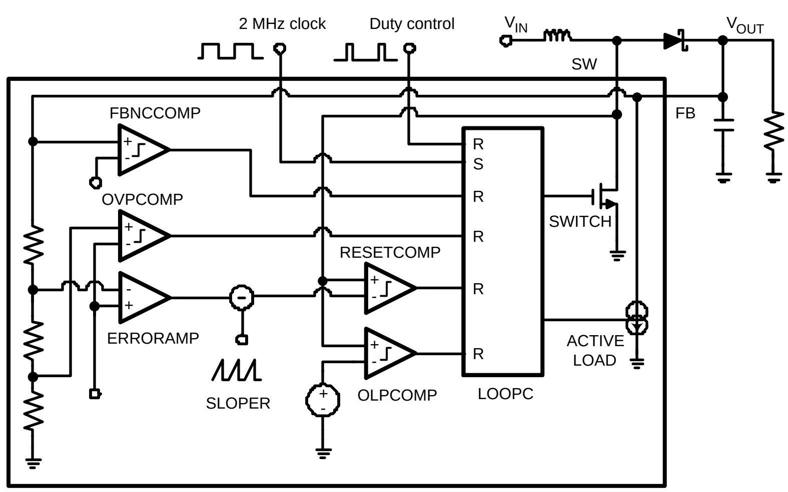


Figure 1. Boost Converter Topology

Magnetic Boost DC/DC Converter Electrical Characteristics

Parameter		Test Conditions	Min	Typ	Max	Units
I_{LOAD}	Load Current	$3.0V \le V_{IN}$ $V_{OUT} = 5V$	0		300	mA
		$3.0V \le V_{IN}$ $V_{OUT} = 4V$	0		400	
V_{OUT}	Output Voltage Accuracy (FB Pin)	$3.0V \le V_{IN} \le V_{OUT} - 0.5$ $V_{OUT} = 5.0V$	**−5**		**+5**	%
	Output Voltage (FB Pin)	$1\ mA \le I_{LOAD} \le 300\ mA$ $V_{IN} > 5V + V_{(SCHOTTKY)}$		$V_{IN}–V_{(SCHOTTKY)}$		V
RDS_{ON}	Switch ON Resistance	$V_{DD1,2} = 2.8V$, $I_{SW} = 0.5A$		0.4	**0.8**	Ω
f_{boost}	PWM Mode Switching Frequency	RT = 82 kΩ freq_sel[2:0] = 1XX		2		MHz
	Frequency Accuracy	2.7 ≤ VDDA ≤ 2.9	−6	±3	+6	%
		RT = 82 kΩ	**−9**		**+9**	
t_{PULSE}	Switch Pulse Minimum Width	no load		25		ns
$t_{STARTUP}$	Startup Time	Boost startup from STANDBY		10		ms
I_{SW_MAX}	SW Pin Current Limit		700	800	900	mA
			550		**950**	

BOOST STANDBY MODE

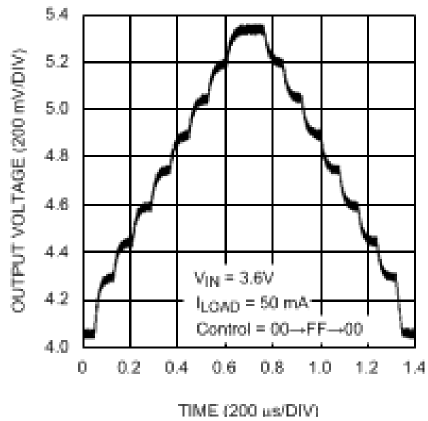
User can stop the Boost Converter operation by writing the Enables register bit EN_BOOST low. When EN_BOOST is written high, the converter starts for 10 ms in PFM mode and then goes to PWM mode.

BOOST OUTPUT VOLTAGE CONTROL

User can control the boost output voltage by boost output 8-bit register.

Boost Output [7:0] Register 0DH		Boost Output Voltage (typical)
Bin	Hex	
0000 0000	00	4.00
0000 0001	01	4.25
0000 0011	03	4.40
0000 0111	07	4.55
0000 1111	0F	4.70
0001 1111	1F	4.85
0011 1111	**3F**	**5.00 Default**
0111 1111	7F	5.15
1111 1111	FF	5.30

Boost Output Voltage Control



BOOST FREQUENCY CONTROL

freq_sel[2:0]	frequency
1XX	2.00 MHz
01X	1.67 MHz
001	1.00 MHz

Register ‘boost freq’ (address 0EH). Register default value after reset is 07H.

Boost Converter Typical Performance Characteristics

Vin = 3.6V, Vout = 5.0V if not otherwise stated

Boost Converter Efficiency

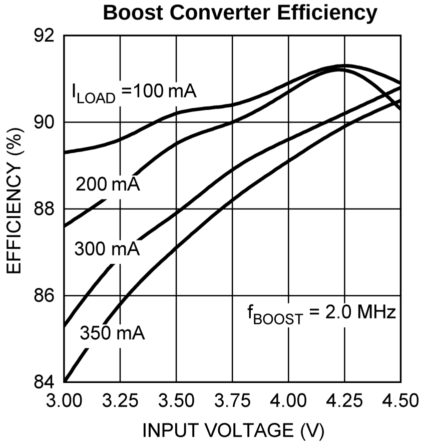


Figure 2.

Boost Typical Waveforms at 100mA Load

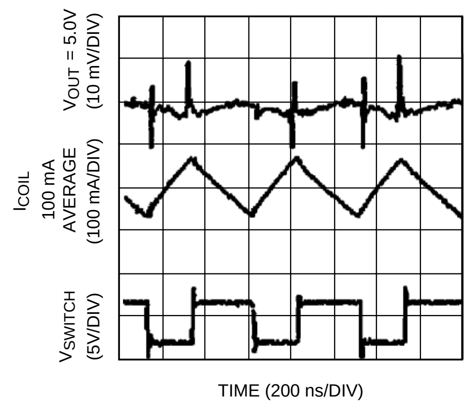


Figure 3.

Battery Current vs Voltage

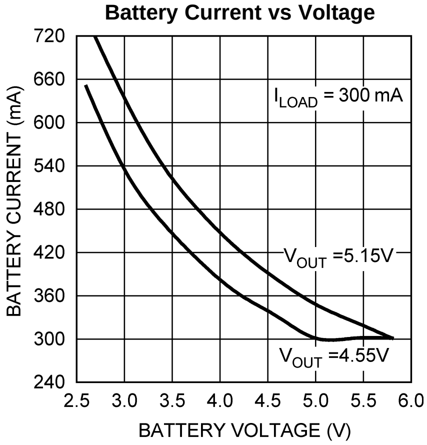


Figure 4.

Battery Current vs Voltage

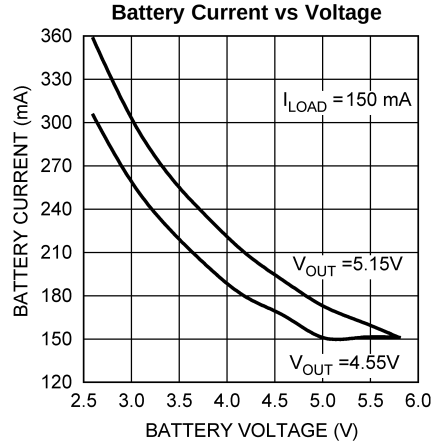


Figure 5.

Boost Line Regulation

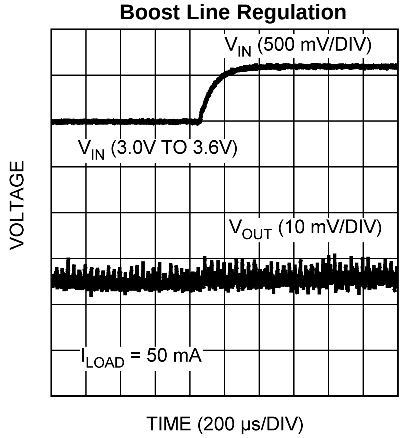


Figure 6.

Boost Startup with No Load

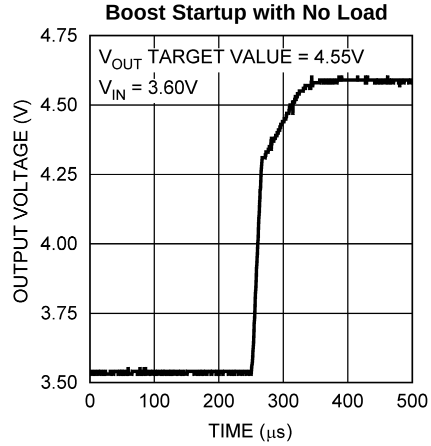


Figure 7.

Boost Converter Typical Performance Characteristics (continued)

Vin = 3.6V, Vout = 5.0V if not otherwise stated

Boost Load Transient, 50 mA–100 mA

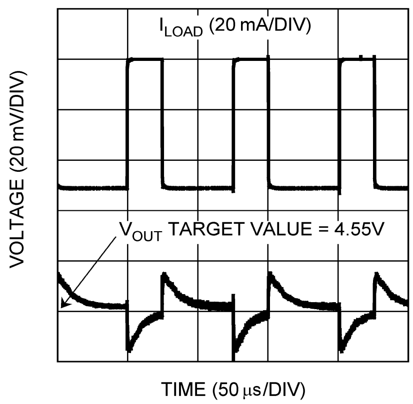


Figure 8.

Boost Switching Frequency

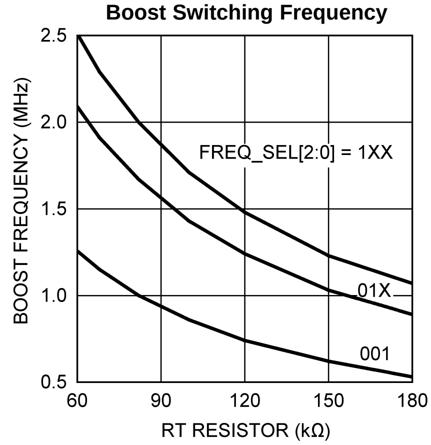


Figure 9.

Output Voltage vs Load Current

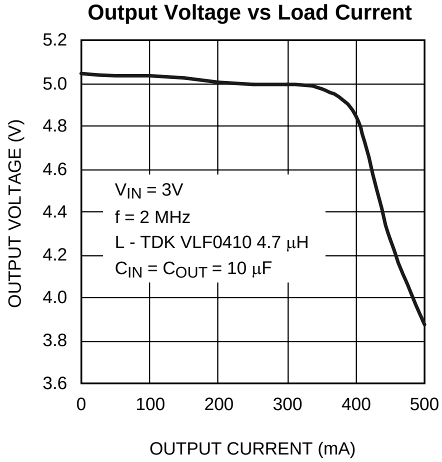


Figure 10.

Efficiency at Low Load vs Autoload

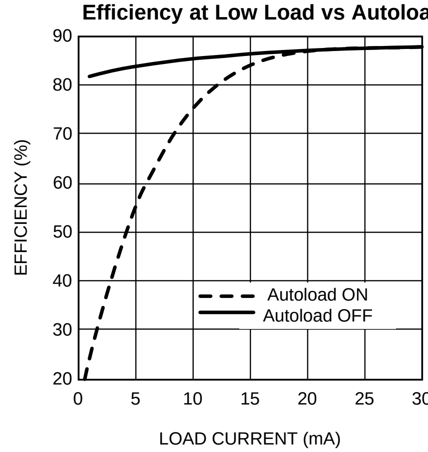


Figure 11.

FUNCTIONALITY OF COLOR LED OUTPUTS (R1, G1, B1; R2, G2, B2)

The LP3952 has 2 sets of RGB/color LED outputs. Both sets have 3 outputs and the sets can be controlled in 4 different ways:

1. Command based pattern generator control (internal PWM)
2. Audio synchronization control
3. Programmable ON/OFF blinking sequences for RGB1
4. External PWM control

By using **command based pattern generator** user can program any kind of color effect patterns. LED intensity, blinking cycles and slopes are independently controlled with 8 16-bit commands. Also real time commands are possible as well as loops and step by step control. If analog audio is available on system, the user can use **audio synchronization** for synchronizing LED blinking to the music. The different modes together with the various sub modes generate very colorful and interesting lighting effects. **Direct ON/OFF** control is mainly for switching on and off LEDs. **External PWM control** is for applications where external PWM signal is available and required to control the color LEDs. PWM signal can be connected to any color LED separately as shown later.

COLOR LED CONTROL MODE SELECTION

The RGB_SEL[1:0] bits in the Enables register (08H) control the output modes for RGB1 (R1, G1, B1) and RGB2 (R2, G2, B2) outputs as seen in the following table.

RGB_SEL[1:0]	Audio sync	Pattern generator	Blinking control
00	-	RGB1 & RGB2	-
01	-	RGB2	RGB1
10	RGB2	RGB1	-
11	RGB1 & RGB2	-	-

RGB Control register (00H) has control bits for direct on/off control of all color LEDs. Note that the LEDs have to be turned on in order to control them with audio synchronization or pattern generator.

The external PWM signal can control any LED depending on the control register setup. External PWM signal is connected to PWM pin. The controls are in the Ext. PWM Control register (address 07H):

Ext. PWM Control (07H)		
r1_pwm	bit 5	PWM controls R1 output
g1_pwm	bit 4	PWM controls G1 output
b1_pwm	bit 3	PWM controls B1 output
r2_pwm	bit 2	PWM controls R2 output
g2_pwm	bit 1	PWM controls G2 output
b2_pwm	bit 0	PWM controls B2 output

CURRENT CONTROL OF COLOR LED OUTPUTS (R1, R2, G1, G2, B1, B2)

Both RGB output sets can be separately controlled as constant current sinks or as switches. This is done using cc_rgb1/2 bits in the RGB control register. In constant current mode one or both RGB output sets are controlled with constant current sinks (no external ballast resistors required). The maximum output current for both drivers is set by one external resistor R_{RGB}. User can decrease the maximum current for an individual LED driver by programming as shown later.

The maximum current for all RGB drivers is set with R_{RGB}. The equation for calculating the maximum current is:

$$I_{MAX} = 100 \times 1.23V / (R_{RGB} + 50\Omega) \quad (1)$$

where:

I_{MAX} - maximum RGB current in any RGB output in constant current mode

1.23V - reference voltage

100 - internal current mirror multiplier

R_{RGB}- resistor value in Ohms

50Ω - internal resistor in the I_{RGB} input

For example if 22mA is required for maximum RGB current R_{RGB} equals to:

$$R_{RGB}=100\times1.23V / I_{MAX}-50\Omega=123V / 0.022A-50\Omega=\mathbf{5.54k\Omega} \quad (2)$$

Each individual RGB output has a separate maximum current programming. The control bits are in registers **RGB1 max current** and **RGB2 max current** (12H and 13H) and programming is shown in table below. The default value after reset is 00b.

IR1[1:0], IG1[1:0], IB1[1:0], IR2[1:0], IG2[1:0], IB2[1:0]	Maximum Current/Output
00	0.25 × I_{MAX}
01	0.50 × I_{MAX}
10	0.75 × I_{MAX}
11	1.00 × I_{MAX}

SWITCH MODE

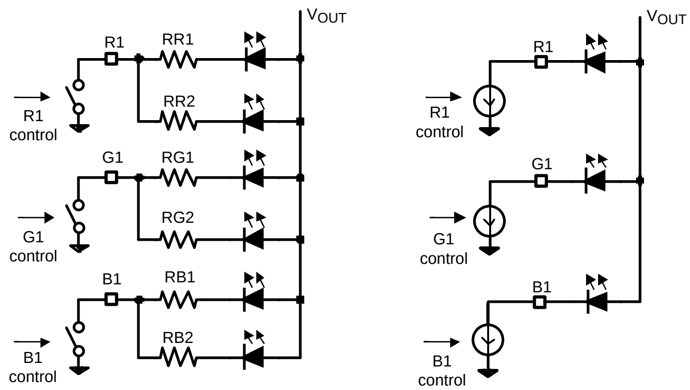
The switch mode is used if there is a need to connect parallel LEDs to output or if the RGB output current needs to be increased.

Please note that the switch mode **requires an external ballast resistors** at each output to limit the LED current.

The switch/current mode and on/off controls for RGB are in the RGB_ctrl register (00H).

Table 1. RGB_ctrl Register (00H) (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

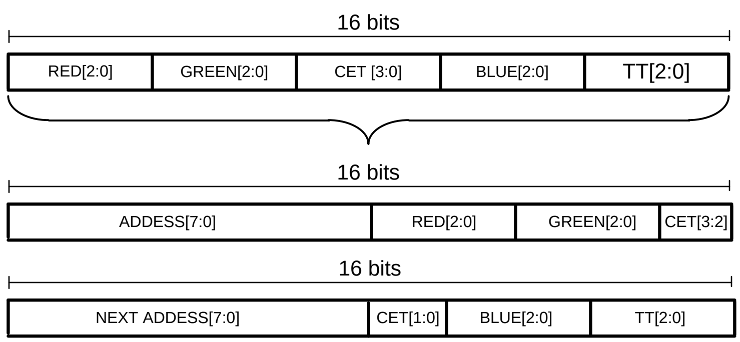
CC_RGB1	bit7	1	R1, G1 and B1 are switches → limit current with ballast resistor
		0	R1, G1 and B1 are constant current sinks, current limited internally
CC_RGB2	bit6	1	R2, G2 and B2 are switches → limit current with ballast resistor
		0	R2, G2 and B2 are constant current sinks, current limited internally
r1sw	bit5	1	R1 is on
		0	R1 is off
g1sw	bit4	1	G1 is on
		0	G1 is off
b1sw	bit3	1	B1 is on
		0	B1 is off
r2sw	bit2	1	R2 is on
		0	R2 is off
g2sw	bit1	1	G2 is on
		0	G2 is off
b2sw	bit0	1	B2 is on
		0	B2 is off



RGB1 output as switch (SW) | **RGB1 output as a constant current sink (CC)**

Command Based Pattern Generator for Color LEDs (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

The LP3952 has an unique stand-alone command based pattern generator with 8 user controllable 16-bit commands. Since registers are 8-bit long one command requires 2 write cycles. Each command has intensity level for each LED, command execution time (CET) and transition time (TT) as seen in the following figures.



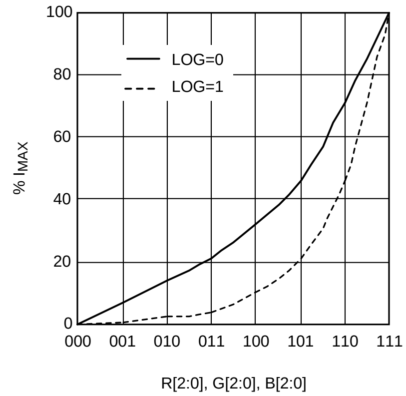
COMMAND REGISTER WITH 8 COMMANDS (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

COMMAND 1	ADDRESS 50H	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 51H	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 2	ADDRESS 52H	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 53H	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 3	ADDRESS 54H	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 55H	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 4	ADDRESS 56H	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 57H	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 5	ADDRESS 58H	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 59H	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 6	ADDRESS 5AH	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 5BH	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 7	ADDRESS 5CH	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 5DH	CET1	CET0	B2	B1	B0	TT2	TT1	TT0
COMMAND 8	ADDRESS 5EH	R2	R1	R0	G2	G1	G0	CET3	CET2
	ADDRESS 5FH	CET1	CET0	B2	B1	B0	TT2	TT1	TT0

COLOR INTENSITY CONTROL (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Each color has 3-bit intensity level. Level control is logarithmic, 2 curves are selectable. The LOG bit in register 11H defines the curve used as seen in the following table.

R[2:0], G[2:0], B[2:0]	CURRENT [% × $I_{MAX(COLOR)}$]	
	LOG=0	LOG=1
000	0	0
001	7	1
010	14	2
011	21	4
100	32	10
101	46	21
110	71	46
111	100	100



COMMAND EXECUTION TIME (CET) AND TRANSITION TIME (TT) (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

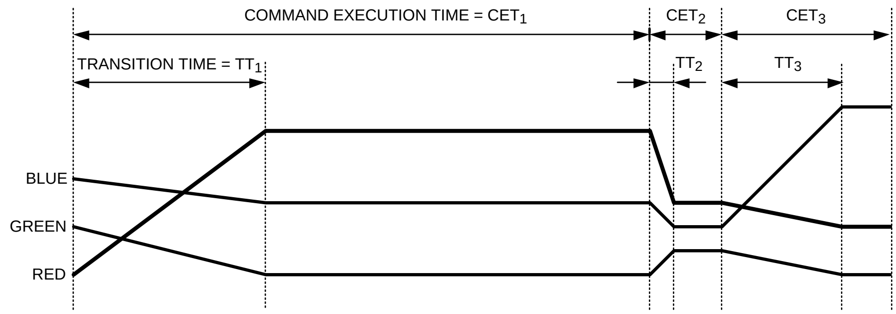
The command execution time CET is the duration of one single command. Command execution times are defined as follows, when R_T=82kΩ:

CET [3:0]	CET duration, ms
0000	197
0001	393
0010	590
0011	786
0100	983
0101	1180
0110	1376
0111	1573
1000	1769
1001	1966
1010	2163
1011	2359
1100	2556
1101	2753
1110	2949
1111	3146

Transition time TT is duration of transition from the previous RGB value to programmed new value. Transition times are defined as follows:

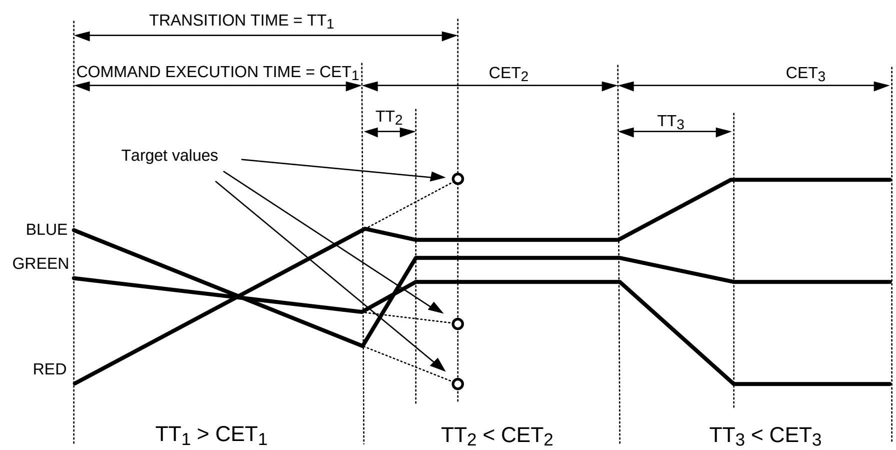
TT [2:0]	Transition time, ms
000	0
001	55
010	110
011	221
100	442
101	885
110	1770
111	3539

The figure below shows an example of RGB CET and TT times.



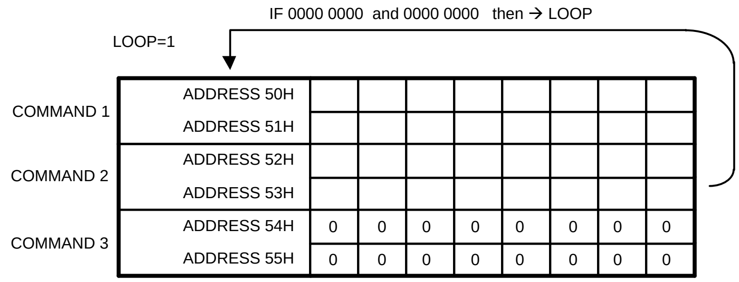
TT < CET

The command execution time also may be less than the transition time – the figure below illuminates this case.



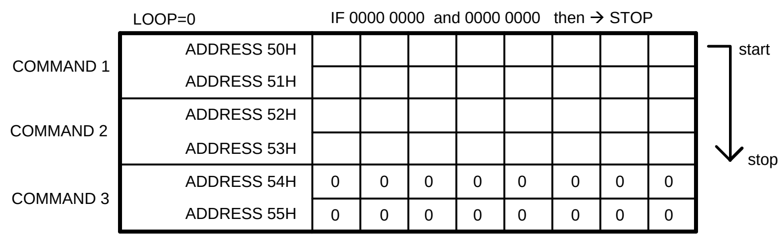
LOOP CONTROL (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Pattern generator commands can be looped using the LOOP bit (D1) in Pattern gen ctrl register (11H). If LOOP=1 the program will be looped from the command 8 register or if there is 0000 0000 and 0000 0000 in one command register. The loop will start from command 1 and continue until stopped by writing rgb_start=0 or loop=0. The example of loop is shown in following figure:



SINGLE PROGRAM (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

If control bit LOOP=0 the program will start from Command 1 and run to either last command or to empty “0000 0000 / 0000 0000” command.



The LEDs maintain the brightness of the last command when the single program stops. Changes in command register will not be effective in this phase. The RGB_START bit has to be toggled off and on to make changes effective.

START BIT (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Pattern_gen_ctrl register’s RGB_START bit will enable command execution starting from Command 1.

Pattern gen ctrl register (11H)		
rgb_start	Bit 2	0 – Pattern generator disabled 1 – execution pattern starting from command 1
loop	Bit 1	0 – pattern generator loop disabled (single pattern) 1 – pattern generator loop enabled (execute until stopped)
log	Bit 0	0 – color intensity mode 0 1 – color intensity mode 1

Audio Synchronization (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

The color LEDs connected to RGB outputs can be synchronized to incoming audio with Audio Synchronization feature. Audio Sync has 2 modes. **Amplitude mode** synchronizes color LEDs based on input signal’s peak amplitude. In the amplitude mode the user can select between 3 different amplitude mapping modes and 4 different speed configurations. The **frequency mode** synchronizes the color LEDs based on bass, middle and treble amplitudes (= low pass, band pass and high pass filters). User can select between 2 different frequency responses and 4 different speed configurations for best audio-visual user experience. Programmable gain and AGC function are also available for adjustment of input signal amplitude to light response. The Audio Sync functionality is described more closely below.

USING A DIGITAL PWM AUDIO SIGNAL AS AN AUDIO SYNCHRONIZATION SOURCE (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

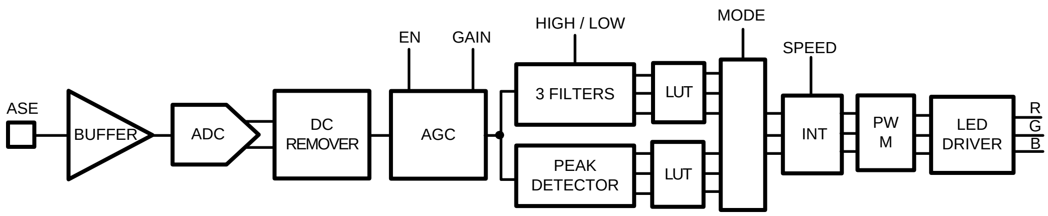
If the input signal is a PWM signal, use a first or second order low pass filter to convert the digital PWM audio signal into an analog waveform. There are two parameters that need to be known to get the filter to work successfully: frequency of the PWM signal and the voltage level of the PWM signal. Suggested cut-off frequency (-3 dB) should be around 2 kHz to 4 kHz and the stop-band attenuation at sampling frequency should be around -48 dB or better. Use a resistor divider to reduce the digital signal amplitude to meet the specification of the analog audio input. Because a low-order low-pass filter attenuates the high-frequency components from audio signal, MODE_CTRL=01b selection is recommended when frequency synchronization mode is enabled. Application example 5 shows an example of a second order RC-filter for 29 kHz PWM signal with 3.3V amplitude. Active filters, such as a Sallen-Key filter, may also be applied. An active filter gives better stop-band attenuation and cut-off frequency can be higher than for a RC-filter.

To make sure that the filter rolls off sufficiently quickly, connect your filter circuit to the audio input(s), turn on the audio synchronization feature, set manual gain to maximum, apply the PWM signal to the filter input and keep an eye on LEDs. If they are blinking without an audio signal (modulation), a sharper roll-off after the cut-off frequency, more stop-band attenuation, or smaller amplitude of the PWM signal is required.

AUDIO SYNCHRONIZATION SIGNAL PATH (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

LP3952 audio synchronization is mainly done digitally and it consists of the following signal path blocks:

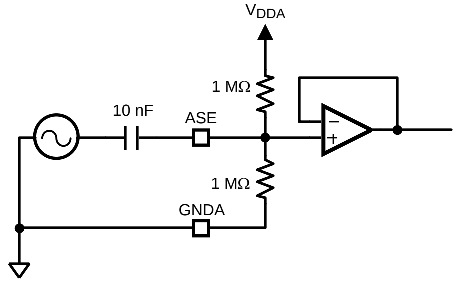
- Input Buffers
- AD Converter
- DC Remover
- Automatic Gain Control (AGC)
- Programmable Gain
- 3 Band Digital Filter
- Peak Detector
- Look-up Tables (LUT)
- Mode Selector
- Integrators
- PWM Generator
- Output Drivers



The digitized input signal has DC component that is removed by digital **DC REMOVER** (-3 dB @ 400 Hz). Since the light response of input audio signal is very much amplitude dependent the AGC adjusts the input signal to suitable range automatically. User can disable **AGC** and the gain can be set manually with **PROGRAMMABLE GAIN**. LP3952 has 2 audio synchronization modes: amplitude and frequency. For amplitude based synchronization the **PEAK DETECTION** method is used. For frequency based synchronization **3 BAND FILTER** separates high pass, low pass and band bass signals. For both modes the predefined LUT is used to optimize the audio visual effect. **MODE SELECTOR** selects the synchronization mode. Different response times to music beat can be selected using **INTEGRATOR** speed variables. Finally **PWM GENERATOR** sets the driver FET duty cycles.

INPUT SIGNAL TYPE AND BUFFERING (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

LP3952 supports single ended audio input as shown in the figure below. The electric parameters of the buffer are described in the Audio Synch table. The buffer is rail-to-rail input operational amplifier connected as a voltage follower. DC level of the input signal is set by a simple resistor divider



AUDIO SYNCHRONIZATION ELECTRICAL PARAMETERS (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Parameter		Test Conditions	Min	Typical	Max	Units
Z_{IN}	Input Impedance of ASE		**250**	500		kΩ
A_{IN}	Audio Input Level Range (peak-to-peak)	Gain = 21 dB	**0.1**			V
		Gain = 0 dB			**V_{DDA}-0.1**	
f_{3dB}	Crossover Frequencies (-3 dB)					kHz
	Narrow Frequency Response	Low Pass		0.5		
		Band Pass		1.0 and 1.5		
		High Pass		2.0		
	Wide Frequency Response	Low Pass		1.0		
		Band Pass		2.0 and 3.0		
		High Pass		4.0		

CONTROL OF ADC AND AUDIO SYNCHRONIZATION (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

The following table describes the controls required for audio synchronization.

Audio_sync_CTRL1 (2AH)					
GAIN_SEL[2:0]	Bits 7-5	Input signal gain control. Range 0...21 dB, step 3 dB:			
		[000] = 0 dB (default)	[011] = 9 dB	[110] = 18 dB	
		[001] = 3 dB	[100] = 12 dB	[111] = 21 dB	
		[010] = 6 dB	[101] = 15 dB		
SYNC_MODE	Bit 4	Synchronization mode selector. SYNCMODE = 0 → Amplitude Mode (default) SYNCMODE = 1 → Frequency Mode			
EN_AGC	Bit 3	Automatic Gain Control enable 1 = enabled 0 = disabled (Gain Select enabled) (default)			
EN_SYNC	Bit 2	Audio synchronization enable 1 = Enabled Note : If AGC is enabled, AGC gain starts from current GAIN_SEL gain value. 0 = Disabled (default)			
INPUT_SEL[1:0]	Bits 1-0	[00] = Single ended input signal, ASE. [01] = Not used [10] = Not used [11] = No input (default)			

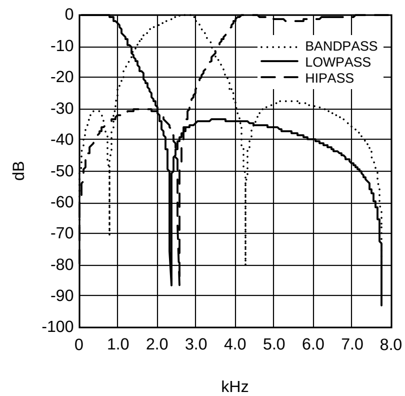
Audio_sync_CTRL2 (2BH)		
EN_AVG	Bit 4	0 – averaging disabled (not applicable in audio sync mode) 1 – averaging enabled (not applicable in audio sync mode)
MODE_CTRL[1:0]	Bits 3-2	See below: Mode control
SPEED_CTRL[1:0]	Bits 1-0	Sets the LEDs light response time to audio input. [00] = FASTEST (default) [01] = FAST [10] = MEDIUM [11] = SLOW (For SLOW setting in amplitude mode f_{MAX}= 3.8 Hz, Frequency mode f_{MAX} = 7.6 Hz)

MODE CONTROL IN FREQUENCY MODE (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

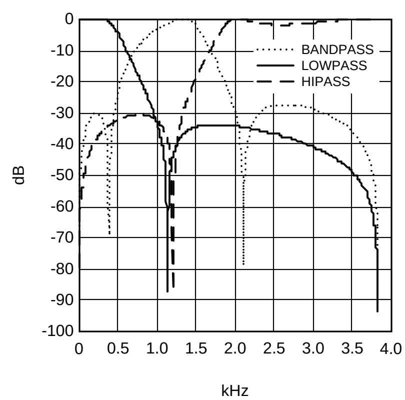
Mode control has two setups based on audio synchronization mode select: the frequency mode and the amplitude mode. During the **frequency mode** user can select two filter options by MODE_CTRL as shown below. User can select the filters based on the music type and light effect requirements. In the first mode the frequency range extends to 8 kHz in the secont to 4 kHz.

The lowpass filter is used for the red, the bandpass filter for the blue and the hipass filter for the green LED.

Higher Frequency Mode
MODE_CTRL = 00 and SYNC_MODE = 1



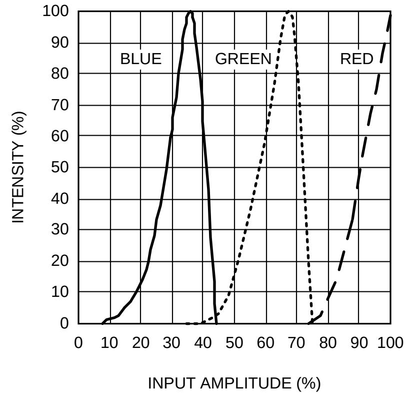
Lower Frequency Mode
MODE_CTRL = 01 and SYNC_MODE = 1



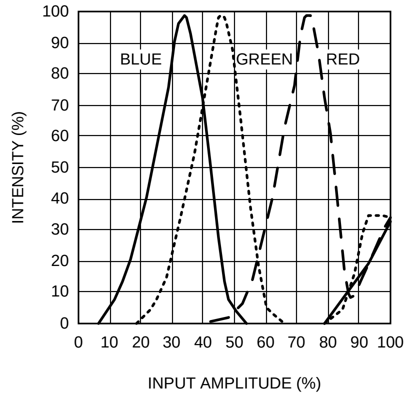
MODE CONTROL IN AMPLITUDE MODE (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

During the **amplitude synchronization mode** user can select between three different amplitude mappings by using MODE_CTRL select. These three mapping options give different light response. The modes are presented in the following graphs.

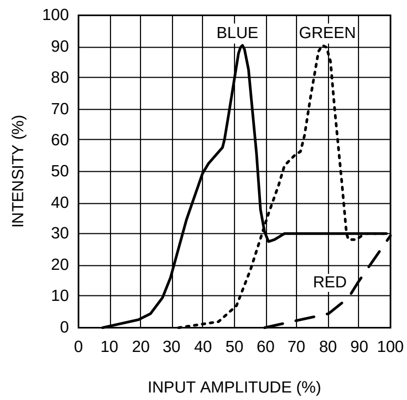
Non-Overlapping Mode
MODE_CTRL[1:0] = [01



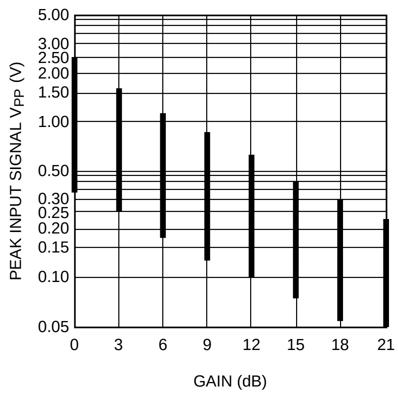
Partly Overlapping Mode
MODE_CTRL[1:0] = [00]



Overlapping Mode
MODE_CTRL[1:0] = [10]



Peak Input Signal Level Range vs Gain Setting



RGB LED Blinking Control (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

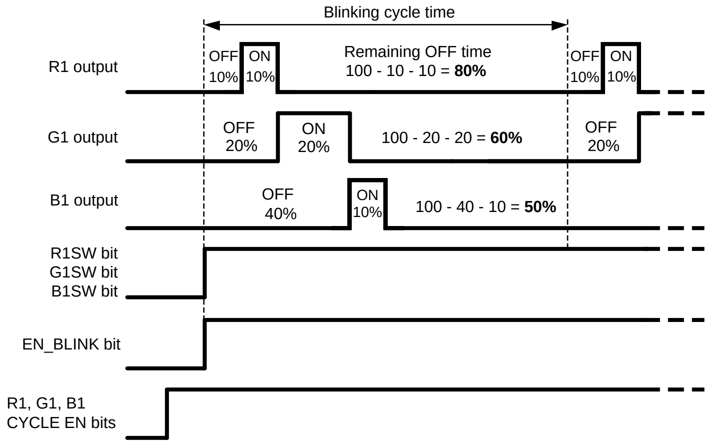
LP3952 has a possibility to drive indicator LEDs with RGB1 outputs with programmable blinking time. Blinking function is enabled with RGB_SEL[1:0] bits set as 01b in 0BH register. R1_CYCLE_EN, G1_CYCLE_EN and B1_CYCLE_EN bits in cycle registers (02H, 04H and 06H) enable/disable blinking function for corresponding output. When EN_BLINK bit is written high in register 11H, the blinking sequences for all outputs (which has CYCLE_EN bit enabled) starts simultaneously. EN_BLINK bit should be written high after selecting wanted blinking sequences and enabling CYCLE_EN bits, to synchronize outputs to get desired lighting effect. R1SW, G1SW and B1SW bits can be used to enable and disable outputs when wanted.

RGB1 blinking sequence is set with R1, G1 and B1 blink registers (01H, 03H and 05H) by setting the appropriate OFF-ON times. Blinking cycle times are set with R1_CYCLE[2:0], G1_CYCLE[2:0] and B1_CYCLE[2:0] bits in R1, G1 and B1 CYCLE registers (02H, 04H and 06H). OFF/ON time is a percentage of the selected cycle time. Values for setting OFF/ON time can be seen in following table.

Table 2. R1, G1 and B1 Blink Registers (01H, 03H and 05H):(1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Name	Bit	Description	
R1_ON[3:0], R1_OFF[3:0] **G1_ON[3:0], G1_OFF[3:0]** **B1_ON[3:0], B1_OFF[3:0]**	7-4, 3-0	RGB1 ON and OFF time	
		Bits	ON/OFF time
		0000	0%
		0001	1%
		0010	2.5%
		0011	5%
		0100	7.5%
		0101	10%
		0110	15%
		0111	20%
		1000	30%
		1001	40%
		1010	50%
		1011	60%
		1100	70%
		1101	80%
		1110	90%
		1111	100%

Blinking ON/OFF cycle is defined so that there will be first OFF-period then ON-period after which follows an off-period for the remaining cycle time that can not be set. If OFF and ON times are together more than 100% the first OFF time will be as set and the ON time is cut to meet 100%. For example, if 50% OFF time is set and ON time is set greater than 50%, only 50% ON time is used, the exceeding ON time is ignored. If OFF and ON times are together less than 100% the remaining cycle time output is OFF.



Values for setting the blinking cycle for RGB1 can be seen in following table:

Table 3. R1, G1 and B1 Cycle Registers (02H, 04H and 06H):(1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Name	Bit	Decription		
R1_CYCLE_EN **G1_CYCLE_EN** **B1_CYCLE_EN**	3	Blinking enable 0 = disabled 1 = enabled, output state is defined with blinking cycle		
R1_CYCLE[2:0] **G1_CYCLE[2:0]** **B1_CYCLE[2:0]**	2-0	RGB1 cycle time		
		Bits	Blinking cycle time	Blinking frequency
		000	0.1s	10 Hz
		001	0.25s	4 Hz
		010	0.5s	2 Hz
		011	1s	1 Hz
		100	2s	0.5 Hz
		101	3s	0.33 Hz
		110	4s	0.25 Hz
		111	5s	0.2 Hz

Table 4. PATTERN_GEN_CTRL Register (11H):(1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Name	Bit	Description
EN_BLINK	3	Blinking sequence start bit 0 = disabled 1 = enabled

RGB Driver Electrical Characteristics (R1, G1, B1, R2, G2, B2 Outputs)(1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Parameter		Test Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	R1, G1, B1, R2, G2, B2 pin leakage current			0.1	**1**	µA
I_{RGB}	Maximum recommended sink current	CC mode			**40**	mA
		SW mode			**50**	mA
	Accuracy @ 37mA	R_{RGB}=3.3 kΩ ±1%, CC mode		±5		%
	Current mirror ratio	CC mode		1:100		
	RGB1 and RGB2 current mismatch	I_{RGB}=37mA, CC mode		±5		%
R_{SW}	Switch resistance	SW mode		2.5	**5**	Ω
f_{RGB}	RGB switching frequency	Accuracy proportional to internal clock freq.	**18.2**	20	**21.8**	kHz

Output Current vs Pin Voltage (Current Sink Mode)

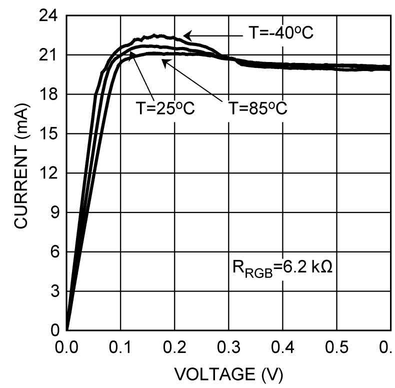


Figure 12.

Pin Voltage vs Output Current (Switch Mode)

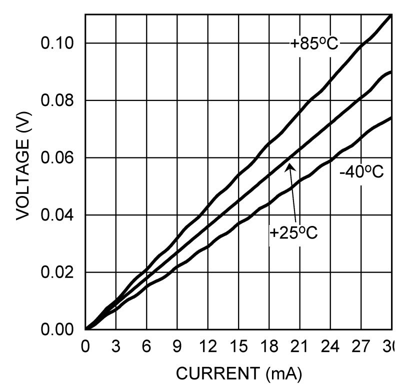


Figure 13.

Output Current vs R_{RGB} (Current Sink Mode)

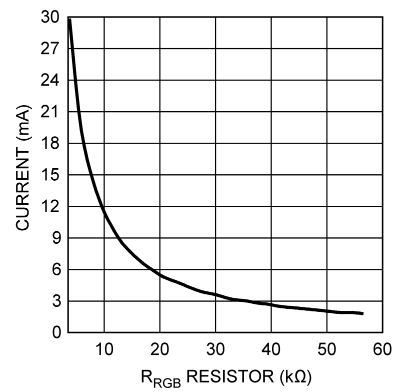
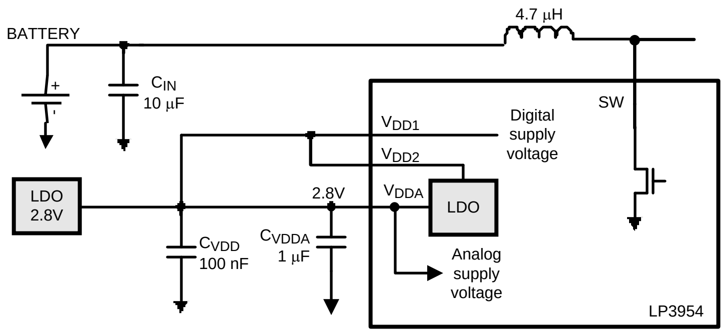


Figure 14.

7V Shielding (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

To shield LP3952 from high input voltages 6…7.2V the use of external 2.8V LDO is required. This 2.8V voltage protects internally the device against high voltage condition. The recommended connection is as shown in the picture below. Internally both logic and analog circuitry works at 2.8V supply voltage. Both supply voltage pins should have separate filtering capacitors.



In cases where high voltage is not an issue the connection is as shown below

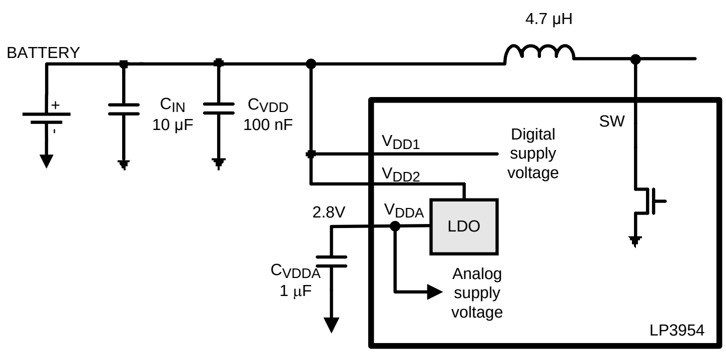


Table 5. Logic Interface Electrical Characteristics (1.65V ≤ V_{DDIO} ≤ $V_{DD1,2}$V) (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS ADDR_SEL, NRST, SCL, PWM, SDA						
V_{IL}	Input Low Level				**0.2×V_{DDIO}**	V
V_{IH}	Input High Level		**0.8×V_{DDIO}**			V
I_L	Logic Input Current		**−1.0**		**1.0**	µA
f_{SCL}	Clock Frequency				**400**	kHz
LOGIC OUTPUT SDA						
V_{OL}	Output Low Level	I_{SDA} = 3 mA		0.3	**0.5**	V
I_L	Output Leakage Current	V_{SDA} = 2.8V			**1.0**	µA

Note: Any unused digital input pin has to be connected to GND to avoid floating and extra current consumption.

I^2C Compatible Interface

INTERFACE BUS OVERVIEW

The I^2C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle. Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

I^2C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

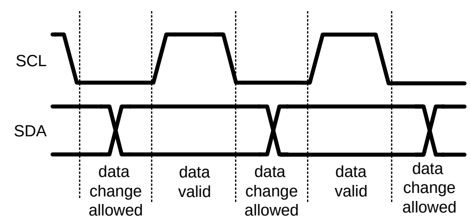
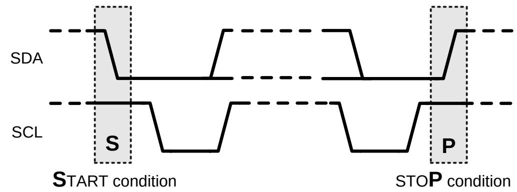


Figure 15. I^2C Signals: Data Validity

I^2C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I^2C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates START and STOP bits. The I^2C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I^2C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I^{2}C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3952 address is 54h or 55H as selected with ADDR_SEL pin. **I^{2}C address for LP3952 is 54H when ADDR_SEL=0 and 55H when ADDR_SEL=1**. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

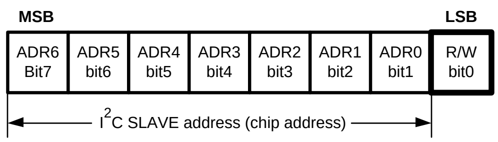
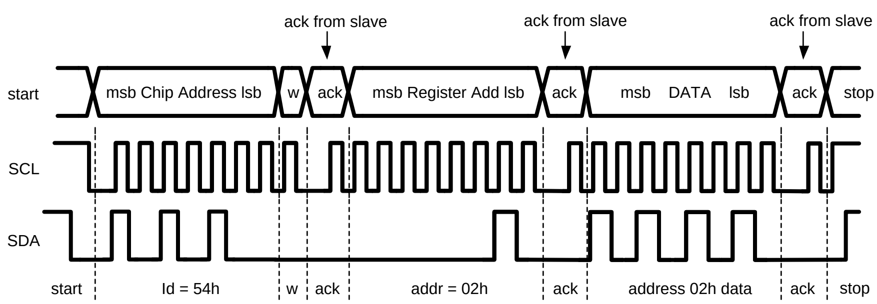


Figure 16. I^{2}C Chip Address

Register changes take an effect at the SCL rising edge during the last ACK from slave.



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = 7-bit chip address, 54H (ADDR_SEL=0) or 55H (ADDR_SEL=1) for LP3952.

Figure 17. I^{2}C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

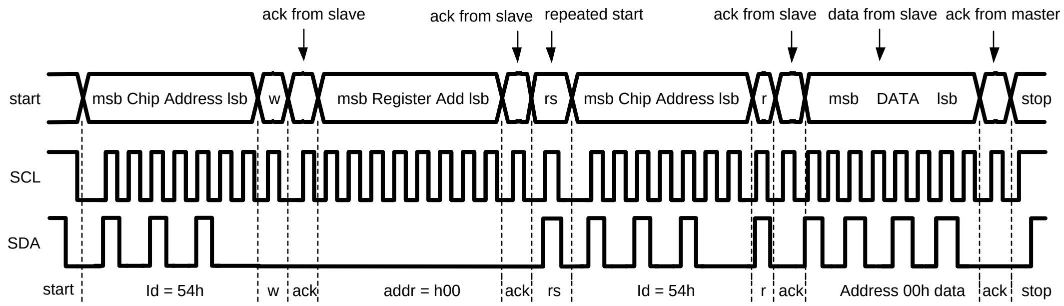


Figure 18. I²C Read Cycle

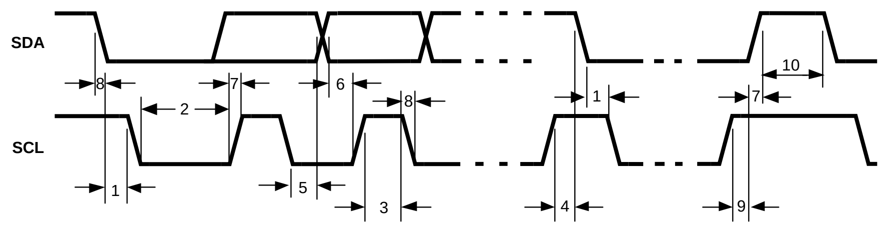


Figure 19. I²C Timing Diagram

I²C Timing Parameters

$V_{DD1,2}$ = 3.0 to 4.5V, V_{DD_IO} = 1.65V to $V_{DD1,2}$

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LP3952)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

Autoincrement mode is available, with this mode it is possible to read or write bytes with autoincreasing addresses. LP3952 has empty spaces in address register map, and it is recommended to use autoincrement mode only for writing in pattern command registers.

Recommended External Components

OUTPUT CAPACITOR, C_{OUT}

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower Vout ripple that the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower Vout ripple magnitude than the tantalums of the same value. However, the dv/dt of the Vout ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied DC voltage, so called DC bias effect. The capacitance value can fall to below half of the nominal capacitance. Too low output capacitance will increase noise and it can make the boost converter unstable. Recommended maximum DC bias effect at 5V DC voltage is -50%.

INPUT CAPACITOR, C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

OUTPUT DIODE, D_1

A schottky diode should be used for the output diode. Peak repetitive current rating of the schottky diode should be larger than the peak inductor current (ca. 1A). Average current rating of the schottky diode should be higher than maximum output current used. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

INDUCTOR, L_1

The LP3952's high switching frequency enables the use of the small surface mount inductor. A 4.7 µH shielded inductor is suggested for 2 MHz operation, 10 µH should be used at 1 MHz. The inductor should have a saturation current rating higher than the rms current it will experience during circuit operation. To get maximum (400 mA) current from the boost, an inductor with 1A saturation current is recommended. If output current is for example 200 mA then inductor with 600 mA saturation current can be used. Less than 300 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. The inductor should be connected to the SW pin as close to the IC as possible. Examples of suitable inductor for 400 mA output current is TDK VLF4012AT-4R7M1R1, and for 200mA application VLF3010AT-4R7MR70 or Panasonic ELLVEG4R7N.

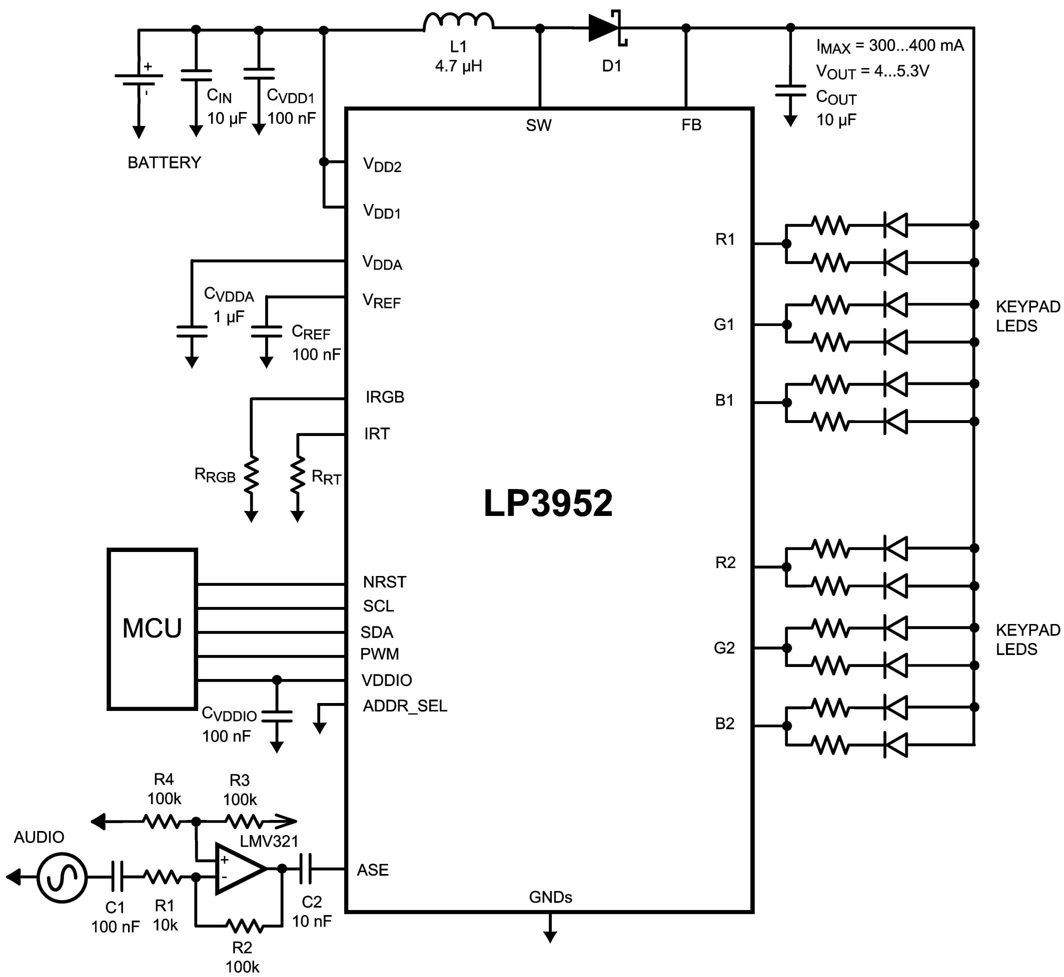
LIST OF RECOMMENDED EXTERNAL COMPONENTS

Symbol	Symbol explanation	Value	Unit	Type
C_{VDD1}	C between VDD1 and GND	100	nF	Ceramic, X7R / X5R
C_{VDD2}	C between VDD2 and GND	100	nF	Ceramic, X7R / X5R
C_{VDDIO}	C between VDDIO and GND	100	nF	Ceramic, X7R / X5R
C_{VDDA}	C between VDDA and GND	1	µF	Ceramic, X7R / X5R
C_{OUT}	C between FB and GND	10	µF	Ceramic, X7R / X5R, 10V
C_{IN}	C between battery voltage and GND	10	µF	Ceramic, X7R / X5R
L_1	L between SW and V_{BAT} at 2 MHz	4.7	µH	Shielded, low ESR, Isat=1A for 400 mA output current, Isat=600 mA for 200 mA output current

Symbol	Symbol explanation	Value	Unit	Type
C_{VREF}	C between V_{REF} and GND	100	nF	Ceramic, X7R
C_{VDDIO}	C between V_{DDIO} and GND	100	nF	Ceramic, X7R
R_{RBG}	R between I_{RGB} and GND	5.6	kΩ	±1%
R_{RT}	R between I_{RT} and GND	82	kΩ	±1%
D_1	Rectifying Diode (Vf @ maxload)	0.3	V	Schottky diode
C_{ASE}	C between Audio input and ASE	100	nF	Ceramic, X7R / X5R
LEDs		User defined		

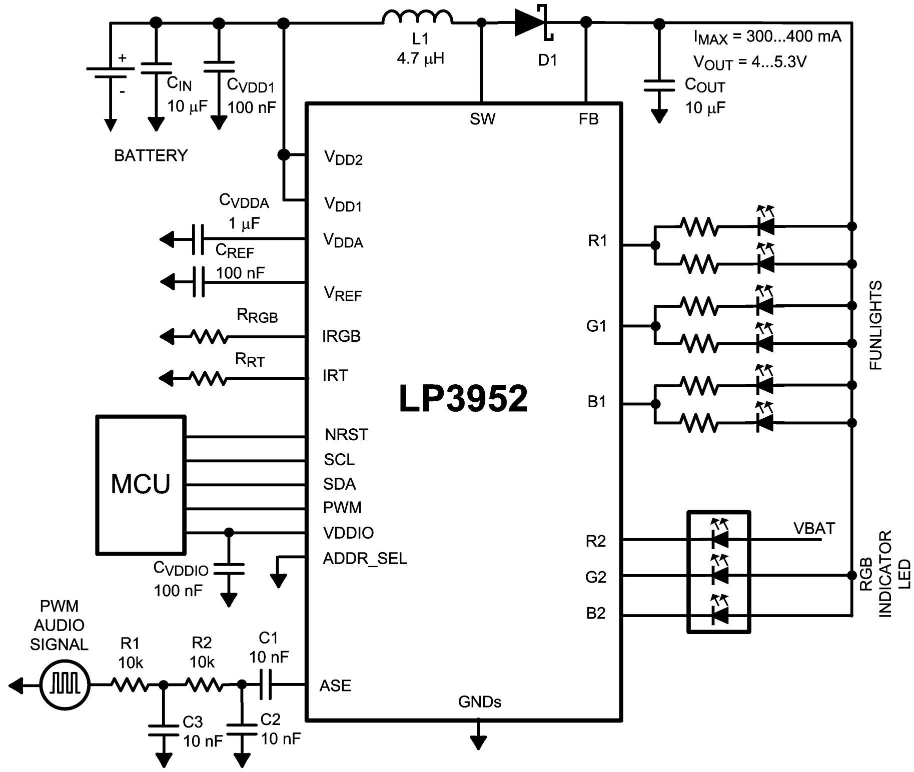
Application Examples

EXAMPLE 1



There may be cases where the audio input signal going into the LP3952 is too weak for audio synchronization. This figure presents a single-supply inverting amplifier connected to the ASE input for audio signal amplification. The amplification is +20 dB, which is well enough for 20 mVp-p audio signal. Because the amplifier (LMV321) is operating in single supply voltage, a voltage divider using R3 and R4 is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor C1 is placed between the inverting input and resistor R1 to block the DC signal going into the audio signal source. The values of R1 and C1 affect the cutoff frequency, fc = 1/(2π*R1*C1), in this case it is around 160 Hz. As a result, the LMV321 output signal is centered around mid-supply, that is V_{DDA}/2. The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system

EXAMPLE 2



Here, a second order RC-filter is used on the ASE input to convert a PWM signal to an analog waveform.

More application information is available in the document "LP3952 Evaluation Kit".

Table 6. LP3952 Control Register Names and Default Values

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	RGB Ctrl	cc_rgb1	cc_rgb2	r1sw	g1sw	b1sw	r2sw	g2sw	b2sw
		1	**1**	**0**	**0**	**0**	**0**	**0**	**0**
01	R1 blink	r1_on[3]	r1_on[2]	r1_on[1]	r1_on[0]	r1_off[3]	r1_off[2]	r1_off[1]	r1_off[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
02	R1 cycle					r1_cycle en	r1_cycle[2]	r1_cycle[1]	r1_cycle[0]
						0	**0**	**0**	**0**
03	G1 blink	g1_on[3]	g1_on[2]	g1_on[1]	g1_on[0]	g1_off[3]	g1_off[2]	g1_off[1]	g1_off[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
04	G1 cycle					g1_cycle en	g1_cycle[2]	g1_cycle[1]	g1_cycle[0]
						0	**0**	**0**	**0**
05	B1 blink	b1_on[3]	b1_on[2]	b1_on[1]	b1_on[0]	b1_off[3]	b1_off[2]	b1_off[1]	b1_off[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
06	B1 cycle					b1_cycle en	b1_cycle[2]	b1_cycle[1]	b1_cycle[0]
						0	**0**	**0**	**0**
07	Ext. PWM control			r1_pwm	g1_pwm	b1_pwm	r2_pwm	g2_pwm	b2_pwm
				0	**0**	**0**	**0**	**0**	**0**
08	**Do not use**								
09	**Do not use**								
0A	**Do not use**								

Table 6. LP3952 Control Register Names and Default Values (continued)

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0B	Enables		nstby	en_ boost			en_ autoload	rgb_sel[1:0]	
			0	**0**			**1**	**0**	**0**
0C	ADC output	data[7:0]							
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0D	Boost output	boost[7:0]							
		0	**0**	**1**	**1**	**1**	**1**	**1**	**1**
0E	Boost_frq						freq_sel[2:0]		
							1	**1**	**1**
10	**Do not use**								
11	Pattern gen ctrl						rgb_start	loop	log
							0	**0**	**0**
12	RGB1 max current			ir1[1:0]		ig1[1:0]		ib1[1:0]	
				0	**0**	**0**	**0**	**0**	**0**
13	RGB2 max current			ir2[1:0]		ig2[1:0]		ib2[1:0]	
				0	**0**	**0**	**0**	**0**	**0**
2A	Audio sync CTRL1	gain_sel[2:0]			sync_mode	en_agc	en_sync	input_sel[1:0]	
		0	**0**	**0**	**0**	**0**	**0**	**1**	**1**
2B	Audio sync CTRL2				en_avg	mode_ctrl[1:0]		speed_ctrl[1:0]	
					0	**0**	**0**	**0**	**0**
50	Command 1A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
51	Command 1B	cet[1:0]		b[2:0]			tt[2:0]		
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
52	Command 2A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
53	Command 2B	cet[1:0]		b[2:0]			tt[2:0]		
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
54	Command 3A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
55	Command 3B	cet[1:0]		b[2:0]			tt[2:0]		
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
56	Command 4A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
57	Command 4B	cet[1:0]		b[2:0]			tt[2:0]		
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
58	Command 5A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
59	Command 5B	cet[1:0]		b[2:0]			tt[2:0]		
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
5A	Command 6A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
5B	Command 6B	cet[1:0]		b[2:0]			tt[2:0]		
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
5C	Command 7A	r[2:0]			g[2:0]			cet[3:2]	
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Table 6. LP3952 Control Register Names and Default Values (continued)

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
5D	Command 7B	cet[1:0]		b[2:0]			tt[2:0]		
		0	0	0	0	0	0	0	0
5E	Command 8A	r[2:0]			g[2:0]			cet[3:2]	
		0	0	0	0	0	0	0	0
5F	Command 8B	cet[1:0]		b[2:0]			tt[2:0]		
		0	0	0	0	0	0	0	0
60	Reset	Writing any data to Reset Register resets LP3952							

LP3952 Registers

REGISTER BIT EXPLANATIONS

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

Register Bit Accessibility and Initial Condition	
Key	**Bit Accessibility**
rw	Read/write
r	Read only
–0,–1	Condition after POR

RGB CTRL (00H) – RGB LEDS CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
cc_rgb1	**cc_rgb2**	**r1sw**	**g1sw**	**b1sw**	**r2sw**	**g2sw**	**b2sw**
rw-1	rw-1	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

cc_rgb1	Bit 7	0 - R1, G1 and B1 are constant current sinks, current limited internally 1 - R1, G1 and B1 are switches, limit current with external ballast resistor
cc_rgb2	Bit 6	0 – R2, G2 and B2 are constant current sinks, current limited internally 1 – R2, G2 and B2 are switches, limit current with external ballast resistor
r1sw	Bit 5	0 – R1 disabled 1 – R1 enabled
g1sw	Bit 4	0 – G1 disabled 1 – G1 enabled
b1sw	Bit 3	0 – B1 disabled 1 – B1 enabled
r2sw	Bit 2	0 – R2 disabled 1 – R2 enabled
g2sw	Bit 1	0 – G2 disabled 1 – G2 enabled
b2sw	Bit 0	0 – B2 disabled 1 – B2 enabled

R1/G1/B1 BLINK (01H, 03H, 05H) – BLINKING ON/OFF TIME CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
R1/G1/B1_ON[3:0]				**R1/G1/B1_OFF[3:0]**			
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

R1_ON[3:0], R1_OFF[3:0] G1_ON[3:0], G1_OFF[3:0] B1_ON[3:0], B1_OFF[3:0]	Bits 7-4, 3-0	**RGB1 ON and OFF time**	
		Bits	ON/OFF time
		0000	0%
		0001	1%
		0010	2.5%
		0011	5%
		0100	7.5%
		0101	10%
		0110	15%
		0111	20%
		1000	30%
		1001	40%
		1010	50%
		1011	60%
		1100	70%
		1101	80%
		1110	90%
		1111	100%

R1/G1/B1 CYCLE (02H, 04H, 06H) – BLINKING CYCLE CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
				R1/G1/B1_CYCLE_EN	**R1/G1/B1_CYCLE[2:0]**		
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

R1_CYCLE_EN G1_CYCLE_EN B1_CYCLE_EN	Bit 3	Blinking enable 0 = disabled, output state is defined with RGB registers 1 = enabled, output state is defined with blinking cycle		
R1_CYCLE[2:0] G1_CYCLE[2:0] B1_CYCLE[2:0]	Bits 2-0	**RGB1 cycle time**		
		Bits	Blinking cycle time	Blinking frequency
		000	0.1s	10 Hz
		001	0.25s	4 Hz
		010	0.5s	2 Hz
		011	1s	1 Hz
		100	2s	0.5 Hz
		101	3s	0.33 Hz
		110	4s	0.25 Hz
		111	5s	0.2 Hz

EXT_PWM_CONTROL (07H) – EXTERNAL PWM CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
		r1_pwm	**g1_pwm**	**b1_pwm**	**r2_pwm**	**g2_pwm**	**b2_pwm**
		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

r1_pwm	Bit 5	0 – R1 PWM control disabled 1 – R1 PWM control enabled
g1_pwm	Bit 4	0 – G1 PWM control disabled 1 – G1 PWM control enabled
b1_pwm	Bit 3	0 – RB PWM control disabled 1 – B1 PWM control enabled
r2_pwm	Bit 2	0 – R2 PWM control disabled 1 – R2 PWM control enabled
g2_pwm	Bit 1	0 – G2 PWM control disabled 1 – G2 PWM control enabled
b2_pwm	Bit 0	0 – B2 PWM control disabled 1 – B2 PWM control enabled

ENABLES (0BH) – ENABLES REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
	nstby	**en_boost**			**en_autoload**	**rgb_sel[1:0]**	
r-0	rw-0	rw-0	r-0	r-0	rw-1	rw-0	rw-0

nstby	Bit 6	0 – LP3952 standby mode 1 – LP3952 active mode			
en_boost	Bit 5	0 – boost converter disabled 1 – boost converter enabled			
en_autoload	Bit 2	0 – internal boost converter loader off 1 – internal boost converter loader on			
rgb_sel[1:0]	Bits 1-0	**Color LED control mode selection**			
		rgb_sel[1:0]	**Audio sync**	**Pattern generator**	**Blinking sequence**
		00	-	RGB1 & RGB2	-
		01	-	RGB2	RGB1
		10	RGB2	RGB1	-
		11	RGB1 & RGB2	-	-

ADC_OUTPUT (0CH) – ADC DATA REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
data[7:0]							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

data[7:0]	Bits 7-0	Data register ADC (Audio input, light or temperature sensors)

BOOST_OUTPUT (0DH) – BOOST OUTPUT VOLTAGE CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Boost[7:0]							
rw-0	rw-0	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

		Adjustment	
		Boost[7:0]	**Typical boost output (V)**
Boost[7:0]	Bits 7-0	0000 0000	4.00
		0000 0001	4.25
		0000 0011	4.40
		0000 0111	4.55
		0000 1111	4.70
		0001 1111	4.85
		0011 1111	5.00 (default)
		0111 1111	5.15
		1111 1111	5.30

BOOST_FRQ (0EH) – BOOST FREQUENCY CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
					freq_sel[2:0]		
r-0	r-0	r-0	r-0	r-0	rw-1	rw-1	rw-1

		Adjustment	
		freq_sel[2:0]	**Frequency**
freq_sel[2:0]	Bits 7-0	1xx	2.00 MHz
		01x	1.67 MHz
		00x	1.00 MHz

PATTERN_GEN_CTRL (11H) – PATTERN GENERATOR CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
				en_blink	**rgb_start**	**loop**	**log**
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

en_blink	Bit 3	0 - blinking sequences start bit disabled 1 - blinking sequences start bit enabled
rgb_start	Bit 2	0 – pattern generator disabled 1 – execution pattern starting from command 1
loop	Bit 1	0 – pattern generator loop disabled (single pattern) 1 – pattern generator loop enabled (execute until stopped)
log	Bit 0	0 – color intensity mode 0 1 – color intensity mode 1

RGB1_MAX_CURRENT (12H) – RGB1 DRIVER INDIVIDUAL MAXIMUM CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
		ir1[1:0]		**ig1[1:0]**		**ib1[1:0]**	
r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

ir1[1:0]	Bits 5-4	**Maximum current for R1 driver**	
		ir1[2:0]	**Maximum output current**
		00	$0.25 \times I_{MAX}$
		01	$0.50 \times I_{MAX}$
		10	$0.75 \times I_{MAX}$
		11	$1.00 \times I_{MAX}$
ig1[1:0]	Bits 3-2	**Maximum current for G1 driver**	
		ig2[1:0]	**Maximum output current**
		00	$0.25 \times I_{MAX}$
		01	$0.50 \times I_{MAX}$
		10	$0.75 \times I_{MAX}$
		11	$1.00 \times I_{MAX}$
ib1[1:0]	Bits 1-0	**Maximum current for B1 driver**	
		ib1[1:0]	**Maximum output current**
		00	$0.25 \times I_{MAX}$
		01	$0.50 \times I_{MAX}$
		10	$0.75 \times I_{MAX}$
		11	$1.00 \times I_{MAX}$

RGB2_MAX_CURRENT (13H) – RGB2 DRIVER INDIVIDUAL MAXIMUM CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
		ir2[1:0]		**ig2[1:0]**		**ib2[1:0]**	
r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

ir2[1:0]	Bits 5-4	**Maximum current for R2 driver**	
		ir2[2:0]	**Maximum output current**
		00	$0.25 \times I_{MAX}$
		01	$0.50 \times I_{MAX}$
		10	$0.75 \times I_{MAX}$
		11	$1.00 \times I_{MAX}$
ig2[1:0]	Bits 3-2	**Maximum current for G2 driver**	
		ig2[1:0]	**Maximum output current**
		00	$0.25 \times I_{MAX}$
		01	$0.50 \times I_{MAX}$
		10	$0.75 \times I_{MAX}$
		11	$1.00 \times I_{MAX}$
ib2[1:0]	Bits 1-0	**Maximum current for B2 driver**	
		ib2[1:0]	**Maximum output current**
		00	$0.25 \times I_{MAX}$
		01	$0.50 \times I_{MAX}$
		10	$0.75 \times I_{MAX}$
		11	$1.00 \times I_{MAX}$

AUDIO_SYNC_CTRL1 (2AH) – AUDIO SYNCHRONIZATION AND ADC CONTROL REGISTER 1

D7	D6	D5	D4	D3	D2	D1	D0
gain_sel[2:0]			**sync_mode**	**en_agc**	**en_sync**	**input_sel[1:0]**	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1	rw-1

gain_sel[2:0]	Bits 7-5	**Input signal gain control**	
		gain_sel[2:0]	**gain, dB**
		000	0 (default)
		001	3
		010	6
		011	9
		100	12
		101	15
		110	18
		111	21
sync_mode	Bit 4	**Input filter mode control** 0 – Amplitude mode 1 – Frequency mode	
en_agc	Bit 3	0 – automatic gain control disabled 1 – automatic gain control enabled	
en_sync	Bit 2	0 – audio synchronization disabled 1 – audio synchronization enabled	
input_sel[1:0]	Bits 1-0	**ADC input selector**	
		input_sel[1:0]	**Input**
		00	Single ended input signal (ASE)
		01	Not used
		10	Not used
		11	No input (default)

AUDIO_SYNC_CTRL2 (2BH) – AUDIO SYNCHRONIZATION AND ADC CONTROL REGISTER 2

D7	D6	D5	D4	D3	D2	D1	D0
			en_avg	**mode_ctrl[1:0]**		**speed_ctrl[1:0]**	
r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0	rw-0

en_avg	Bit 4	0 – averaging disabled. f_{sample} = 122 Hz, data in register changes every 8.2 ms. 1 – averaging enabled. f_{sample} = 244 Hz, averaging of 64 samples, data in register changes every 262 ms (3.2Hz).	
mode_ctrl[1:0]	Bits 3-2	Filtering mode control	
speed_ctrl[1:0]	Bits 1-0	LEDs light response time to audio input	
		speed_ctrl[1:0]	**Response**
		00	FASTEST (default)
		01	FAST
		10	MEDIUM
		11	SLOW

PATTERN CONTROL REGISTERS

Command_[1:8]A – Pattern Control Register A							
D7	D6	D5	D4	D3	D2	D1	D0
r[2:0]			**g[2:0]**			**cet[3:2]**	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Command_[1:8]B – Pattern Control Register B							
D7	D6	D5	D4	D3	D2	D1	D0
cet[1:0]		**b[2:0]**			**tt[2:0]**		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

r[2:0]	Bits 7-5A	**Red color intensity**		
		r[2:0]	**current, %**	
			log=0	**log=1**
		000	$0 \times I_{MAX}$	$0 \times I_{MAX}$
		001	$7\% \times I_{MAX}$	$1\% \times I_{MAX}$
		010	$14\% \times I_{MAX}$	$2\% \times I_{MAX}$
		011	$21\% \times I_{MAX}$	$4\% \times I_{MAX}$
		100	$32\% \times I_{MAX}$	$10\% \times I_{MAX}$
		101	$46\% \times I_{MAX}$	$21\% \times I_{MAX}$
		110	$71\% \times I_{MAX}$	$46\% \times I_{MAX}$
		111	$100\% \times I_{MAX}$	$100\% \times I_{MAX}$
g[2:0]	Bits 4-2A	**Green color intensity**		
		g[2:0]	**current, %**	
			log=0	**log=1**
		000	$0 \times I_{MAX}$	$0 \times I_{MAX}$
		001	$7\% \times I_{MAX}$	$1\% \times I_{MAX}$
		010	$14\% \times I_{MAX}$	$2\% \times I_{MAX}$
		011	$21\% \times I_{MAX}$	$4\% \times I_{MAX}$
		100	$32\% \times I_{MAX}$	$10\% \times I_{MAX}$
		101	$46\% \times I_{MAX}$	$21\% \times I_{MAX}$
		110	$71\% \times I_{MAX}$	$46\% \times I_{MAX}$
		111	$100\% \times I_{MAX}$	$100\% \times I_{MAX}$

cet[3:0]	Bits 1-0A 7-6B	**Command execution time**		
		cet[3:0]	**CET duration, ms**	
		0000	197	
		0001	393	
		0010	590	
		0011	786	
		0100	983	
		0101	1180	
		0110	1376	
		0111	1573	
		1000	1769	
		1001	1966	
		1010	2163	
		1011	2359	
		1100	2556	
		1101	2753	
		1110	2949	
		1111	3146	
b[2:0]	Bits 5-3B	**Blue color intensity**		
		b[2:0]	**current, %**	
			log=0	**log=1**
		000	$0 \times I_{MAX}$	$0 \times I_{MAX}$
		001	$7\% \times I_{MAX}$	$1\% \times I_{MAX}$
		010	$14\% \times I_{MAX}$	$2\% \times I_{MAX}$
		011	$21\% \times I_{MAX}$	$4\% \times I_{MAX}$
		100	$32\% \times I_{MAX}$	$10\% \times I_{MAX}$
		101	$46\% \times I_{MAX}$	$21\% \times I_{MAX}$
		110	$71\% \times I_{MAX}$	$46\% \times I_{MAX}$
		111	$100\% \times I_{MAX}$	$100\% \times I_{MAX}$
tt[2:0]	Bits 2-0B	**Transition time**		
		tt[2:0]	**Transition time, ms**	
		000	0	
		001	55	
		010	110	
		011	221	
		100	442	
		101	885	
		110	1770	
		111	3539	

RESET (60H) - RESET REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Writing any data to Reset Register in address 60H can reset LP3952							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	40

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3952RL/NOPB	ACTIVE	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-30 to 85	D62B	Samples
LP3952RLX/NOPB	ACTIVE	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-30 to 85	D62B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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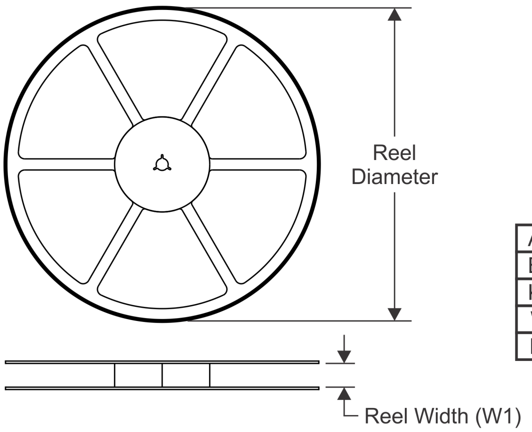
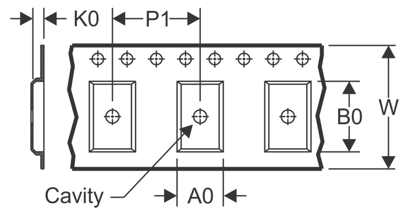
TAPE AND REEL INFORMATION

REEL DIMENSIONS

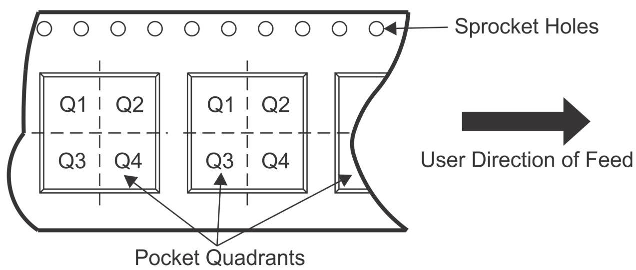


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

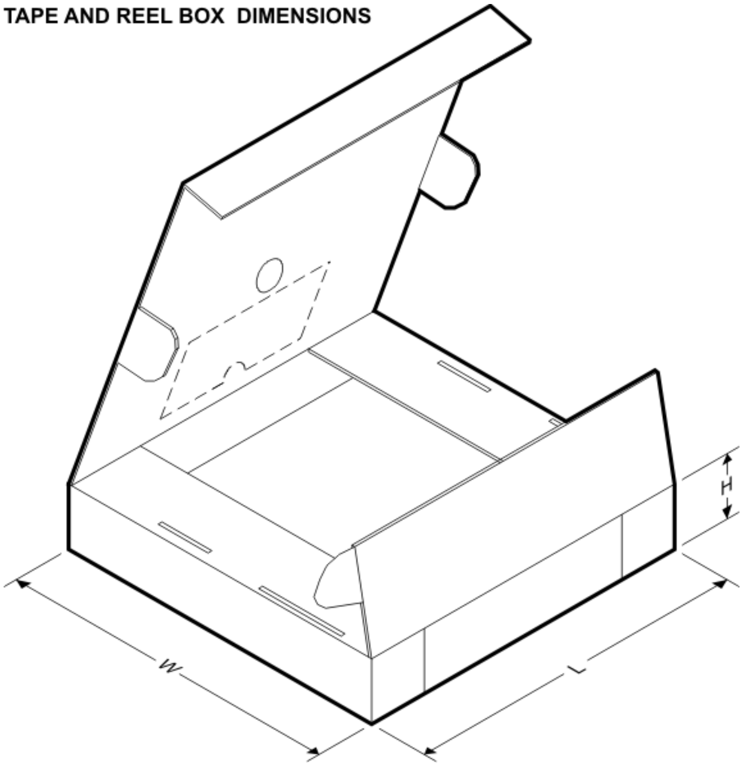
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3952RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1
LP3952RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1

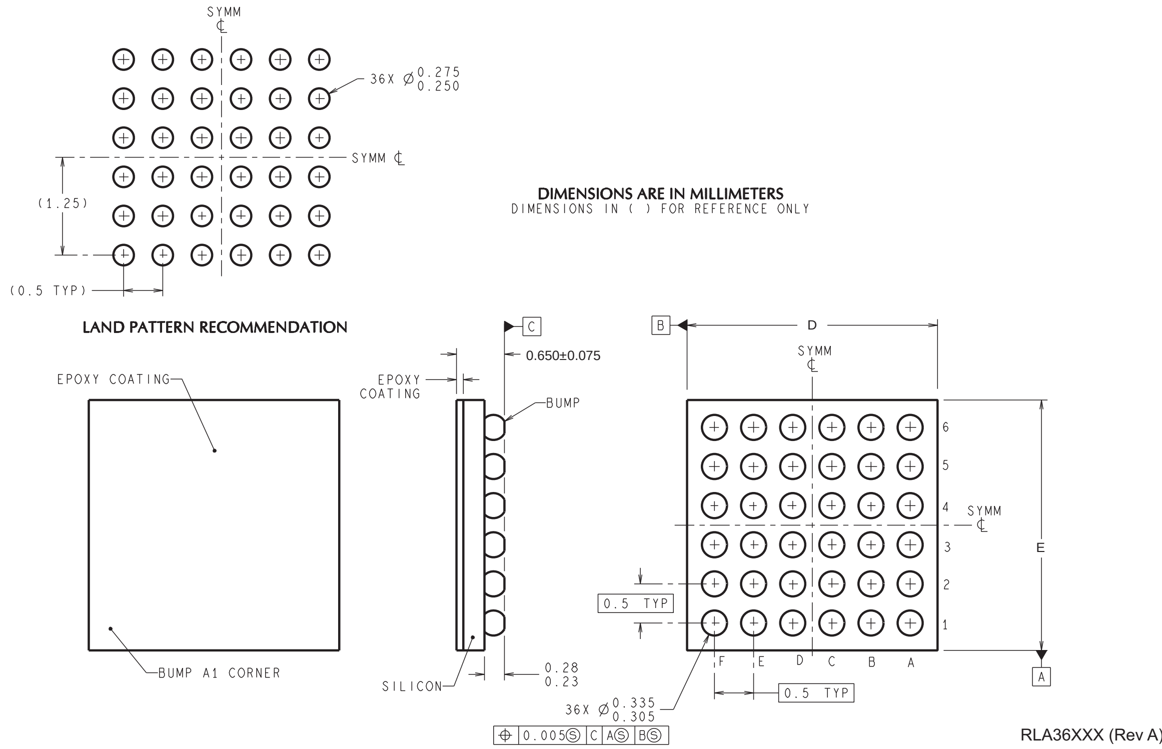
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3952RL/NOPB	DSBGA	YPG	36	250	210.0	185.0	35.0
LP3952RLX/NOPB	DSBGA	YPG	36	1000	210.0	185.0	35.0

YPG0036



D: Max = 3.013 mm, Min =2.952 mm

E: Max = 3.013 mm, Min =2.952 mm

4214895/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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