Tiny LED Driver for Camera Flash and Four LEDs With I^{2}C Programmability, Connectivity Test, and Audio Synchronization

Check for Samples: LP55271

FEATURES

- **High Current Boost DC-DC Converter (up to 1-A Output Current)**
- **Programmable Boost Output Voltage**
- **370-mA Flash LED Constant-Current Driver With Low Tolerance and a Safety Circuit**
- **Synchronization Pin for Flash Timing**
- **Two Single-Ended Audio Inputs With Gain Control**
- **Four Constant-Current 15-mA LED Drivers With 8-Bit Programmable Brightness Control**
- **Audio Synchronization Feature**
- **I^{2}C Compatible Control Interface**
- **Built-in LED Connectivity Test to Maximize Manufacturing Yield**
- **Small DSBGA-30 Package (2.5 mm x 3.0 mm x 0.6 mm)**

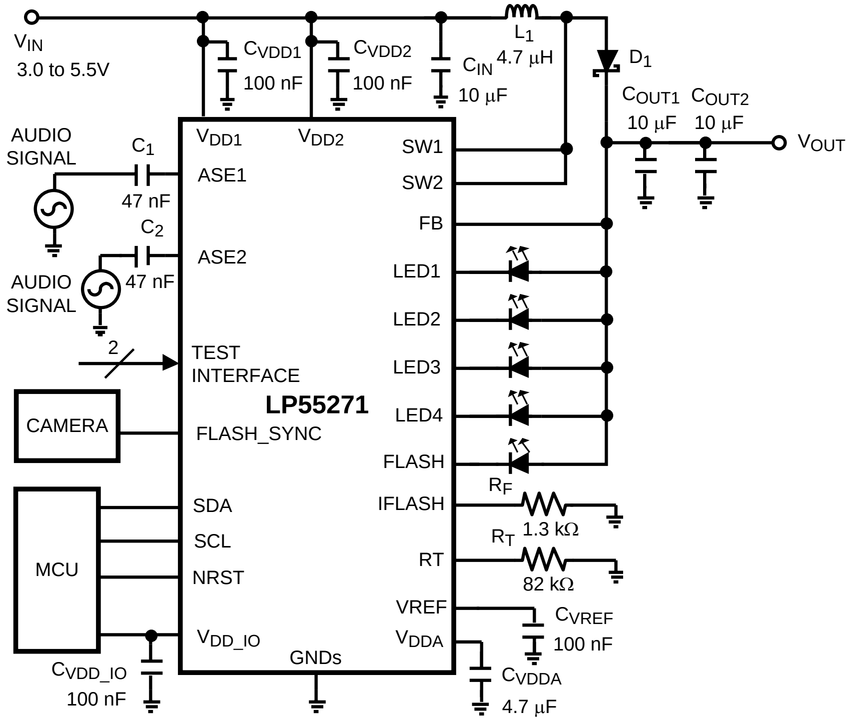
APPLICATIONS

- **Camera Flash, Funlight, and Backlight Driving in Battery-Powered Devices**

DESCRIPTION

The LP55271 is a lighting management unit for handheld devices with I^{2}C compatible control interface. The LP55271 has a step-up DC/DC converter with high current output and it drives display and keypad backlights and powers the camera flash LED. In addition the DC/DC converter has the output current to power for example an audio amplifier simultaneously. The chip has four 8-bit programmable high efficiency constant current LED drivers and a FLASH LED driver. Built-in audio synchronization feature allows the user to synchronize one of the LEDs to audio input.

Typical Application



DESCRIPTION (CONTINUED)

The LP55271 has an integrated 370 mA flash driver with a safety stop feature and 46 mA torch mode. An external enable pin is provided for the synchronizing the flash with the camera action. An external software independent test interface provides a fast way to find a broken path or short on LED circuits. Very small DSBGA package together with minimum number of external components is a best fit for handheld devices.

CONNECTION DIAGRAMS

DSBGA-30 package, 2.466 x 2.974 x 0.60 mm body size, 0.5 mm pitch, Package Number YZR0030

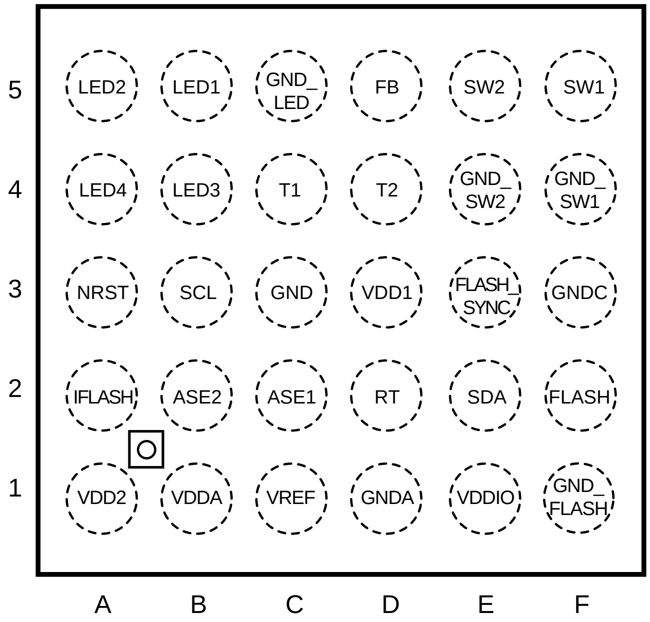


Figure 1. Top View

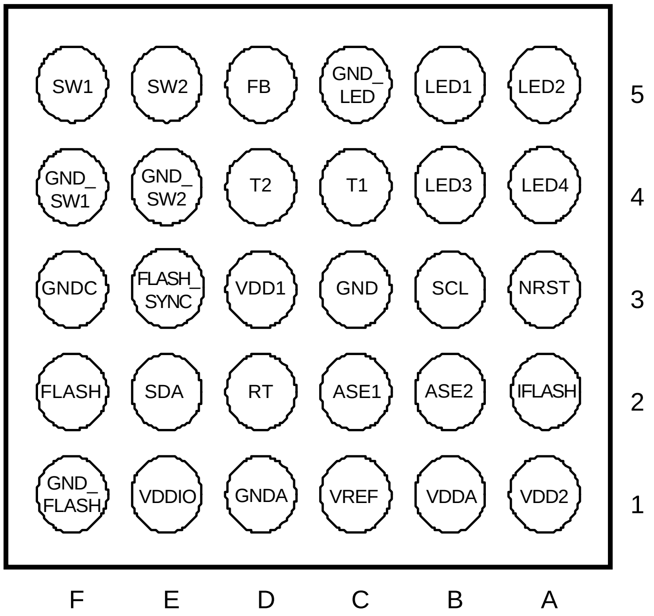


Figure 2. Bottom View

Table 1. Pin Descriptions

Pin	Name	Type[1]	Description
D3	VDD1	P	Supply Voltage
A1	VDD2	P	Supply Voltage
F5	SW1	A	Boost Converter Switch
E5	SW2	A	Boost Converter Switch
D5	FB	A	Boost Converter Feedback
B5	LED1	O	LED1 Driver Output
A5	LED2	O	LED2 Driver Output
B4	LED3	O	LED3 Driver Output
A4	LED4	O	LED4 Driver Output
F2	FLASH	O	Flash LED Driver Output
F3	GNDC	G	Ground for Core Circuitry
D2	RT	A	Oscillator Frequency Setting
C1	VREF	A	Reference Voltage
B1	VDDA	P	Internal LDO
F4	GND_SW1	G	Boost Converter Ground
E4	GND_SW2	G	Boost Converter Ground
C5	GND_LED	G	LEDs 1 to 4 Driver Ground Connection
F1	GND_FLASH	G	Flash Driver Ground Connection

(1) A: Analog Pin D: Digital Pin G: Ground Pin P: Power Pin, I: Input Pin I/O: Input/Output Pin O: Output Pin OD: Open Drain Pin

Table 1. Pin Descriptions (continued)

Pin	Name	Type[1]	Description
A2	IFLASH	A	Resistor for Flash Current Setting
D1	GNDA	G	Analog Ground Connection
C3	GND	G	Ground
E1	VDD_IO	P	Supply Voltage for Digital Interface
A3	NRST	DI	Low Active Reset
B3	SCL	DI	I^{2}C Compatible Interface Clock Signal
E2	SDA	OD	I^{2}C Compatible Interface Data Signal
E3	FLASH_SYNC	DI	FLASH LED Control
D4	T2	DO	Test Pin (Result)
C4	T1	DI	Test Pin (Clock)
C2	ASE1	AI	Audio Input
B2	ASE2	AI	Audio Input

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)(3)

Voltage on power pins ($V_{DD1,2}$)	-0.3V to +6.0V
Voltage on analog pins	-0.3V to $V_{DD1,2}$+0.3V with 6.0V max
Voltage on input/output pins	-0.3V to $V_{DD1,2}$+0.3V with 6.0V max
V(all other pins): Voltage to GND	-0.3V to 6.0V
I(V_{REF})	10 µA
I(FLASH)	500 mA
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	125ºC
Storage Temperature Range	-65ºC to +150ºC
Maximum Lead Temperature (Reflow soldering, 3 times) (5)	260ºC
ESD Rating, Human Body Model (6)	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160ºC (typ.) and disengages at T_J = 140ºC (typ.).
(5) For detailed soldering specifications and information, see application note AN1112 : DSBGA Wafer Level Chip Scale Package.
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. MIL-STD-883 3015.7

Operating Ratings (1), (2)

Voltage on power pins ($V_{DD1,2}$)	3.0 to 5.5V
Voltage on ASE1, ASE2	0V to 1.6V
V_{DD_IO}	1.65V to V_{DD1}
Junction Temperature (T_J) Range	-30ºC to +125ºC
Ambient Temperature (T_A) Range (3)	-30ºC to +85ºC

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (1)	60 - 100ºC/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

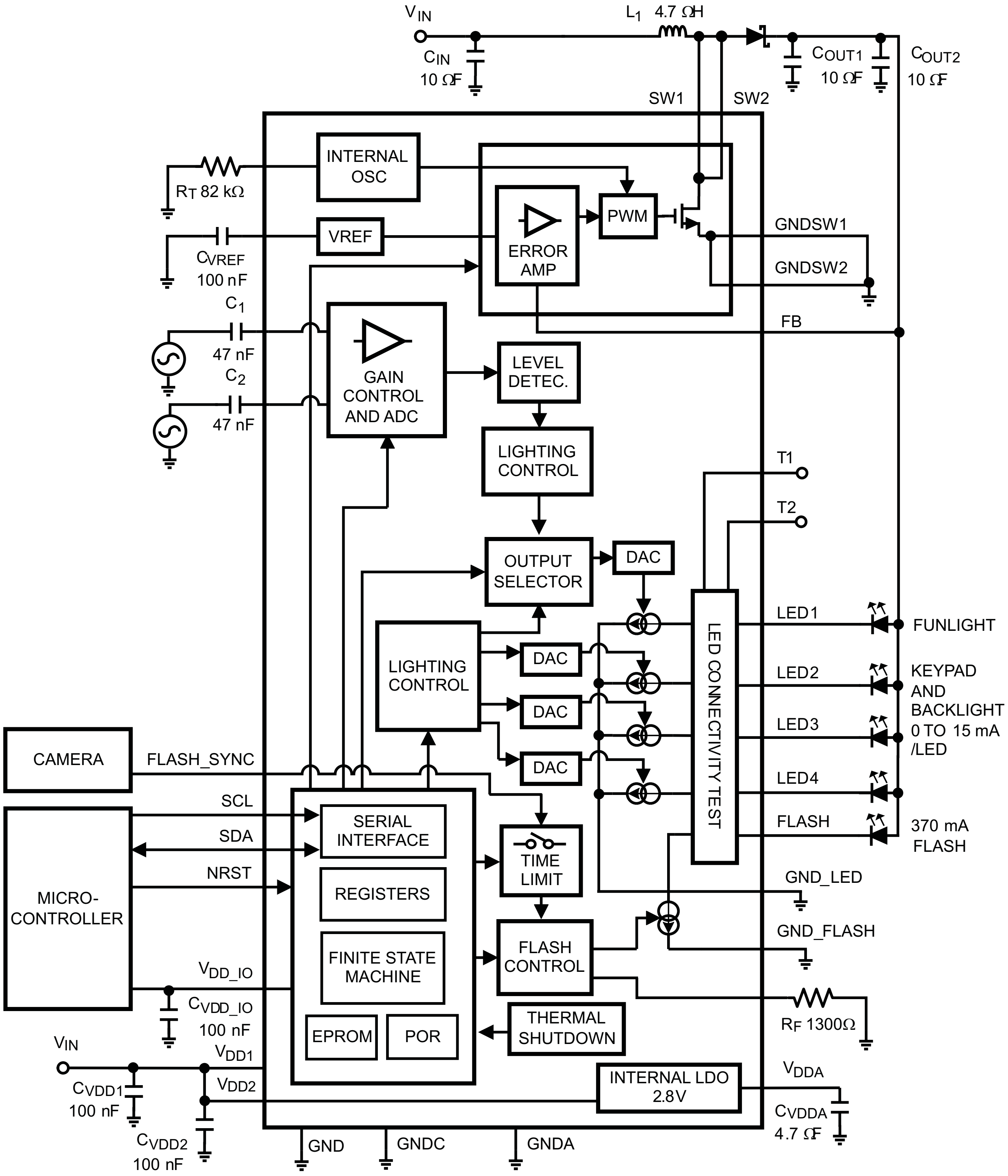
Electrical Characteristics(1) (2)

Limits in standard typeface are for T_J = 25ºC. Limits in boldface type apply over the operating ambient temperature range (-30ºC < T_A < +85ºC). Unless otherwise noted, specifications apply to the LP55271 Block Diagram with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, C_{VDD_IO} = 100 nF, C_{VREF} = 100 nF, C_{VDDA} = 4.7 µF, C_{VDD1} = 100 nF, C_{VDD2} = 100 nF, L_1 = 4.7 µH. (3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{SHUT\ DOWN}$	Current of V_{DD1} + V_{DD2} pins + Leakage Current of SW1, SW2, LED1 to 4 and FLASH	Voltage on V_{DD_IO} = 0V, NRST = L, NSTBY(bit) = L		1	**5**	µA
I_{DD}	Active Mode Supply Current (V_{DD1} + V_{DD2} current)	NRST = H, NSTBY(bit) = H, no load, EN_BOOST(bit) = L, SCL, SDA = H		350		µA
I_{DD}	No load supply current (V_{DD1} + V_{DD2} current)	NSTBY(bit) = H, EN_BOOST(bit) = H, SCL, SDA, NRST = H, AUTOLOAD_EN(bit) = L		850		µA
I_{VDDIO}	V_{DD_IO} Standby Supply current	NSTBY(bit) = L			**1**	µA
V_{DDA}		I_{VDDA} = 1 mA	**-4%**	2,8V	**+4%**	V

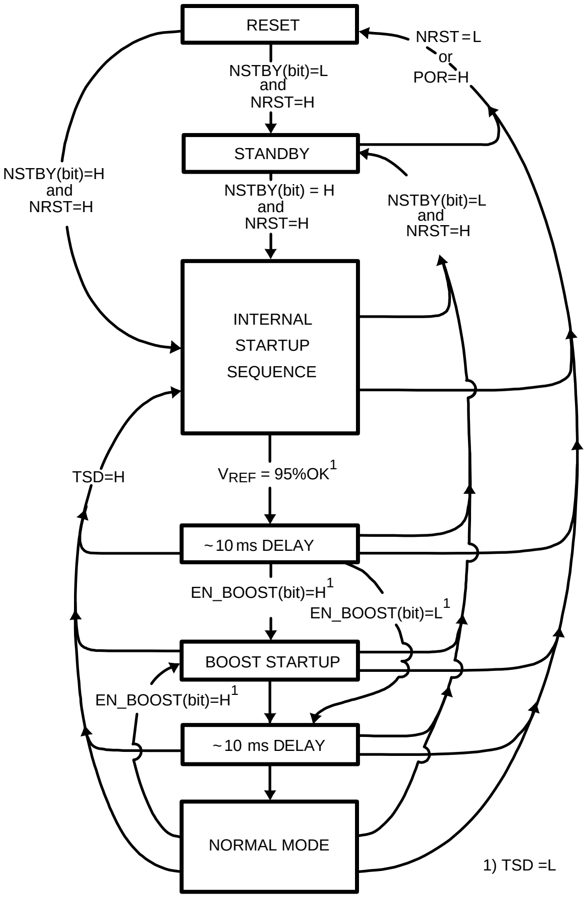
(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

LP55271 BLOCK DIAGRAM



DEVICE INFORMATION

Modes of Operation



RESET: In the reset mode all the internal registers are reset to the default values. Reset is entered always if input NRST is LOW or internal Power On Reset (POR) is active. Power on reset will activate during the chip startup or when the supply voltage V_{DD2} falls below 1.5V. Once V_{DD2} rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode. NSTBY control bit is low after POR by default.

STANDBY: The standby mode is entered if the register bit NSTBY is LOW and reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after start up.

STARTUP: When NSTBY bit is written high, the internal startup sequence powers up all the needed internal blocks (V_{REF}, Oscillator, etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. If the chip temperature rises too high, the thermal shutdown (TSD) disables the chip operation and startup mode is entered until no thermal shutdown event is present.

BOOST STARTUP: Soft-start for boost output is generated in the boost startup mode. The boost output is raised in a low current PWM mode during the 10 ms delay generated by the state-machine. The boost startup is entered from internal startup sequence if EN_BOOST is HIGH or from normal mode when EN_BOOST is written HIGH.

NORMAL: During normal mode the user controls the chip using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

Magnetic Boost DC/DC Converter

The LP55271 boost DC/DC converter generates a 4.00 – 5.40V output voltage to drive the LEDs from a single Li-Ion battery (3.0V to 4.5V). The output voltage is controlled with a 4-bit register in 8 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter has 2.0 MHz / 1.0 MHz selectable switching frequency operation, when the timing resistor RT is 82 kΩ.

The LP55271 boost converter uses pulse-skipping elimination method to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An internal active load is used to remove the excess charge from the output capacitor when needed.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The output voltage control changes the resistor divider in the feedback loop.

Figure 3 shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage.
   - Keeps the output below breakdown voltage.
   - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current.
   - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback (FB) protection for no connection.
4. Duty cycle limiting, done with digital control.

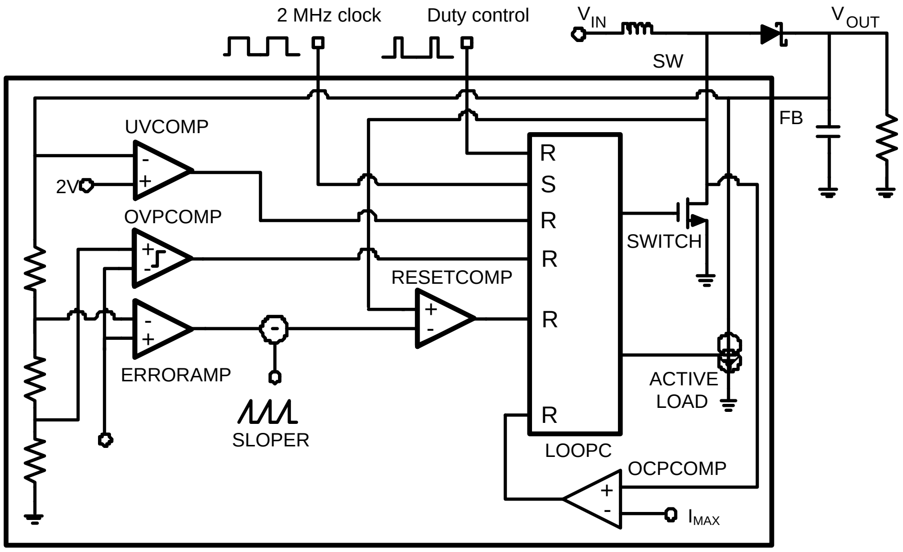


Figure 3. Boost Converter Topology

MAGNETIC BOOST DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for $T_J = 25ºC$. Limits in **boldface** type apply over the operating ambient temperature range ($-30ºC < T_A < +85ºC$). Unless otherwise noted, specifications apply to the LP55271 Block Diagram with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, C_{VDDIO} = 100 nF, C_{VREF} = 100 nF, C_{VDDA} = 4.7 µF, C_{VDD1} = 100 nF, C_{VDD2} = 100 nF, L_1 = 4.7 µH. (4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LOAD}	Load Current (1)	$3.2V \le V_{IN} \le 4.5V$ $V_{OUT} = 5.0V$			670	mA
V_{OUT}	Output Voltage Accuracy (FB pin)	$3.2V \le V_{IN} \le 4.5V$ V_{OUT} (target value) = 5.0V, active load off	**−5**		**+5**	%
	Output Voltage (FB Pin)	$3.0V \le V_{IN} \le (5.0V+V_{SCHOTTKY})$ active load off		5.0		V
		$V_{IN} > (5.0V + V_{SCHOTTKY})$		$V_{IN} - V_{SCHOTTKY}$		
RDS_{ON}	Switch ON Resistance	$V_{IN} = 3.6V$, $I_{SW} = 1.0A$		0.20	0.4	Ω
f_{PWF}	PWM Mode Switching Frequency	RT = 82 kΩ FREQ_SEL (bit) = 1 FREQ_SEL (bit) = 0		 2.0 1.0		MHz
	Frequency Accuracy	$3.2V \le V_{DD1,2} \le 5.0V$ RT = 82 kΩ	−6 **-9**	±3	+6 **+9**	%
t_{PULSE}	Switch Pulse Minimum Width	no load		25		ns
$t_{STARTUP}$	Startup Time			10		ms
I_{CL_OUT}	SW1 + SW2 current limit			1.7		A

(4) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(1) Specified currents are the worst case currents. If input voltage is larger or output voltage is smaller, current can be increased according to graph "Boost Maximum Output Current".

BOOST STANDBY MODE

User can set the boost converter to STANDBY mode by writing the register bit EN_BOOST low when there is no load to avoid idle current consumption. When EN_BOOST is written high, the converter starts in low current PWM (Pulse Width Modulation) mode for 10 ms and then goes to normal PWM mode.

BOOST CONTROL REGISTERS

User can control the boost output voltage and the switching frequency according to the following tables.

Boost Output Voltage [3:0] Register	Boost Output Voltage (V) (Typical)
0000	4.00
0001	4.20
0011	4.40
0111	4.60 default
1000	4.80
1001	5.00
1011	5.20
1111	5.40

FREQ_SEL Bit	Boost Switching Frequency (Typical)
0	1.0 MHz default
1	2.0 MHz

Boost Converter Typical Performance Characteristics

T_J = 25ºC. Unless otherwise noted, typical performance characteristics apply to the LP55271 Block Diagram with: V_{IN} = 3.6V, V_{OUT} = 5.0V, C_{IN} = 10 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, C_{VDD_IO} = 100 nF, C_{VREF} = 100 nF, C_{VDDA} = 4.7 µF, C_{VDD1} = 100 nF, C_{VDD2} = 100 nF, L1 = 4.7 µH (1).

Boost Converter Efficiency

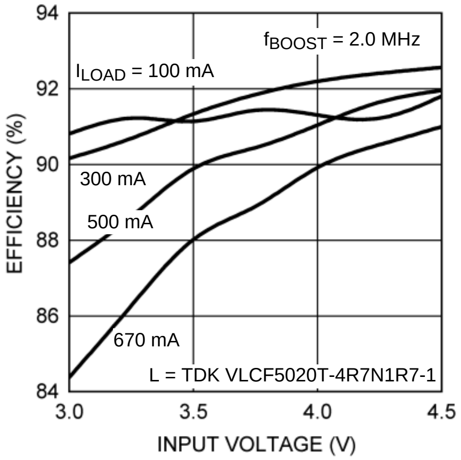


Figure 4.

Boost Typical Waveforms at 100 mA Load

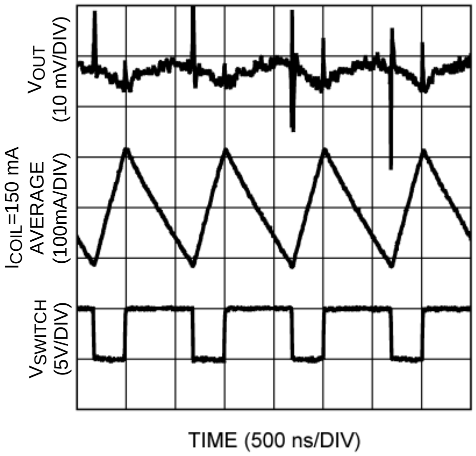


Figure 5.

Battery Current vs Voltage

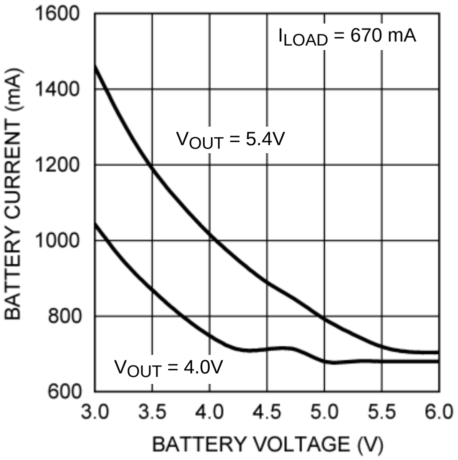


Figure 6.

Boost Frequency vs RT Resistor

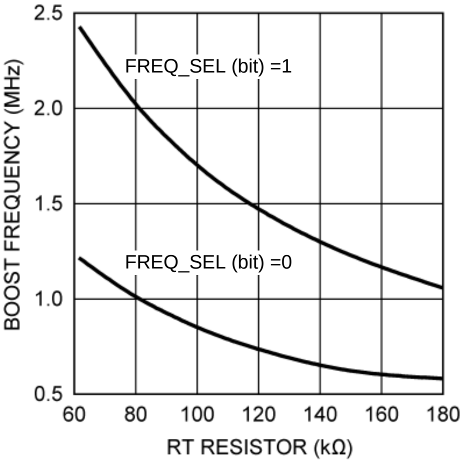


Figure 7.

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(1) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Boost Line Regulation 3.0V - 3.6V

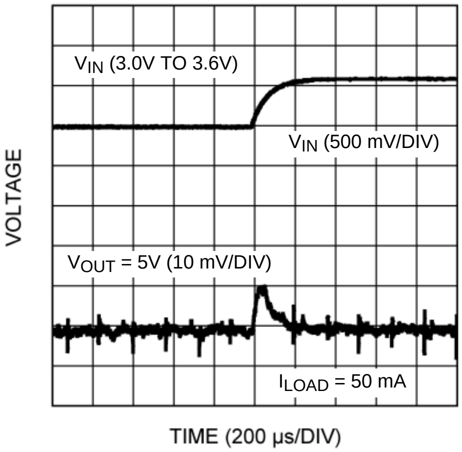


Figure 8.

Boost Startup to 5.4V with no Load

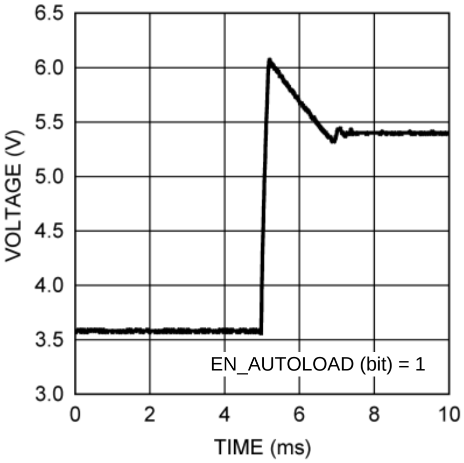


Figure 9.

Boost Load Transient Response, 50 mA to 100 mA

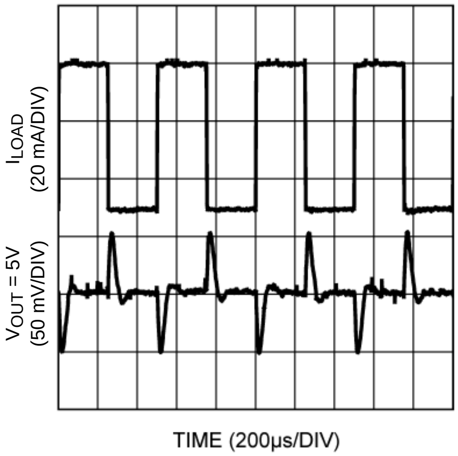


Figure 10.

Boost Maximum Output Current

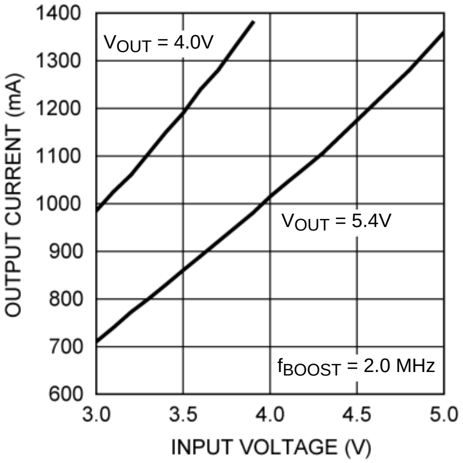


Figure 11.

Flash Driver

LP55271 has an internal constant current driver that is capable for sinking low (46 mA) and high (370 mA) current mainly targeted for torch and flash LED in camera phone applications. 370 mA flash driver can be hardware or software enabled. Flash safety function prevents hardware damages due to possible overheating when the flash has been stuck on because of a hardware, software or user error.

Flash safety counter starts counting when the flash is activated and disables the flash automatically when the pre-defined 1.0s or 2.0s time limit is reached. Flash is activated with FLASH_SYNC bit or FLASH_SYNC pin, as defined in the table below. Safety time limit is defined by SAFETY_TIME bit. (Time limit is 2.0s if SAFETY_TIME bit is low and 1.0s if the bit is high.)

Flash driver currents — both torch and flash — are set with external resistor R_F. The flash current is $480/R_F$ amperes and the torch current is $60/R_F$ amperes. User should not use lower resistance value than 1200Ω.

Table 2. Flash LED Control(1)

EN_TORCH bit	EN_FLASH bit	FLASH_SYNC bit or pin	SAFETY_TIME bit	Flash LED Action
0	0	X	X	Off
1	0	X	X	Torch
X	1	Change from LOW to HIGH to engage; from HIGH to LOW to disengage	0 for 2.0 seconds; 1 for 1.0 second	Flash

(1) X = don't care

Table 3. Flash Programming Example

Address	Data	Function
00H	8FH	Sets safety time to 1.0s. In this example LED1 to LED4 are enabled.
00H	9FH	Enables torch.
00H	FFH	Activates FLASH. EN_FLASH bit and FLASH_SYNC bit are written simultaneously because EN_FLASH disables torch.
00H	BFH	Disables FLASH. If FLASH is disabled by safety time, FLASH_SYNC bit needs to be written to 0 before next FLASH.

FLASH DRIVER ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25ºC. Limits in **boldface** type apply over the operating ambient temperature range (-30ºC < T_A < +85 ºC). Unless otherwise noted, specifications apply to the LP55271 Block Diagram with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, C_{VDDIO} = 100 nF, C_{VREF} = 100 nF, C_{VDDA} = 4.7 µF, C_{VDD1} = 100 nF, C_{VDD2} = 100 nF, L_1 = 4.7 µH, R_F = 1300Ω

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{FLASH}	Flash Mode Sink Current(1)	3.0V ≤ V_{IN} ≤ 5.5V, V_{FLASH} = 1.0V		370		mA
			-7.5		**+7.5**	%
I_{TORCH}	Torch Mode Sink Current(1)	3.0V ≤ V_{IN} ≤ 5.5V		46		mA
$I_{LEAKAGE}$	Flash Driver Leakage Current	V_{FB} = 5.0V		0.1		µA
t_{FLASH}	Flash Turn-On Time (2)			20		µs
V_{SAT}	Saturation Voltage	3.0V ≤ V_{IN} ≤ 5.5V, Current Decreased to 95% of the Maximum Sink Current		550		mV
t_{SAFETY}	Safety Time Accuracy		**-9**		**+9**	%

(1) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers represent the most likely norm.
(2) Flash turn-on time is measured from the moment the flash is activated until the flash current crosses 90% of its target value.

Constant Current Sink Outputs LED1, LED2, LED3, LED4

LP55271 has four independent backlight/keypad LED drivers. All the drivers are regulated constant current sinks. LED currents are controlled by 8-bit current mode DACs. Every driver can be controlled in two ways:

1. Brightness control with constant current drivers

2. Direct ON/OFF control. The current is pre-set by 8-bit current mode DAC.

In addition, LED1 driver can be synchronized to audio input signal amplitude.

By using brightness control user can set brightness of every single LED by using 8-bit brightness control registers. If analog audio is available on system the user can use audio synchronization for synchronizing LED1 to the music. Direct ON/OFF control is mainly for switching LEDs on and off.

LED Control Register (00 hex) has control bits for direct on/off control of all the LEDs. Note that the LEDs have to be turned on in order to control them with audio synchronization (LED1 only) or brightness control.

The brightness is programmed as described in the following.

$I_{LED} = n \text{ x } (15 \text{ mA} / 255)$

where

- n = LED[7:0] (8-bit)
- step = 15 mA / 255 ≈ 0.05882 mA (1)

For example if 13.2 mA is required for driver current:

n = 13.2 mA / (15 mA / 255) ≈ 224

224 = 1110 0000, E0 hex

Table 4. LED1 to LED4 Brightness Control

LED1[7:0], LED2[7:0], LED3[7:0] and LED4[7:0] Registers	Driver Current, mA (typical)
0000 0000	0
0000 0001	0.059
0000 0010	0.118
•	•
1110 0000	13.176
•	•
1111 1110	14.941
1111 1111	15

LED1 TO LED4 DRIVERS ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25ºC. Limits in **boldface** type apply over the operating ambient temperature range (-30ºC < T_A < +85ºC). Unless otherwise noted, specifications apply to the LP55271 Block Diagram with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, C_{VDDIO} = 100 nF, C_{VREF} = 100 nF, C_{VDDA} = 4.7 µF, C_{VDD1} = 100 nF, C_{VDD2} = 100 nF, L_1 = 4.7 µH. (1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{MAX}	Maximum Sink Current			15		mA
$I_{LEAKAGE}$	Leakage Current	V_{FB} = 5.0V		0.03		µA
I_{LED}	Current Tolerance	I_{SINK} = 13.2 mA (target value)		13.2		mA
			-7		**+7**	%
I_{MATCH}	Sink Current Matching Between LED 1 to 4 (1)	I_{SINK} = 13.2 mA		1		%
V_{SAT}	Saturation Voltage	3.0V ≤ V_{IN} ≤ 5.5V, Current Decreased to 95% of the Maximum Sink Current		150	**230**	mV

(1) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(1) Sink current matching is the maximum difference from the average.

Audio Synchronization

The LED1 output can be synchronized to incoming audio signal with Audio Synchronization feature. Audio Synchronization synchronizes LED1 based on input signal's peak amplitude. Programmable gain and automatic gain control function are also available for adjustment of input signal amplitude to light response. Control of LED1 brightness refreshing frequency is done with four different frequency configurations. The digitized input signal has a DC component that is removed by a digital DC-remover. The DC-remover is a high-pass filter where corner frequency is user selectable by using DC_FREQ bit. LP55271 has 2-channel audio (stereo) input for audio synchronization, as shown in Figure 12. The inputs accept signals in the range of 0V to 1.6V peak-to-peak and these signals are mixed into a single wave so that they can be filtered simultaneously.

LP55271 audio synchronization is mainly done digitally and it consists following signal path blocks (see Figure 12).

- Input buffer
- AD converter
- Automatic Gain Control (AGC) and manually programmable gain
- Peak detector

Automatic Gain Control (AGC) adjusts the input signal to suitable range automatically. User can disable AGC and the gain can be set manually with programmable gain. Audio synchronization is based on peak detection method.

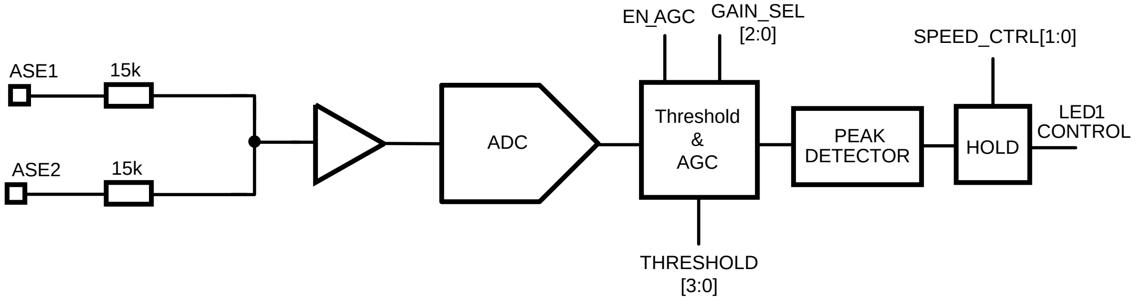


Figure 12.

Audio Synchronization Input Electrical Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Z_{IN}	Input Impedance of ASE1, ASE2		10	15		kΩ
A_{IN}	ASE1, ASE2 Audio Input Level Range (peak-to-peak)	Min input level needs maximum gain; Max input level for minimum gain.	0		1600	mV

CONTROL OF AUDIO SYNCHRONIZATION

The following table describes the controls required for audio synchronization. LED1 brightness control through serial interface is not available when audio synchronization is enabled.

Table 5. Audio Synchronization Control

EN_SYNC	Audio synchronization enabled. Set EN_SYNC = 1 to enable audio synchronization or 0 to disable.
EN_AGC	Automatic gain control. Set EN_AGC = 1 to enable automatic control or 0 to disable. When EN_AGC is disabled, the audio input signal gain value is defined by GAIN_SEL.
GAIN_SEL[2:0]	Input signal gain control. Gain has a range from 0 dB to -46 dB.
SPEED_CTRL[1:0]	Control for refreshing frequency. Sets the typical refreshing rate for the LED1 output.
THRESHOLD[3:0]	Control for the audio input threshold. Sets the typical threshold for the audio inputs signals. May be needed if there is noise on the audio lines.
DC_FREQ	Control for the high-pass filter corner frequency. 0 = 80 Hz 1 = 510 Hz

Table 6. Audio Input Threshold Setting

Threshold[3:0]	Threshold Level, mV (typical)
0000	Disabled
0001	0.2
0010	0.4
*	*
*	*
1110	2.5
1111	2.7

Table 7. Typical Gain Values vs. Audio Input Amplitude

Audio Input Amplitude mV_{P-P}	Gain Value dB
0 to 10	0
0 to 20	-6
0 to 40	-12
1 to 85	-18
3 to 170	-24
5 to 400	-31
10 to 800	-37
20 to 1600	-46

Table 8. Input Signal Gain Control

GAIN_SEL[2:0]	Gain dB
000	0
001	-6
010	-12
011	-18
100	-24
101	-31
110	-37
111	-46

Table 9. Refreshing Frequency

SPEED_CTRL[1:0]	Refreshing Rate Hz
00	FASTEST
01	15
10	7.6
11	3.8

Logic Interface Characteristics

Limits in standard typeface are for T_J = 25ºC. Limits in **boldface** type apply over the operating ambient temperature range (-30ºC < T_A < +85ºC). Unless otherwise noted, specifications apply to the LP55271 Block Diagram with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, C_{VDDIO} = 100 nF, C_{VREF} = 100 nF, C_{VDDA} = 4.7 µF, C_{VDD1} = 100 nF, C_{VDD2} = 100 nF, L_1 = 4.7 µH (1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Logic Inputs SCL and FLASH_SYNC						
V_{IL}	Input Low Level	V_{DD_IO} = 1.65V to $V_{DD1,2}$			**0.2 x V_{DD_IO}**	V
V_{IH}	Input High Level		**0.8 x V_{DD_IO}**			V
I_I	Input Current		**-1.0**		**1.0**	µA
f_{SCL}	SCL Pin Clock Frequency			400		kHz
Logic Input NRST						
V_{IL}	Input Low Level	V_{DD_IO} = 1.65V to $V_{DD1,2}$			**0.5**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Input Current		**-1.0**		**1.0**	µA
t_{NRST}	Reset Pulse Width		**10**			µs
Logic Input/Output SDA						
V_{OL}	Output Low Level	I_{OUT} = 3 mA		0.3	**0.5**	V
I_L	Output leakage current	V_{OUT} = 2.8V			**1.0**	µA

(1) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

I²C Compatible Interface

I²C SIGNALS

The SCL pin is used for the I²C clock and the SDA pin is used for bidirectional data transfer. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus (typ. ~1.8 kΩ). Signal timing specifications are shown in table I²C Timing Parameters.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

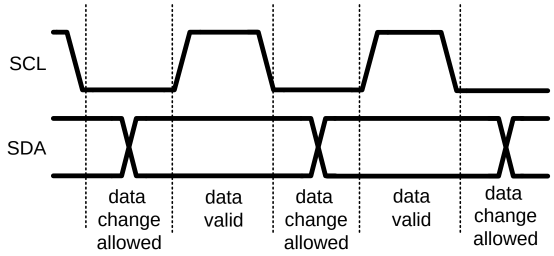


Figure 13. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

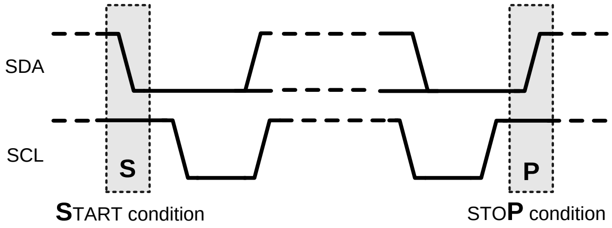


Figure 14. I^2C Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

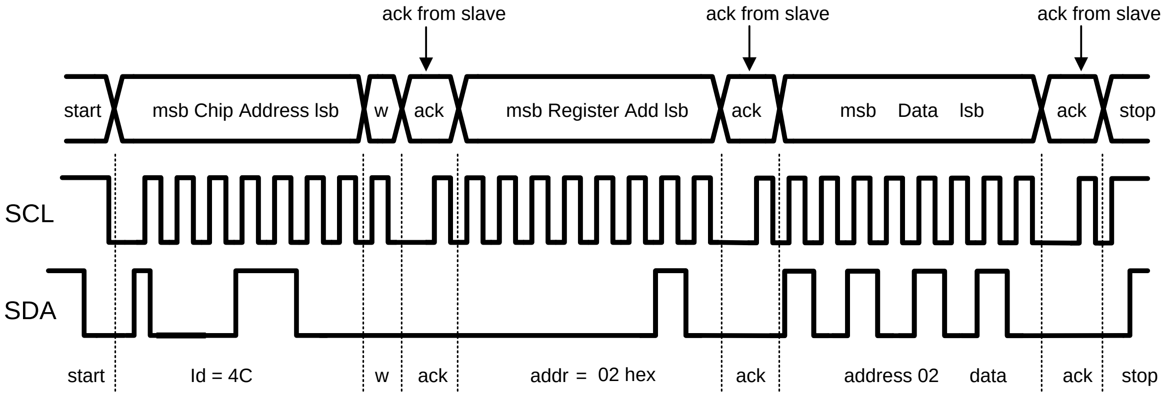
After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP55271 address is 4C hex. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the I^2C Read Cycle waveform.

MSB							LSB
ADR6 Bit7	ADR5 bit6	ADR4 bit5	ADR3 bit4	ADR2 bit3	ADR1 bit2	ADR0 bit1	R/W bit0

← I^2C SLAVE address (chip address) →

Figure 15. I^2C Chip Address 4C hex for LP55271



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = chip address, 4C hex for LP55271.

Figure 16. I^2C Write Cycle

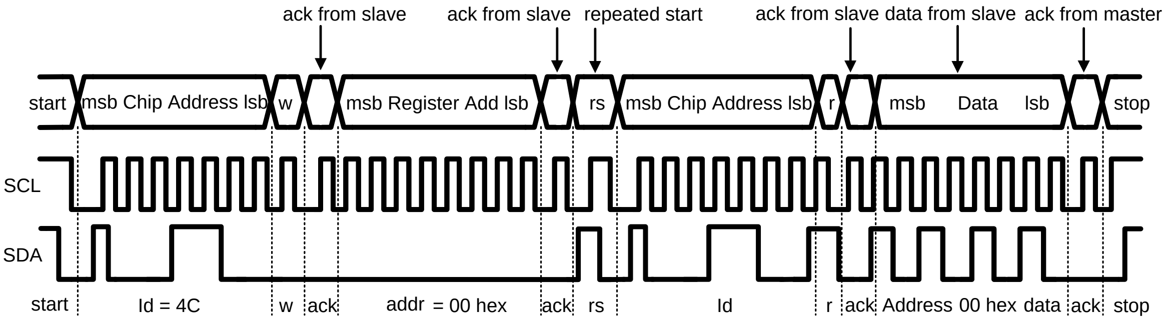


Figure 17. I²C Read Cycle

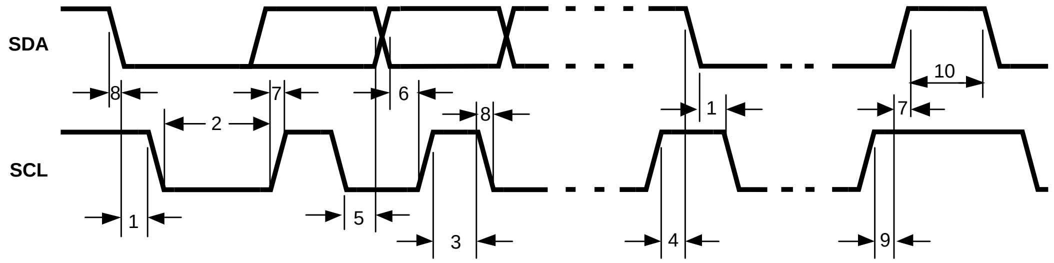


Figure 18. I²C Timing Diagram

I²C TIMING PARAMETERS ($V_{DD1,2}$ = 3.0 to 4.5V, V_{DDIO} = 1.65V to $V_{DD1,2}$)

Symbol	Parameter	Limit[1]		Unit
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LP55271)	300	900	ns
5	Data Hold Time (Input direction)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

(1) Specified by design. Not production tested.

Test Interface

The test bus can be controlled externally or internally. For the external control, the LP55271 pins $V_{DD1,2}$ only need to be powered. External control is independent on status of NRST and V_{DDIO} pins. T1 is an input and it has an internal 6 kΩ pull-down resistor. T2 is an output line for the test result with an internal 200 kΩ pull-down resistor. When T1 is low, T2 is always pulled down; when T1 is high, T2 is indicating the result of the test.

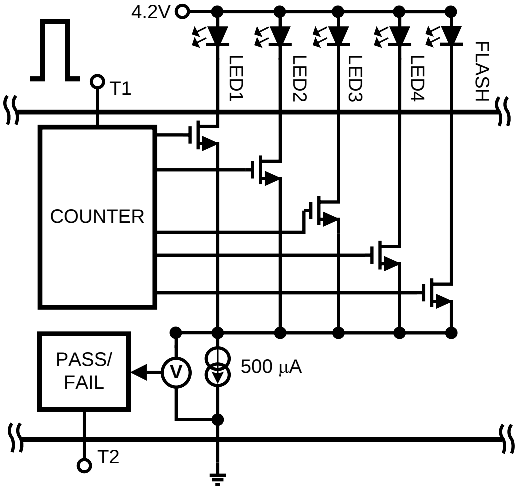


Figure 19. High Level Schematic Representation of the Test Interface

The device is capable of detecting a defective unit in three cases:

- **Production test 1:** The LP55271 is assembled on a printed wiring board (PWB), but there is no LEDs connected on current sink outputs. An external 4.2V test voltage is supplied on the V_{DD1} and V_{DD2} pins, from which follows that the reset operating mode is entered with POR. Test pin T1 is pulled high. The chip will send an acknowledge “1” onto the T2 pin if the chip is in working order; otherwise T2 stays low (0). Refer to Test Interface Timing Diagram.
- **Production test 2:** The LP55271 is assembled on a PWB with the external components shown in LP55271 Block Diagram. 4.2V voltage is connected to V_{DD1}, V_{DD2} and FB pins (see Figure 19), from which follows that the reset operating mode is entered with POR. Test pin T1 is pulled high. The chip will send an acknowledge “1” onto the T2 pin if the chip is in working order; otherwise T2 stays low (0). If the ACK is “1”, a repetitive test pattern “0-1-0-1-0-1-0-1-0-1-0-1” is applied to T1 pin and if the LED corresponding the pattern (see Test Interface Timing Diagram) is connected properly T2 gives “1”, otherwise T2 stays low. The last “1” disengages the test.
- **Field test:** Build-in self-test through the I^2C compatible control interface. The LP55271 is enabled (NSTBY(bit) = 1, EN_BOOST(bit) = 1) and external test pins T1 and T2 are disconnected. The result can be read through the I^2C compatible control interface. LED test is enabled by writing to address 0Ch hex data 01h. Result can be read from the same address during the next I^2C cycle. Note: I^2C compatible interface clock signal controls the timing of the test procedure. For that reason the clock signal frequency should be 50 kHz or less during the build-in self-test.

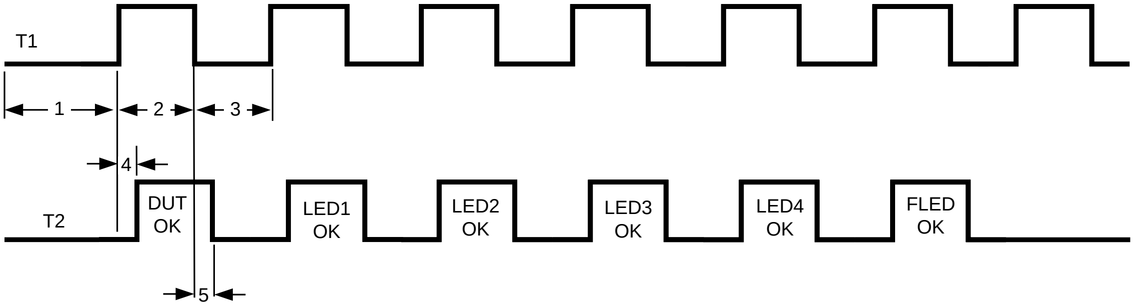


Figure 20. Test Interface Timing Diagram

Table 10. Test Interface Timing Parameters

Symbol	Test Conditions	Parameter	Limit[1]		Unit
			Min	Max	
1	$V_{DD1,2}$ = 4.2V	Setup Time after $V_{DD1,2}$ = 4.2V	1		ms
2		Clock High Time	200		µs
3		Clock Low Time	200		µs
4		Test Result Settling Time		10	µs
5		Data Hold Time	0	10	ns

(1) Specified by design. Not production tested.

Test Interface Characteristics

Limits in standard typeface are for T_J = 25ºC.

Symbol	Parameter[1]	Test Conditions	Min	Typ	Max	Unit
Logic Input T1						
V_{IL}	Input Low Level	$V_{DD1,2}$ = 4.2V			0.5	V
V_{IH}	Input High Level		1.2			V
Logic Output T2						
V_{OL}	Output Low Level	$V_{DD1,2}$ = 4.2V, I_{OUT} = 3 mA (pull-up current)		0.3	0.5	V
V_{OH}	Output High Level	$V_{DD1,2}$ = 4.2V, I_{OUT} = -3 mA (pull-down current)	$V_{DD1,2}$ - 0,5	3.9		V
Internal Current Sink						
I_{SINK}	Sink Current	$V_{DD1,2}$ = 4.2V		500		µA
Connectivity Test Pass Range						
V_{PASS1}	Voltage Over the Internal Current Sink; Low Level	Production test cases $V_{DD1,2}$ = 4.2V V_{OUT} = 3.9V to 4.2V		0.10		V
			-50		+50	%
V_{PASS2}	Voltage Over the Internal Current Sink; High Level			2.90		V
			-10		+10	%
V_{PASS3}	Voltage Over the Internal Current Sink; Low Level	Field test cases $V_{DD1,2}$ = 3.0V to 4.2V V_{OUT} = 5.0V ± 5%		0.40		V
			-30		+30	%
V_{PASS4}	Voltage Over the Internal Current Sink; High Level			3.95		V
			-10		+10	%

(1) Specified by design. Not production tested.

APPLICATION INFORMATION

Recommended External Components

OUTPUT CAPACITOR, C_{OUT1}, C_{OUT2}

The output capacitors C_{OUT1}, C_{OUT2} directly affect the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower V_{OUT} ripple that the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower V_{OUT} ripple magnitude than the tantalums of the same value. However, the dv/dt of the V_{OUT} ripple with the ceramics is much lower that the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V is recommended

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage. The capacitance value can fall to below half of the nominal capacitance. Too low output capacitance can make the boost converter unstable.

INPUT CAPACITOR, C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

OUTPUT DIODE, D_1

The output diode for a boost converter must be chosen correctly depending on the output voltage and the output current. The diode must be rated for a reverse voltage greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current (~1.7A at maximum load). A Schottky diode should be used for the output diode. Schottky diodes with a low forward voltage drop (V_F) and fast switching speeds are ideal for increasing efficiency in portable applications. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer. In Schottky barrier diodes reverse leakage current increases quickly with the junction temperature. Therefore, reverse power dissipation and the possibility of thermal runaway has to be considered when operating under high temperature conditions. Examples of suitable diodes are Diodes Incorporated type DFLS220L, ON Semiconductor type MBRA210LT3 and Philips type PMEG1020.

INDUCTOR, L_1

The LP55271 high switching frequency enables the use of the small surface mount inductor. A 4.7 µH shielded inductor is suggested for 2 MHz switching frequency. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (~1.7A at maximum load). Less than 300 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW1 and SW2 pins as close to the I_C as possible. Example of a suitable inductor is TDK type VLCF5020T-4R7N1R7-1.

Table 11. Recommended External Components

Symbol	Symbol Explanation	Value	Unit	Type
C_{VDD1}	V_{DD1} Bypass Capacitor	100	nF	Ceramic, X5R
C_{VDD2}	V_{DD2} Bypass Capacitor	100	nF	Ceramic, X5R
$C_{OUT1,2}$	Output Capacitors from FB to GND	2 x 10 µF ± 10%	µF	Ceramic, X5R, 10V
C_{IN}	Input Capacitor from Battery Voltage to GND	10 ± 10%	µF	Ceramic, X5R, 10V
C_{VDDIO}	V_{DD_IO} Bypass Capacitor	100	nF	Ceramic, X5R
C_{VDDA}	V_{DDA} Bypass Capacitor	4.7	µF	Ceramic, X5R, 6.3V
$C_{1,2}$	Audio Input Capacitors	47	nF	Ceramic, X5R
R_T	Oscillator Frequency Bias Resistor	82	kΩ	1%
R_F	Flash Current Set Resistor for 370 mA Sink Current	1300	Ω	1%

Table 11. Recommended External Components (continued)

Symbol	Symbol Explanation	Value	Unit	Type
C_{VREF}	Reference Voltage Capacitor, between V_{REF} and GND	100	nF	Ceramic, X5R
L_1	Boost Converter Inductor	4.7	µH	Shielded, low ESR, I_{SAT} ~1.7A
D_1	Rectifying Diode, V_F at maxload	0.35	V	Schottky diode
	Flash LED	User defined		
	LED1 to LED4			

Control Registers

Table 12. LP55271 Control Registers and Default Values

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	**LED Control Register**	safety_time	flash_sync	en_flash	en_torch	en_led1	en_led2	en_led3	en_led4
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
01	**LED1**	led1[7]	led1[6]	led1[5]	led1[4]	led1[3]	led1[2]	led1[1]	led1[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
02	**LED2**	led2[7]	led2[6]	led2[5]	led2[4]	led2[3]	led2[2]	led2[1]	led2[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
03	**LED3**	led3[7]	led3[6]	led3[5]	led3[4]	led3[3]	led3[2]	led3[1]	led3[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
04	**LED4**	led4[7]	led4[6]	led4[5]	led4[4]	led4[3]	led4[2]	led4[1]	led4[0]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0B	**ENABLES**		nstby	en_boost		en_autoload	freq_sel		
			0	**0**		**1**	**0**		
0C	**LED Test Control**		led1_ok	led2_ok	led3_ok	led4_ok	flashled_ok		en_test
			r/o	**r/o**	**r/o**	**r/o**	**r/o**		**0**
0D	**Boost Output**					boost[3]	boost[2]	boost[1]	boost[0]
						0	**1**	**1**	**1**
2A	**Audio Sync Control1**	gain_sel[2]	gain_sel[1]	gain_sel[0]	dc_freq	en_agc	en_sync	speed_ctrl[1]	speed_ctrl[2]
		0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2B	**Audio Sync Control2**	threshold[3]	threshold[2]	threshold[1]	threshold[0]				
		0	**0**	**1**	**1**				

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP55271TL/NOPB	ACTIVE	DSBGA	YZR	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D55B	Samples
LP55271TLX/NOPB	ACTIVE	DSBGA	YZR	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D55B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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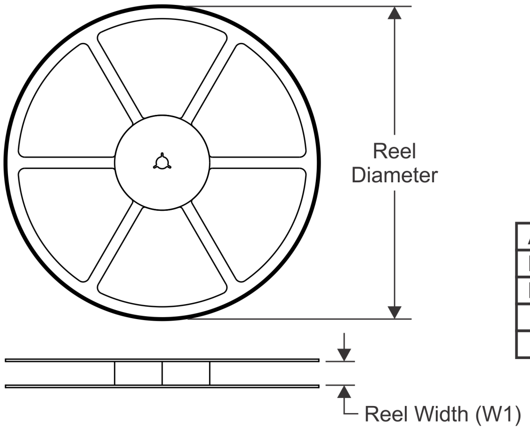
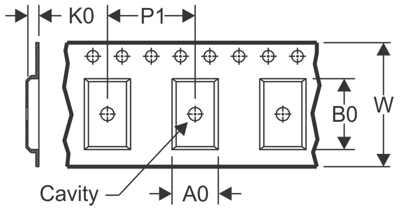
TAPE AND REEL INFORMATION

REEL DIMENSIONS

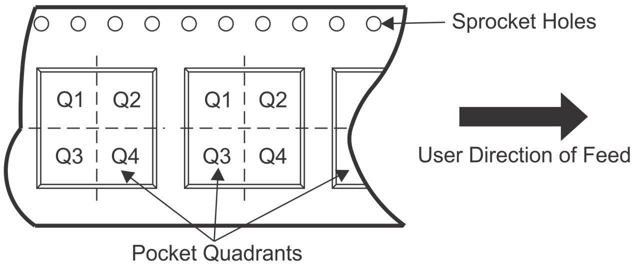


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

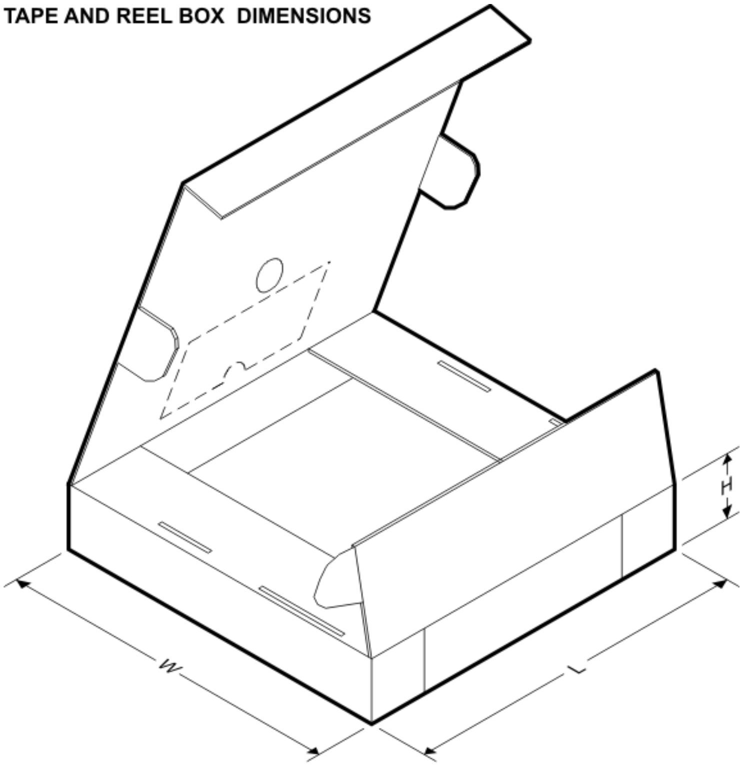
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP55271TL/NOPB	DSBGA	YZR	30	250	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1
LP55271TLX/NOPB	DSBGA	YZR	30	3000	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1

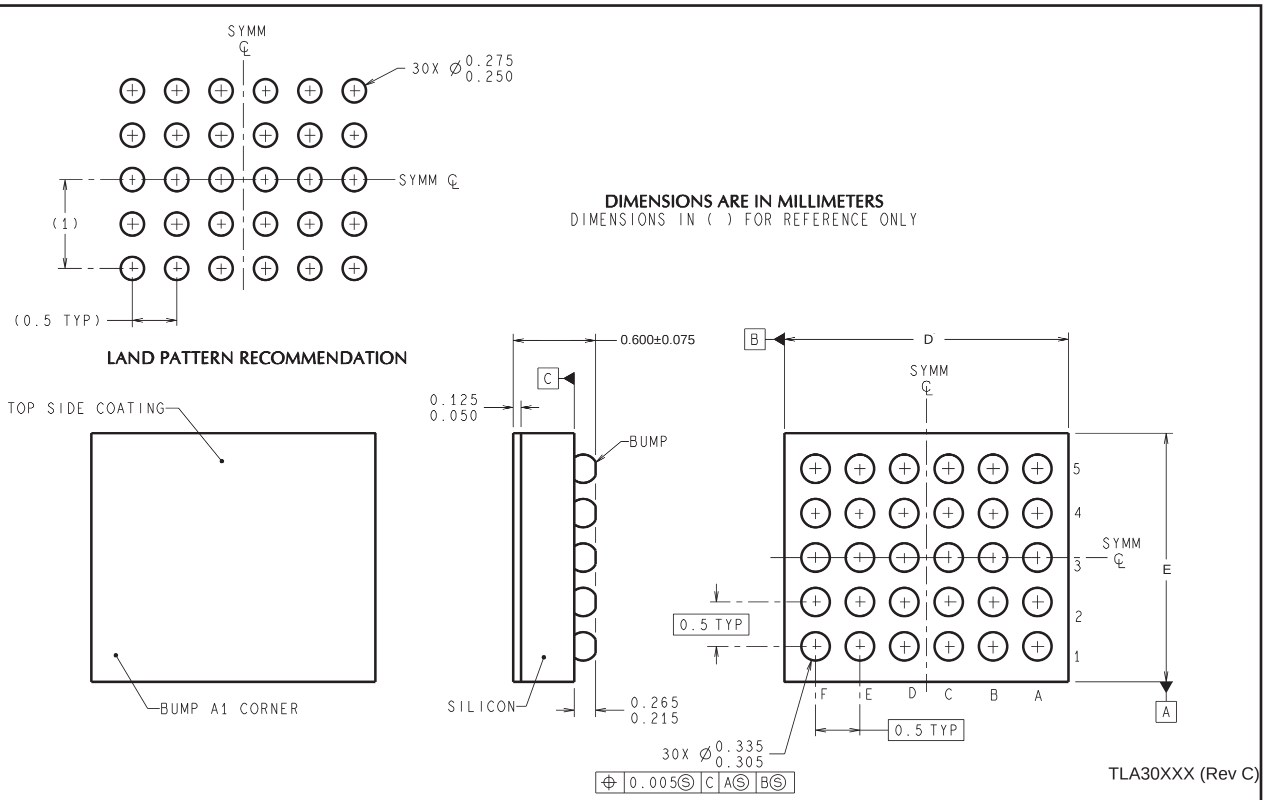
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP55271TL/NOPB	DSBGA	YZR	30	250	210.0	185.0	35.0
LP55271TLX/NOPB	DSBGA	YZR	30	3000	210.0	185.0	35.0

YZR0030



D: Max = 2.998 mm, Min =2.938 mm

E: Max = 2.498 mm, Min =2.438 mm

4215057/A 12/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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