LP5552 PWI 2.0 and PowerWise® Technology Compliant Energy Management Unit

Check for Samples: LP5552

FEATURES

- **High-efficiency PowerWise Technology Adaptive Voltage Scaling for Intelligent Energy Management in AVS and DVS Environments**
- **PWI 2.0 Open Standard Interface for System-level Power Management**
- **Two Digitally Programmable 3.6MHz Buck Regulators to Power Dual-voltage Domains**
- **Five Programmable LDOs for System Functions Such as:**
  - **PLL/Clock Generation**
  - **I/O**
  - **Memory Retention**
- **Internal Soft Start**
- **Variable Regulator Power up Sequencing**

APPLICATIONS

- **GSM/GPRS/EDGE & UMTS Cellular Handsets**
- **Hand-held Radios**
- **PDAs**
- **Battery-powered Devices**
- **Portable Instruments**

KEY SPECIFICATIONS

- **2.7V to 4.8V Input Voltage Range**
- **±2% (typical) Output Voltage Accuracy**
- **Programmable DC/DC Buck Converters**
  - **800mA Output Current per Switcher**
  - **Up to 88% Switcher Efficiency**
  - **Digitally programmable from 0.6V — 1.235V**
- **Programmable LDOs**
  - **Five digitally programmable LDOs**

DESCRIPTION

The LP5552 is a PWI™ 2.0 compliant Energy Management Unit (EMU) for reducing power consumption in low-power, portable applications.

The LP5552 contains 2 advanced, digitally controlled switching regulators for supplying variable voltages to a SoC or processor. The device also incorporates 5 programmable low-dropout, low-noise linear regulators for powering I/O, peripheral logic blocks, auxiliary system functions, and maintaining memory retention (dual-domains) in shutdown-mode.

The device is controlled via the high-speed serial PWI 2.0 open-standard interface. The LP5552 operates cooperatively with PowerWise® technology-compatible processors to optimize supply voltages adaptively (AVS - Adaptive Voltage Scaling) over process and temperature variations. It also supports dynamic voltage scaling (DVS) using frequency/voltage pairs from pre-characterized lookup tables.

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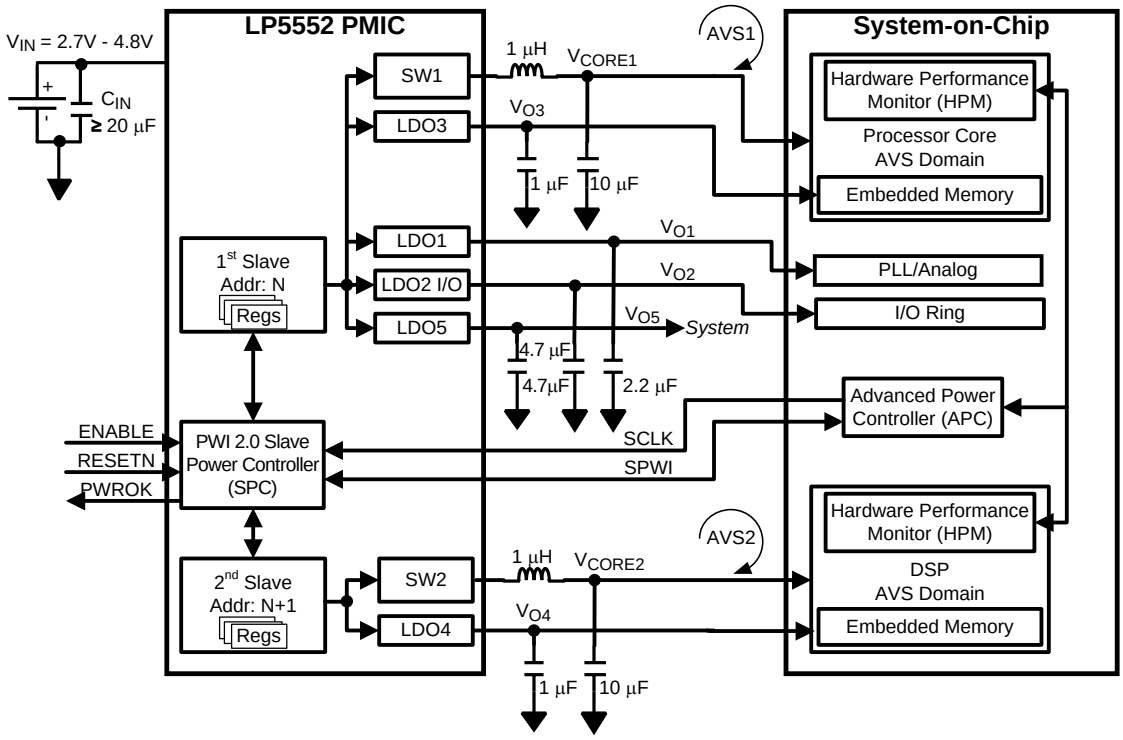
SYSTEM DIAGRAM



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CONNECTION DIAGRAM

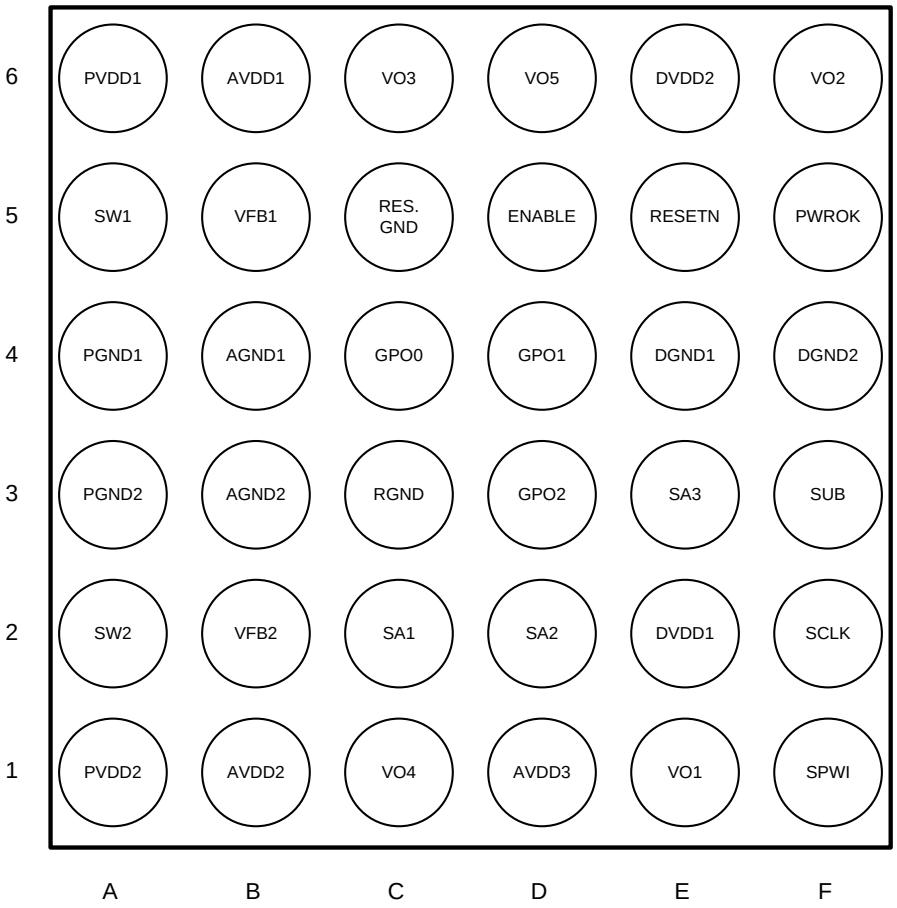

Figure 1. LP5552 Pinout — Top View

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Pin Descriptions

Pin #	Pin Name	I/O[1]	Type[1]	Function
E2	DVDD1	P	P	Power supply voltage input for digital. Connect to V_{IN}.
E6	DVDD2	P	P	Power supply voltage input for digital, LDO2, and LDO5. Connect to V_{IN}.
B6	AVDD1	P	P	Power supply voltage input for analog, switching regulator #1, and LDO3. Connect to VIN.
B1	AVDD2	P	P	Power supply voltage input for analog, switching regulator #2, and LDO4. Connect to V_{IN}.
D1	AVDD3	P	P	Power supply voltage input for analog, and LDO1. Connect to V_{IN}.
A6	PVDD1	P	P	Power supply voltage input to internal PFET of switching regulator #1. Connect to V_{IN}.
A1	PVDD2	P	P	Power supply voltage input to internal PFET of switching regulator #2. Connect to V_{IN}.
E4	DGND1	G	G	Digital Ground. Connect to system Ground.
F4	DGND2	G	G	Digital Ground. Connect to system Ground.
B4	AGND1	G	G	Analog Ground. Connect to system Ground.
B3	AGND2	G	G	Analog Ground. Connect to system Ground.
A4	PGND1	G	G	Power Ground. Connect to system Ground.
A3	PGND2	G	G	Power Ground. Connect to system Ground.
F3	SUB	G	G	Substrate Ground. Connect to system Ground.
C3	RGND	G	G	Reference/sense Ground. Should connect to the Ground node of the switching regulators output capacitors.
D5	ENABLE	I	D	Enable input. Set this digital input high for normal operation.
F2	SCLK	I	D	PowerWise Interface (PWI) clock input
F1	SPWI	I/O	D	PowerWise Interface (PWI) bi-directional data
E5	RESETN	I	D	Active low Reset input. Set this digital input high for normal operation.
F5	PWROK	O	D	Power OK indicator. This is a digital, active high output signal.
E1	VO1	P	P	LDO1 output voltage.
F6	VO2	P	P	LDO2 output voltage. PWI signals SCLK and SPWI reference voltage.
C1	VO4	P	P	LDO4 output voltage. Can be programmed to track V_{CORE2} voltage.
D6	VO5	P	P	LDO5 output voltage.
A5	SW1	P	P	V_{CORE1} Switching node; connected to filter inductor.
A2	SW2	P	P	V_{CORE2} Switching node; connected to filter inductor.
C6	VO3	P	P	LDO3 output voltage. Can be programmed to track V_{CORE1} voltage.
B5	VFB1	I	A	V_{CORE1} Switcher analog feedback input. Connect to the V_{CORE1} output voltage.
B2	VFB2	I	A	V_{CORE2} Switcher analog feedback input. Connect to the V_{CORE2} output voltage.
C4	GPO0	O	D/OD	General Purpose Output 0. Can be programmed as a CMOS output referenced to V_{O2} or as an open-drain output to a user selected voltage.
D4	GPO1	O	D/OD	General Purpose Output 1. Can be programmed as a CMOS output referenced to V_{O2} or as an open-drain output to a user selected voltage.
D3	GPO2	O	D/OD	General Purpose Output 2. Can be programmed as a CMOS output referenced to V_{O2} or as an open-drain output to a user selected voltage.
C2	SA1	I	D	PWI Slave Address Bit 1. Tie to Ground or V_{IN} for 0 or 1, respectively. (Note: SA0 is internal. '0' = Slave(N) = V_{CORE1}; '1' = Slave(N+1) = V_{CORE2})
D2	SA2	I	D	PWI Slave Address Bit 2. Tie to Ground or V_{IN} for 0 or 1, respectively.
E3	SA3	I	D	PWI Slave Address Bit 3 (MSB). Tie to Ground or V_{IN} for 0 or 1, respectively.
C5	Reserved	G	G	Must be tied to Ground. Failure to do so may result in undefined behavior.

(1)

A: Analog Pin **D: Digital Pin** **G: Ground Pin** **P: Power Pin**

I: Input Pin **I/O: Input/Output Pin** **O: Output Pin** **OD: Open Drain Output Pin**

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2) (3)

V_{IN} pins (All V_{DD} pins)	−0.3V to +6.0V
SW1, SW2, V_{01}, V_{02}, V_{03}, V_{04},V_{05} to GND	−0.3V to +(V_{IN}+0.3)V
ENABLE, RESETN, SCLK, SA1, SA2, SA3	−0.3V to +(V_{IN}+0.3)V
SPWI, PWROK, V_{FB1}, V_{FB2}, GPO0, GPO1, GPO2	−0.3V to +(V_{IN}+0.3)V
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Max Continuous Power Dissipation, P_{D-MAX} (4) (5)	Internally limited
Maximum Lead Temperature (Soldering, 10 seconds)	+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(4) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$ where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(5) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160ºC (typ.) and disengages at T_J = 140ºC (typ.).

ESD Ratings (1)

All pins	2kV HBM
	200V MM

(1) The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7.

Operating Ratings (1) (2)

Input voltage range V_{IN}	2.7V to 4.8V
ENABLE, RESETN, PWROK	0V to V_{IN} V
SPWI, SCLK	0V to V_{O2} V
SA1, SA2, SA3	0V to V_{IN} V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.

Thermal Properties

Junction Temperature (T_J)	−40°C to +125°C
Ambient Temperature (T_A) (1)	−40°C to +85°C
Junction-to-Ambient Thermal Resistance (θ_{JA}) (2)	60°C/W

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(2) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51–3. The test board is a 4-layer FR-4 board. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note 1112: DSBGA Wafer Level Chip Scale Package* and *Application Note 1610: LP5552 Evaluation Board*.

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General Electrical Characteristics (1) (2) (3)

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C ≤ T_J≤+125°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	Shutdown Supply Current	All circuits off; -40ºC ≤T_A= T_J≤ +125ºC		1	**75**	µA
	Memory retention current in Deep Sleep (i.e., both slaves in Sleep state)	V_{CORE1} and V_{CORE2} in Sleep state; V_{O1}, V_{O2}, and V_{O5} on, but unloaded; V_{03} and V_{O4} in low I_Q		130	**350**	
	No load supply current	All regulators active and unloaded; switching regulators in Burst-PWM		735	**930**	
UVLO-high	Under Voltage Lockout, high threshold			2.6	2.7	V
UVLO-low	Under Voltage Lockout, low threshold		2.5	2.6		V
Thermal Shutdown						
TSD	Threshold (4) Hysteresis (4)		160 20			°C
Logic and Control Inputs						
V_{IL}	Logic Input Low	ENABLE, RESETN, SPWI, SCLK 2.7V ≤ V_{IN} ≤ 4.8V			**0.2**	V
$V_{IH-SIDEBAND}$	Logic Input High	ENABLE, RESETN 2.7V ≤ V_{IN} ≤ 4.8V	**2.0**			V
V_{IH-PWI}	Logic Input High	SPWI, SCLK 1.5V ≤ V_{O2} ≤ 3.3V	**V_{O2}-0.2**			V
I_{IL}	Input Leakage Current	ENABLE, RESETN 2.7V ≤ V_{IN} ≤ 4.8V	**-1**		**+1**	µA
	Input Leakage Current (Note: Largely due to pull-down resistors)	SPWI, SCLK 1.5V ≤ V_{O2} ≤ 3.3V	**-1**		**+5**	
R_{PD-PWI}	Pull-down resistance for PWI signals	SPWI, SCLK	**0.5**	1	**2**	MΩ
Logic and Control Outputs						
V_{OL}	Logic Output Low	PWROK, SPWI, GPOx I_{SINK} ≤ 1mA			**0.4**	V
$V_{OH-SIDEBAND}$	Logic Output High	PWROK I_{SOURCE} ≤ 1mA	**V_{IN}-0.4**			V
V_{OH-PWI}	Logic Output High	SPWI I_{SOURCE} ≤ 1mA	**V_{O2}-0.4**			V
$V_{OH-GPOx}$	Logic Output High	GPOx, GPOs set for CMOS out I_{SOURCE} ≤ 1mA	**V_{O2}-0.4**			V
$V_{OD-GPOx}$	Maximum Open-Drain High Voltage	GPOx			**V_{IN}+0.3**	V
I_{GPO}	GPO Source/Sink Current			1		mA
T_{ENL}	Minimum ENABLE low pulse time		100			nS
T_{RSTL}	Minimum RESETN low pulse time		100			nS

(1) All voltages are with respect to the potential at the GND pins.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Guaranteed specifically by design.

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Output Specification (1) (2)

Supply	Output Voltage Range (V)	Default Output Voltage (V)	Output Voltage Resolution (mV)	I_{MAX} Maximum Output Current (mA)	Typical Application
V_{CORE1}	0.6 to 1.235	1.235	5	800	Voltage Scaling Domain 1
V_{CORE2}	0.6 to 1.235	1.235	5	800	Voltage Scaling Domain 2
LDO1	0.7 to 2.2	1.2	100	100	PLL/Fixed Logic
LDO2	1.5 to 3.3	3.3	100-300	250	I/O Ring
LDO3	0.6 to 1.35	1.25	50	50	Embedded Memory Domain 1
LDO4	0.6 to 1.35	1.25	50	50	Embedded Memory Domain 2
LDO5	1.2 to 3.3	3.3	100-300	250	Peripheral(s)

(1) All voltages are with respect to the potential at the GND pins.
(2) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

V_{CORE1}/V_{CORE2} Switchers 1 and 2 Output Voltage Characteristics

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output voltage, Static accuracy	0.65V ≤ V_{OUT} ≤ 1.235V I_{OUT} = 0 - 800mA	**-2**		**+2**	%
	Output voltage, Static accuracy	0.60V ≤ V_{OUT} ≤ 0.65V I_{OUT} = 0 - 800mA	**-4**		**+4**	
V_{OUT} Range	Programmable Output Voltage Range	0mA ≤ I_{OUT} ≤ 800mA	0.6	1.235 (default)	1.235	V
ΔV_{OUT}	Line regulation	2.7V ≤ V_{IN} ≤ 4.8V, I_{OUT} = 100mA		0.05		%/V
	Load regulation	100mA ≤ I_{OUT} ≤ 800mA		0.001		%/mA
$T_{SCALING}$	V_{OUT} Setting Time	From min to max output voltage I_{OUT} = 400mA			**30**	µS
I_Q	Quiescent current	No Load, Burst-PWM Mode		325		µA
$R_{DS-ON(P)}$	P-FET resistance	V_{IN} = V_{SG} = 3.6V		255		mΩ
$R_{DS-ON(N)}$	N-FET resistance	V_{IN} = V_{GS} = 3.6V		135		mΩ
I_{OUT}	Continuous load current		**0**		**800**	mA
I_{LIM}	Peak switching current limit		**850**	1200	**1560**	mA
η	Efficiency peak	I_{OUT} = 200mA, V_{IN} = 2.7V, V_{COREx} = 1.235V		88		%
f_{OSC}	Oscillator frequency	PWM-mode	**3.45**	3.6	**3.75**	MHz
C_{OUT}	Output Filter Capacitance	0mA ≤ I_{OUT} ≤ 800mA	7	10	13	µF
	Output Capacitor ESR		0		20	mΩ
L	Output Filter Inductance	0mA ≤ I_{OUT} ≤ 800mA	0.7	1.0	1.3	µH
t_{SS}	Soft start ramp time			120		µs
$t_{START-UP}$	Start-Up Time from V_{COREx} enable to V_{OUT}	V_{COREx} = 1.235V, unloaded		200		µs

(1) All voltages are with respect to the potential at the GND pins.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.

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V_{O1} LDO1 Output Voltage Characteristics

Unless otherwise noted, V_{IN} = 3.6V, V_{OUT} = 1.2V (default). Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range, -40° to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1mA ≤ I_{OUT} ≤ 100mA, 2.7V ≤ V_{IN} ≤ 4.8V	**-2**		**2**	%
V_{OUT} Range	Programmable Output Voltage Range	0mA ≤ I_{OUT} ≤ 100mA 16 steps of 100mV	0.7	1.2 (default)	2.2	V
I_{OUT}	Output Current	2.7V ≤ V_{IN} ≤ 4.8V			**100**	mA
	Output Current Limit	V_{O1} = 0V (i.e., tied to Ground)			**400**	
I_Q	Quiescent Current (4)	I_{OUT} = 50mA		19		µA
ΔV_{OUT}	Line Regulation	2.7V ≤ V_{IN} ≤ 4.8V I_{OUT} = 50mA	-0.1		0.1	%/V
	Load Regulation	1mA ≤ I_{OUT} ≤ 100mA	-0.005		0.005	%/mA
	Line Transient Regulation	V_{IN} = 3.9V→3.6V→ 3.9V T_{RISE} = T_{FALL} = 10µS		10		mV
	Load Transient Regulation	V_{IN} = 3.6V I_{OUT} = 10mA→90mA→10mA T_{RISE} = T_{FALL} = 10µS		60		mV
e_N	Output Noise Voltage	10Hz ≤ f ≤ 100kHz C_{OUT} = 2.2µF		100		µVRMS
PSRR	Power Supply Ripple Rejection Ratio	f = 1kHz C_{OUT} = 2.2µF		50		dB
		f = 10kHz C_{OUT} = 2.2µF		40		
C_{OUT}	Output Capacitance	0mA ≤ I_{OUT} ≤ 100mA	1	2.2	20	µF
	Output Capacitor ESR		5		500	mΩ
$t_{START-UP}$	Start-Up Time from LDO1 enable	C_{OUT} = 2.2µF, I_{OUT} = 100mA		50		µs

(1) All voltages are with respect to the potential at the GND pins.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Quiescent currents for LDO1 through LDO5 do not include shared blocks such as the bandgap reference.

V_{O2} LDO2 (I/O Supply) Output Voltage Characteristics

Unless otherwise noted, V_{IN} = 3.6V, I_{OUT} = 125mA, V_{O2} = 3.3V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range, -40 to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1mA ≤ I_{OUT} ≤ 250mA, 3.6V ≤ V_{IN} ≦ 4.8V	**-2**		**2**	%
V_{OUT} Range	Programmable Output Voltage Range	1.5 through 2.3 in 100mV steps, 2.5, 2.8, 3.0V and 3.3V	1.5	3.3 (default)	3.3	V
I_{OUT}	Output Current	(V_{O2} + 0.4)V ≤ V_{IN} ≤ 4.8V			**250**	mA
	Output Current Limit	V_{O2} = 0V (i.e., tied to Ground)			**800**	
V_{IN} - V_{O2}	Dropout Voltage (4)	I_{OUT} = 125mA		70	**260**	mV
I_Q	Quiescent Current (5)	I_{OUT} = 125mA		19		µA

(1) All voltages are with respect to the potential at the GND pins.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. Other parameters are not guaranteed when the LDO is in dropout. This specification applies only when the output voltage is greater than 2.7V.
(5) Quiescent currents for LDO1 through LDO5 do not include shared blocks such as the bandgap reference.

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V_{O2} LDO2 (I/O Supply) Output Voltage Characteristics (continued)

Unless otherwise noted, V_{IN} = 3.6V, I_{OUT} = 125mA, V_{O2} = 3.3V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range, -40 to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_{OUT}	Line Regulation	$(V_{O2} + 0.4)V \le V_{IN} \le 4.8V$ I_{OUT} = 125mA	-0.1		0.1	%/V
	Load Regulation	V_{IN} = 3.6V $1mA \le I_{OUT} \le 250mA$	-0.005		+0.005	%/mA
	Line Transient Regulation (6)	V_{IN} = 4.0V→3.6V→4.0V V_{O2} = 3.3V $T_{RISE} = T_{FALL}$ = 10µS		10		mV
	Load Transient Regulation	V_{IN} = 3.6V I_{OUT} = 25mA→225mA→25mA $T_{RISE} = T_{FALL}$ = 1µS		125		mV
PSRR	Power Supply Ripple Rejection Ratio	f = 1kHz C_{OUT} = 4.7µF		55		dB
		f = 10kHz C_{OUT} = 4.7µF		40		
C_{OUT}	Output Capacitance	$0mA \le I_{OUT} \le 250mA$	2	4.7	20	µF
	Output Capacitor ESR		5		500	mΩ
$t_{START-UP}$	Start-Up Time from LDO2 enable	C_{OUT} = 4.7µF, I_{OUT} = 250mA		50		µs

(6) V_{IN} for line transient is above the default 3.6V to allow for 400mV of headroom from V_{IN} to V_{OUT}.

V_{O3}/V_{O4} LDO3 and LDO4 Output Voltage Characteristics

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the full operating junction temperature range, -40 to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Active/Independent, High I_Q	$I_{OUT} \le 50mA$, $2.7V \le V_{IN} \le 4.8V$ Low I_Q bit is cleared	**-2.5**		**2.5**	%
	Active/Independent, Low I_Q	$I_{OUT} \le 5mA$, $2.7V \le V_{IN} \le 4.8V$ Low I_Q bit is cleared	**-2.5**		**2.5**	
V_{OFFSET}	Active state offset from tracked V_{CORE} Offset = V_{O3} — V_{FB1} Offset = V_{O4} — V_{FB2}	$0mA \le I_{OUT} \le 50mA$, V_{FB} = 0.9V $2.7V \le V_{IN} \le 4.8V$	**0**	25	**70**	mV
V_{OUT} Range	Programmable Output Voltage Range	16 steps of 50mV	0.6	1.25(default)	1.35	V
I_Q	Quiescent Current (4)	Active state/Tracking mode I_{OUT} = 10µA Low I_Q bit is set		35		µA
		Sleep state or Active/Independent mode I_{OUT} = 10µA Low I_Q bit is set		10		

(1) All voltages are with respect to the potential at the GND pins.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Quiescent currents for LDO1 through LDO5 do not include shared blocks such as the bandgap reference.

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V_{O3}/V_{O4} LDO3 and LDO4 Output Voltage Characteristics (continued)

Unless otherwise noted, V_{IN} = 3.6V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the full operating junction temperature range, -40 to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	Output Current Low I_Q bit is cleared	2.7V ≤ V_{IN} ≤ 4.8V		50		mA
	Output Current Limit Active state/Tracking	2.7V ≤ V_{IN} ≤ 4.8V		50		
	Output Current Sleep state/Tracking, Low I_Q bit is set	2.7V ≤ V_{IN} ≤ 4.8V		5		
	Output Current, Independent, Low I_Q bit is set	2.7V ≤ V_{IN} ≤ 4.8V		5		
	Output Current Limit	V_{O2} = 0V (i.e., tied to Ground)			**420**	
PSRR	Power Supply Ripple Rejection Ratio	f = 1kHz C_{OUT} = 1.0µF		37		dB
C_{OUT}	Output Capacitance	0mA ≤ I_{OUT} ≤ 5mA	0.75	1	2.2	µF
	Output Capacitor ESR		5		500	mΩ
$t_{START-UP}$	Start-Up Time from LDOx enable	C_{OUT} = 1.0µF, I_{OUT} = 20mA		50		µs

V_{O5} LDO5 Output Voltage Characteristics

Unless otherwise noted, V_{IN} = 3.6V, I_{OUT} = 125mA, V_{O2} = 3.3V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the full operating junction temperature range, -40 to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT} Accuracy	Output Voltage	1mA ≤ I_{OUT} ≤ 250mA, V_{O2} = 3.3V 3.6V ≤ V_{IN} ≤ 4.8V	**-2**		**2**	%
V_{OUT} Range	Programmable Output Voltage Range	1.2 through 2.3 in 100mV steps, 2.5, 2.8, 3.0V, and 3.3V	1.2	3.3 (default)	3.3	V
I_{OUT}	Output Current	(V_{O5} + 0.4)V ≤ V_{IN} ≤ 4.8V			**250**	mA
	Output Current Limit	V_{O5} = 0V (i.e., tied to Ground)			**800**	
V_{IN} - V_{O5}	Dropout Voltage (4)	I_{OUT} = 125mA		70	**260**	mV
I_Q	Quiescent Current (5)	I_{OUT} = 125mA		19		µA
ΔV_{OUT}	Line Regulation	(V_{O5} + 0.4)V ≤ V_{IN} ≤ 4.8V I_{OUT} = 125mA	-0.1		0.1	%/V
	Load Regulation	V_{IN} = 3.6V 1mA ≤ I_{OUT} ≤ 250mA	-0.005		0.005	%/mA
	Line Transient Regulation (6)	V_{IN} = 4.0V→3.6V→4.0V V_{O5} = 3.3V T_{RISE} = T_{FALL} = 10µS		10		mV
	Load Transient Regulation	V_{IN} = 3.6V I_{OUT} = 25mA→225mA→25mA T_{RISE} = T_{FALL} = 1µS		125		
PSRR	Power Supply Ripple Rejection Ratio	f = 1kHz C_{OUT} = 4.7µF		55		dB
		f = 10kHz C_{OUT} = 4.7µF		40		

(1) All voltages are with respect to the potential at the GND pins.
(2) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Capacitors: Low-ESR Multi-Layer Ceramic Capacitors are (MLCCs) used in setting electrical characteristics.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. Other parameters are not guaranteed when the LDO is in dropout. This specification applies only when the output voltage is greater than 2.7V.
(5) Quiescent currents for LDO1 through LDO5 do not include shared blocks such as the bandgap reference.
(6) V_{IN} for line transient is above the default 3.6V to allow for 400mV of headroom from V_{IN} to V_{OUT}.

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V_{O5} LDO5 Output Voltage Characteristics (continued)

Unless otherwise noted, V_{IN} = 3.6V, I_{OUT} = 125mA, V_{O2} = 3.3V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the full operating junction temperature range, -40 to +125°C. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Output Capacitance	0mA ≤ I_{OUT} ≤250mA	2	4.7	20	µF
	Output Capacitor ESR		5		500	mΩ
$t_{START-UP}$	Start-Up Time from LDO5 enable	C_{OUT} = 4.7µF, I_{OUT} = 250mA		50		µs

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Typical Performance Characteristics - LP5552

Unless otherwise specified: V_{IN} = 3.6V, T_A = 25ºC, output voltages and external components are default values specified in electrical characteristics table.

Sleep I_Q Curves Over Temperature

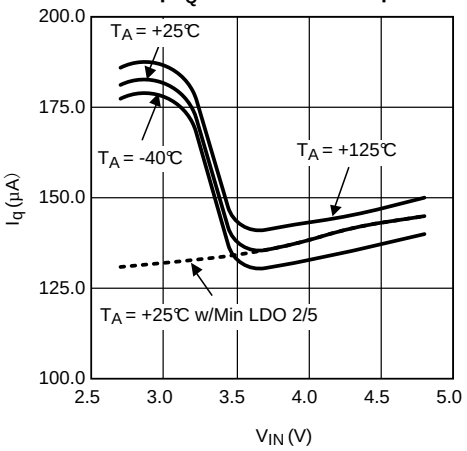

Figure 2.

Shutdown I_Q Curves Over Temperature

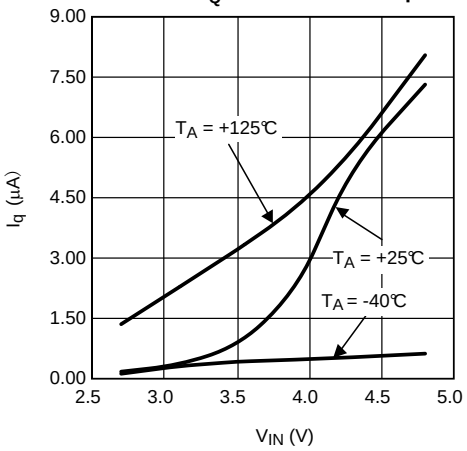

Figure 3.

LP5552 Startup Timing
All Outputs at No Load

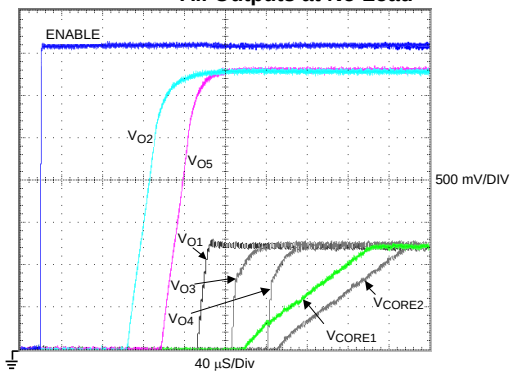

Figure 4.

V_{O3}/V_{O4} Line Transient Response

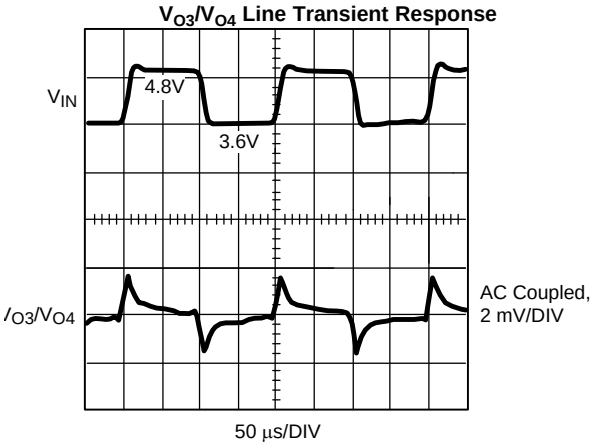

Figure 5.

Switcher Load Transient Response
20mA <--> 800mA / 3µS

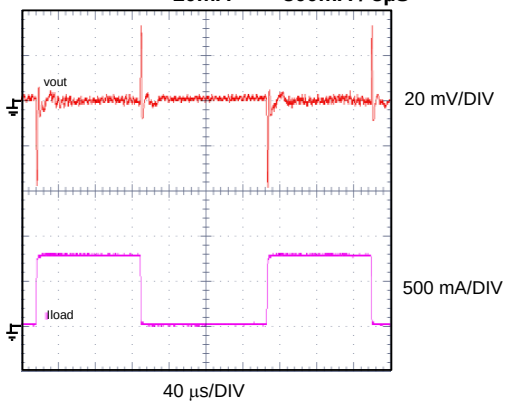

Figure 6.

Switcher Load Transient Response
20mA <--> 575mA / 2µS

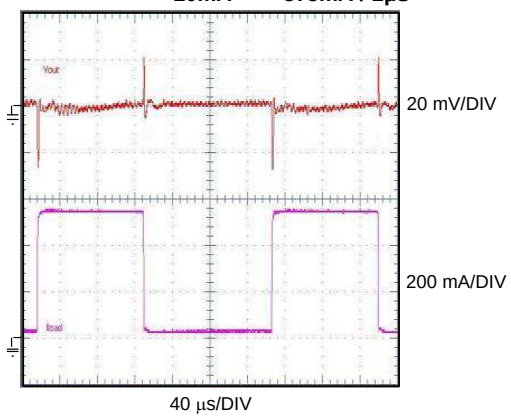

Figure 7.

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Typical Performance Characteristics - LP5552 (continued)

Unless otherwise specified: V_{IN} = 3.6V, T_A = 25ºC, output voltages and external components are default values specified in electrical characteristics table.

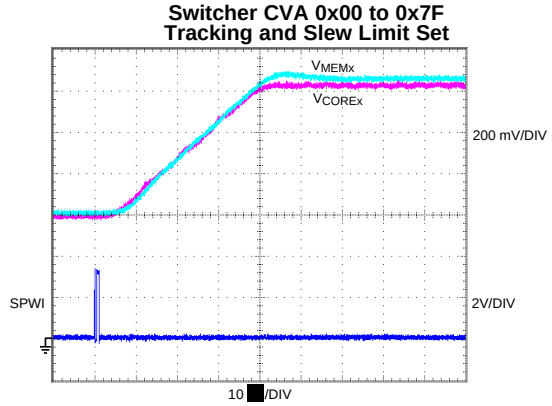

Figure 8.

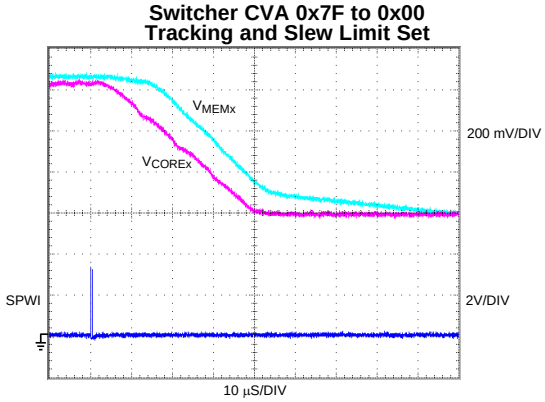

Figure 9.

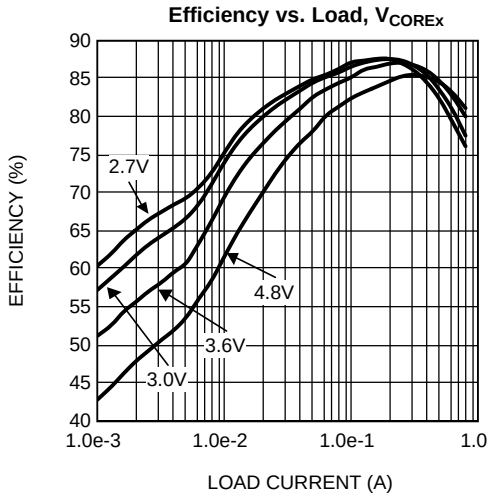

Figure 10.

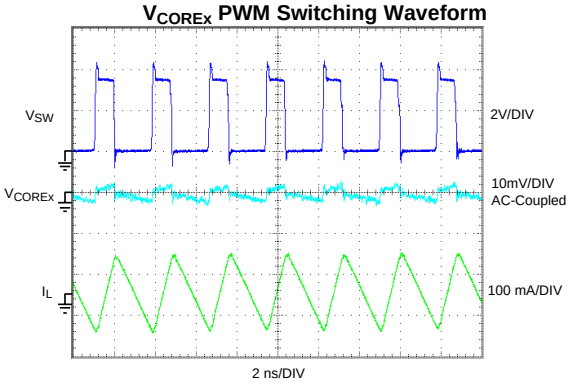

Figure 11.

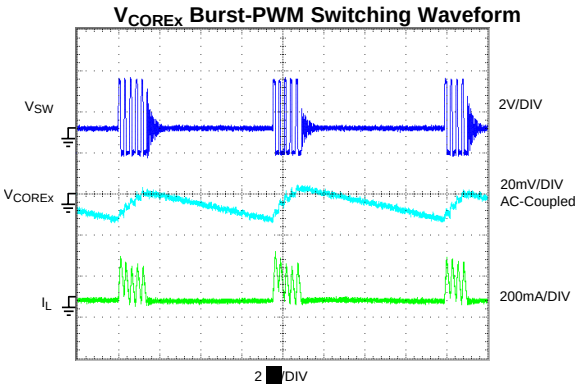

Figure 12.

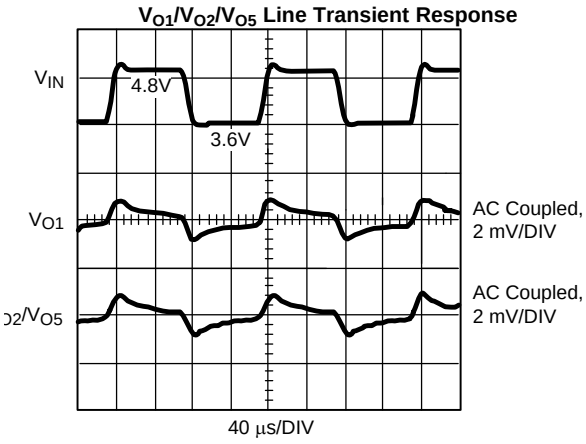

Figure 13.

Typical Performance Characteristics - LP5552 (continued)

Unless otherwise specified: V_{IN} = 3.6V, T_A = 25ºC, output voltages and external components are default values specified in electrical characteristics table.

V_{O2}/V_{O5} Load Transient Response

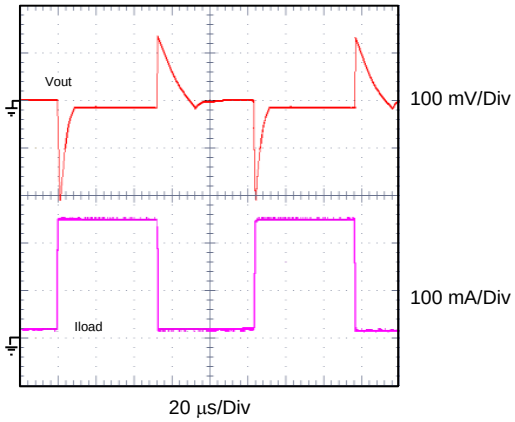

Figure 14.

V_{O1} Load Transient Response

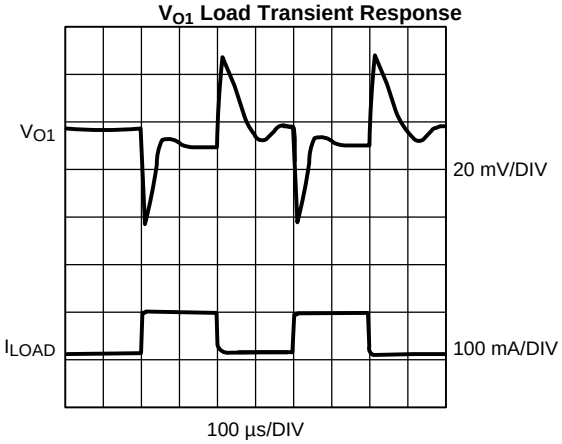

Figure 15.

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LP5552 PWI Register Map

The PWI 2.0 standard defines 32 8-bit base registers, and up to 256 8-bit extended registers, on each PWI slave. The table below summarizes these registers and shows default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of each individual register.

	Slave Address [N]									
	Base Registers									
Register Address	**Register Name**	**Register Usage**	**Type**	**Reset Default Value**						
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	R0	Core Voltage 1 Switcher #1	R/W	0 *	1	1	1	1	1	1	1
0x01	R1	Memory Voltage 1 Independent Mode	R/W	0 *	1	1	0	1	0 *	0 *	0 *
0x02	R2	LDO3 Memory Retention Voltage 1 Sleep State	R/W	0 *	1	1	0	1	0 *	0 *	0 *
0x03	R3	Status Register 1	R/O	0 *	0 *	0 *	0 *	1 *	1 *	1 *	1 *
0x04	R4	Device Capability Register 1	R/O	0	0	0	0	0	0	1	0
0x05	R5	Not Implemented	N/A	-	-	-	-	-	-	-	-
0x06	R6	Not Implemented	N/A	-	-	-	-	-	-	-	-
0x07	R7	LDO2 voltage (I/O voltage)	R/W	0 *	1	1	1	1	0 *	0 *	0 *
0x08	R8	LDO1 voltage	R/W	0 *	0	1	0	1	0 *	0 *	0 *
0x09	R9	LDO5 voltage	R/W	0 *	1	1	1	1	0 *	0 *	0 *
0x0A	R10	Enable Control 1	R/W	0 *	1 V_{CORE1} Enable	1 LDO3 Enable	1 LDO2 Enable	1 LDO1 Enable	1 LDO5 Enable	0*	0 Force PWM Switcher #1
0x0B	R11	Not Implemented	N/A	-	-	-	-	-	-	-	-
0x0C	R12	GPO Data Register	R/W	0 *	0 *	0 *	0 *	0 *	0 GP2	0 GP1	0 GP0
0x0D	R13	Miscellaneous Control 1	R/W	0*	0*	0*	0*	1 GPO Open Drain Select	0 SW1 Slew Control	0 LDO3 Track Select	0 LDO3 Low IQ Bit
0x0E-0x1E	R14-R30	Not Implemented	N/A	-	-	-	-	-	-	-	-
0x1F	R31	Reserved Do not write to	Res.	-	-	-	-	-	-	-	-
Extended Registers											
0x00-0xFF	ER0-ER255	Extended Register Space Not Implemented	N/A	-	-	-	-	-	-	-	-

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Slave Address [N+1]											
Base Registers											
Register Address	Register Name	Register Usage	Type	Reset Default Value(1)							
				7	6	5	4	3	2	1	0
0x00	R0	Core Voltage 2 Switcher #2	R/W	0 *	1	1	1	1	1	1	1
0x01	R1	Memory Voltage 2 Independent Mode	R/W	0 *	1	1	0	1	0 *	0 *	0*
0x02	R2	LDO4 Memory Retention Voltage 2 Sleep State	R/W	0 *	1	1	0	1	0 *	0 *	0 *
0x03	R3	Status Register 2	R/O	0 *	0 *	0 *	0 *	1 *	1 *	1 *	1 *
0x04	R4	Device Capability Register 2	R/O	0	0	0	0	0	0	1	0
0x05-0x09	R5-R9	Not Implemented	N/A	-	-	-	-	-	-	-	-
0x0A	R10	Enable Control 2	R/W	0*	1 V_{CORE2} Enable	1 LDO4 Enable	0*	0*	0*	0*	0 Force PWM Switcher #2
0x0B-0x0C	R11-R12	Not Implemented	N/A	-	-	-	-	-	-	-	-
0x0D	R13	Miscellaneous Control 2	R/W	0 *	0*	0*	0*	0*	0 SW2 Slew Control	0 LDO4 Track Select	0 LDO4 Low IQ Bit
0x0E-0x1F	R14-R31	Not Implemented	N/A	-	-	-	-	-	-	-	-
Extended Registers											
0x00-0xFF	ER0-ER255	Extended Register Space Not Implemented	N/A	-	-	-	-	-	-	-	-

(1) Note: A bit with an asterisk (*) denotes a register bit that is always read as a fixed value. Writes to these bits will be ignored. A bit with a hyphen (-) denotes a bit in an unimplemented register location. A write into unimplemented register(s) will be ignored. A read of an unimplemented register(s) will produce a “No response frame”. Please refer to PWI specification version 2.0 for further information.

Slave Address [N] - 1st Slave Device R0 - V_{CORE1} - Core Voltage 1

Address	0x00
Slave Address	N
Type	R/W
Reset Default	8h'7F

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:0	Voltage	Programmed voltage value. Default value is in **bold.**	
		Voltage Data Code [6:0]	Voltage Value (V)
		7h'00	0.60
		7h'xx	Linear scaling
		7h'7F	**1.235 (default)**

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R1 - V_{O3} - LDO3 Memory Voltage 1 - Independent Mode

Address	0x01
Slave Address	N
Type	R/W
Reset Default	8h'68

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.60
		4h'1	0.65
		4h'2	0.70
		4h'3	0.75
		4h'4	0.80
		4h'5	0.85
		4h'6	0.90
		4h'7	0.95
		4h'8	1.00
		4h'9	1.05
		4h'A	1.10
		4h'B	1.15
		4h'C	1.20
		4h'D	**1.25 (default)**
		4h'E	1.30
		4h'F	1.35
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

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R2 - V_{O3} - LDO3 Memory Retention Voltage 1 - Sleep State Value

Address	0x02
Slave Address	N
Type	R/W
Reset Default	8h'68

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.6
		4h'1	0.65
		4h'2	0.70
		4h'3	0.75
		4h'4	0.80
		4h'5	0.85
		4h'6	0.90
		4h'7	0.95
		4h'8	1.00
		4h'9	1.05
		4h'A	1.10
		4h'B	1.15
		4h'C	1.20
		4h'D	**1.25 (default)**
		4h'E	1.30
		4h'F	1.35
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

R3 - Status Register 1

Address	0x03
Slave Address	N
Type	Read Only
Reset Default	8h'0F

Bit	Field Name	Description or Comment
7:4	Unused	Unused, read returns 0.
3:0	Unused	Unused, read returns 1.

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R4 - Device Capability Register 1

Address	0x04
Slave Address	N
Type	Read Only
Reset Default	8h'02

Bit	Field Name	Description or Comment
7:3	Optional Function Support	Extended Register Read and Write are not supported by LP5552, read returns '0'.
3:0	Version	Read transaction will return 0x2 indicating PWI 2.0 specification. Write transactions to this register are ignored.

R7 - V_{O2} - LDO2 Voltage

Address	0x07
Slave Address	N
Type	R/W
Reset Default	8h'78

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	1.5
		4h'1	1.5
		4h'2	1.5
		4h'3	1.5
		4h'4	1.6
		4h'5	1.7
		4h'6	1.8
		4h'7	1.9
		4h'8	2.0
		4h'9	2.1
		4h'A	2.2
		4h'B	2.3
		4h'C	2.5
		4h'D	2.8
		4h'E	3.0
		4h'F	**3.3 (default)**
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

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R8 - V_{O1} - LDO1 Voltage

Address	0x08
Slave Address	N
Type	R/W
Reset Default	8h'28

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.7
		4h'1	0.8
		4h'2	0.9
		4h'3	1.0
		4h'4	1.1
		4h'5	**1.2 (default)**
		4h'6	1.3
		4h'7	1.4
		4h'8	1.5
		4h'9	1.6
		4h'A	1.7
		4h'B	1.8
		4h'C	1.9
		4h'D	2.0
		4h'E	2.1
		4h'F	2.2
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

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R9 - V_{O5} - LDO5 Voltage

Address	0x09
Slave Address	N
Type	R/W
Reset Default	8h'78

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	1.2
		4h'1	1.3
		4h'2	1.4
		4h'3	1.5
		4h'4	1.6
		4h'5	1.7
		4h'6	1.8
		4h'7	1.9
		4h'8	2.0
		4h'9	2.1
		4h'A	2.2
		4h'B	2.3
		4h'C	2.5
		4h'D	2.8
		4h'E	3.0
		4h'F	**3.3 (default)**
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

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R10 - Enable Control Register 1

Address	0x0A
Slave Address	N
Type	R/W
Reset Default	8h'7C

Bit	Field Name	Description or Comment
7	Unused	This bit is fixed to ‘0’. Reading this bit will result in a ‘0’. Any data written into this bit position using the Register Write command is ignored.
6	R0, Core Voltage 1 Enable	1 : regulator is enabled (default) 0 : regulator is disabled
5	R2, LDO3 Voltage Enable	1 : regulator is enabled (default) 0 : regulator is disabled
4	R7, LDO2 Voltage Enable	1 : regulator is enabled (default) 0 : regulator is disabled
3	R8, LDO1 Voltage Enable	1 : regulator is enabled (default) 0 : regulator is disabled
2	R9, LDO5 Voltage Enable	1 : regulator is enabled (default) 0 : regulator is disabled
1	Unused	This bit is fixed to ‘0’. Reading this bit will result in a ‘0’. Any data written into this bit position using the Register Write command is ignored.
0	Forced PWM Mode — Switcher #1	0 : Intelligent and Automatic PWM/Burst-PWM Transition - Most Energy Efficient (default) 1 : Forced PWM - No Burst Mode Allowed - Smallest Voltage Ripple

R12 - GPO Data Register

Address	0x0C
Slave Address	N
Type	R/W
Reset Default	8h'00

Bit	Field Name	Description or Comment
7:3	Unused	These bits are fixed to ‘0’. Reading these bits will result in a ‘00000’. Any data written into these bits using the Register Write command is ignored.
2	GPO2	General purpose output - digital. This bit is drives the GP2 pin
1	GPO1	General purpose output - digital. This bit is drives the G1 pin
0	GPO0	General purpose output - digital. This bit is drives the GP0 pin

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R13 - Misc Control Register 1

Address	0x0D
Slave Address	N
Type	R/W
Reset Default	8h'08

Bit	Field Name	Description or Comment
7:4	Unused	These bits are fixed to '0'. Reading these bits will result in a '0000'. Any data written into these bits using the Register Write command is ignored.
3	GPO Open Drain Select	'0': GPOs will behave as push-pull CMOS outputs referenced to VO2 '1': GPOs will act as open-drain outputs (default)
2	SW1 Slew Control	'0': No slew rate restriction on VCORE1 switcher output voltage (default) '1': Slew rate of VCORE1 switcher output voltage is reduced
1	LDO3 Tracking Select	'0': LDO3 at R1 register value in Active mode. LDO3 does not track VCORE1 (default) '1': LDO3 tracks VCORE1 with offset
0	LDO3 Low I_Q Bit	'0': Selects the higher bias point for LDO3 which results in 50mA operation (default) '1': Selects the lower bias point for LDO3 which results in 5mA operation See Table 3 for a more detailed explanation of this bit

R31 - Reserved

Address	0x1F
Slave Address	N
Type	Reserved
Reset Default	8h'00

Bit	Field Name	Description or Comment
7:0	Reserved	This register is reserved. The user should avoid accessing this register to prevent undefined behavior of the LP5552.

Slave Address [N+1] - 2nd Slave Device - R0 - V_{CORE2} - Core Voltage 2

Address	0x00
Slave Address	N + 1
Type	R/W
Reset Default	8h'7F

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:0	Voltage	Programmed voltage value. Default value is in **bold.**	
		Voltage Data Code [6:0]	Voltage Value (V)
		7h'00	0.60
		7h'xx	Linear scaling
		7h'7F	**1.235 (default)**

R1 - V_{O4} - LDO4 Memory Voltage 2 - Independent Mode

Address	0x01
Slave Address	N + 1
Type	R/W
Reset Default	8h'68

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6:3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.60
		4h'1	0.65
		4h'2	0.70
		4h'3	0.75
		4h'4	0.80
		4h'5	0.85
		4h'6	0.90
		4h'7	0.95
		4h'8	1.00
		4h'9	1.05
		4h'A	1.10
		4h'B	1.15
		4h'C	1.20
		4h'D	**1.25 (default)**
		4h'E	1.30
		4h'F	1.35
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

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R2 - V_{O4} - LDO4 Memory Retention Voltage 2 - Sleep State Value

Address	0x02
Slave Address	N + 1
Type	R/W
Reset Default	8h'68

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to '0'. Reading this bit will result in a '0'. Any data written into this bit position using the Register Write command is ignored.	
6.3	Voltage	Programmed voltage value. A code of all ones indicates maximum voltage while a code of all zero indicates minimum voltage. Default value is in **bold.**	
		Voltage Data Code [6:3]	Voltage Value (volts)
		4h'0	0.6
		4h'1	0.65
		4h'2	0.70
		4h'3	0.75
		4h'4	0.80
		4h'5	0.85
		4h'6	0.90
		4h'7	0.95
		4h'8	1.00
		4h'9	1.05
		4h'A	1.10
		4h'B	1.15
		4h'C	1.20
		4h'D	**1.25 (default)**
		4h'E	1.30
		4h'F	1.35
2:0	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.	

R3 - Status Register 2

Address	0x03
Slave Address	N + 1
Type	Read Only
Reset Default	8h'0F

Bit	Field Name	Description or Comment
7:4	Unused	Unused, read returns 0.
3:0	Unused	Unused, read returns 1.

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R4 - Device Capability Register 2

Address	0x04
Slave Address	N + 1
Type	Read Only
Reset Default	8h'02

Bit	Field Name	Description or Comment
7:3	Optional Function Support	Extended Register Read and Write are not supported by LP5552, read returns '0'.
2:0	Version	Read transaction will return 0x2 indicating PWI 2.0 specification. Write transactions to this register are ignored.

R10 - Enable Control Register 2

Address	0x0A
Slave Address	N + 1
Type	R/W
Reset Default	8h'60

Bit	Field Name	Description or Comment
7	Unused	This bit is fixed to ‘0’. Reading this bit will result in a ‘0’. Any data written into this bit position using the Register Write command is ignored.
6	R0, Core Voltage 2 Enable	1 : regulator is enabled (default) 0 : regulator is disabled
5	R2, LDO4 Voltage Enable	1 : regulator is enabled (default) 0 : regulator is disabled
4:1	Unused	These bits are fixed to '0'. Reading these bits will result in a '000'. Any data written into these bits using the Register Write command is ignored.
0	Forced PWM Mode - Switcher #2	0 : Intelligent and Automatic PWM/Burst-PWM Transition - Most Energy Efficient (default) 1 : Forced PWM - No Burst Mode Allowed - Smallest Voltage Ripple

R13 - Misc Control Register 2

Address	0x0D
Slave Address	N + 1
Type	R/W
Reset Default	8h'00

Bit	Field Name	Description or Comment
7:3	Unused	These bits are fixed to ‘0’. Reading these bits will result in a ‘00000’. Any data written into these bits using the Register Write command is ignored.
2	SW2 Slew Control	'0': No slew rate restriction on VCORE1 switcher output voltage (default) '1': Slew rate of VCORE1 switcher output voltage is reduced
1	LDO4 Tracking Select	'0': LDO4 at R1 register value in Active mode. LDO4 does not track V_{CORE2} (default) '1': LDO4 tracks V_{CORE2} with offset
0	LDO4 Low I_Q Bit	'0': Selects the higher bias point for LDO4 which results in 50mA operation (default) '1': Selects the lower bias point for LDO4 which results in 5mA operation See Table 3 for a more detailed explanation of this bit

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LP5552 Operation

GENERAL DESCRIPTION

The LP5552 is a PowerWise Interface (PWI) 2.0 compliant energy management unit (EMU) for application or baseband processors in mobile phones and other portable equipment. It operates cooperatively with processors using National Semiconductor's Advanced Power Controller (APC) to provide Adaptive Voltage Scaling (AVS) which drastically improves efficiencies compared to conventional power delivery methods. The LP5552 consists of two high-efficiency switching DC/DC buck converters to supply two voltage scaling domains, and five LDOs for supplying additional support circuitry.

VOLTAGE SCALING

The LP5552 is designed to be used in a voltage scaling system to lower the power dissipation of the system. By scaling supply voltage with the clock frequency of a processor, dramatic power savings can be achieved. Two types of voltage scaling are supported, dynamic voltage scaling (DVS) and adaptive voltage scaling (AVS). Both Switcher 1 and Switcher 2 support AVS and DVS modes. DVS systems switch between pre-characterized voltages, which are paired to clock frequencies used for frequency scaling in the processor. AVS systems track the processor performance and optimize the supply voltage to the required performance. AVS is a closed loop system that provides process and temperature compensation such that for any given processor, temperature, or clock frequency, the minimum supply voltage is delivered.

POWERWISE INTERFACE

What follows is only a brief description of the parts of the PWI 2.0 spec that are relevant to the LP5552. Please see the PWI 2.0 spec for a complete description.

To support DVS and AVS, the LP5552 is programmable via the low-power, 2-wire PowerWise Interface (PWI). This serial interface controls the various voltages and states of all the regulators in the LP5552.

Both slaves in the LP5552 support the full PWI command set, other than the optional Extended Register Read and Write, as described in the PWI 2.0 specification:

- Core Voltage Adjust
- Reset
- Sleep
- Shutdown
- Wakeup
- Register Read
- Register Write
- Authenticate

The 2-wire PWI interface is composed of the SCLK and SPWI pins on the LP5552. SCLK is always an input to the LP5552 and should be driven by a PowerWise master in the system. The SCLK clock rate can operate from 32kHz – 15MHz. SPWI is the bi-directional serial data line. It can drive a 50pF line and meet timing standards for a 15MHz PWI bus. Both signals are referenced to the voltage present at V_{O2}, the LDO2 output voltage. Both signals contain an internal pull-down resistor of ~1MΩ, in accordance with the PWI 2.0 specification.

SLAVE ADDRESSING DESCRIPTION

PWI 2.0 supports up to 16 logical slaves in the same system. Four slave address bits are included at the start of every PWI communications frame to identify which slave is being targeted by the PWI master. The LP5552 contains 2 logical slaves in its package. The 3 MSBs of the LP5552's slave address are set by the SA1, SA2, and SA3 pins. They are actively decoded by the LP5552 on every transaction. The LSB of the slave address is hard-wired inside the LP5552. Slave 'N' will always be located at SA[0] = 0, and slave 'N+1' will always exist at SA[0] = 1. As an example, if we were to tie SA1 = SA3 = VDD and SA2 = GND in our system, then the LP5552's slave 'N' would be located at SA[3:0] = 0xA and slave 'N+1' would be SA[3:0] = 0xB.

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CONTROL AND STATUS SIGNALS

The LP5552 implements all 3 of the PWI 2.0 control and status signals. ENABLE and RESETN are inputs to the LP5552 that allow for power-up and power-down sequencing, as well as resetting the EMU to a known state. Both ENABLE and RESETN must be a logic '1' during normal operation. PWROK is an indicator to the system that the LP5552 is in regulation and power is stable. Its output is dependent upon the state of the two slave devices. See Table 1, "PWROK Value Per Slave State," below for details. All 3 signals are asynchronous signals.

Table 1. PWROK Value Per Slave State

		SLAVE (N+1)			
		STARTUP	**ACTIVE**	**SLEEP**	**SHUTDOWN**
SLAVE (N)	STARTUP	0	1	1	0
	ACTIVE	1	1	1	1
	SLEEP	1	1	1	1
	SHUTDOWN	0	1	1	0

General Purpose Outputs

The LP5552 contains 3 digital output pins that can be used as the system designer sees fit. By default, they are configured as open-drain outputs, outputting a logic '0'. They can be changed to a push-pull CMOS output by clearing Slave 'N', R13[3]. In the open-drain configuration, they can be referenced to any voltage less than the VDD of the LP5552. The push-pull output mode will reference the high-side to the voltage of LDO2.

SLAVE OPERATING STATES

Each slave in the LP5552 has four operating states: Startup, Active, Sleep, and Shutdown. (Figure 16.)

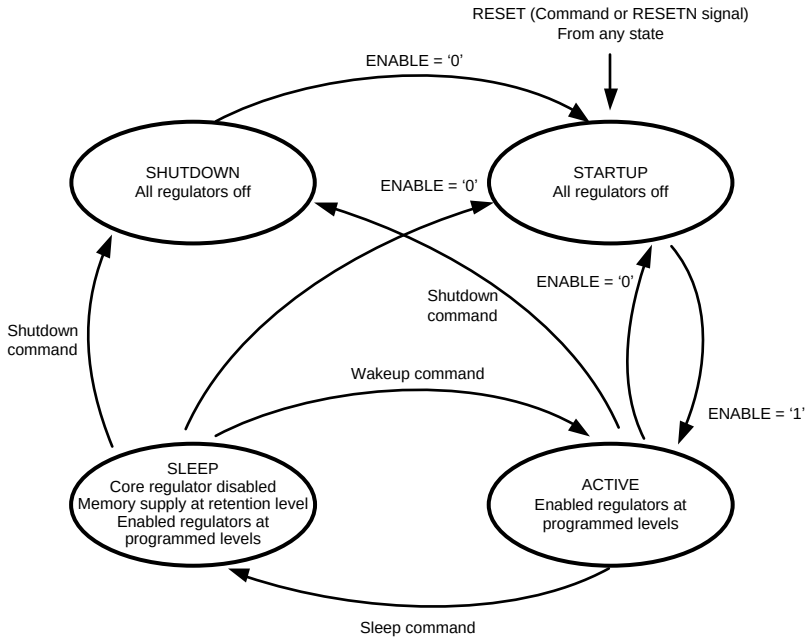

Figure 16. LP5552 Slave State Diagram

The Startup state is the default state for both slaves after reset. All regulators are off and PWROK output is a '0'.

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The device will move to the Active state when the external ENABLE and RESETN signals are both pulled high. After the state transition completes, both slaves will be in the Active state, but each slave will maintain its own independent state thereafter.

The default, factory-programmed power-up sequence of the LP5552 can be seen in Figure 17. From the global ENABLE of the chip, there is ~80uS of time for powering on and stabilizing internal support circuitry. Once this time has expired, the start-up time slots begin. Table 2 shows the time slots that each regulator begins in. Note that for the switchers, there is an additional ~75uS of set-up time from the beginning of the time slot until the soft-start ramp begins.

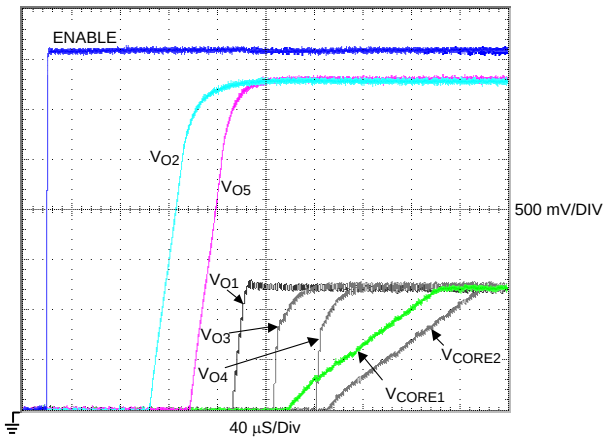

Figure 17. LP5552 Startup Timing

Table 2. Factory Programmed Startup Time Slots

Time slot	Start time (µS)	Regulator(s)
0	0	LDO2
1	32	LDO5/AVS1
2	64	LDO1/AVS2
3	96	LDO3
4	128	LDO4

In the Active state, all regulators that are enabled are on, and their outputs are defined by their programmed register values. If the Active state has been reached from the Startup state, the regulators will be programmed to their default value. In the Active state, the PWI master has complete control over the LP5552's operation. The PWROK output is '1' if either slave is in this state.

The Sleep state is entered by issuing the Sleep command on the PWI bus. The core regulator of the addressed slave, and the associated memory LDO will both respond to the Sleep command. For the first 32uS after the command is decoded, the core regulator will transition to its zero-code value of 0.6V, and the LDO will move to its POR value of 1.25V. After the 32uS has expired, the core regulator will be turned off and the LDO will transition to its memory retention value as programmed in register R2. See Figure 18. LDO1, LDO2, and LDO5 are unaffected by the Sleep command and will maintain their programmed values. They may be turned off manually, if desired. The LP5552 will still respond to all PWI traffic as long as LDO2 remains active.

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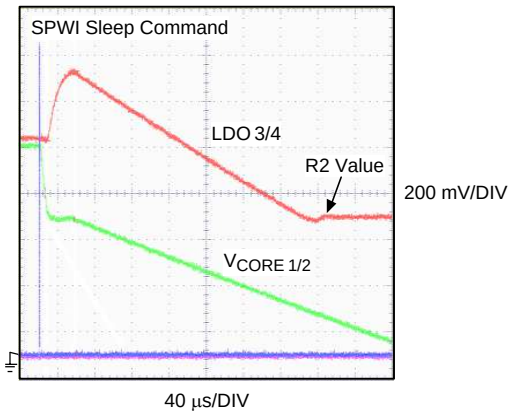

Figure 18. Sleep Behavior of Core and Memory

A slave may return to the Active state by issuing the Wakeup command. This will result in the core regulator turning on after a ~75uS delay and a soft-start ramp. It will wake up at its maximum value of 1.235V. The associated memory LDO will go to its default POR value of 1.25V until the core has reached the end of its soft-start period and then will transition to its programmed configuration (i.e., either tracking the core or to the value programmed in R1). See Figure 19. The PWROK output is '1' if either slave is in this state.

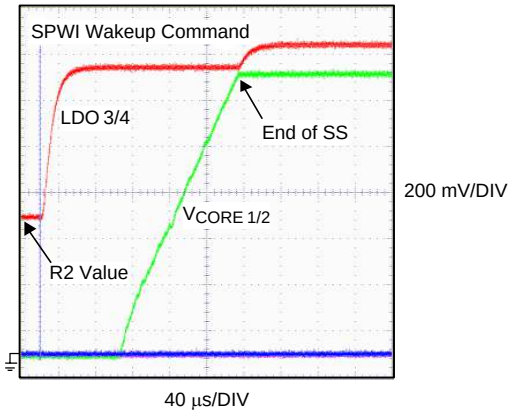

Figure 19. Wakeup Behavior of Core and Memory

The Shutdown command will place the addressed slave in the Shutdown state. This command may be issued to any slave in either the Active or Sleep states. All regulators within that state will turn off. The LP5552 holds out one exception to this rule. LDO1, LDO2, and LDO5 act as a shared resource between the two slave devices in the EMU. Therefore, placing just slave 'N' into Shutdown will not turn off these regulators even though their registers exist within that space. Slave 'N' can be in the Shutdown state, but as long as Slave 'N+1' is still in either Active or Sleep states, these shared LDOs will remain on, and PWI traffic will be decoded. Once the Shutdown command has been sent to both slaves, all regulators on the LP5552 will be turned off. The PWROK signal will be '0' if both slaves are in the Shutdown state. The only way to transition away from the Shutdown state is by disabling or resetting the LP5552. By taking the ENABLE pin or the RESETN pin low, the LP5552 will transition to the Startup state.

Power-down sequencing is not actively managed by the LP5552 logic, but can be handled by turning off regulators in the desired order within the application, prior to Shutdown.

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PWM/BURST-PWM OPERATION

The switching regulators in the LP5552 have two modes of operation, pulse width modulation (PWM) and "Burst"-PWM. In PWM, the converter switches at 3.6MHz. Each period can be split into two cycles. During the first cycle, the high-side switch is on and the low-side switch is off. During this cycle, the inductor current is rising. In the second cycle, the high-side switch is off and the low-side switch is on causing the inductor current to decrease. The output ripple voltage is lowest in PWM mode. As the load current decreases, the converter efficiency becomes worse due to switching losses. The LP5552 will automatically transition to Burst mode at light load current levels. The exact transition point is dependent upon the present operating environment, and the mode assessment is constantly evaluated. The transition is approximately equal to:

$$I_{PWM/Burst\text{-}PWM} \approx \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{2 \times L \times f_S} \quad (1)$$

In this mode, the output voltage will be allowed to coast with no switching action by the regulator. When the output voltage dips to 1% below nominal, the switches are enabled, the voltage is boosted back up to the programmed value, and the coast process repeats itself. If the user desires tighter control of the output voltage, at the expense of light-load efficiency, the switchers can be commanded to stay in PWM-only mode by setting bit 0 of R10 in the slave's registers.

CURRENT LIMITING

A current limit feature exists for all regulators to help protect the LP5552 and external components during overload conditions. The switcher's current limit feature will trip around 1.2A (typ). Once the fault has occurred and current limit has been entered, the switcher will not resume operation until the output current has decreased to a hysteretic low-level set point. Normal operation will proceed after the fault has been cleared. Likewise, the LDOs all implement current limit and will turn off their pass element when their trip point is reached. Please refer to the Electrical Characteristics section for details.

SOFT START

Both switching regulators implement a digital soft-start feature to limit in-rush current during the Startup to Active state transition. The voltage output of the switchers will be gradually increased to the default value of 1.235V. An unloaded switcher output will reach its final value in 120µS (typ.) while a fully loaded switcher – 800mA -- will reach its output in 135µS (typ). Because the LP5552 uses voltage increments to handle soft-start, its turn-on time is less dependent on output capacitance and load current than regulators that gradually increase current limit to implement soft-start.

LDO2

The on-board LDO2 regulator has special significance to the LP5552. All digital data on the SCLK, SPWI, and the GPOx pins while in push-pull mode, is referenced to this voltage. This regulator is used internally to power the I/O drivers. As such, this regulator must be on in order to communicate with the LP5552. The user should ensure that this regulator does not go into dropout or PWI communication will most likely not be possible. If it is not desirable to use this regulator in the system, the user can turn this regulator off by setting bit 4 of R10 in Slave 'N' during system initialization while back-driving the required I/O voltage onto the pin.

TRACKING, SLEW RATE LIMITING, AND LOW I_Q BITS

There are 3 bits in each slave's R13 register that determine the performance and operational behavior of the V_{COREx} and V_{O3}/V_{O4} outputs. Their significance and interaction is described below.

The Low I_Q bit setting in R13, bit 0, of each slave allows the selection of a lower I_Q bias point at the expense of decreased output current capability for V_{O3} and V_{O4}. At reset, the default setting is high I_Q mode (i.e., bit 0 is cleared) which results in a 50mA output capability for the associated LDO. If bit 0 is set, the quiescent current draw of the part will decrease, but the output current capability of the associated LDO will drop to 5mA. Setting V_{O3} and V_O4 up for low I_Q mode is useful in situations where just a trickle of current is required, such as when maintaining some type of low-power memory.

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The Tracking bit, bit 1 in R13, determines whether or not the LDO3 voltage will track the V_{CORE1} voltage in Slave 'N'. Slave 'N+1' has its own tracking bit which will determine whether LDO4 tracks V_{CORE2}. Each slave device can be independently configured to tracking or independent mode. When set to operate independently, LDO3 and LDO4 will maintain a voltage output equal to the programmed value of R1 while in the Active state. When set to operate in tracking mode, LDO3 and LDO4 will track the output voltage of their associated switcher, attempting to maintain approximately a 25mV positive offset.

There is some interaction between the Low I_Q and Tracking bits based on the state of the slave device, and that is detailed in the following table:

Table 3. Tracking, IQ Bit, Slave State Truth Table

Input			Output
Tracking, R13[1]	**Low I_Q, R13[0]**	**State**	**LDO3/LDO4 Capability**
0	0	Active	50mA
0	0	Sleep	50mA
0	1	Active	5mA
0	1	Sleep	5mA
1	0	Active	50mA
1	0	Sleep	50mA
1	1	Active	50mA
1	1	Sleep	5mA

The final bit, the Slew Rate Limiting bit (R13[2]), places a limit on how fast the output voltage of the V_{COREx} regulators can change. If slew rate limiting is not enabled while in tracking mode (i.e., R13[2] is cleared), then the switcher will achieve its new programmed value faster than the tracking LDO can change its output. By setting the Slew Rate Limiting bit, the LP5552 will attempt to keep the positive offset of the tracking LDO in relation to the V_{COREx} output.

For AVS systems, the expected configuration is to have all 3 bits, R13[2:0] set to '1'. It generally will not make sense to set the Slew Rate Limiting bit while not in tracking mode. Setting all 3 bits will result in a system which has the following properties:

1. The tracking LDO will maintain positive offset from V_{COREx} in Active state.
2. Tracking LDO will be 50mA output capable in Active state, and 5mA capable in Sleep state.

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Application Hints

SWITCHERS

Input Capacitors

The input capacitor to a switching regulator supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle this current:

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \text{ (A)} \quad (2)$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = I^2_{RMS\_CIN} \times R_{ESR\_CIN} \text{ (W)} \quad (3)$$

The input capacitor must be rated to handle both the RMS current and the dissipated power. A 10µF ceramic capacitor, rated to handle at least 10V, is recommended for each PVDDx/PGNDx pair.

Inductor

A 1µH inductor should be used for the switchers' output filter. The inductor should be rated to handle the peak load current plus the ripple current:

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta i_{L(MAX)}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN(MAX)} - V_{OUT})}{2 \times L \times f_S}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN(MAX)} - V_{OUT})}{7.2} \text{ (A)}, \quad \begin{cases} f_S = 3.6 \text{ MHz} \\ L = 1.0\ \mu\text{H} \end{cases} \quad (4)$$

Table 4. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	DCR (Typical)
LPS3010–102	Coilcraft	3.0 x 3.0 x 1.0	85mΩ
LQM31PN1R0MC0	muRata	3.2 x 1.6 x 0.5	140mΩ

Output Capacitors

The switchers in the LP5552 are designed to be used with 10µF of capacitance in the output filter. It is recommended that a 10µF ceramic capacitor, rated to handle at least 10V, and comprised of X5R dielectric material, be chosen. The output capacitor of a switching regulator absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converters is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor or the PCB interconnect, depending upon the frequency of the ripple current. Ceramic capacitors are predominantly used in portable systems and have very low ESR and should remain capacitive given good PCB layout practices. The switcher peak-to-peak output voltage ripple in steady state can be calculated as:

$$V_{PP} = I_{LPP} \left(R_{ESR} + \frac{1}{F_S \times 8 \times C_{OUT}}\right) \quad (5)$$

Table 5. Suggested Switcher Output Capacitors and Their Suppliers

Model	Vendor	Value	Type	Voltage	Case Size (Height)
GRM219R61A106KE44	muRata	10µF	Ceramic, X5R	10V	0805 (0.85mm)
LMK212BJ106KD	Taiyo Yuden	10µF	Ceramic, X5R	10V	0805 (0.85mm)

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A NOTE ABOUT CAPACITORS

Capacitors are typically specified by their manufacturers as a particular value +/-X%. These specified values are only valid for a particular test condition that is often not applicable to the final application circuit. If you were to take a ceramic 10µF capacitor in 0805 package and measure it with an LCR meter, a typical result would be around 7µF. This is before you even insert the capacitor into the application circuit. Capacitance will decrease with increasing frequency and DC bias point, and will generally vary with temperature. A typical 6.3V, 10µF, 0603 capacitor may only be providing 4 - 5µF of capacitance when used as the output capacitor in the switching regulators' loop filter. It is highly recommended that measurements be done on your selected capacitor(s) to ensure you have the proper amount of capacitance.

LDOs

Input Capacitors

While not mandatory, it is highly recommended that some input capacitance be provided for the DVDDx and AVDDx pins. Typical values may be in the 0.1 - 1.0µF range. These capacitors will provide bypass for the LP5552 control electronics and LDOs.

Output Capacitors

The output capacitor of an LDO sets a low frequency pole and a high frequency zero in the control loop of an LDO, as well as providing the initial response for a load transient. The capacitance and the equivalent series resistance (ESR) of the capacitor must be within a specified range to meet stability requirements. The LDOs in the LP5552 are designed to be used with ceramic output capacitors. The following table can be used to select suitable output capacitors:

Table 6. LDO Output Capacitor Selection Guide

	Output Capacitance Range (Recommended Typical Value)	ESR Range
LDO1	1.0µF — 20µF (2.2µF)	5mΩ - 500mΩ
LDO2	2.0µF — 20µF (4.7µF)	5mΩ - 500mΩ
LDO3	0.7µF — 2.2µF (1.0µF)	5mΩ - 500mΩ
LDO4	0.7µF — 2.2µF (1.0µF)	5mΩ - 500mΩ
LDO5	2.0µF — 20µF (4.7µF)	5mΩ - 500mΩ

Dropout Voltages

All linear regulators are subject to dropout. Dropout Voltage is the minimum voltage required across the regulator (V_{IN} - V_{OUT}) to maintain a constant, specified output voltage. The LP5552 has a V_{IN} range of 2.7V – 4.8V. V_{O1}, V_{O3}, and V_{O4} cannot be programmed to a level that would make dropout a factor. However, V_{O2} and V_{O5} can reach as high as 3.3V on their outputs. Both of those regulators have a dropout voltage of 260mV (MAX). To ensure proper operation of those regulators, the user should ensure that $V_{IN} \geq (V_{Ox\text{-}PROGRAMMED} + 260mV)$. If a regulator does go into dropout, the output voltage will start to track the input: $V_O = V_{IN} - V_{DROPOUT}$. Also, the PSRR will go to zero, meaning any noise on the input will be seen at the output.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. It is highly recommended that the user consult Application Note AN-1610 for detailed guidelines and best methods for PCB layout of the LP5552. It is also recommended that the user reference AN-1112 for information on the DSBGA package and its requirements.

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REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	34

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5552TL/NOPB	ACTIVE	DSBGA	YZR	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SLKB	Samples
LP5552TLX/NOPB	ACTIVE	DSBGA	YZR	36	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SLKB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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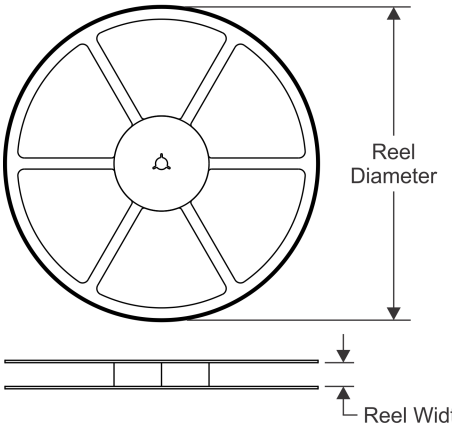
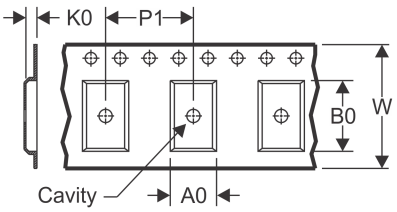
TAPE AND REEL INFORMATION

REEL DIMENSIONS

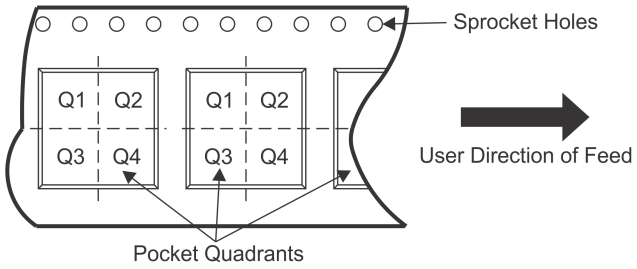


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

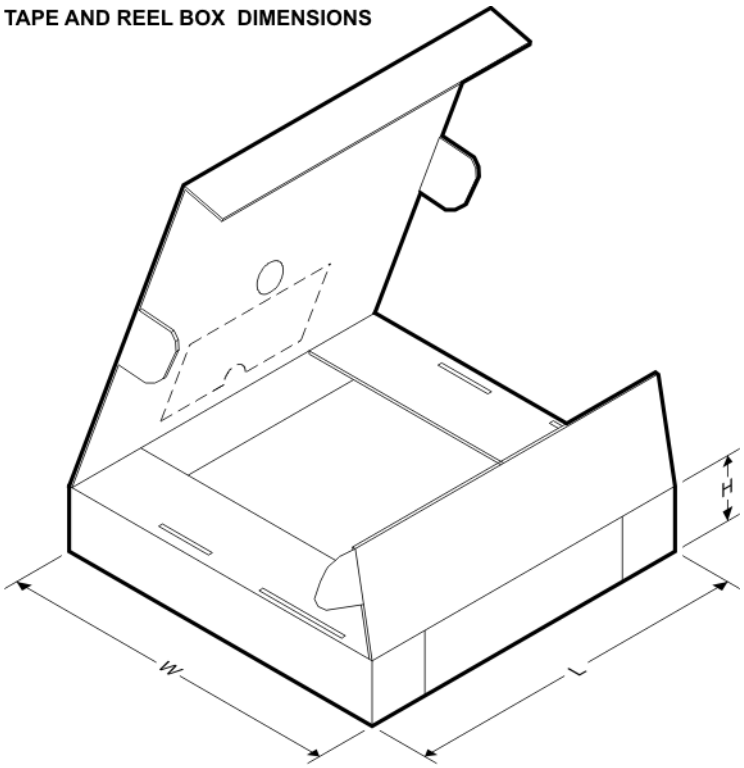
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5552TL/NOPB	DSBGA	YZR	36	250	178.0	12.4	3.63	3.63	0.76	8.0	12.0	Q1
LP5552TLX/NOPB	DSBGA	YZR	36	1000	178.0	12.4	3.63	3.63	0.76	8.0	12.0	Q1

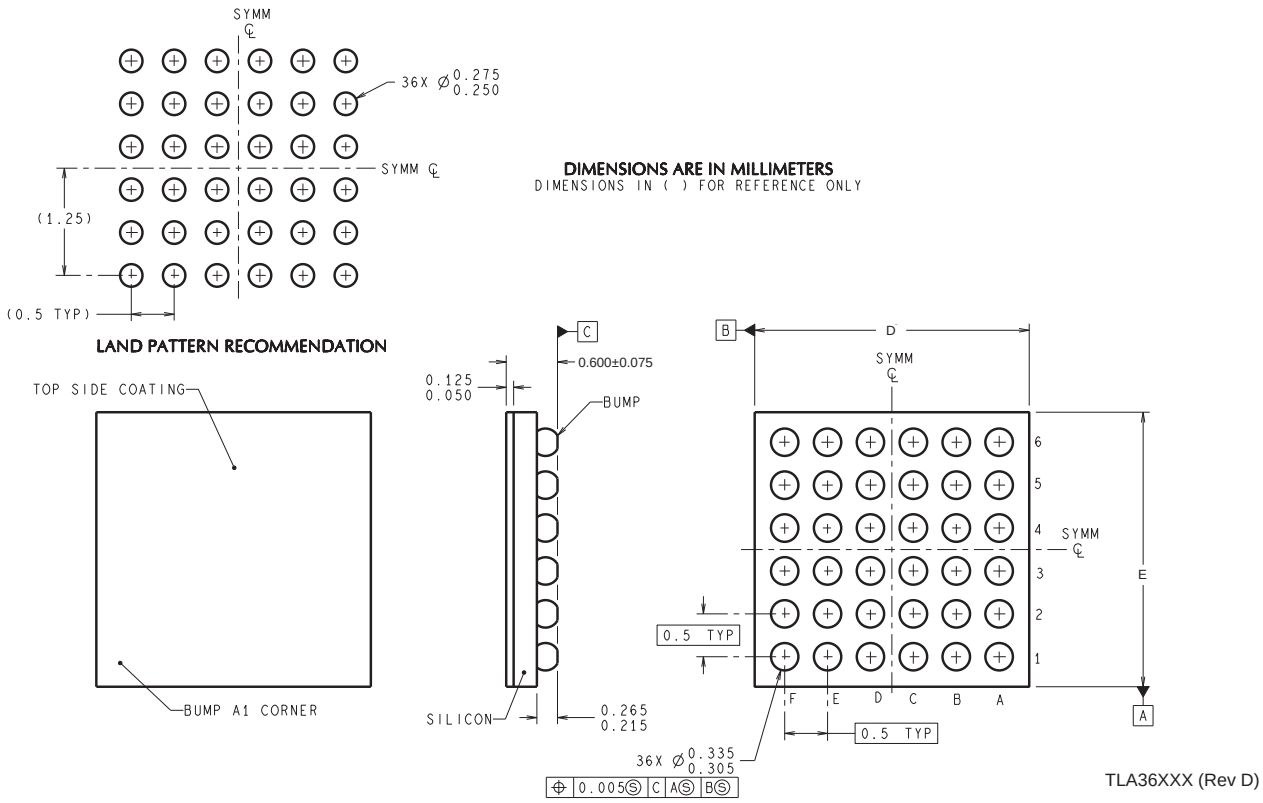
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5552TL/NOPB	DSBGA	YZR	36	250	210.0	185.0	35.0
LP5552TLX/NOPB	DSBGA	YZR	36	1000	210.0	185.0	35.0

YZR0036



D: Max = 3.489 mm, Min =3.429 mm

E: Max = 3.489 mm, Min =3.429 mm

4215058/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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