NOTE: PLEASE REVIEW THE ML410 BOM FOR ITEMS DESIGNATED AS "NOSTUFF".

NOSTUFF ITEMS ARE NOT POPULATED ON THE PCB.

THE ML410 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT

NOSTUFF DISCRETES AND COMPONENTS.

XILINX PART NUMBERS

SCHEMATICS	0381203
PCB ARTWORK	0531499
PCB FABRICATION	1280372

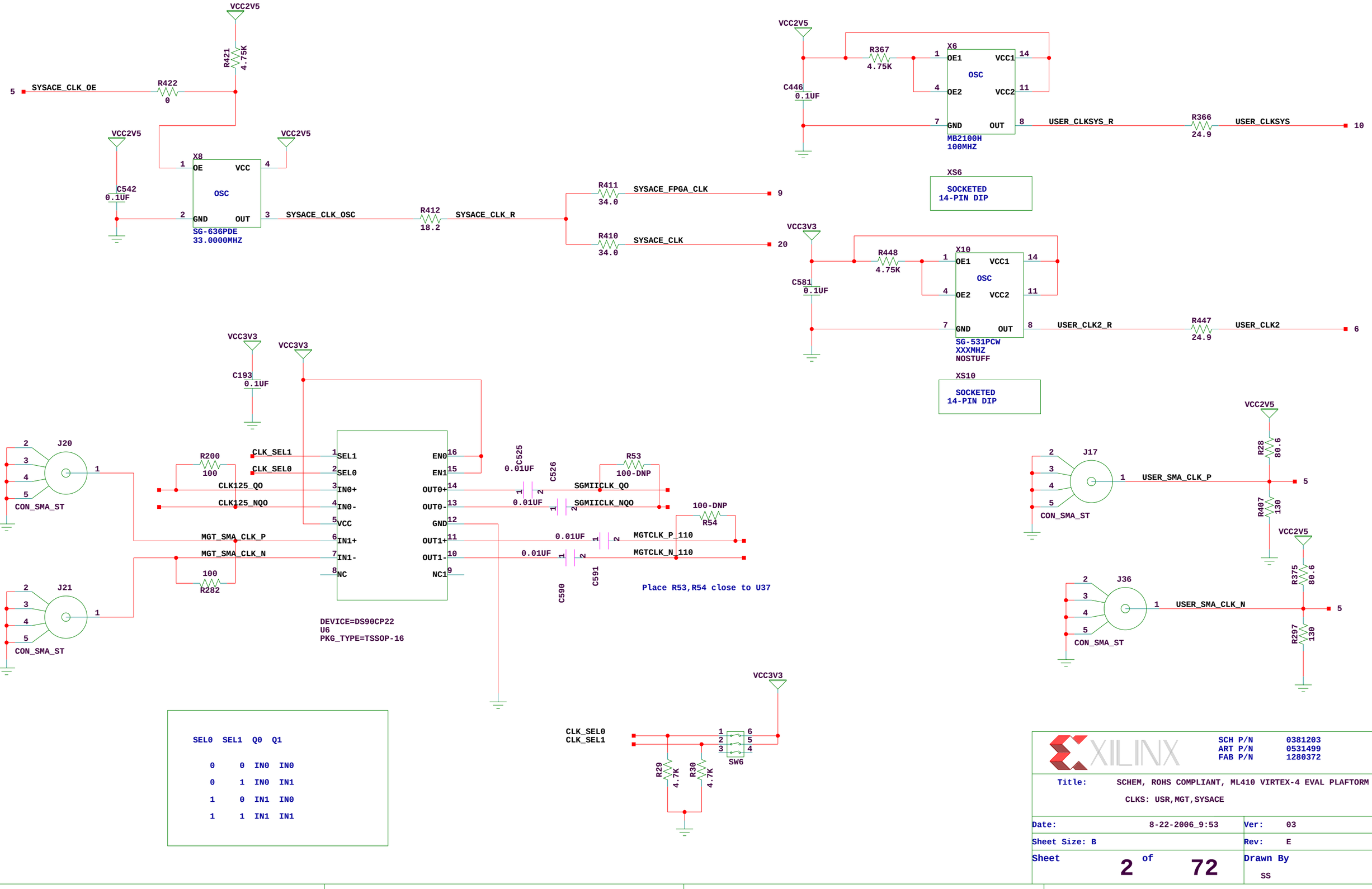
XILINX

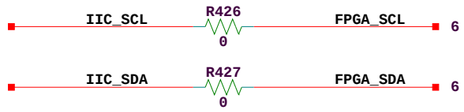
SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

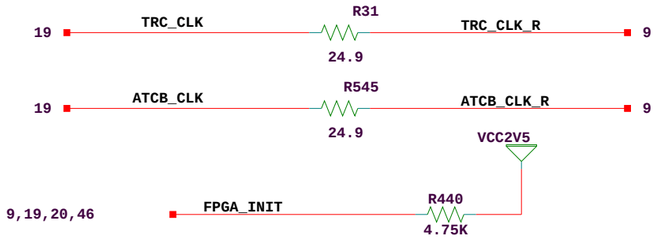
TABLE OF CONTENTS

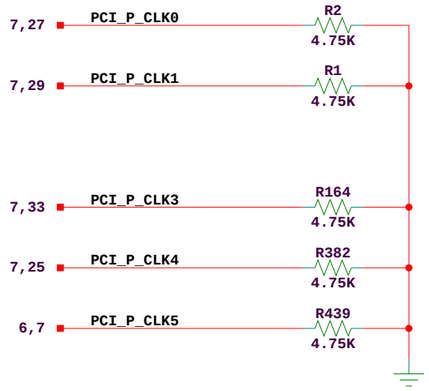
Date: 8-22-2006_9:53	Ver: 03
Sheet Size: B	Rev: E
Sheet 1 of 72	Drawn By SS


VCC2V5
R421
4.75K
5
SYSACE_CLK_OE
R422
0
VCC2V5
VCC2V5
X8
1
OE
VCC
4
C542
0.1UF
OSC
2
GND
OUT
3
SG-636PDE
33.0000MHZ
SYSACE_CLK_OSC
R412
18.2
SYSACE_CLK_R
R411
34.0
SYSACE_FPGA_CLK
9
R410
34.0
SYSACE_CLK
20
VCC2V5
R367
4.75K
X6
1
OE1
VCC1
14
OSC
4
OE2
VCC2
11
C446
0.1UF
7
GND
OUT
8
MB2100H
100MHZ
USER_CLKSYS_R
R366
24.9
USER_CLKSYS
10
XS6
SOCKETED
14-PIN DIP
VCC3V3
R448
4.75K
X10
1
OE1
VCC1
14
C581
0.1UF
OSC
4
OE2
VCC2
11
7
GND
OUT
8
SG-531PCW
XXXMHZ
NOSTUFF
USER_CLK2_R
R447
24.9
USER_CLK2
6
XS10
SOCKETED
14-PIN DIP
VCC3V3
C193
0.1UF
VCC3V3
2
J20
3
4
5
CON_SMA_ST
1
R200
100
CLK_SEL1
CLK_SEL0
CLK125_QO
CLK125_NQO
MGT_SMA_CLK_P
MGT_SMA_CLK_N
100
R282
2
J21
3
4
5
CON_SMA_ST
1
SEL1
SEL0
IN0+
IN0-
VCC
IN1+
IN1-
NC
1
2
3
4
5
6
7
8
EN0
EN1
OUT0+
OUT0-
GND
OUT1+
OUT1-
NC1
16
15
14
13
12
11
10
9
C525
0.01UF
C526
0.01UF
R53
100-DNP
SGMIICLK_QO
SGMIICLK_NQO
100-DNP
R54
0.01UF
MGTCLK_P_110
0.01UF
MGTCLK_N_110
C590
C591
Place R53,R54 close to U37
DEVICE=DS90CP22
U6
PKG_TYPE=TSSOP-16
VCC2V5
R28
80.6
2
J17
3
4
5
CON_SMA_ST
1
USER_SMA_CLK_P
5
R407
130
VCC2V5
R375
80.6
2
J36
3
4
5
CON_SMA_ST
1
USER_SMA_CLK_N
5
R297
130
VCC3V3
CLK_SEL0
CLK_SEL1
1
2
3
6
5
4
SW6
R29
4.7K
R30
4.7K
SEL0 SEL1 Q0 Q1
0 0 IN0 IN0
0 1 IN0 IN1
1 0 IN1 IN0
1 1 IN1 IN1
XILINX
SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
CLKS: USR,MGT,SYSACE
Date: 8-22-2006_9:53
Ver: 03
Sheet Size: B
Rev: E
Sheet 2 of 72
Drawn By
SS

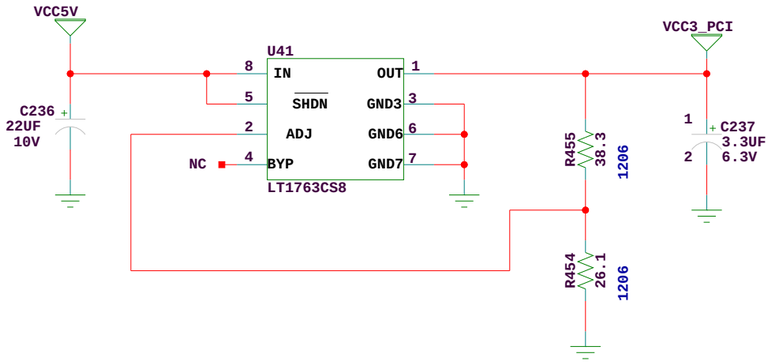


NOTE: TRC_CLK RESISTOR ALLOWS CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.

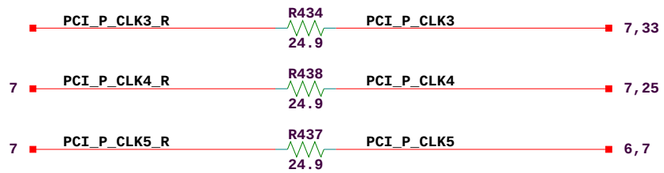




NOTE: THE PCI SPEC RECOMMENDS THAT
CLOCKS BE PULLED LOW WHEN THE
BUS IS NOT ACTIVELY CLOCKED.



NOTE: PCI_CLK RESISTORS ALLOW CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



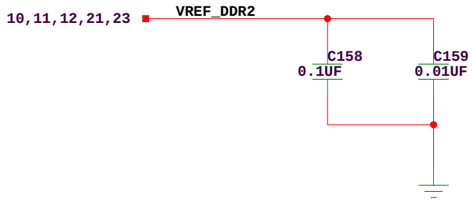
NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN
FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT
THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON
THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY
THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.

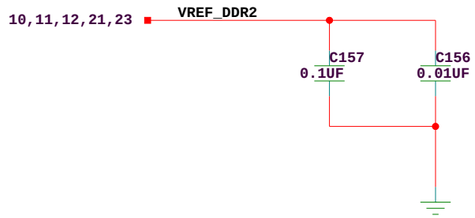
XILINX

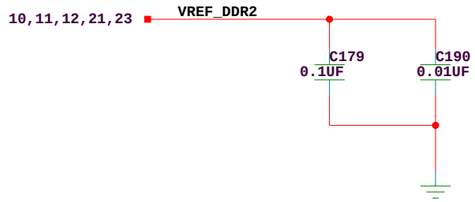
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

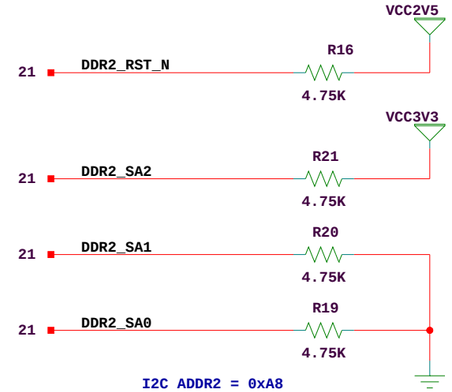
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
PCI_SUPPLY ....

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	3 of 72	Drawn By	SS

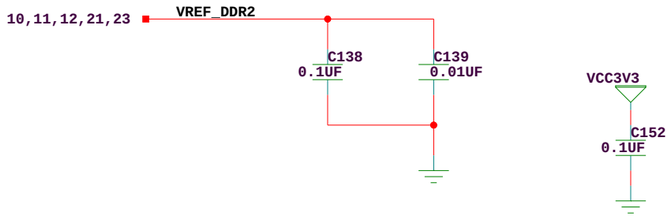


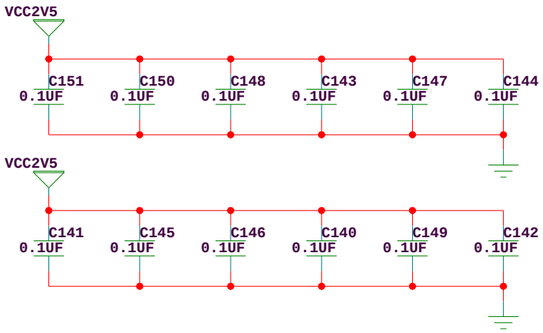






I2C ADDR2 = 0xA8





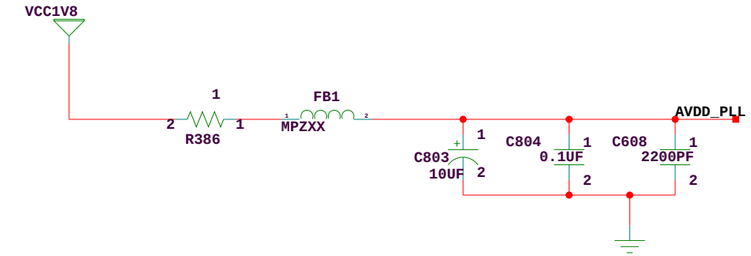
NOTE: THE PINOUT OF THE DDR2 DQ AND DQS
SIGNALS IS INTENDED TO ALLOW THE
USE OF LOCAL CLOCKING RESOURCES
AS DESCRIBED IN XAPP609.

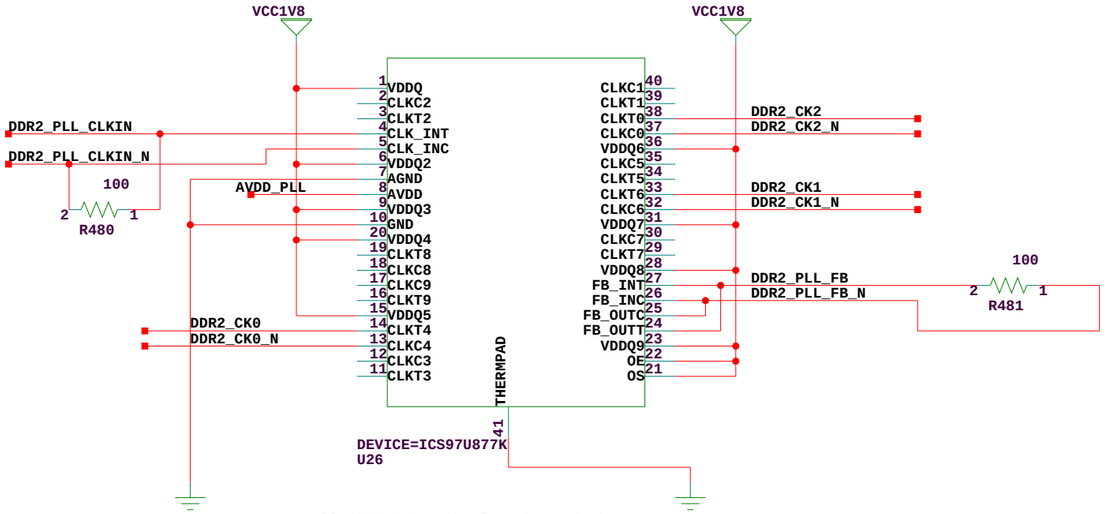
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
DDR2 DECOUPLING

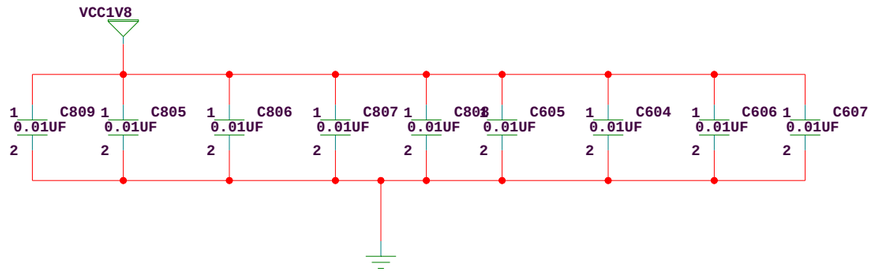
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	4 of 72	Drawn By	SS

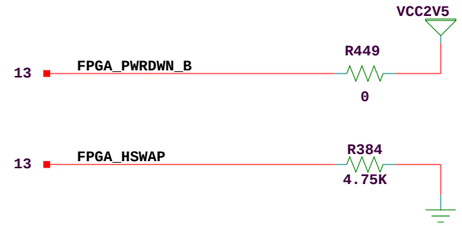


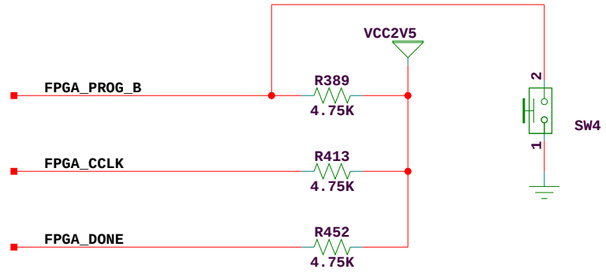


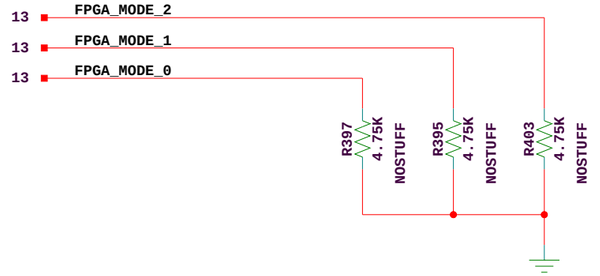
All DDR2_CK* to be length matched

DDR2_PLL_FB* to be length matched to DDR2_CK*









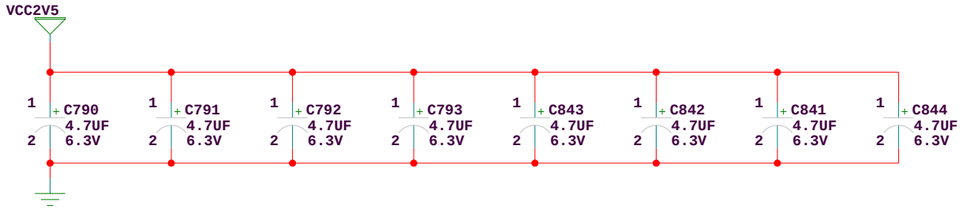
NOTE: MODE BITS HAVE INTERNAL PULLUPS AND DEFAULT
TO SLAVE-SERIAL MODE. THERE MAY BE SOME
CONFLCITS BETWEEN THE JTAG MODES AND ICAP
HOWEVER SLAVE-SERIAL MODE IS KNOWN TO WORK.

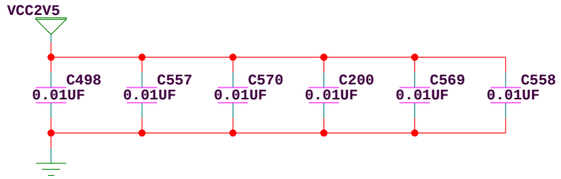
XILINX

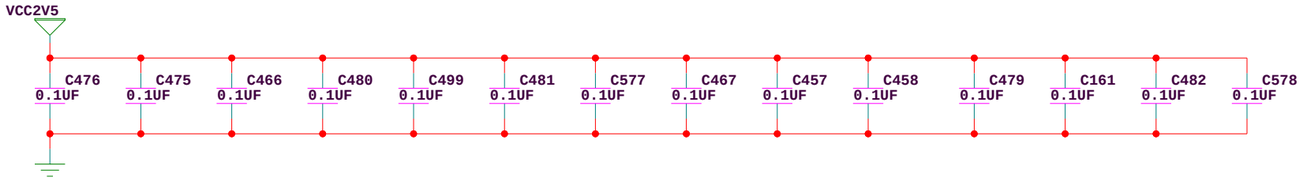
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

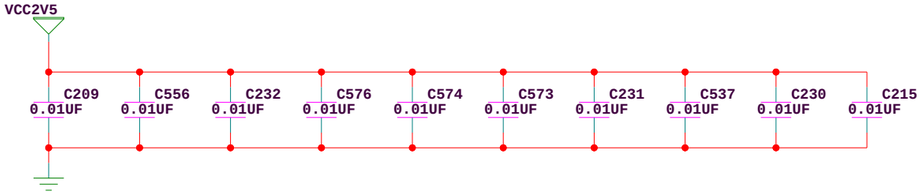
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
FPGA CONFIG AND MISC I/O

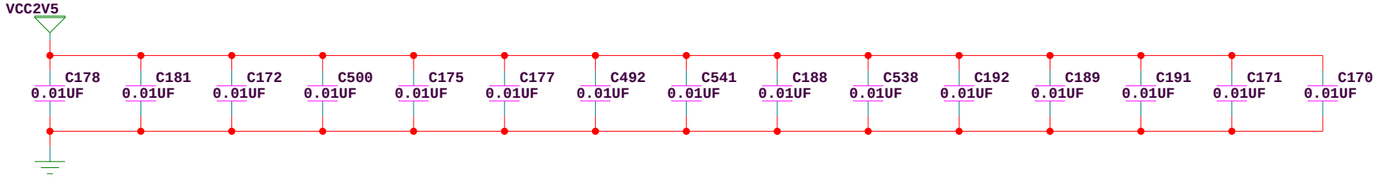
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	5 of 72	Drawn By	SS



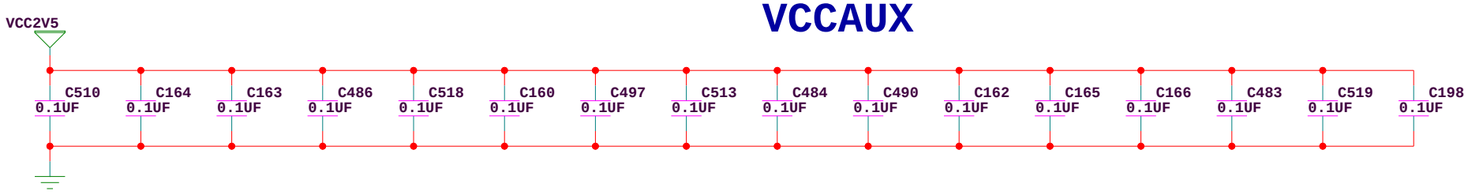




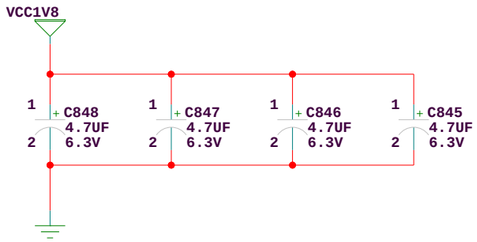


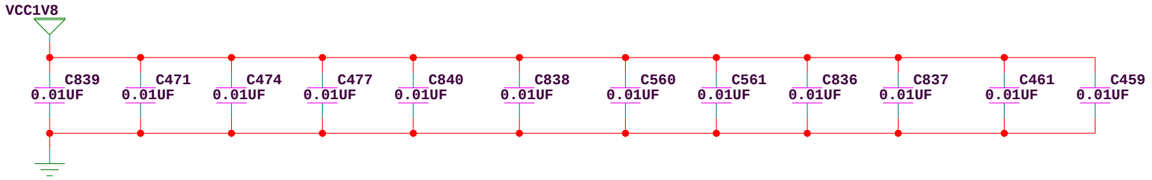


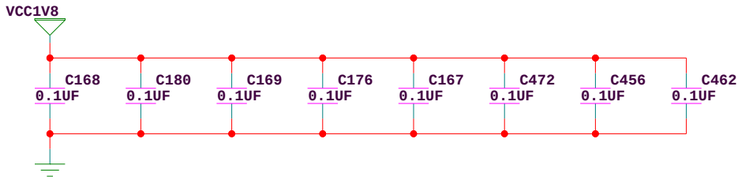
VCCAUX



BANK 1,2,3,4,5,7,8,9,11







XILINX

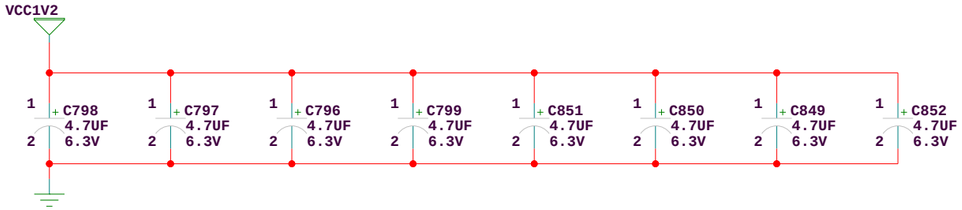
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

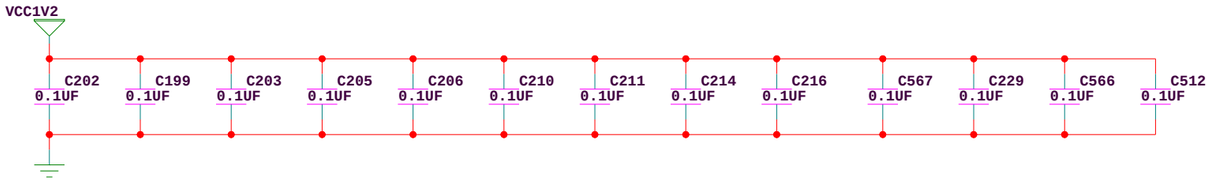
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

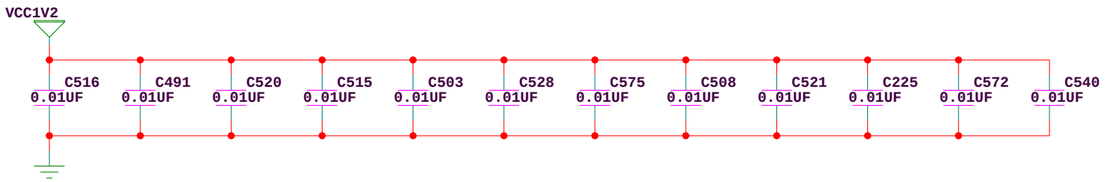
FPGA DECOUPLING

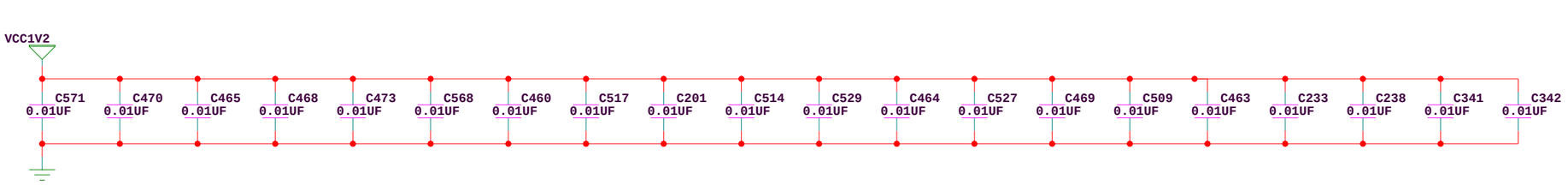
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	6 of 72	Drawn By	SS

VCORE

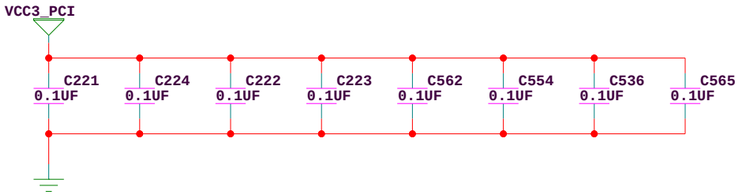


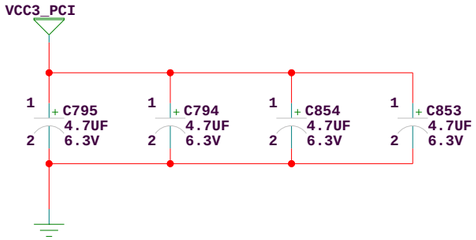


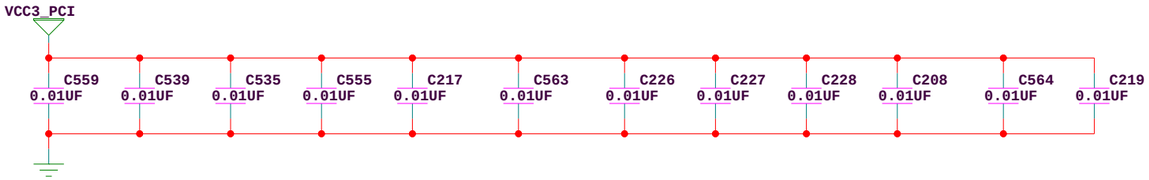




BANK 6,10,12





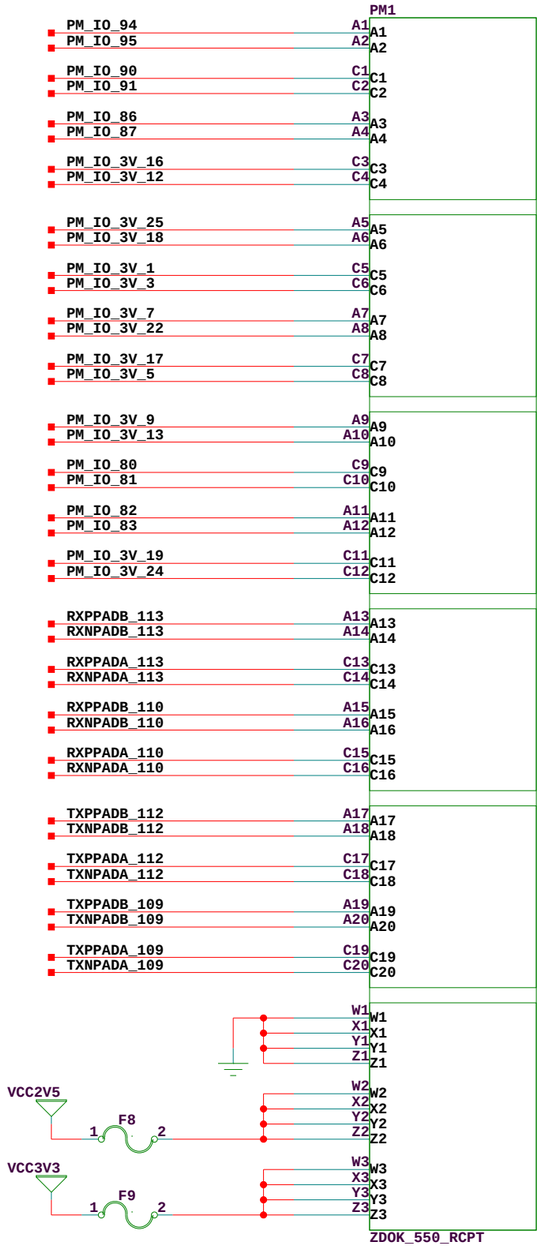


XILINX

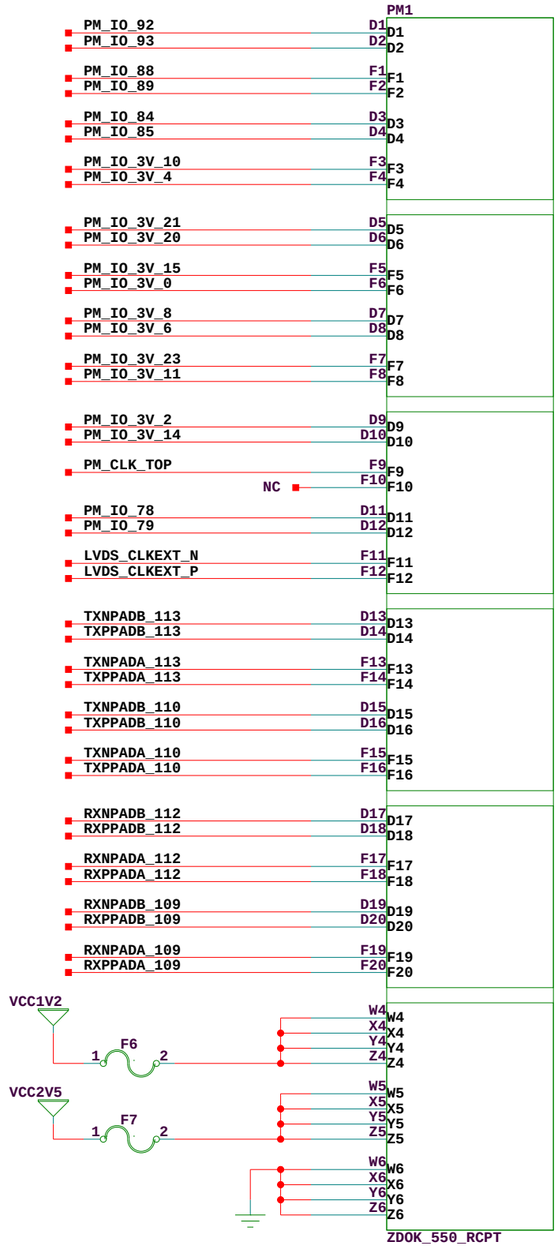
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

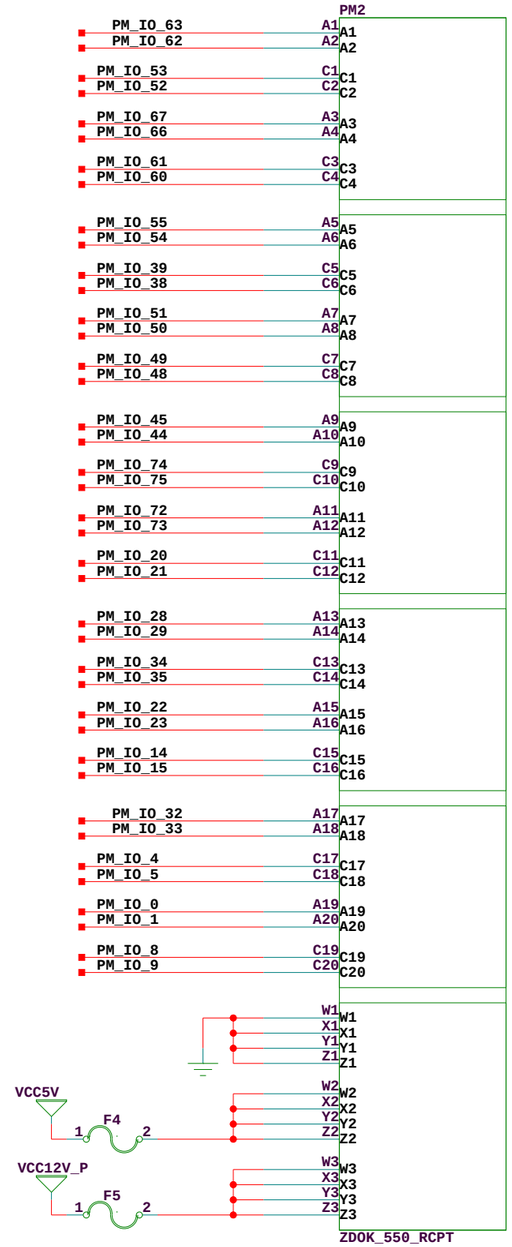
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
FPGA DECOUPLING

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	7 of 72	Drawn By	SS

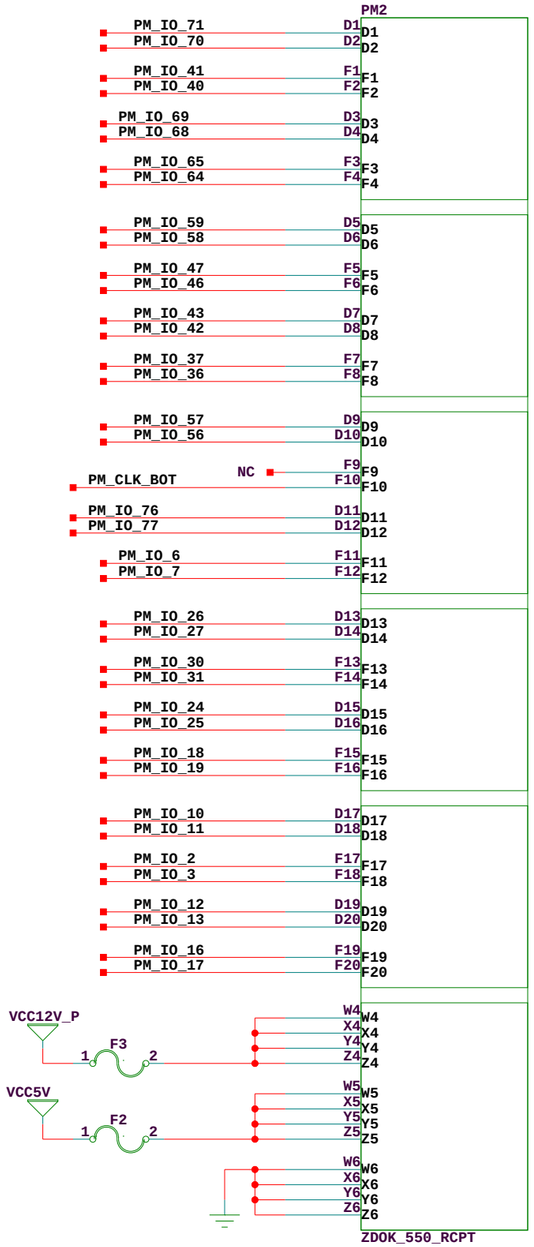


GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20





GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20

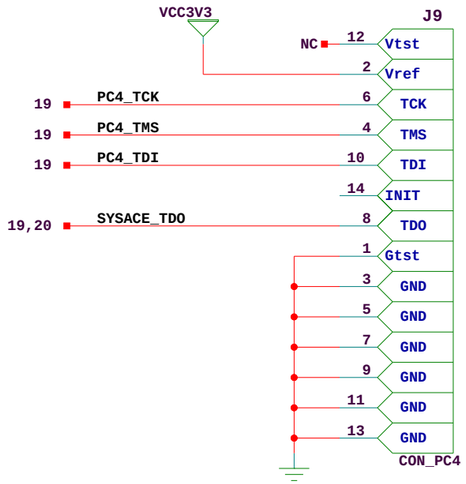


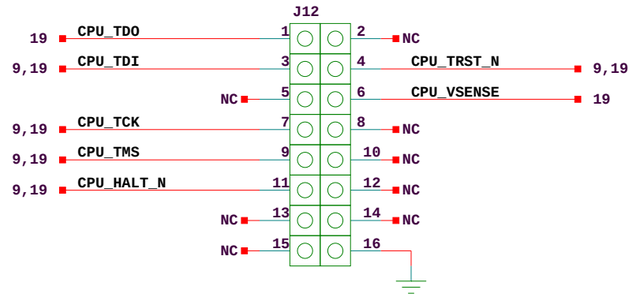
XILINX	SCH P/N	0381203
	ART P/N	0531499
	FAB P/N	1280372

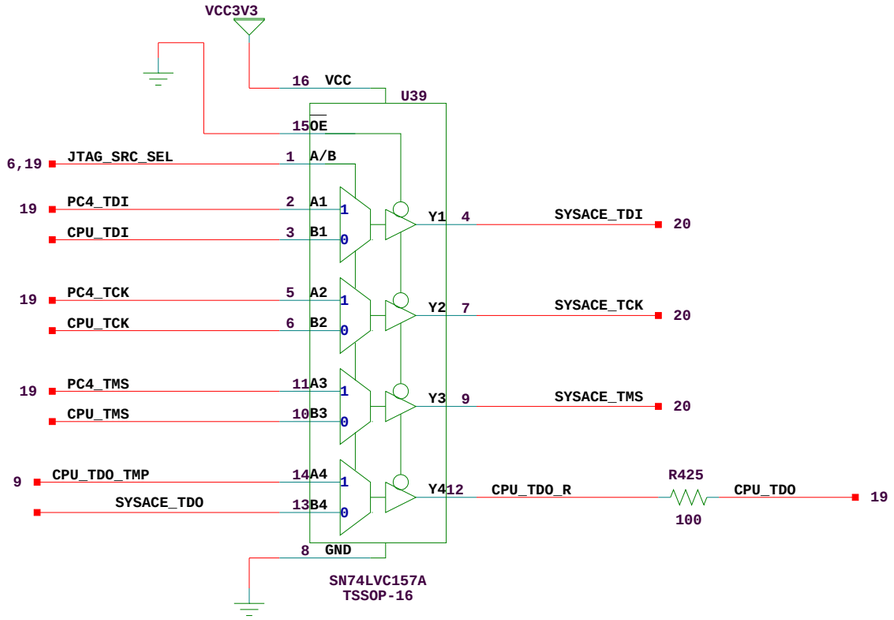
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

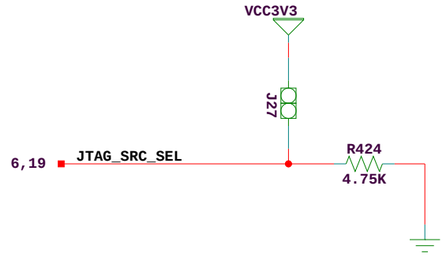
PERSONALITY MODULE CONNECTORS

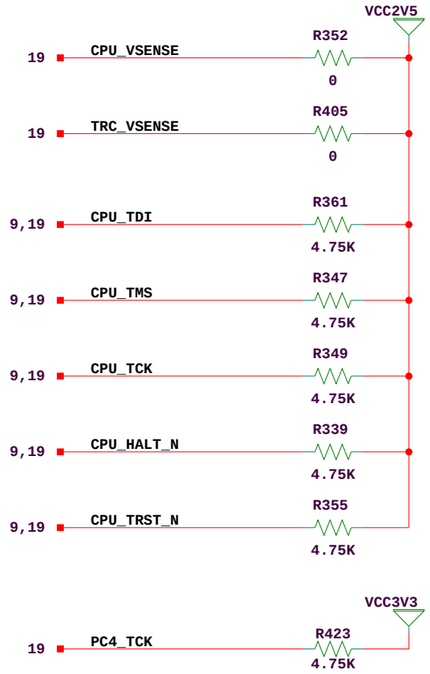
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	8 of 72	Drawn By	SS



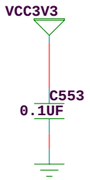


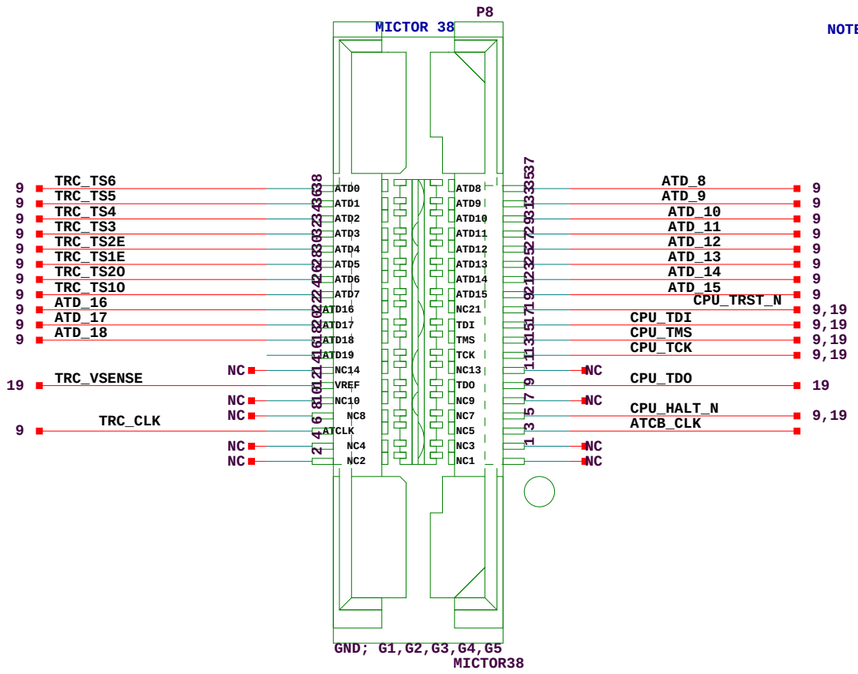




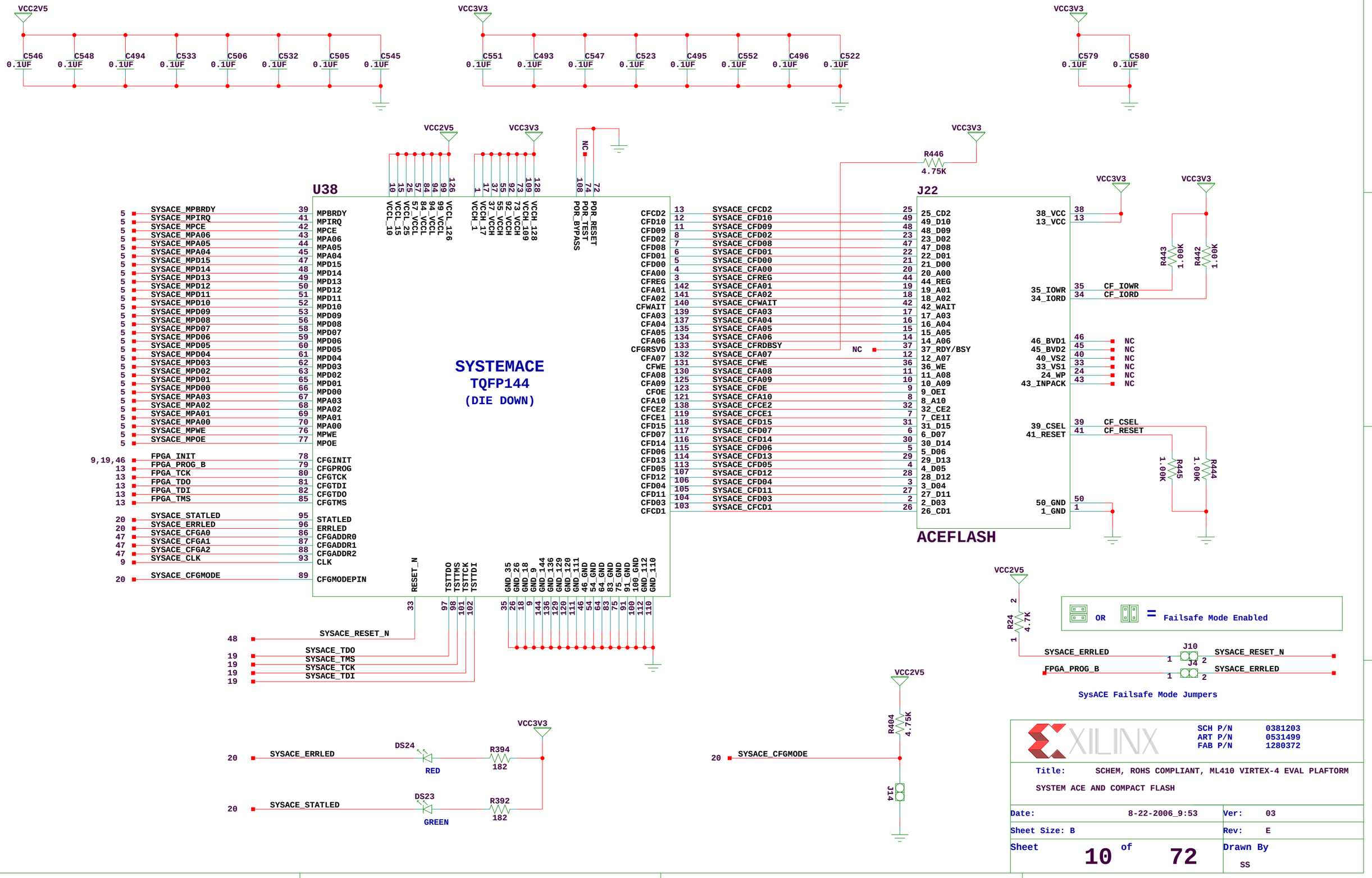


NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO
3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS.
THE SERIES RESISTOR ON CPU_TDO IS INTENDED
TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.





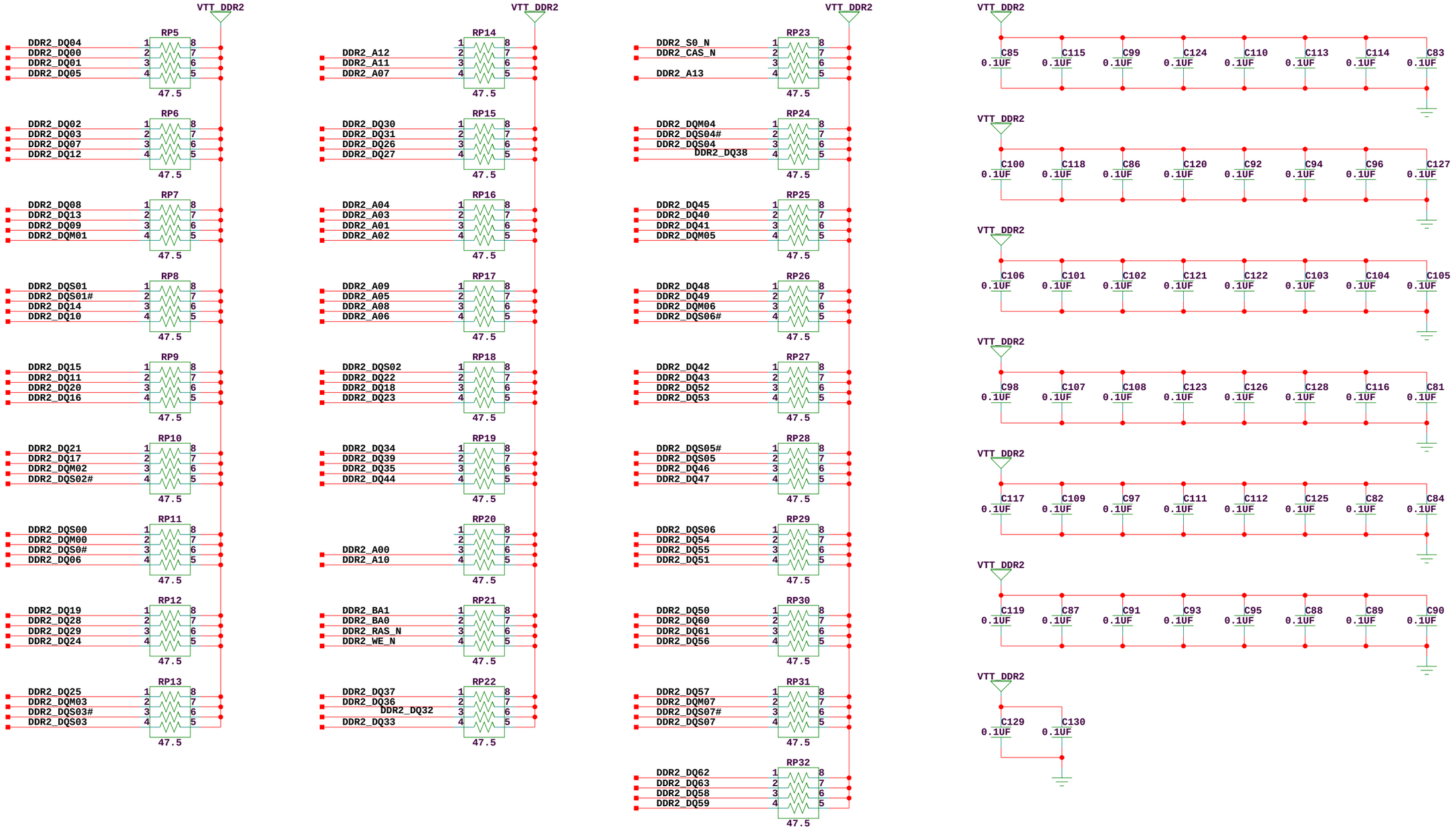
XILINX	SCH P/N	0381203	
	ART P/N	0531499	
	FAB P/N	1280372	
Title:	SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM JTAG, DEBUG, TRACE CONNECTORS		
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	9 of 72	Drawn By	SS

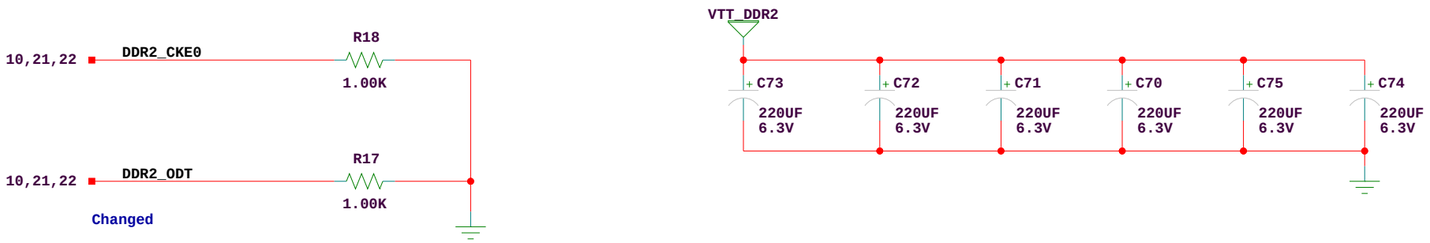


SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
SYSTEM ACE AND COMPACT FLASH

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	10 of 72	Drawn By	SS





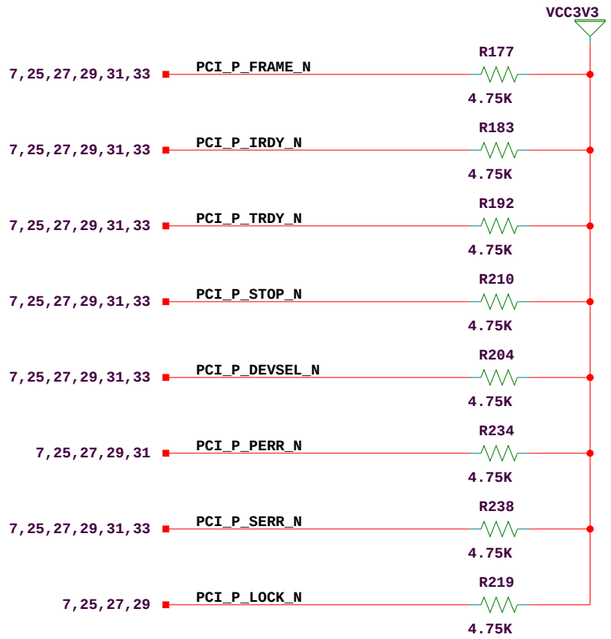
XILINX

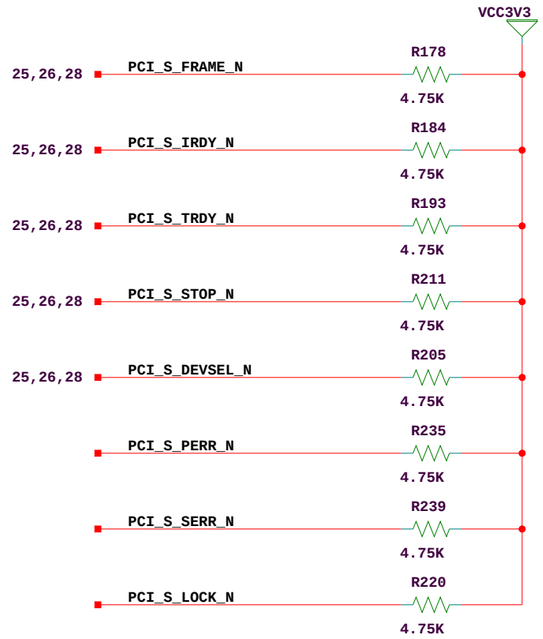
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

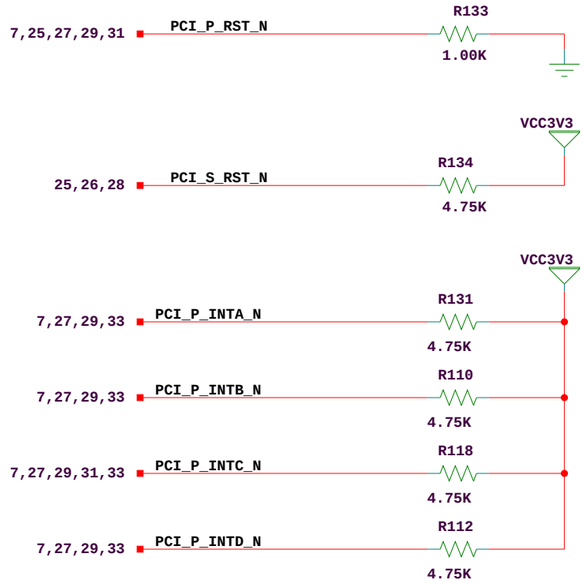
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

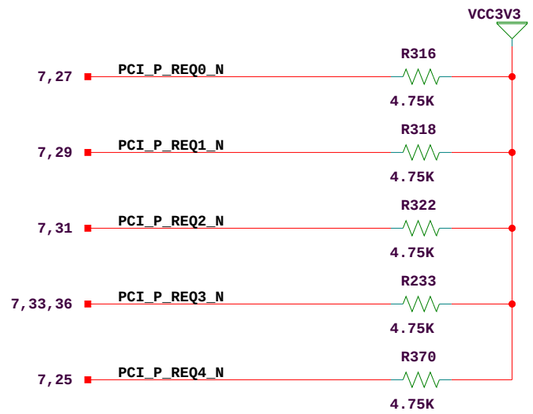
DDR2 SSTL-2 TERMINATION

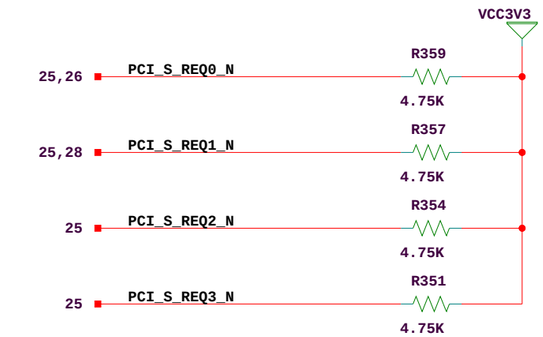
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	11 of 72	Drawn By	SS











XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

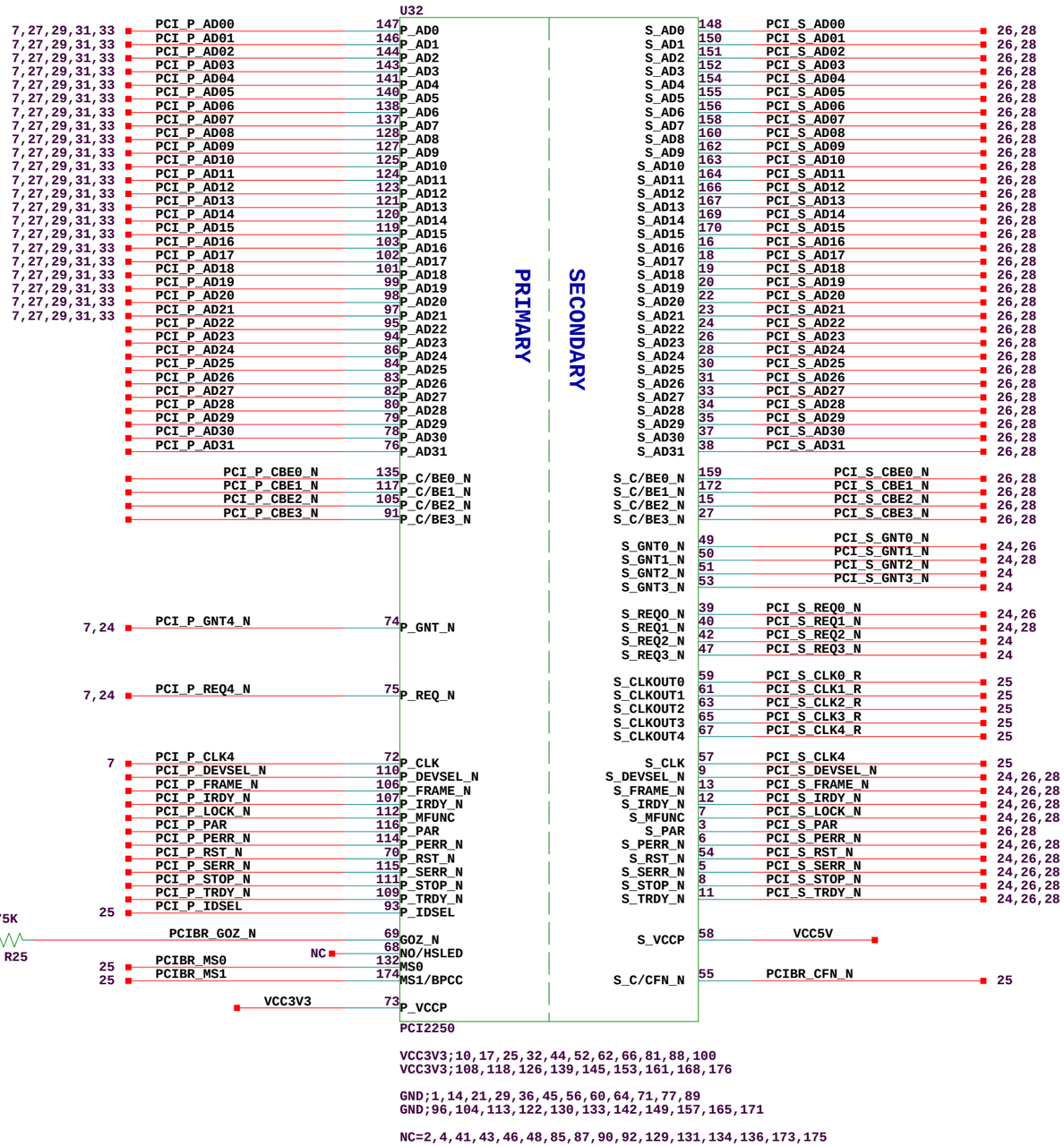
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

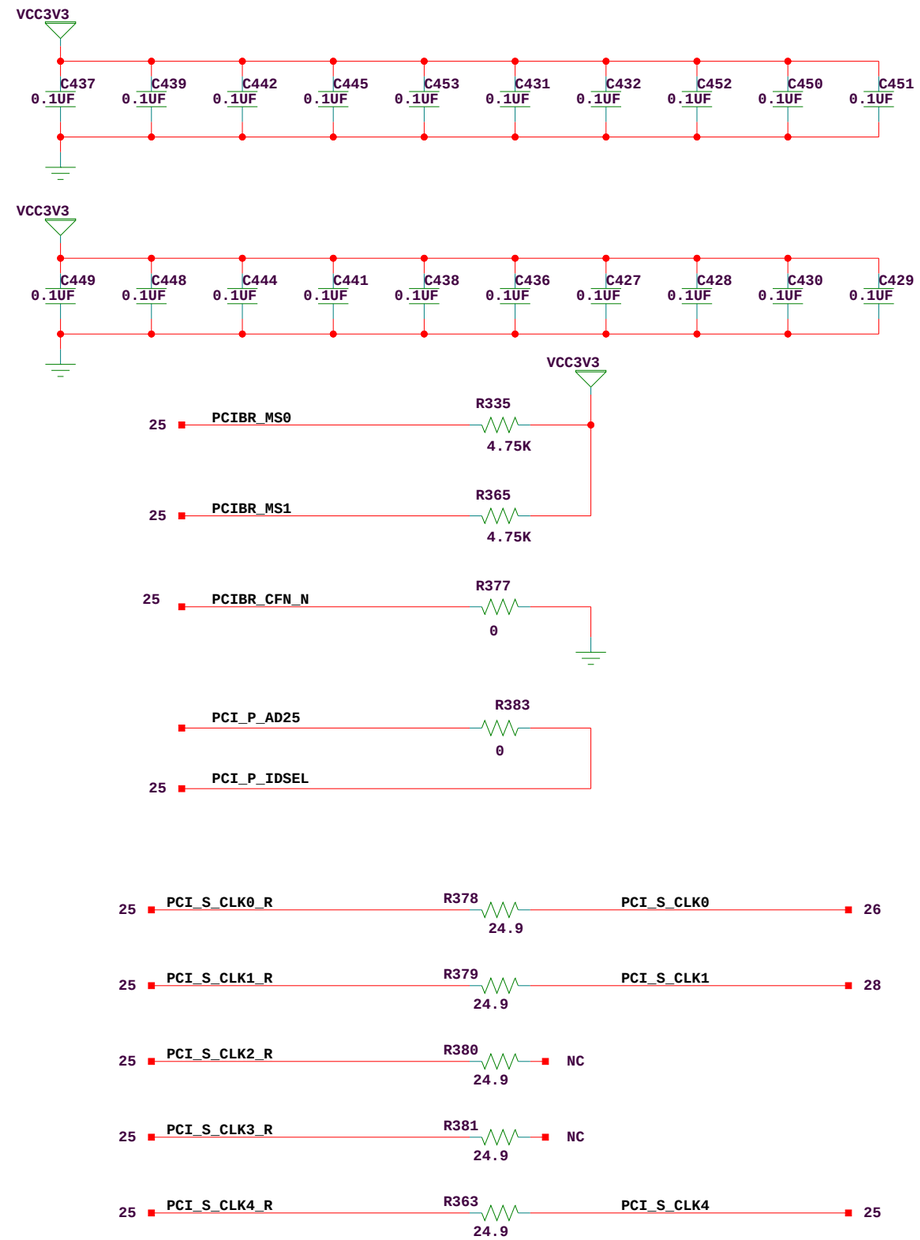
PCI BUS PULLUPS

Date: 8-22-2006_9:53	Ver: 03
Sheet Size: B	Rev: E
Sheet 12 of 72	Drawn By SS

PCI-PCI BRIDGE

PCI2250_PGF





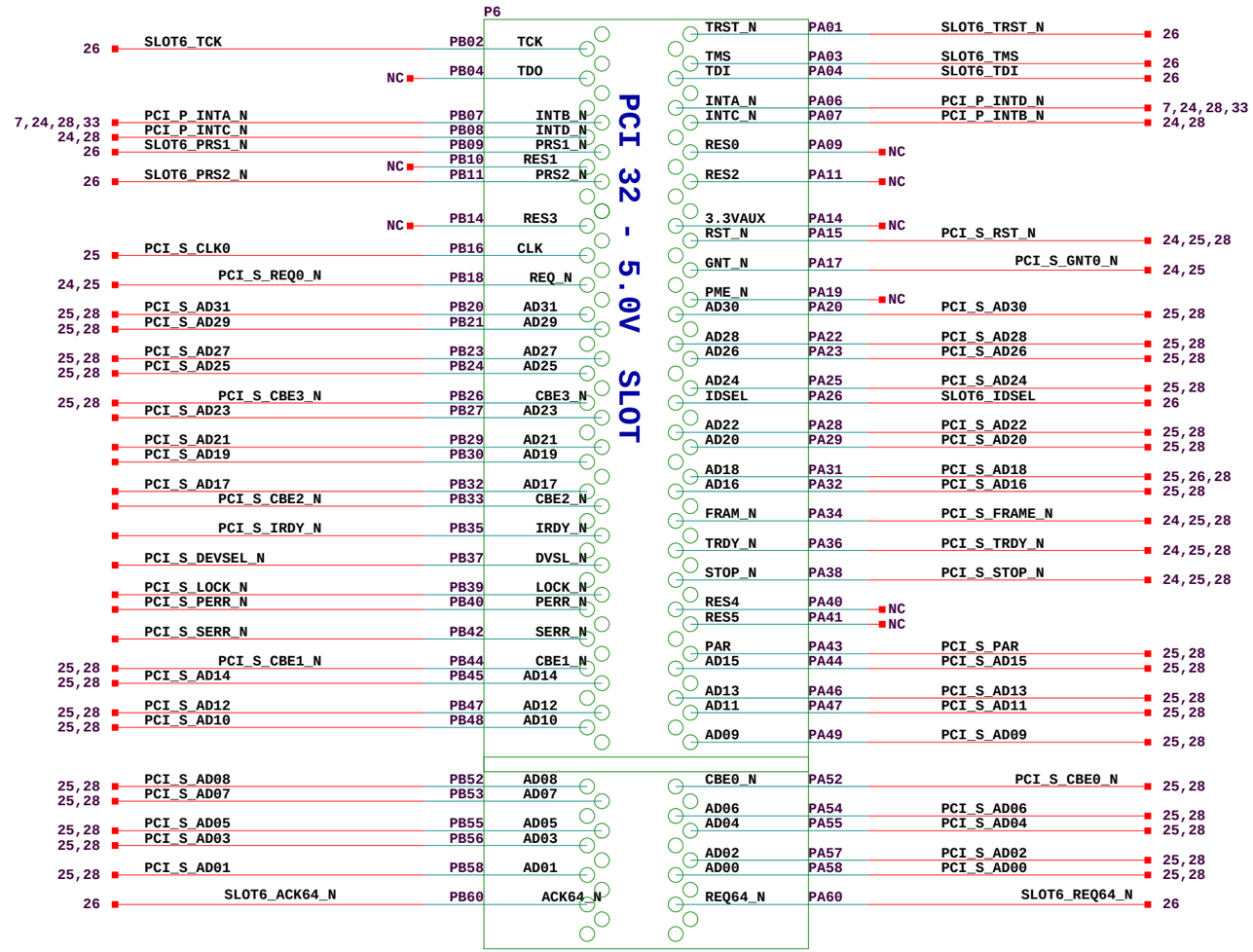
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI-PCI BRIDGE

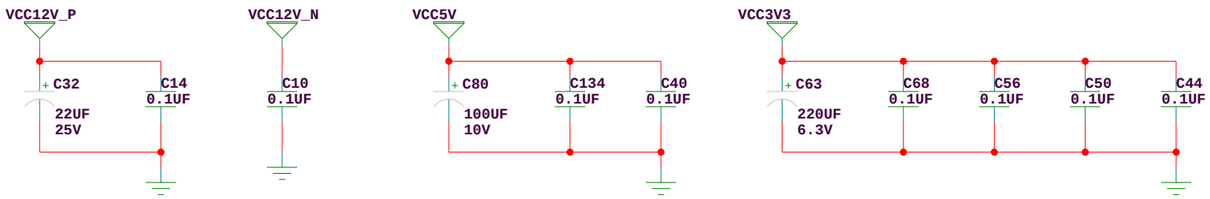
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	13 of 72	Drawn By	SS

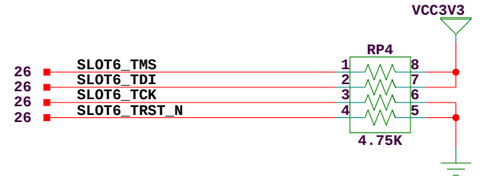


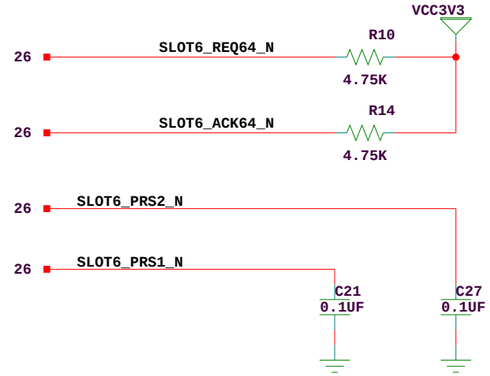
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

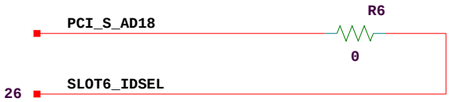
VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13









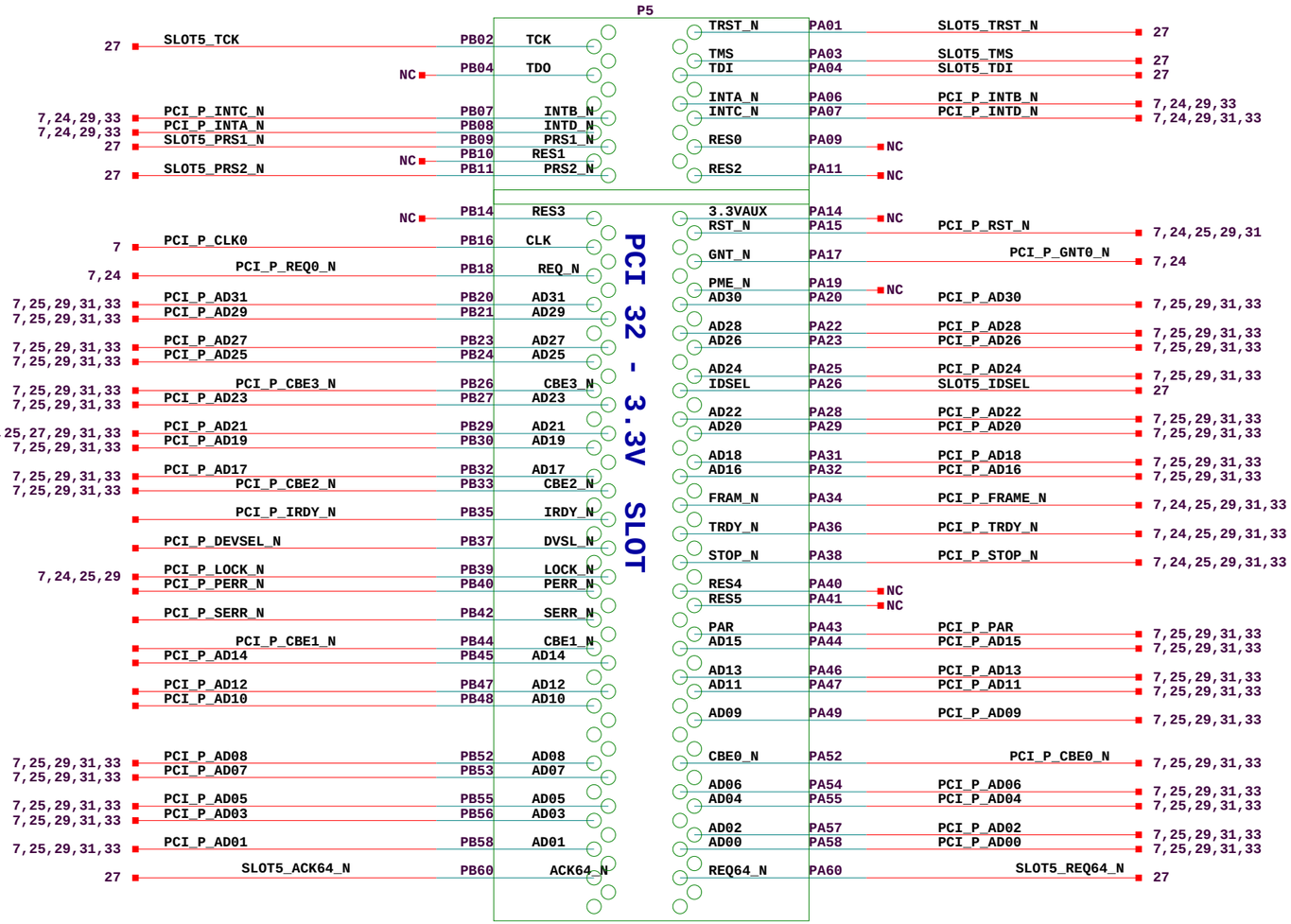
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 6, 5.0V, SECONDARY BUS

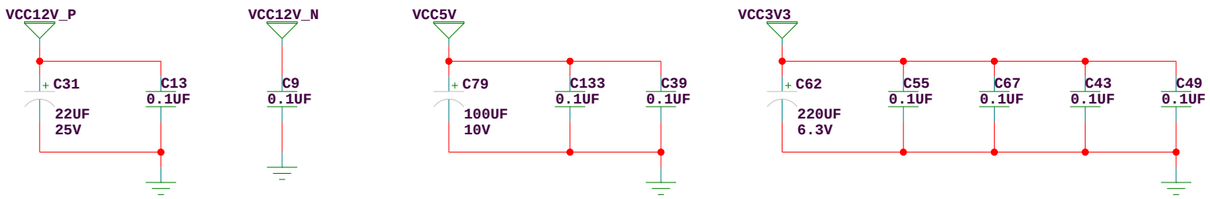
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	14 of 72	Drawn By	SS

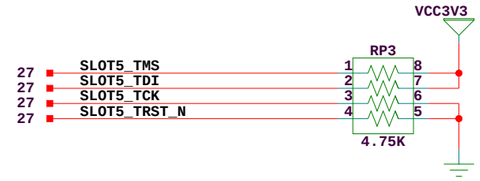


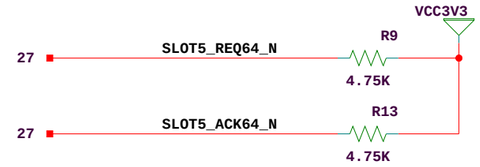
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

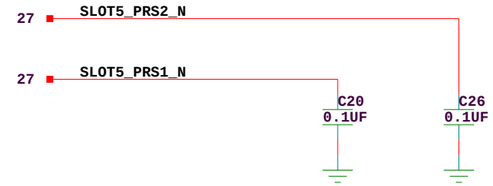
VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

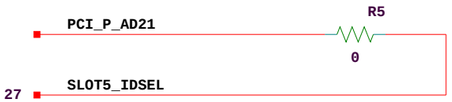
GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB50,PA50,PB51,PA51











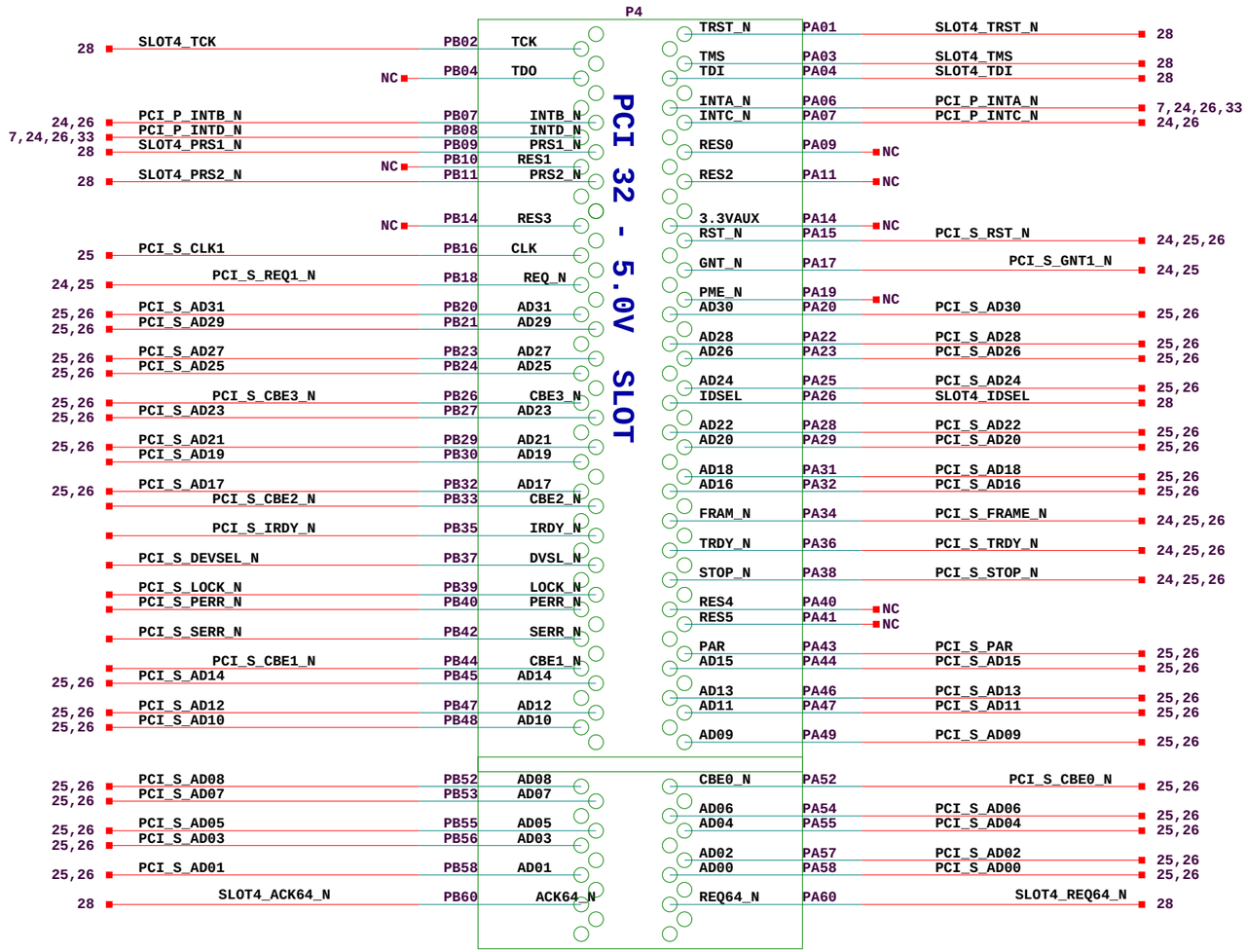
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 5, 3.3V, PRIMARY BUS

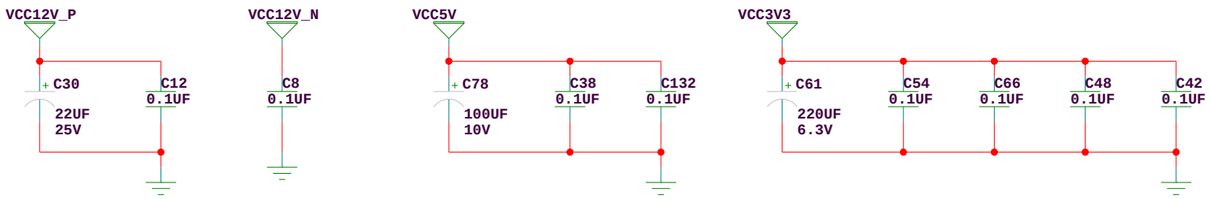
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	15 of 72	Drawn By	SS

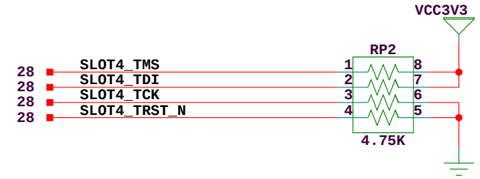


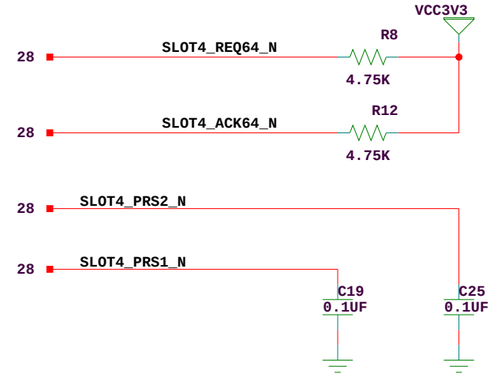
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

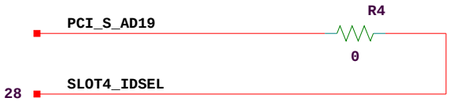
VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13









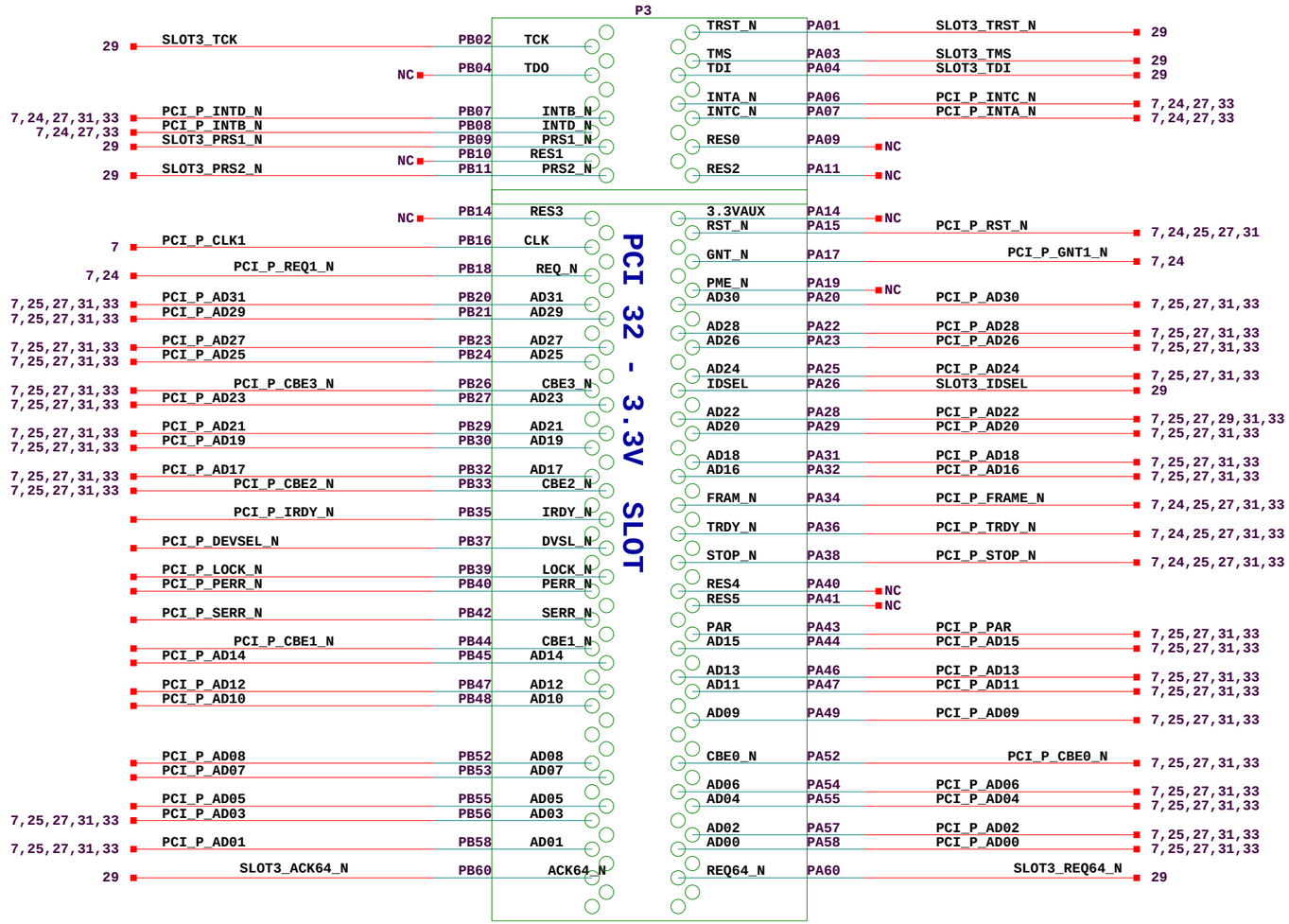
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 4, 5.0V, SECONDARY BUS

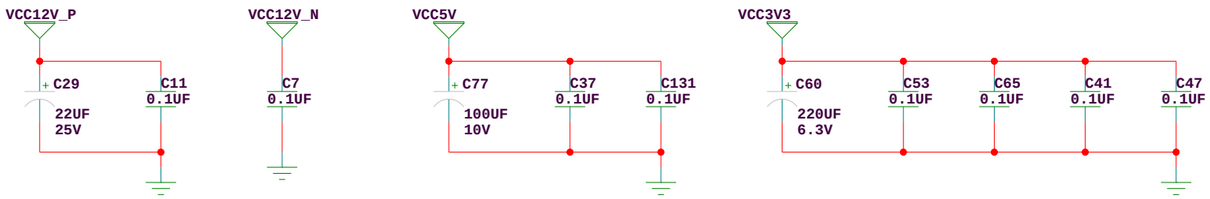
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	16 of 72	Drawn By	SS

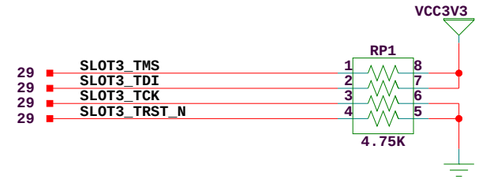


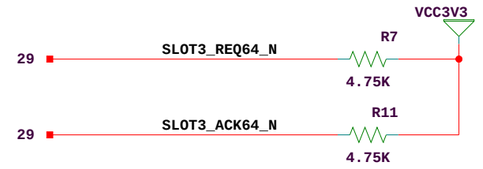
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

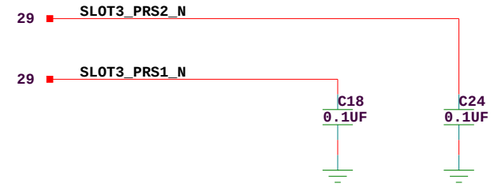
VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

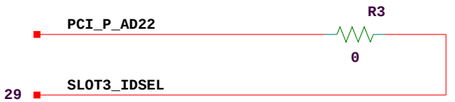
GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB50,PA50,PB51,PA51











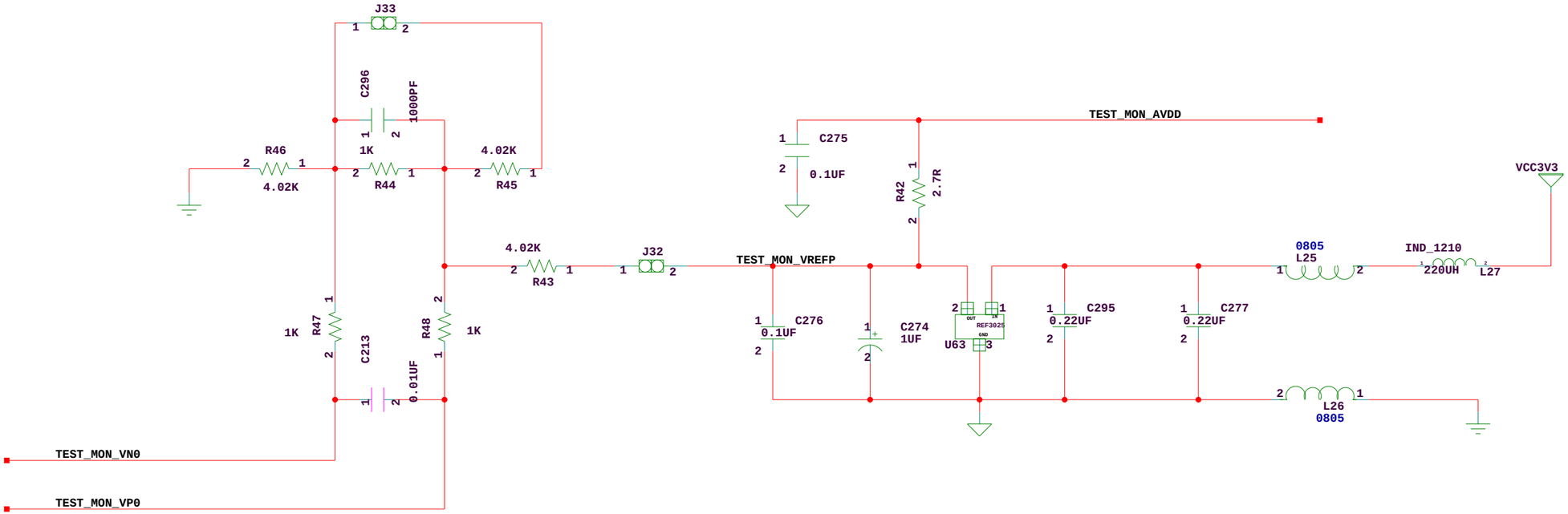
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 3, 3.3V, PRIMARY BUS

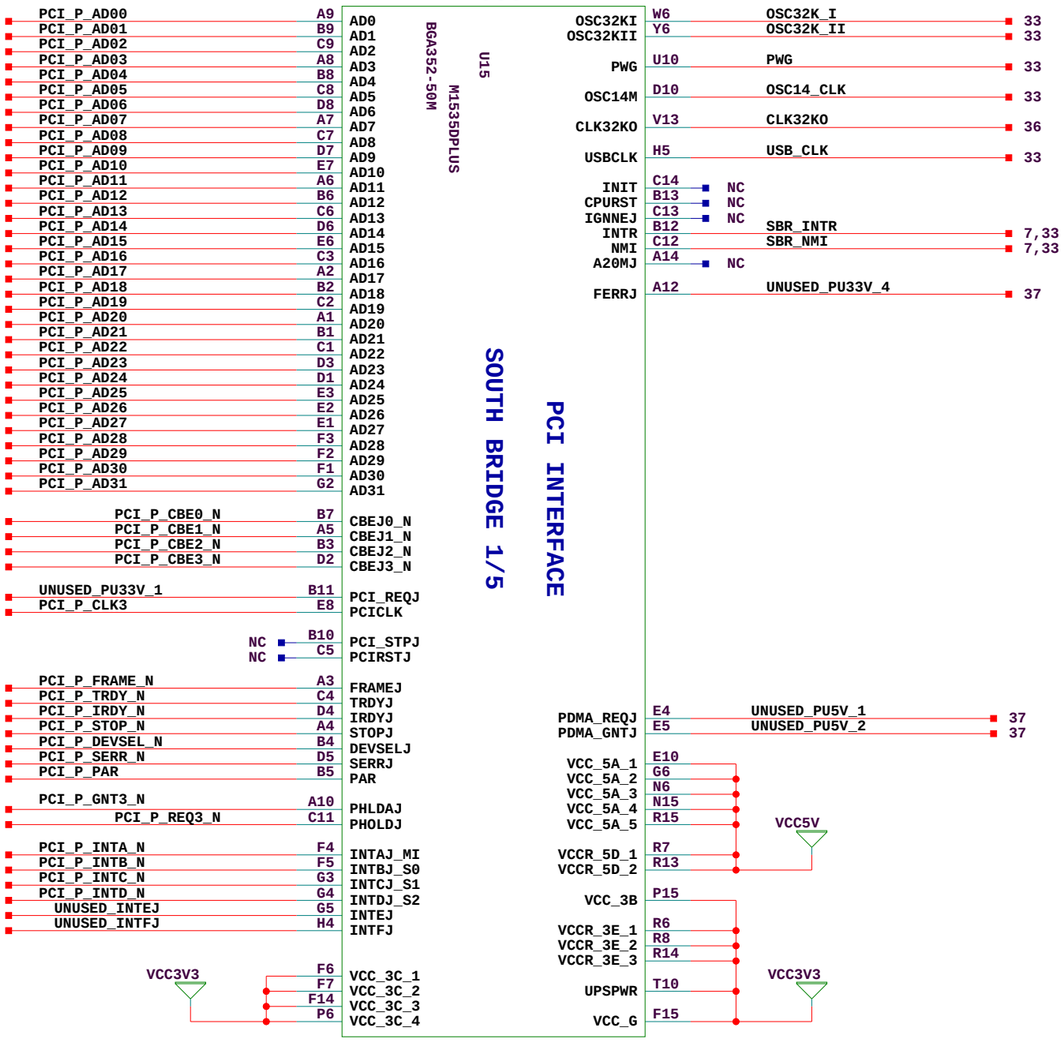
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	17 of 72	Drawn By	SS

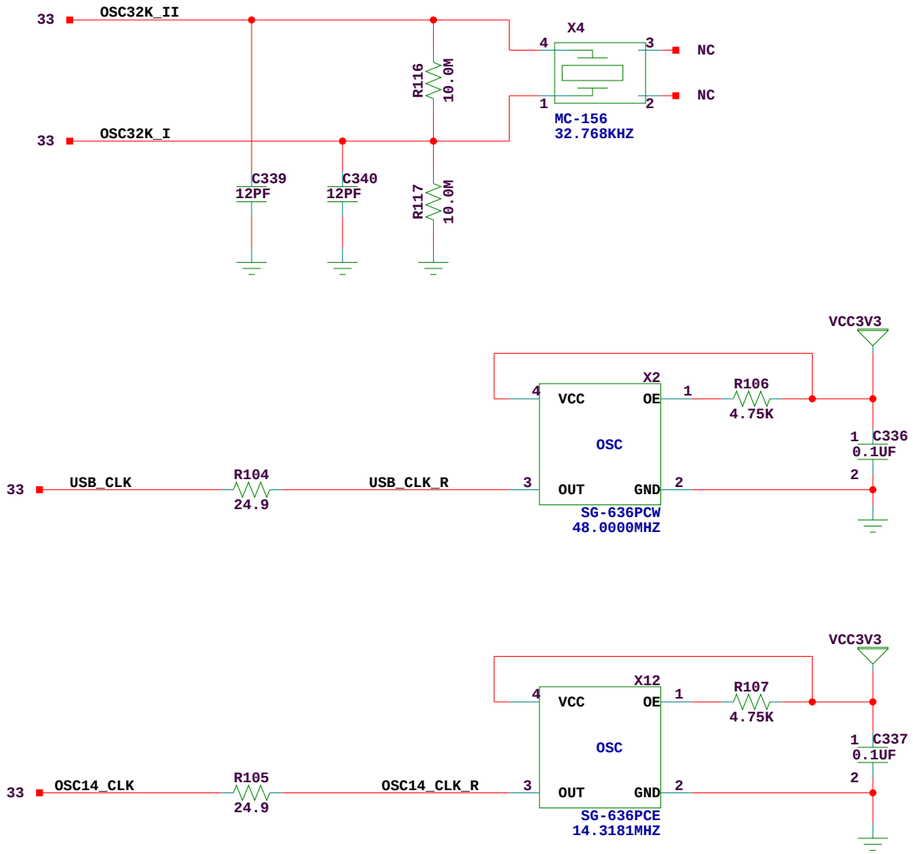


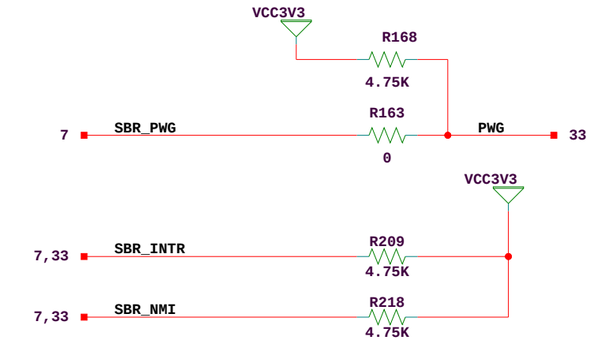
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

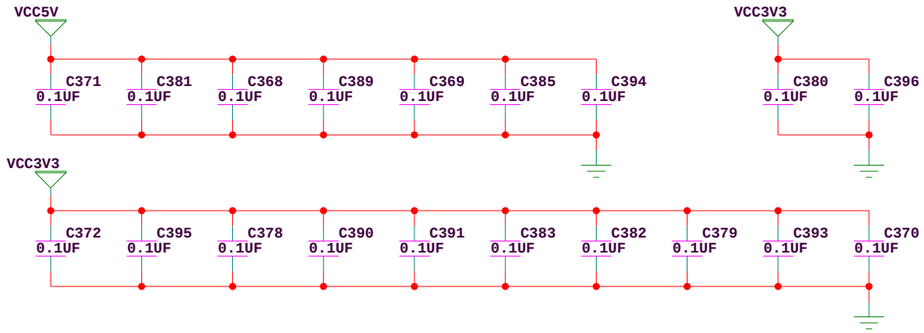
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
TEST INTERFACE

Date: 8-22-2006_9:53	Ver: 03
Sheet Size: B	Rev: E
Sheet 18 of 72	Drawn By SS









XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 1

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	19 of 72	Drawn By	SS

M1535D+

U15 — M1535DPLUS — BGA352-50M

SOUTH BRIDGE 2/5

PARALLEL PORT	STROBJ	P1	PP_STROBE_N_R 38
	AUTOFDJ	R1	PP_AUTOFD_N_R 38
	PD0	P2	PP_DATA0_R 38
	ERRORJ	T1	PP_ERROR_N_R 38
	PD1	P3	PP_DATA1_R 38
	PRINITJ	R2	PP_INIT_N_R 38
	PD2	N1	PP_DATA2_R 38
	SLCTINJ	R3	PP_SLCTIN_N_R 38
	PD3	N2	PP_DATA3_R 38
	PD4	N3	PP_DATA4_R 38
	PD5	N4	PP_DATA5_R 38
	PD6	N5	PP_DATA6_R 38
	PD7	M2	PP_DATA7_R 38
	PRNACKJ	M3	PP_ACK_N_R 38
	BUSY	M4	PP_BUSY_R 38
	PE	M5	PP_PEND_R 38
	SLCT	L5	PP_SELECT_R 38
SERIAL PORT1	SIN1	H2	
	SOUT1	J5	
	RTS1J	H1	
	DTR1J	J3	
	CTS1J	J4	
	DSR1J	H3	
	DCD1J	G1	
	RI1J	J2	
SERIAL PORT2	SIN2	K4	
	SOUT2	K2	
	RTS2J	K3	
	DTR2J	L2	
	CTS2J	K1	
	DSR2J	K5	
	DCD2J	J1	
	RI2J	L1	
USB PORTS	OVCRJ1	T6	USB1_OVCR_N 40
	OVCRJ0	T5	USB0_OVCR_N 40
	USB_PWENJ	V9	USB_POWEN_N 40
	GPIO22	U5	GPIO_23 42
	GPIO23	U6	GPIO_22 42
	USBP0+	W8	USB0_DP_R 40
	USBP0-	V8	USB0_DN_R 40
	USBP1+	U9	USB1_DP_R 40
	USBP1-	Y7	USB1_DN_R 40
	USBP2+	W7	GPI_34 42
	USBP2-	V7	UNUSED_PD_1 37
	USBP3+	U8	GPI_36 42
	USBP3-	T8	UNUSED_PD_2 37
IrDA	IRRXH	L4	UNUSED_PD_3 37
	IRRX	L3	UNUSED_PD_4 37
	IRTX	M1	NC
KEYBRD MOUSE	KBCLK	U11	KBCLK_R 40
	KBDATA	U12	KBDATA_R 40
	KBINH	V12	KBINH 34,47
	MSCLK	T11	MSCLK_R 40
	MSDATA	T12	MSDATA_R 40

M1535D+

U15 — M1535DPLUS — BGA352-50M

SOUTH BRIDGE 3/5

IDE INTERFACE	PIDED0	G17	PIDE_D0_R 41
	PIDED1	F20	PIDE_D1_R 41
	PIDED2	F18	PIDE_D2_R 41
	PIDED3	F16	PIDE_D3_R 41
	PIDED4	E19	PIDE_D4_R 41
	PIDED5	D20	PIDE_D5_R 41
	PIDED6	D18	PIDE_D6_R 41
	PIDED7	B20	PIDE_D7_R 41
	PIDED8	C20	PIDE_D8_R 41
	PIDED9	D19	PIDE_D9_R 41
	PIDED10	E18	PIDE_D10_R 41
	PIDED11	E20	PIDE_D11_R 41
	PIDED12	F17	PIDE_D12_R 41
	PIDED13	F19	PIDE_D13_R 41
	PIDED14	G16	PIDE_D14_R 41
	PIDED15	G18	PIDE_D15_R 41
	PIDEA0	H20	PIDE_A0_R 41
	PIDEA1	H19	PIDE_A1_R 41
	PIDEA2	J16	PIDE_A2_R 41
	SIRQI	N16	PIDE_INTRQ_R
	PIDEDRQ	G19	PIDE_DMARQ_R 41
	PIDEDAKJ	H18	PIDE_DMACK_N_R 41
	PIDERDY	H17	PIDE_IORDY_R 41
	PIDEIORJ	H16	PIDE_DIOR_N_R 41
	PIDEIOWJ	G20	PIDE_DIOW_N_R 41
	PIDECS1J	J17	PIDE_CS1_N_R 41
	PIDECS3J	J18	PIDE_CS3_N_R 41
	CBLID_P	D11	PIDE_PDIAG_N_R 41
	SIDED0	A17	SIDE_D0_R
	SIDED1	D16	SIDE_D1_R 41
	SIDED2	B16	SIDE_D2_R 41
	SIDED3	E15	SIDE_D3_R 41
	SIDED4	C15	SIDE_D4_R 41
	SIDED5	A15	SIDE_D5_R 41
	SIDED6	D14	SIDE_D6_R 41
	SIDED7	E13	SIDE_D7_R 41
	SIDED8	D13	SIDE_D8_R 41
	SIDED9	E14	SIDE_D9_R 41
	SIDED10	B15	SIDE_D10_R 41
	SIDED11	D15	SIDE_D11_R 41
	SIDED12	A16	SIDE_D12_R 41
	SIDED13	C16	SIDE_D13_R 41
	SIDED14	E16	SIDE_D14_R 41
	SIDED15	B17	SIDE_D15_R 41
	SIDEA0	A19	SIDE_A0_R
	SIDEA1	C18	SIDE_A1_R 41
	SIDEA2	B19	SIDE_A2_R 41
	SIRQII	P16	SIDE_INTRQ_R
	SIDEDRQ	C17	SIDE_DMARQ_R 41
	SIDEDAKJ	B18	SIDE_DMACK_N_R 41
	SIDERDY	A18	SIDE_IORDY_R 41
	SIDEIORJ	E17	SIDE_DIOR_N_R 41
	SIDEIOWJ	D17	SIDE_DIOW_N_R 41
	SIDECS1J	C19	SIDE_CS1_N_R 41
	SIDECS3J	A20	SIDE_CS3_N_R 41
	CBLID_S	E11	SIDE_PDIAG_N_R 41
GROUP F VCC=3.3V	VCC_F1	G15	VCC3V3
	VCC_F2	K16	VCC3V3

VCC5V

34,47 — KBINH — R202 4.75K

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 2-3

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	20 of 72	Drawn By	SS

M1535D+

U15 M1535DPLUS BGA352-50M

SOUTH BRIDGE 4/5

POWER MANAGEMENT UNIT1

RSM_RSTJ	W10	RSM_RSTJ	
SUSPENDJ	W13	NC	
PWRBTNJ	Y15	UNUSED_PU33V_5	
SLPBTNJ	V10	UNUSED_PU33V_6	
OFF_PWR0	V14	NC	
OFF_PWR1	W14	NC	
OFF_PWR2	Y14	NC	
SPLED	Y13	SPLED	
RSM_ENT0	W11	RSM_ENT0	
RSM_ENT1	Y11	UNUSED_PU5V_3	
RSM_ENT8	Y10	UNUSED_PD_5	
PMEJ	W12	UNUSED_PU33V_7	
RI	V11	UNUSED_PD_6	
IRQ8J	Y12	UNUSED_PU5V_4	
RSM_ENT3	T9	UNUSED_PD_7	

POWER MANAGEMENT UNIT2

SMIJ	A13	NC	
STPCLKJ	B14	NC	
SLEEPJ	D12	NC	
ZZ	E12	UNUSED_PU5V_5	37
NUINP1	A11	UNUSED_PD_8	37
CPU_STPJ	C10	NC	
THRMJ	T18	IIC_THERM_N	6,45
SQWO	V6	SQWO	36
SMBCLK	T7	SMB_SCL	35
SMBDATA	U7	SMB_SDA	35
SMBALERTJ	T2	IIC_ALERT_N	6,45
GPI25	E9	GPI_25	42
GPO34	P18	GPO_34	36,42
GPO35	P19	GPO_35	36,42

AC97 INTERFACE

ACRESETJ	Y9	AC_RESET_N	43
ACSDATA_IN0	W9	AC_SDATA_IN0	43
ACSDATA_IN1	Y8	UNUSED_PD_9	37
ACSDATA_OUT	U1	AC_SDATA_OUT	43
ACSYNC	P4	AC_SYNC	43
ACBIT_CLK	P5	AC_BIT_CLK	43
ACMIDI_TXD	R4	NC	
ACMIDI_RXD	T4	UNUSED_PD_10	37

SOUND CNTRL

ACGAME0	V1	NC	
ACGAME1	V2	NC	
ACGAME2	V3	NC	
ACGAME3	W1	NC	
ACGAME4	W2	NC	
ACGAME5	W3	NC	
ACGAME6	Y1	NC	
ACGAME7	Y2	NC	
ACGP_UPJ	U3	UNUSED_PU5V_7	37
ACGP_MUTEJ	U2	UNUSED_PU5V_8	37
ACGP_DOWNJ	R5	UNUSED_PU5V_9	37
FANOUT1	W5	NC	
FANOUT2	V5	NC	
FANIN2	Y5	UNUSED_PU5V_6	37
SPDIF_OUT	D9	NC	
SPDIF_IN	U4	UNUSED_PU5V_10	37

M1535D+

U15 M1535DPLUS BGA352-50M

SOUTH BRIDGE 5/5

XD(ISA) BUS

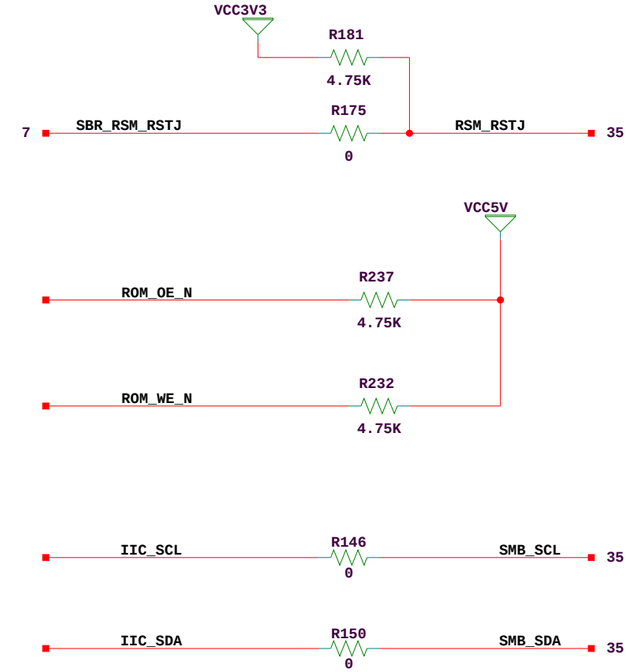
XD0	U20	ROM_D0	42
XD1	U19	ROM_D1	42
XD2	U18	ROM_D2	42
XD3	Y20	ROM_D3	42
XD4	W20	ROM_D4	42
XD5	V20	ROM_D5	42
XD6	Y19	ROM_D6	42
XD7	W19	ROM_D7	42
SA0	V19	ROM_A0	42
SA1	Y18	ROM_A1	42
SA2	W18	ROM_A2	42
SA3	V18	ROM_A3	42
SA4	Y17	ROM_A4	42
SA5	W17	ROM_A5	42
SA6	V17	ROM_A6	42
SA7	U17	ROM_A7	42
SA8	T17	ROM_A8	42
SA9	R17	ROM_A9	42
SA10	Y16	ROM_A10	42
SA11	W16	ROM_A11	42
SA12	V16	ROM_A12	42
SA13	U16	ROM_A13	42
SA14	T16	ROM_A14	42
SA15	W15	ROM_A15	42
BIOSA16	V15	ROM_A16	42
BIOSA17	U15	ROM_A17	42
BIOSA18	T15	ROM_A18	42
MEMRJ	T14	ROM_OE_N	35,42
MEMWJ	U14	ROM_WE_N	35,42
IORJ	T13	NC	
IOWJ	U13	NC	

FLOPPY DISK

RDATAJ	M18	UNUSED_PU5V_11	37
WGATEJ	L19	NC	
WDATAJ	L18	NC	
HDSELJ	M19	NC	
FD_DIRJ	L16	NC	
STEPJ	L17	NC	
DSKCHGJ	M20	UNUSED_PU5V_12	37
DRV0J	K19	NC	
DRV1J	K20	NC	
MOT0J	K17	NC	
MOT1J	K18	NC	
WPROTJ	M16	UNUSED_PU5V_13	37
TRK0J	L20	UNUSED_PU5V_14	37
INDEXJ	J20	UNUSED_PU5V_15	37
DENSEL	J19	NC	

MISCELLANEOUS LOGIC

SPKR	T19	SPKR	43,47
RTCAS	R20	NC	
RTCRW	R19	NC	
RTCDS	R18	NC	
ROMKBCSJ	T20	ROMKBCSJ	36,42
IRQSER	N19	UNUSED_PU5V_16	37
GPI24	M17	GPI_24	42
GPO29	N17	GPO_29	36,42
GPO30	N18	GPO_30	36,42
PCSOJ	P20	PCS0J	36
PCS1J	R16	PCS1J	36
RUN_ENT0	Y3	GPIO_0	42
RUN_ENT1	V4	GPIO_1	42
RUN_ENT2	W4	GPIO_2	42
RUN_ENT3	Y4	GPIO_3	42
GPO10	T3	GPO_10	42
LFRAMEJ	N20	UNUSED_PU5V_17	37
LDRQJ	P17	UNUSED_PU5V_18	37



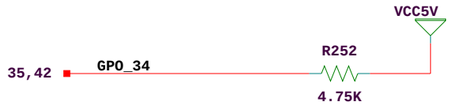
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

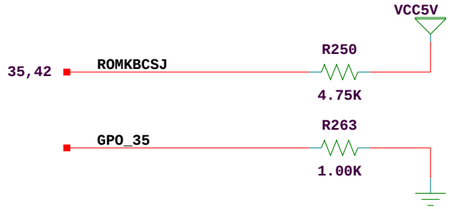
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 4-5

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	21 of 72	Drawn By	SS

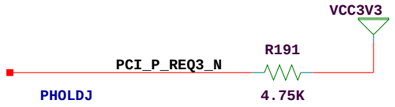


RESERVED/PULLED HIGH FOR NORMAL OPERATION



FLASH ROM FUNCTION MODE SELECT

DISABLED



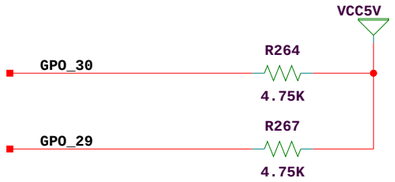
RESERVED/PULLED HIGH FOR NORMAL OPERATION

4MBIT FLASH ROM LINEAR MODE

ENABLED

SWITCH GPI24/IOCHRDY AND GPO30/AEN FUNCTIONS

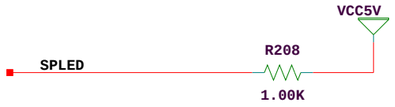
GPI24 AND GPO30 ENABLED



RESERVED/PULLED HIGH FOR NORMAL OPERATION

CPU SUPPORT SELECT

PENTIUM-II MODE

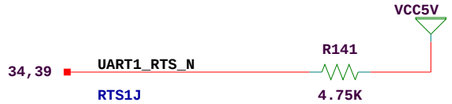


AT/ATX MODE SELECT

AT MODE

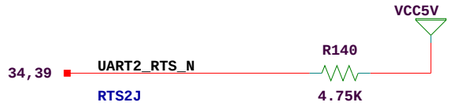
NOTE: AT MODE IS USED HERE TO DISABLE THE SOFT-POWER FUNCTIONALITY OF THE SOUTH BRIDGE

PULLED DOWN FOR NORMAL OPERATION



SIO BASE ADDRESS CONFIGURATION

BASE ADDR = 0x3F0

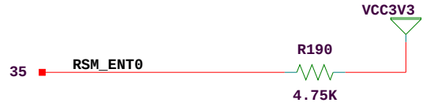


INTERNAL KEYBOARD CONTROLLER ENABLE

ENABLED

KEYBOARD CONTROLLER MODE SELECT

PS/2 MODE



POWER CONTROL ACTIVE LEVEL SELECT

ACTIVE HIGH

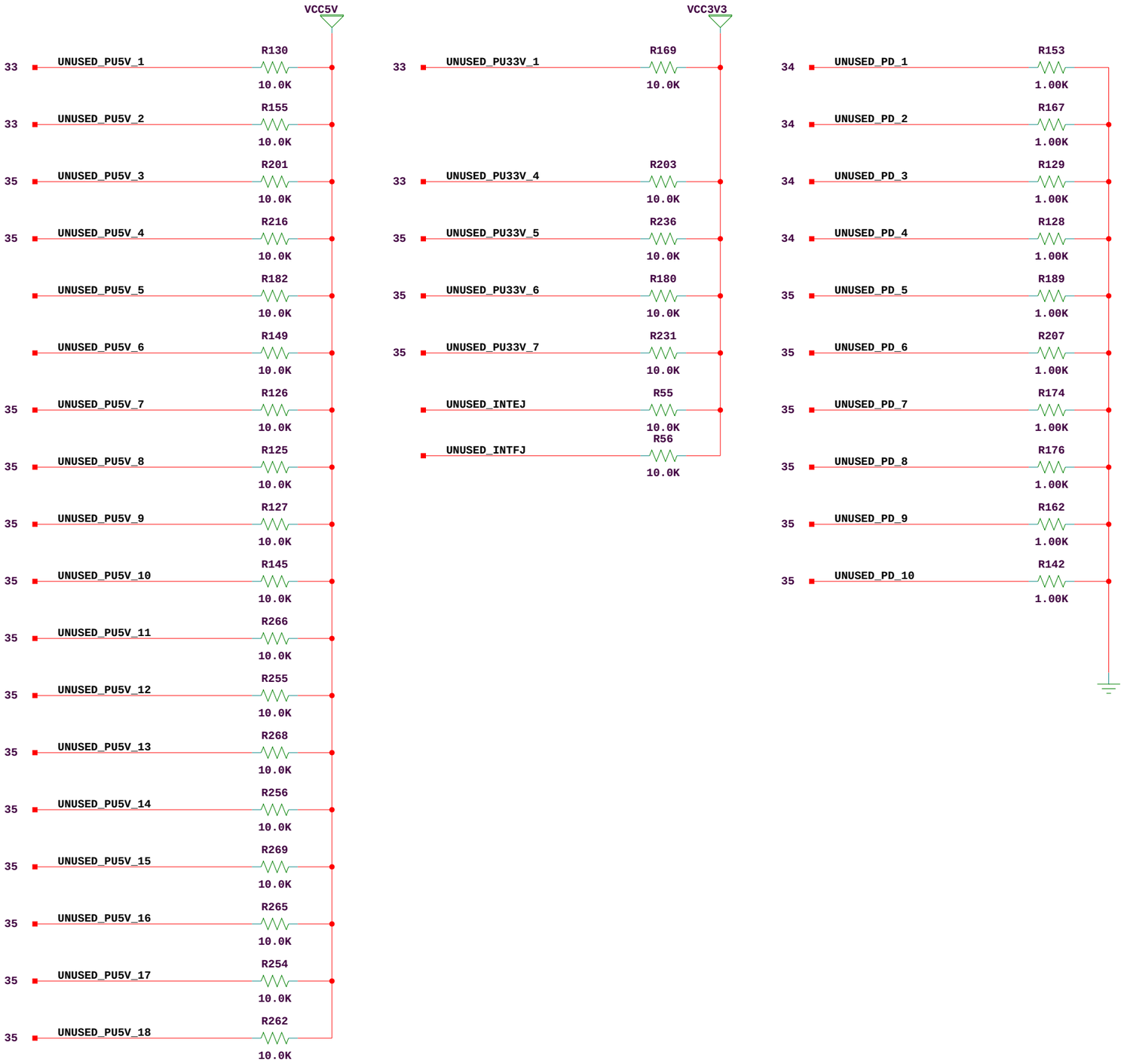
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SOUTH BRIDGE, CONFIG RESISTORS

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	22 of 72	Drawn By	SS

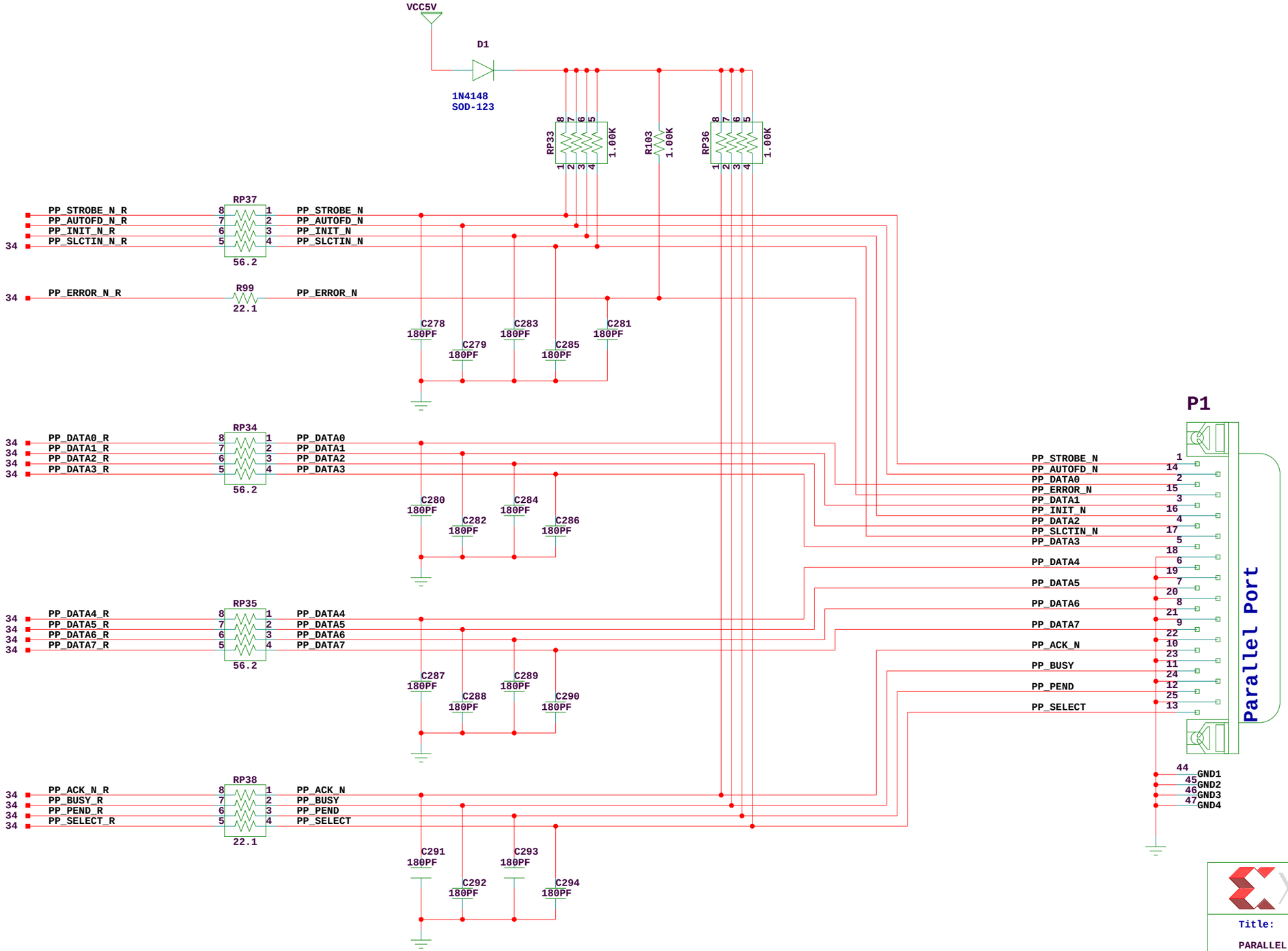


XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
PCI SOUTH BRIDGE, UNUSED PIN RESISTORS

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	23 of 72	Drawn By	SS

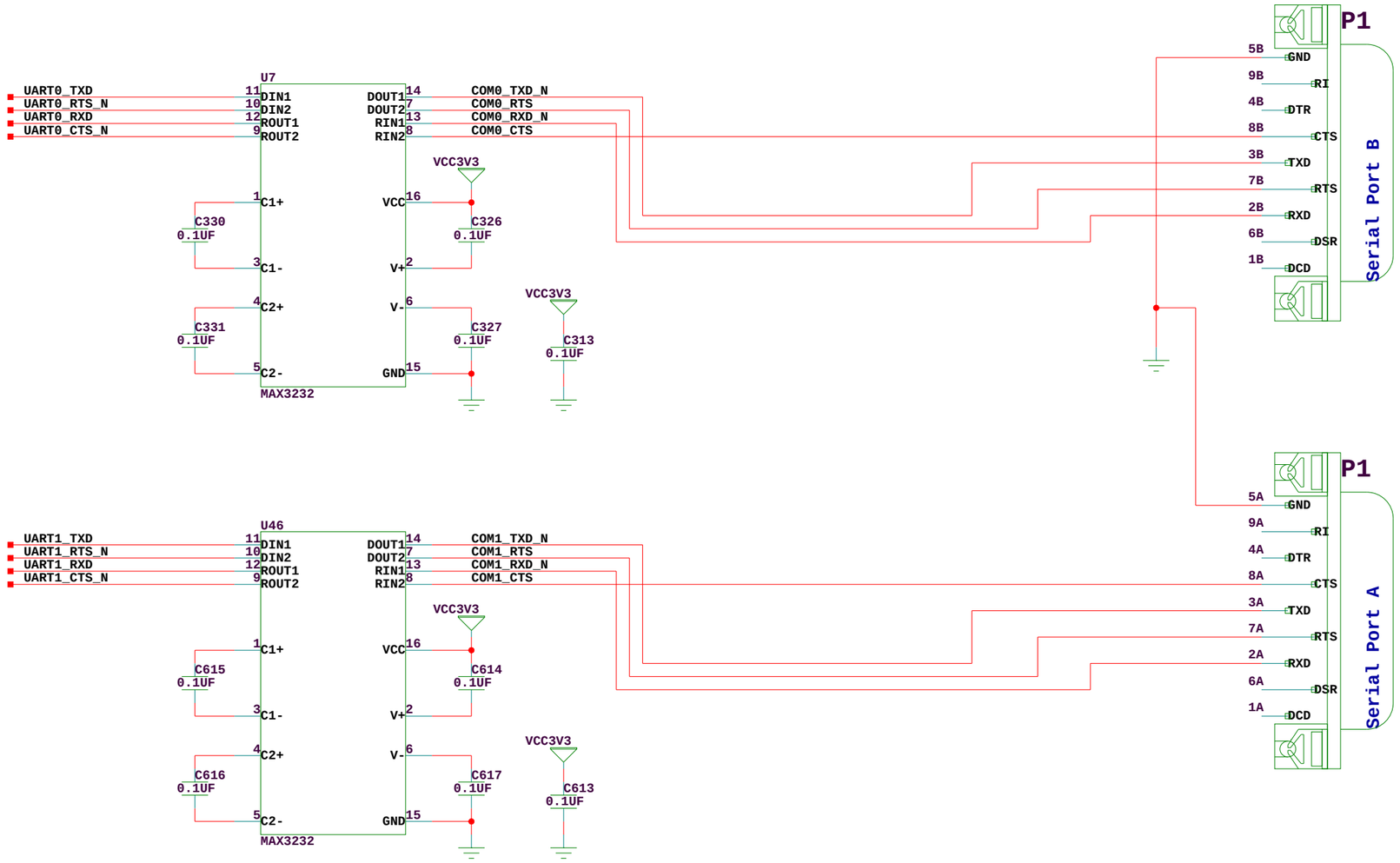


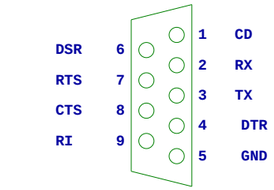
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PARALLEL PORT INTERFACE

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet 24 of 72		Drawn By	SS





LOOKING INTO DB9 PLUG

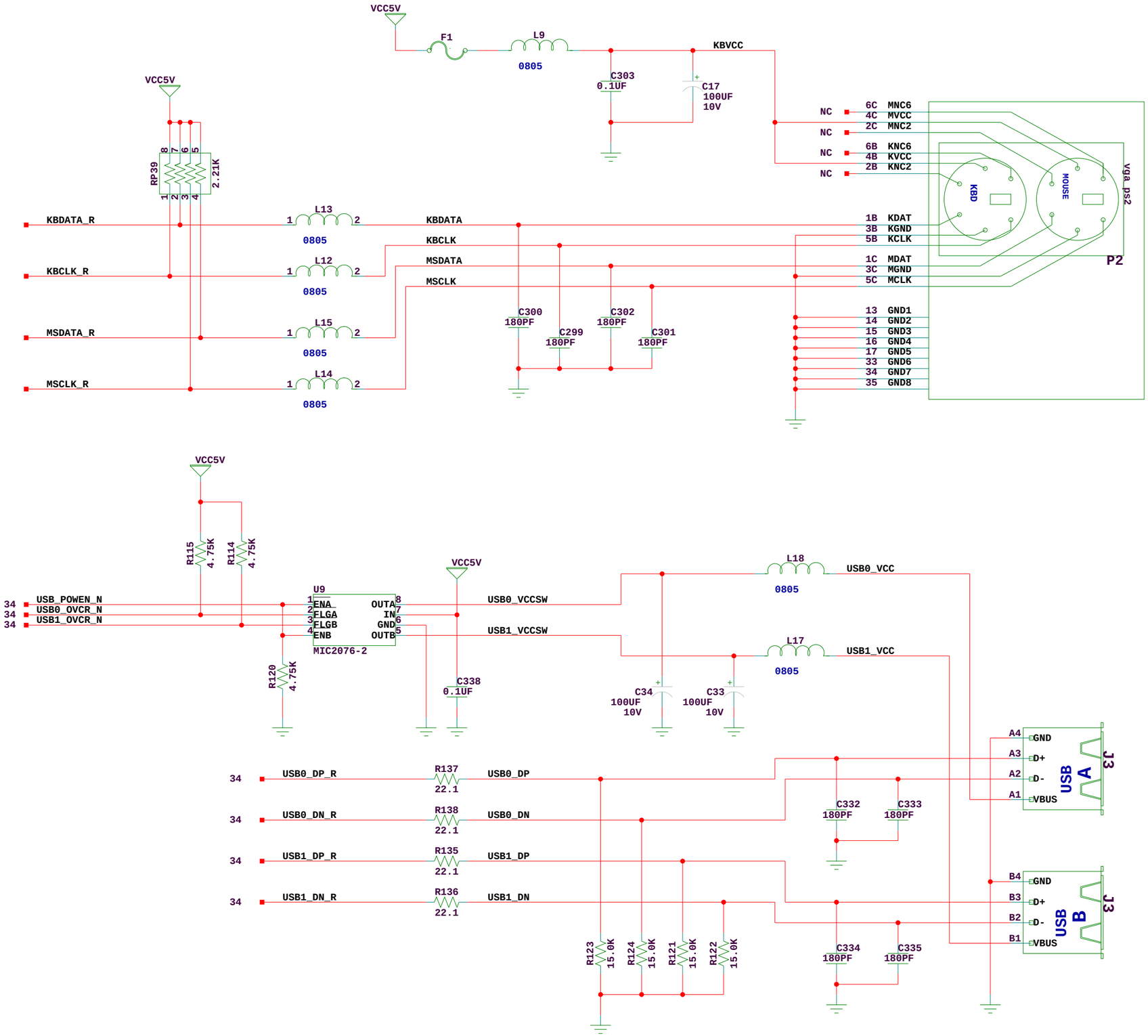
RS232 DTE PINOUT
CONNECTS TO PC WITH
F/F NULL MODEM CABLE.

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
RS232 SERIAL PORT INTERFACE

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	25 of 72	Drawn By	SS



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
KBD/MOUSE AND USB INTERFACES

Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	26 of 72	Drawn By	SS

Pin 20 must be removed.
Silkscreen:
"IDE PRIMARY"

RP51
34 PIDE_D7_R 8 1 PIDE_D7 41
34 PIDE_D8_R 7 2 PIDE_D8 41
34 PIDE_D6_R 6 3 PIDE_D6 41
34 PIDE_D9_R 5 4 PIDE_D9 41
47.5

RP50
34 PIDE_D5_R 8 1 PIDE_D5 41
34 PIDE_D10_R 7 2 PIDE_D10 41
34 PIDE_D4_R 6 3 PIDE_D4 41
34 PIDE_D11_R 5 4 PIDE_D11 41
47.5

RP49
PIDE_D3_R 8 1 PIDE_D3 41
PIDE_D12_R 7 2 PIDE_D12 41
PIDE_D2_R 6 3 PIDE_D2 41
PIDE_D13_R 5 4 PIDE_D13 41
47.5

RP48
PIDE_D1_R 8 1 PIDE_D1 41
PIDE_D14_R 7 2 PIDE_D14 41
PIDE_D0_R 6 3 PIDE_D0 41
PIDE_D15_R 5 4 PIDE_D15 41
47.5

34 PIDE_DMARQ_R 1 R303 2 PIDE_DMARQ 41
82.0

RP47
34 PIDE_DIOW_N_R 8 1 PIDE_DIOW_N 41
34 PIDE_DIOR_N_R 7 2 PIDE_DIOR_N 41
34 PIDE_IORDY_R 6 3 PIDE_IORDY 41
34 PIDE_DMACK_N_R 5 4 PIDE_DMACK_N 41
33.2

34 PIDE_INTRQ_R 1 R301 2 PIDE_INTRQ 41
82.0

RP46
34 PIDE_A1_R 8 1 PIDE_A1 41
34 PIDE_A0_R 7 2 PIDE_A0 41
34 PIDE_A2_R 6 3 PIDE_A2 41
34 PIDE_CS1_N_R 5 4 PIDE_CS1_N 41
33.2

34 PIDE_CS3_N_R R302 PIDE_CS3_N 41
33.2

34 PIDE_PDIAG_N_R R304 PIDE_PDIAG_N 41
0

VCC3V3
41 PIDE_IORDY R311 10.0K
41 PIDE_INTRQ R306 4.75K
41 PIDE_D7 R313 10.0K
41 PIDE_DMARQ R309 5.62K
41 PIDE_CSEL R299 475
41 PIDE_PDIAG_N R314 100K
C425
0.047UF

Mark Pin 1
Pin20=Key
J16

41 PIDE_RESET_N 1
2
41 PIDE_D7 3
41 PIDE_D8 4
41 PIDE_D6 5
41 PIDE_D9 6
41 PIDE_D5 7
41 PIDE_D10 8
41 PIDE_D4 9
41 PIDE_D11 10
41 PIDE_D3 11
41 PIDE_D12 12
41 PIDE_D2 13
41 PIDE_D13 14
41 PIDE_D1 15
41 PIDE_D14 16
41 PIDE_D0 17
41 PIDE_D15 18
19
NC 20
41 PIDE_DMARQ 21
22
41 PIDE_DIOW_N 23
24
41 PIDE_DIOR_N 25
26
41 PIDE_IORDY 27
41 PIDE_CSEL 28
41 PIDE_DMACK_N 29
30
41 PIDE_INTRQ 31
NC 32
41 PIDE_A1 33
41 PIDE_PDIAG_N 34
41 PIDE_A0 35
41 PIDE_A2 36
41 PIDE_CS1_N 37
41 PIDE_CS3_N 38
41,47 PIDE_DASP_N 39
40
CON_IDE40

IDE PRIMARY CONN

VCC3V3
R390 182
GREEN
DS22
41,47 PIDE_DASP_N

Silkscreen:
"IDE P LED"

7,41 SBR_IDE_RST_N R288 0 SIDE_RESET_N 41
7,41 SBR_IDE_RST_N R300 0 PIDE_RESET_N 41

Pin 20 must be removed.
Silkscreen:
"IDE SECONDARY"

RP40
34 SIDE_D7_R 8 1 SIDE_D7 41
34 SIDE_D8_R 7 2 SIDE_D8 41
34 SIDE_D6_R 6 3 SIDE_D6 41
34 SIDE_D9_R 5 4 SIDE_D9 41
47.5

RP41
34 SIDE_D5_R 8 1 SIDE_D5 41
34 SIDE_D10_R 7 2 SIDE_D10 41
34 SIDE_D4_R 6 3 SIDE_D4 41
34 SIDE_D11_R 5 4 SIDE_D11 41
47.5

RP42
34 SIDE_D3_R 8 1 SIDE_D3 41
34 SIDE_D12_R 7 2 SIDE_D12 41
34 SIDE_D2_R 6 3 SIDE_D2 41
34 SIDE_D13_R 5 4 SIDE_D13 41
47.5

RP44
34 SIDE_D1_R 8 1 SIDE_D1 41
34 SIDE_D14_R 7 2 SIDE_D14 41
34 SIDE_D0_R 6 3 SIDE_D0 41
34 SIDE_D15_R 5 4 SIDE_D15 41
47.5

34 SIDE_DMARQ_R 1 R291 2 SIDE_DMARQ 41
82.0

RP43
34 SIDE_DIOW_N_R 8 1 SIDE_DIOW_N 41
34 SIDE_DIOR_N_R 7 2 SIDE_DIOR_N 41
34 SIDE_IORDY_R 6 3 SIDE_IORDY 41
34 SIDE_DMACK_N_R 5 4 SIDE_DMACK_N 41
33.2

34 SIDE_INTRQ_R 1 R289 2 SIDE_INTRQ 41
82.0

RP45
34 SIDE_A1_R 8 1 SIDE_A1 41
34 SIDE_A0_R 7 2 SIDE_A0 41
34 SIDE_A2_R 6 3 SIDE_A2 41
34 SIDE_CS1_N_R 5 4 SIDE_CS1_N 41
33.2

34 SIDE_CS3_N_R R292 SIDE_CS3_N 41
33.2

34 SIDE_PDIAG_N_R R290 SIDE_PDIAG_N 41
0

VCC3V3
41 SIDE_IORDY R312 10.0K
41 SIDE_INTRQ R305 4.75K
41 SIDE_D7 R307 10.0K
41 SIDE_DMARQ R310 5.62K
41 SIDE_CSEL R287 475
41 SIDE_PDIAG_N R308 100K
C424
0.047UF

Mark Pin 1
Pin20=Key
J15

41 SIDE_RESET_N 1
2
41 SIDE_D7 3
41 SIDE_D8 4
41 SIDE_D6 5
41 SIDE_D9 6
41 SIDE_D5 7
41 SIDE_D10 8
41 SIDE_D4 9
41 SIDE_D11 10
41 SIDE_D3 11
41 SIDE_D12 12
41 SIDE_D2 13
41 SIDE_D13 14
41 SIDE_D1 15
41 SIDE_D14 16
41 SIDE_D0 17
41 SIDE_D15 18
19
NC 20
41 SIDE_DMARQ 21
22
41 SIDE_DIOW_N 23
24
41 SIDE_DIOR_N 25
26
41 SIDE_IORDY 27
41 SIDE_CSEL 28
41 SIDE_DMACK_N 29
30
41 SIDE_INTRQ 31
NC 32
41 SIDE_A1 33
41 SIDE_PDIAG_N 34
41 SIDE_A0 35
41 SIDE_A2 36
41 SIDE_CS1_N 37
41 SIDE_CS3_N 38
41,47 SIDE_DASP_N 39
40
CON_IDE40

IDE SECONDARY CONN

VCC3V3
R387 182
GREEN
DS21
SIDE_DASP_N

Silkscreen:
"IDE S LED"

XILINX

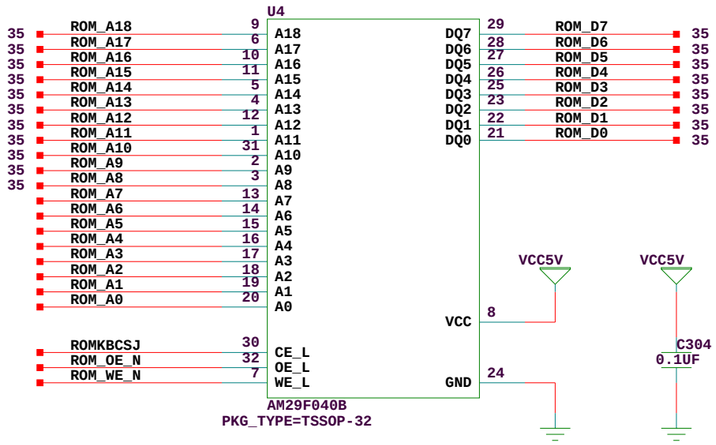
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

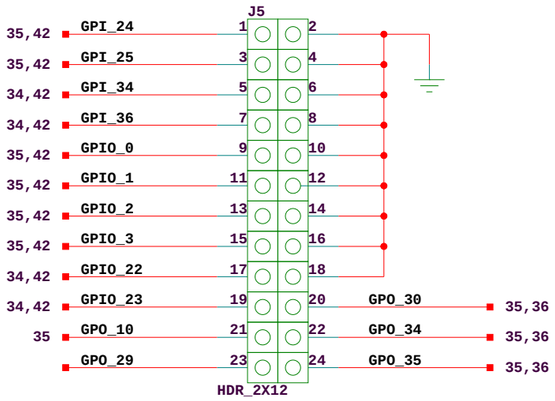
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
IDE INTERFACES

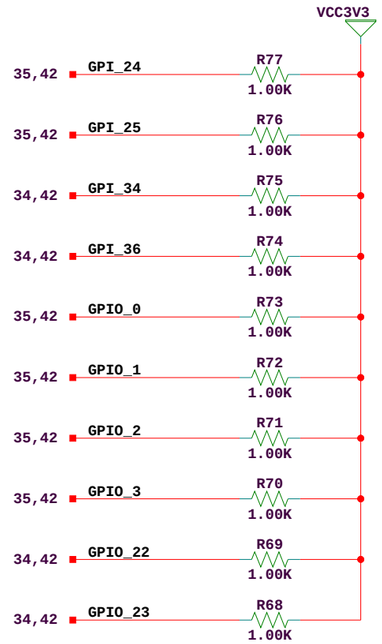
Date:	8-22-2006_9:53	Ver:	03
Sheet Size: B		Rev:	E
Sheet	27 of 72	Drawn By	SS

SOUTH BRIDGE

GPIO HEADER







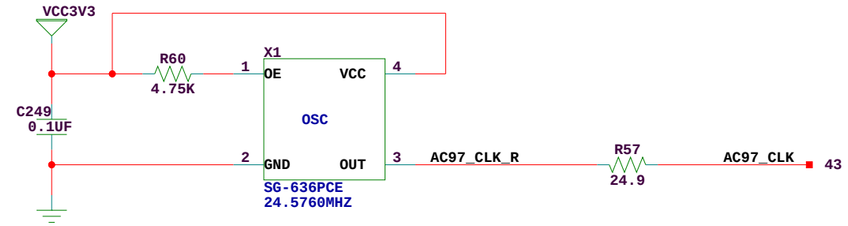
XILINX

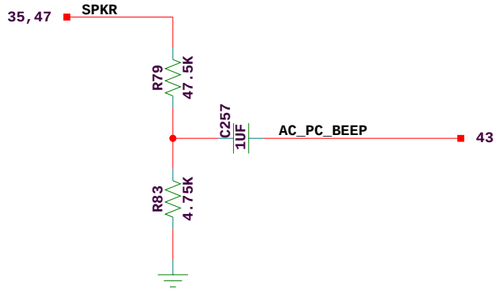
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

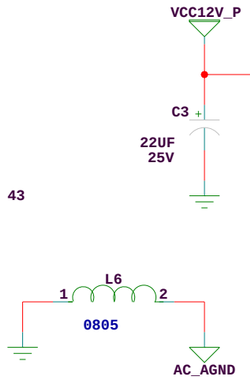
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

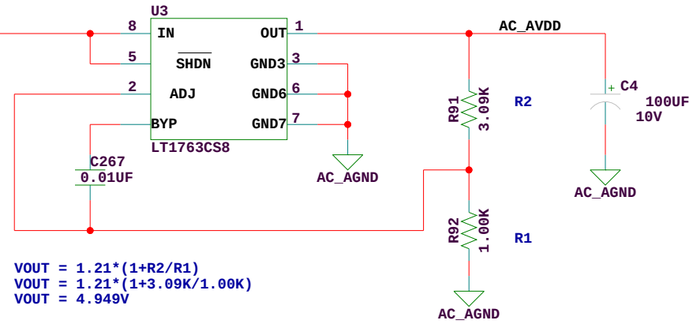
SOUTH BRIDGE ROM AND GPIO

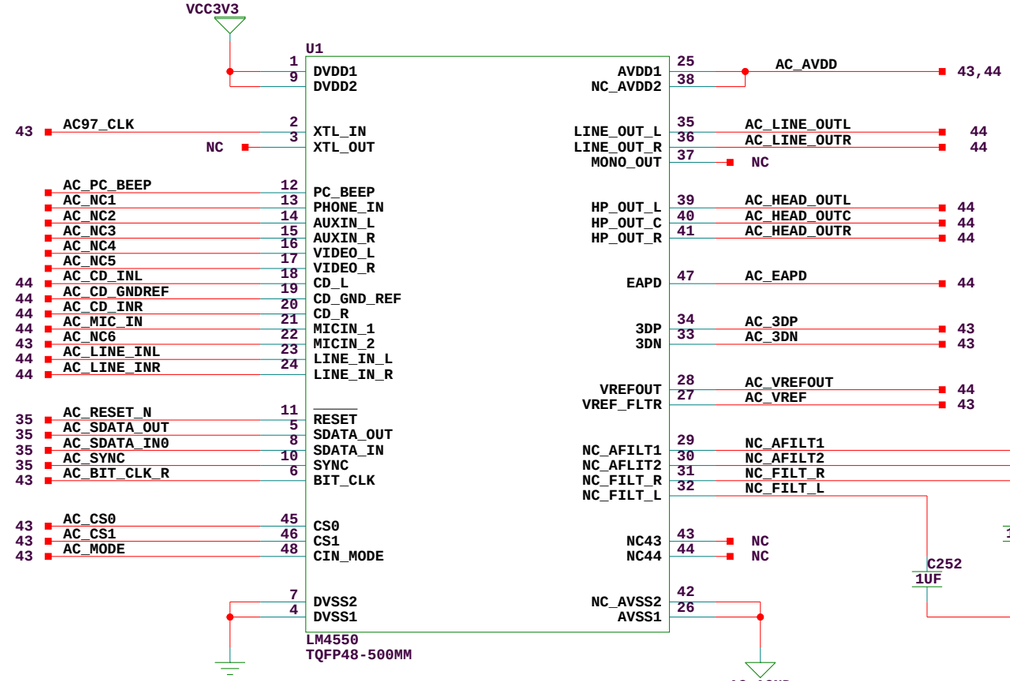
Date: 8-22-2006_9:53	Ver: 03
Sheet Size: B	Rev: E
Sheet 28 of 72	Drawn By SS

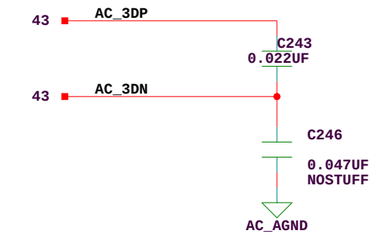


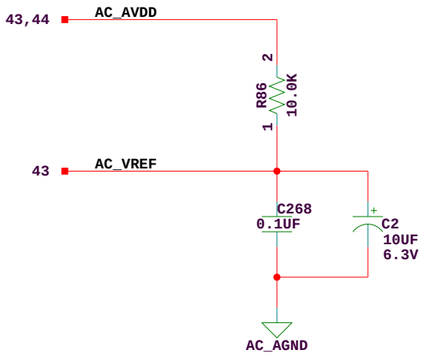


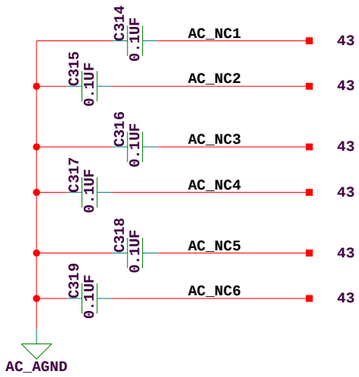


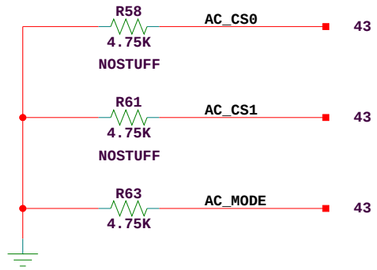


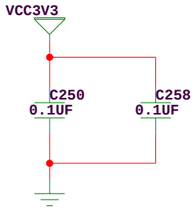


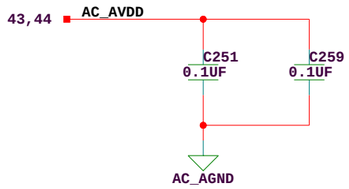












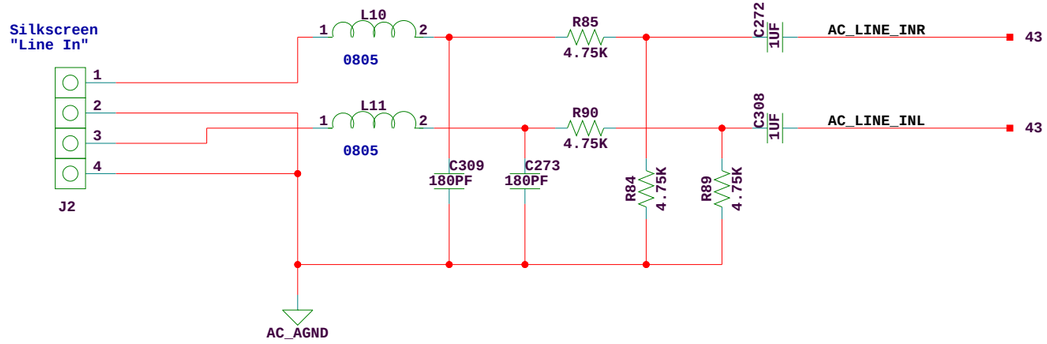
XILINX

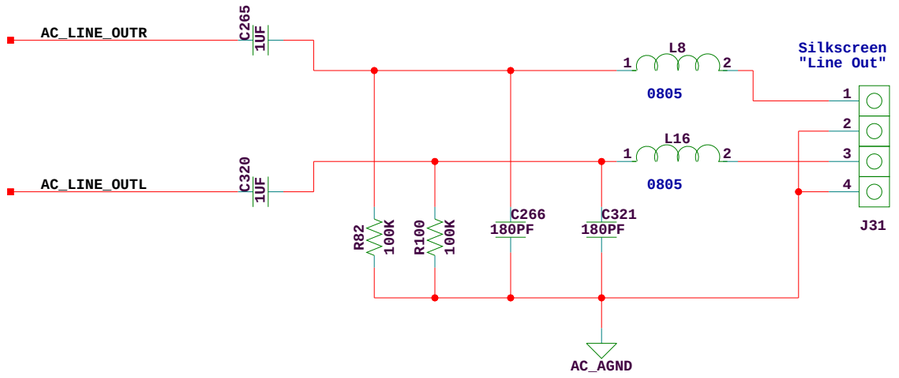
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

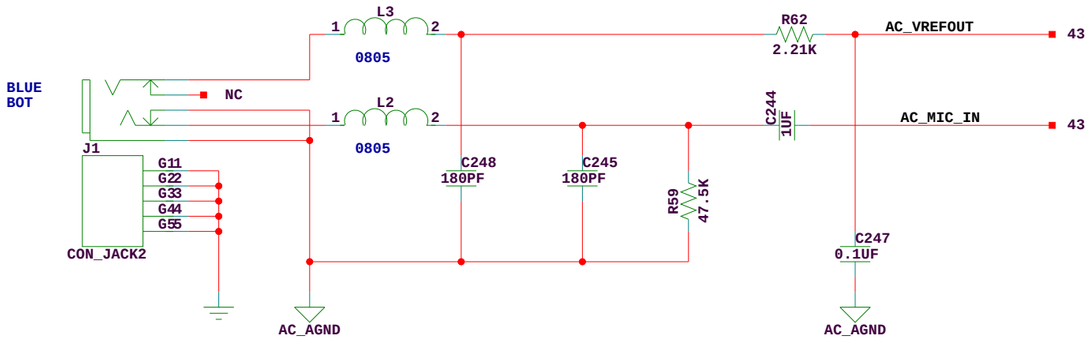
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

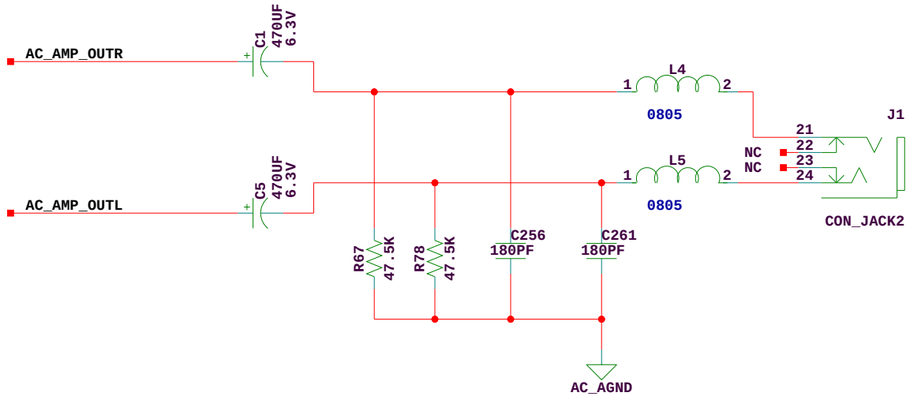
AC97 CODEC

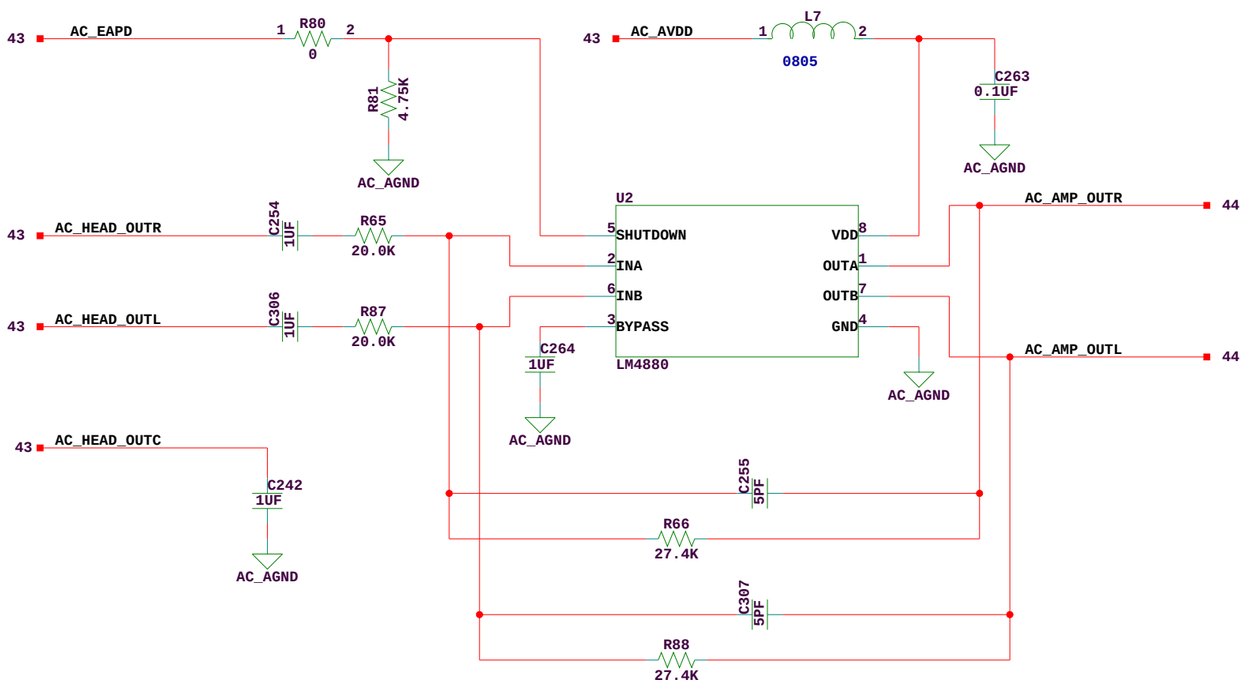
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	29 of 72	Drawn By	SS

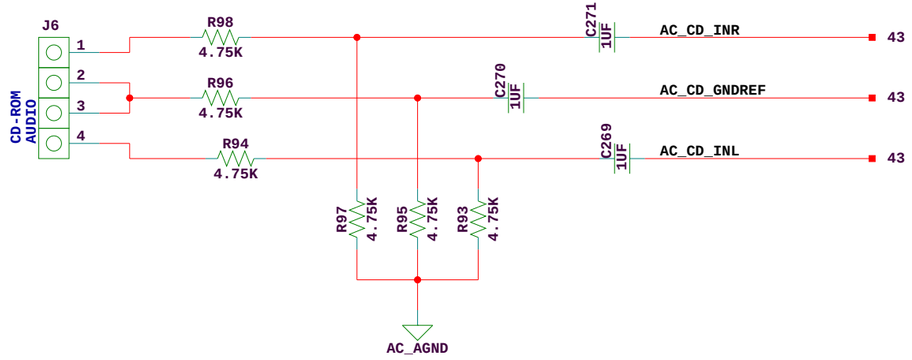












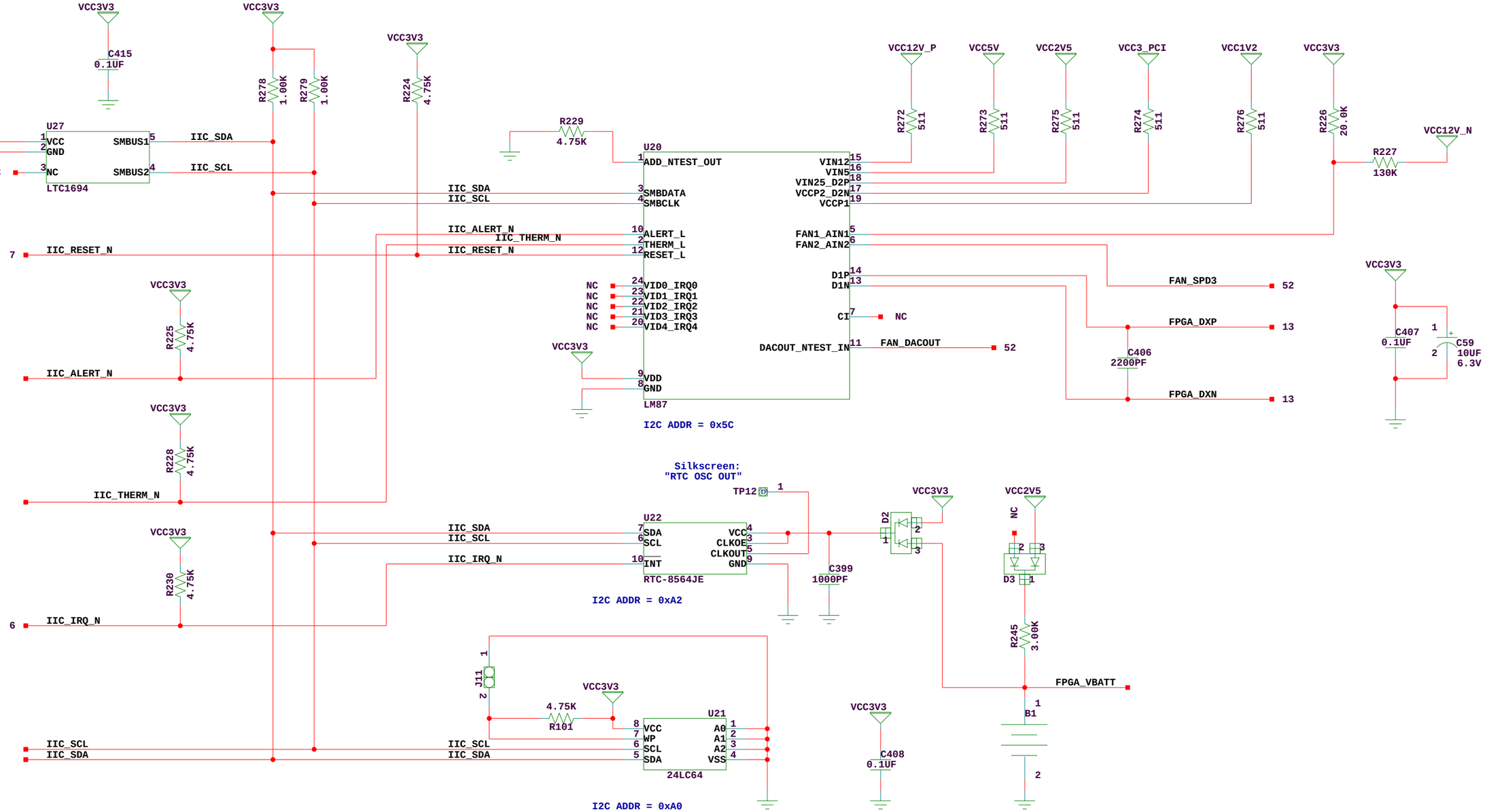
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

AC97 CONNECTORS

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	30 of 72	Drawn By	SS

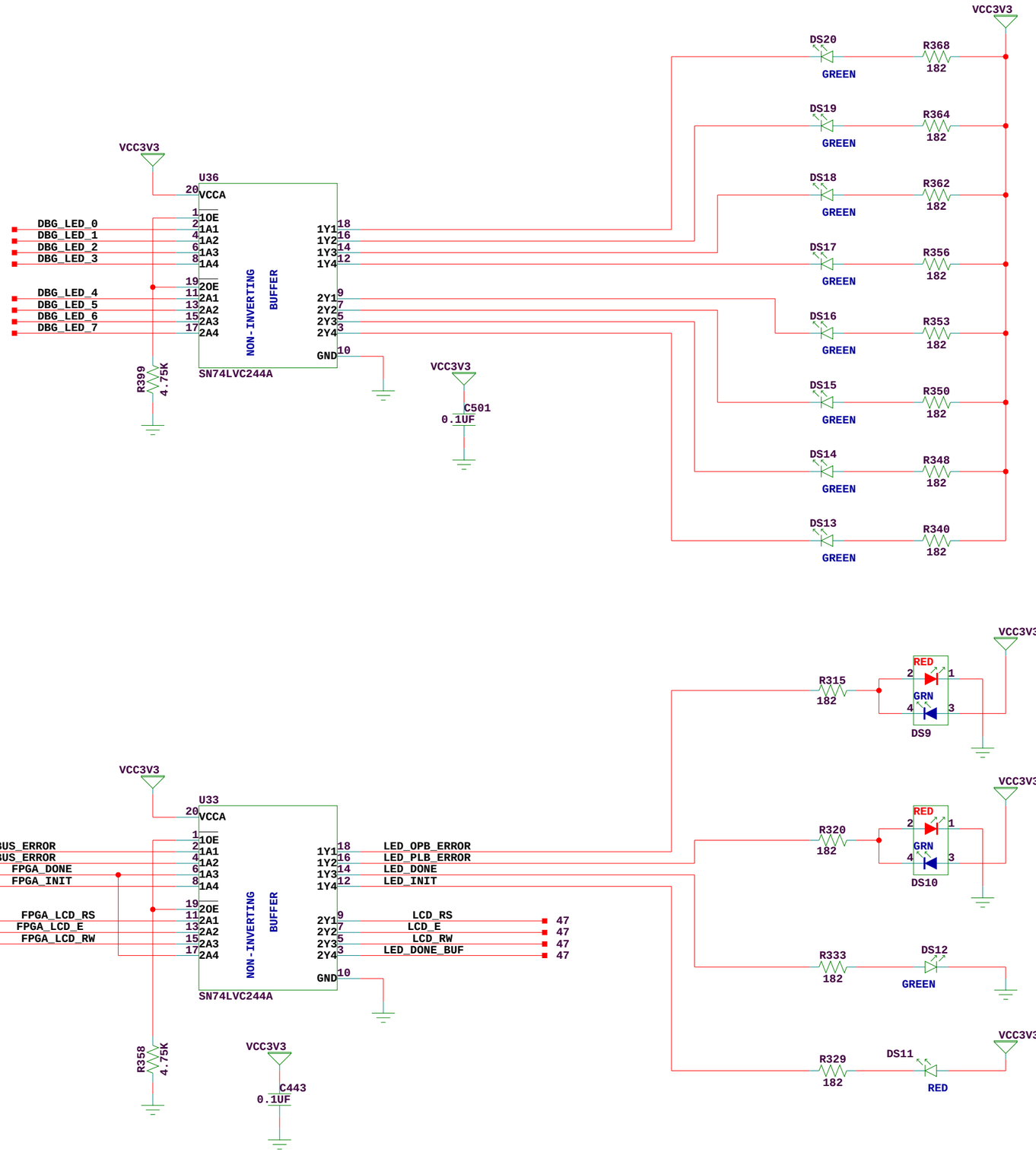


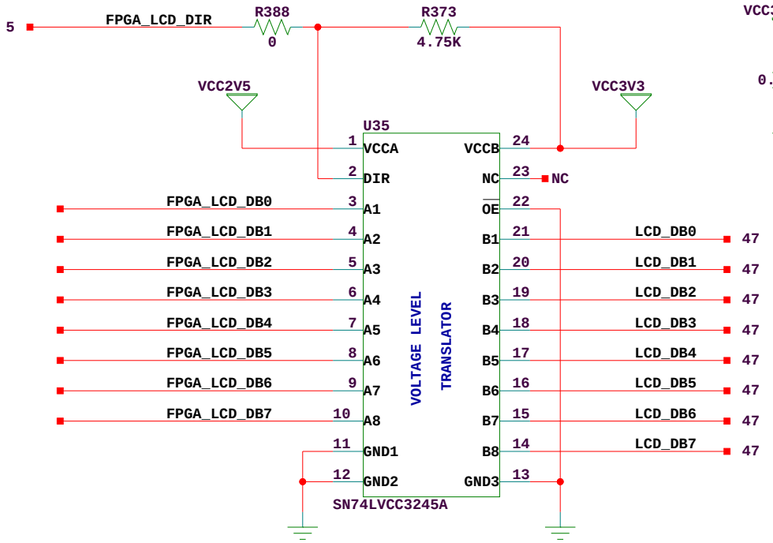
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

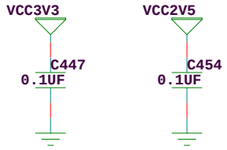
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

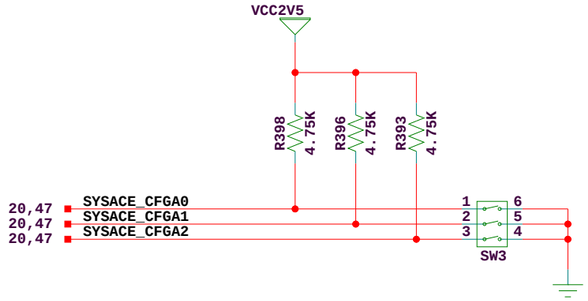
I2C AND SPI DEVICES

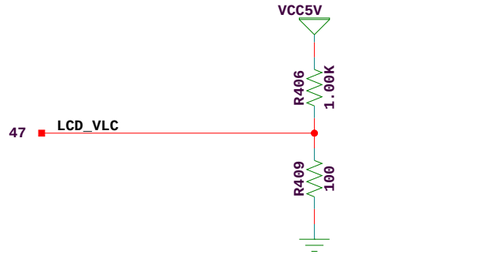
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	31 of 72	Drawn By	SS

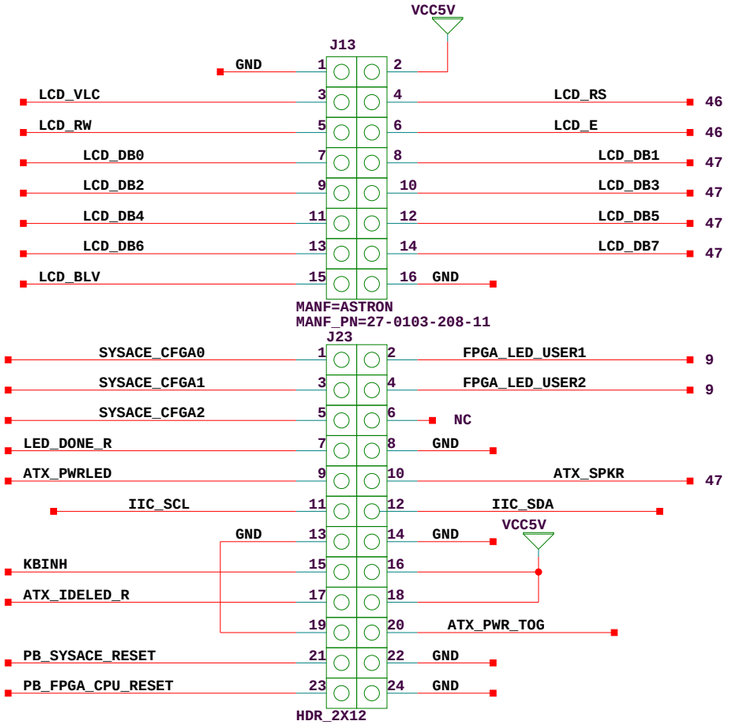

VCC3V3
U36
20 VCCA
1 1OE
2 1A1
4 1A2
6 1A3
8 1A4
19 2OE
11 2A1
13 2A2
15 2A3
17 2A4
NON-INVERTING BUFFER
SN74LVC244A
GND 10
1Y1 18
1Y2 16
1Y3 14
1Y4 12
2Y1 9
2Y2 7
2Y3 5
2Y4 3
DBG_LED_0
DBG_LED_1
DBG_LED_2
DBG_LED_3
DBG_LED_4
DBG_LED_5
DBG_LED_6
DBG_LED_7
R399 4.75K
C501 0.1UF
DS20 GREEN
DS19 GREEN
DS18 GREEN
DS17 GREEN
DS16 GREEN
DS15 GREEN
DS14 GREEN
DS13 GREEN
R368 182
R364 182
R362 182
R356 182
R353 182
R350 182
R348 182
R340 182
U33
OPB_BUS_ERROR
PLB_BUS_ERROR
FPGA_DONE
FPGA_INIT
FPGA_LCD_RS
FPGA_LCD_E
FPGA_LCD_RW
LED_OPB_ERROR
LED_PLB_ERROR
LED_DONE
LED_INIT
LCD_RS
LCD_E
LCD_RW
LED_DONE_BUF
47
R358 4.75K
C443 0.1UF
R315 182
DS9 RED GRN
R320 182
DS10 RED GRN
R333 182
DS12 GREEN
R329 182
DS11 RED
XILINX
SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
DEBUG AND STATUS LEDS
Date: 8-22-2006_9:52
Ver: 03
Sheet Size: B
Rev: E
Sheet 32 of 72
Drawn By SS

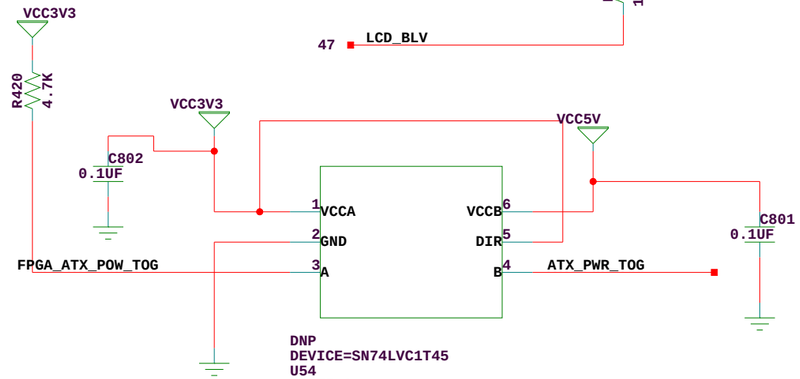


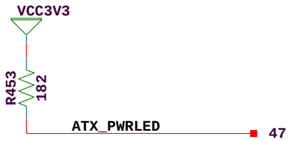


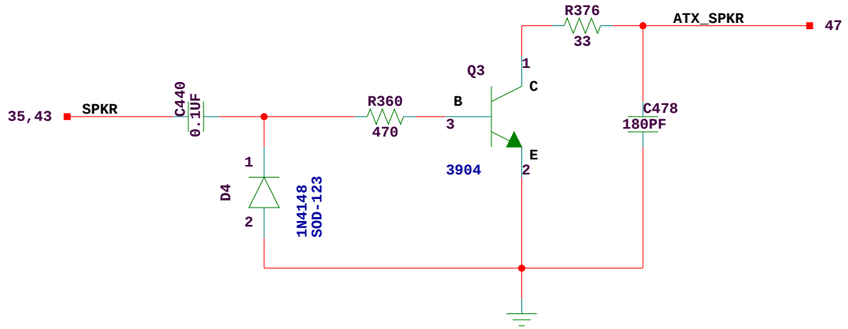


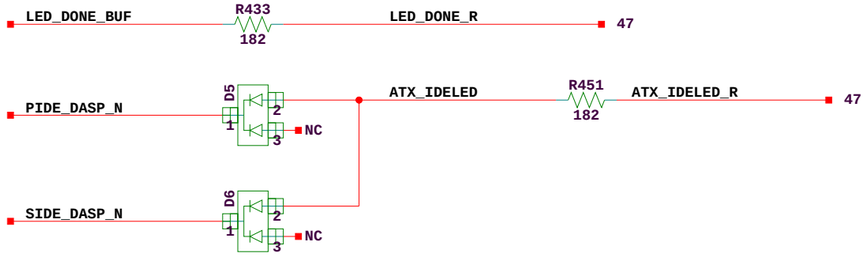


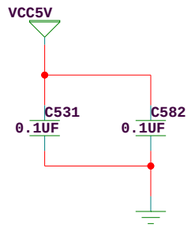












XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

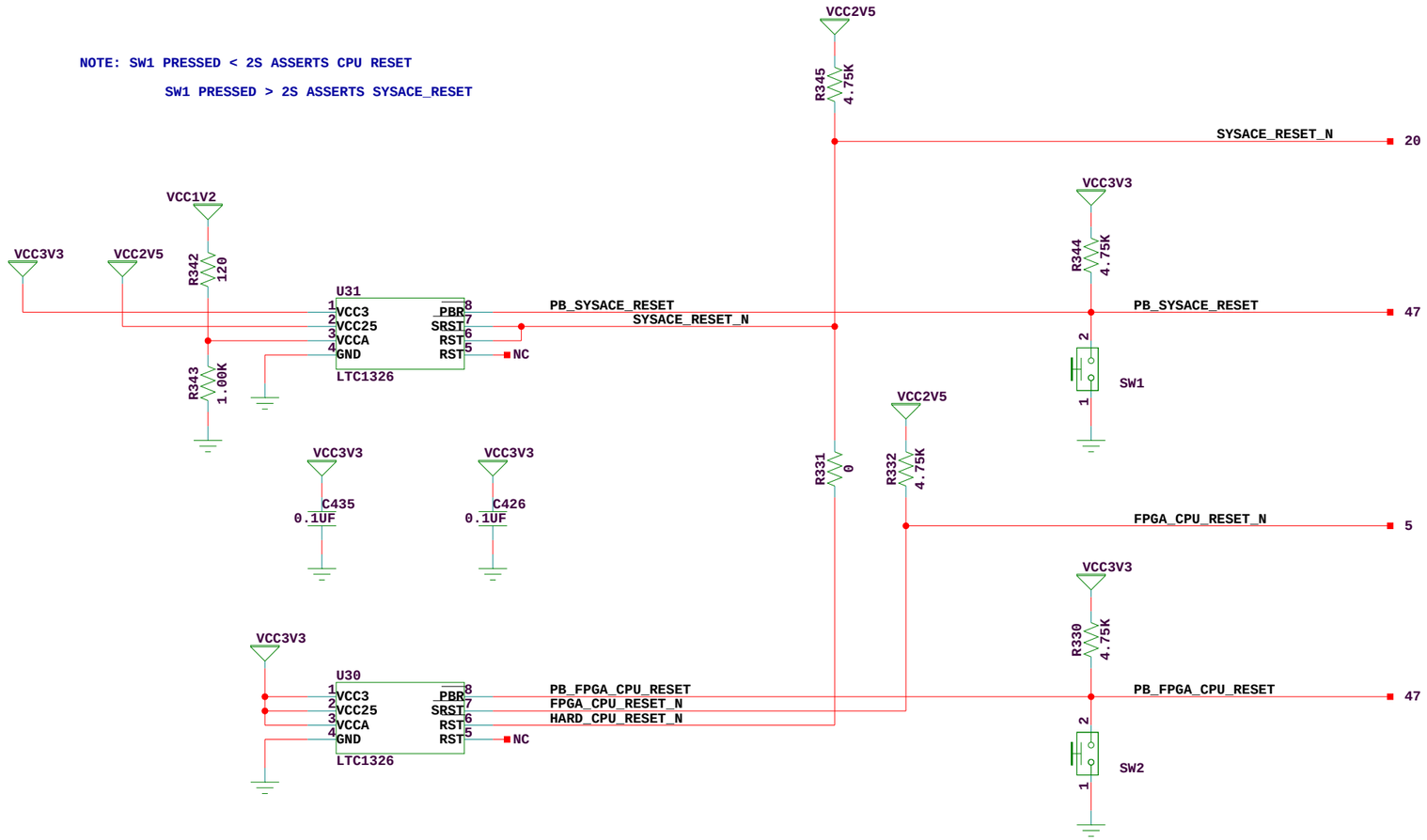
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

ATX AND FRONT PANEL CONNECTORS

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	33 of 72	Drawn By	SS

NOTE: SW1 PRESSED < 2S ASSERTS CPU RESET

SW1 PRESSED > 2S ASSERTS SYSACE_RESET



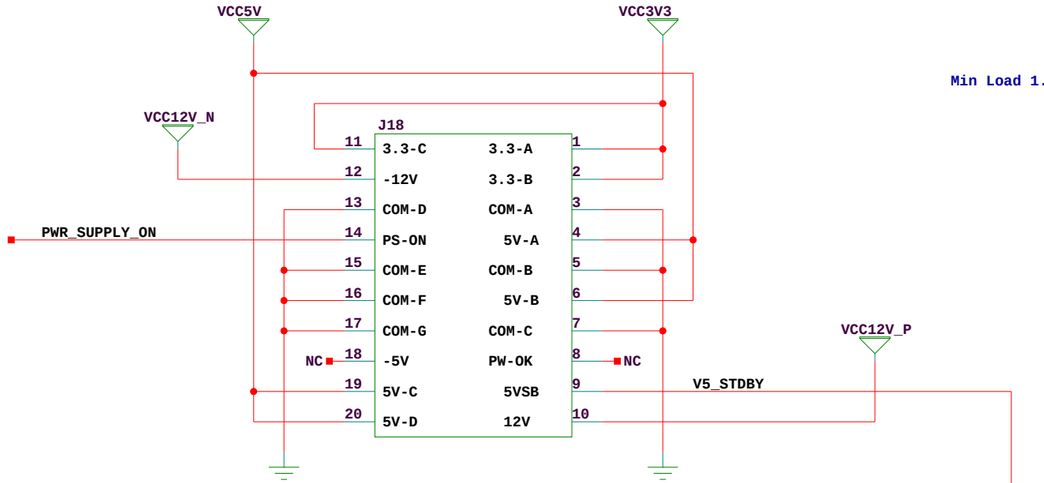
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

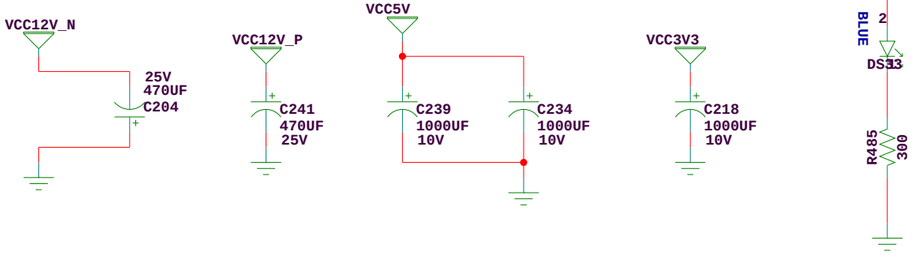
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

RESET SWITCHES

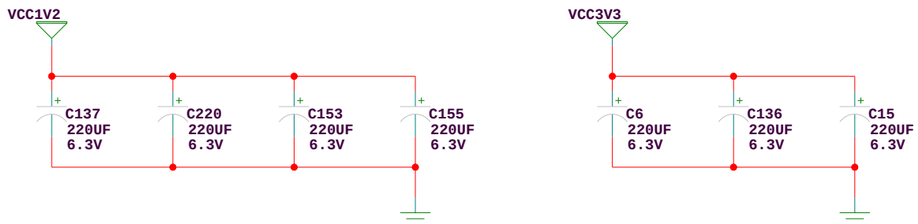
Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 34 of 72	Drawn By SS

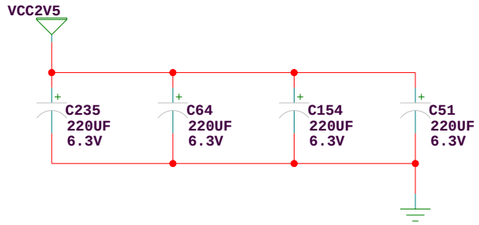
Min Load 1.5A on 5v, 0.8A on 3.3V and 0.5A on 12V

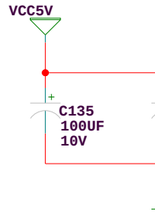


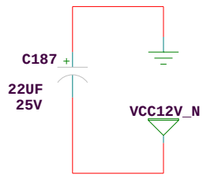


ATX Power Connector









BULK CAPS DISTRIBUTED AROUND BOARD.

Power_ON/OFF Toggle

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
ATX CONNECTOR, PWR TOGGLE AND HEADER

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	35 of 72	Drawn By	SS

VCCA <= 1V implies ~RST is low
VCCA > 1V implies ~RST is high

VCC1V2 R483 120 R482 1.00K
VCC3V3
U5 LTC1326 (VCC3, VCC25, VCCA, GND, PBR, SRST, RST, RST)
Silkscreen: "VCC 1.2V"
DS8 (RED, GRN) R298 330 R283 330
VCC5V C423 0.1UF

VCC5V C416 0.1UF
VCC5V R280 4.42K R295 1.62K
U28 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 5.0V"
DS7 (RED, GRN) R296 330 R281 330
VCC5V C422 0.1UF

VCC2V5 C401 0.1UF
VCC2V5 R242 1.33K R248 1.62K
U24 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 2.5V"
DS6 (RED, GRN) R249 330 R243 330
VCC5V C410 0.1UF

VTT_DDR2 C400 0.1UF
VTT_DDR2 R132 10
U23 DEVICE=NCP300 (NC1, NC2, RESET, INPUT, GND)
Silkscreen: "VTT_DDR2"
DS5 (RED, GRN) R247 15K R241 120
VCC5V C409 0.1UF

VCC3_PCI C388 0.1UF
VCC3_PCI R196 1.96K R214 1.62K
U18 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 3.0V"
DS4 (RED, GRN) R215 330 R197 330
VCC5V C398 0.1UF

AVCCAUXMGT
2.5V
C387 0.1UF
R194 1.33K R212 1.62K
U17 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "AVCCAUXMGT"
DS3 (RED, GRN) R213 330 R195 330
VCC5V C397 0.1UF

VCC3V3 C360 0.1UF
VCC3V3 R160 2.32K R172 1.62K
U13 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 3.3V"
DS2 (RED, GRN) R173 330 R161 330
VCC5V C367 0.1UF

1.8V
VCC1V8 C359 0.1UF
VCC1V8 R158 523 R170 1.62K
U12 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 1.8"
DS1 (RED, GRN) R171 330 R159 330
VCC5V C366 0.1UF

"1.2V" VCC1V2 TP17
"2.5V" VCC2V5 TP14
"VCC3_PCI" VCC3_PCI TP10
"3.3V" VCC3V3 TP8
"5V" VCC5V TP16
"VTT_DDR2" VTT_DDR2 TP13
VCC12V_N TP19
VCC12V_P TP18
"1.8V" VCC1V8 TP7

AVCCAUXMGT TP9

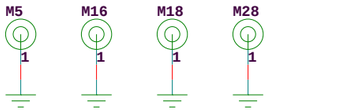
XILINX

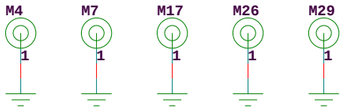
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

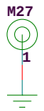
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
POWER SUPPLY MONITORS AND LEDS

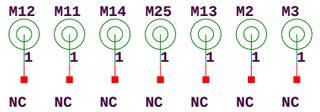
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	36 of 72	Drawn By	SS

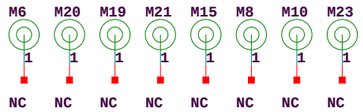
Mounting holes for ATX Form Factor

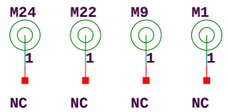




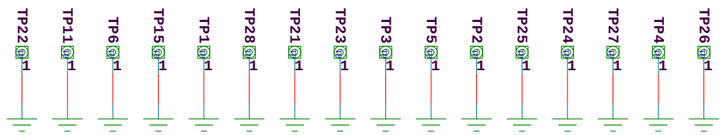








Spread out on the board.



Silkscreen:
"GND"

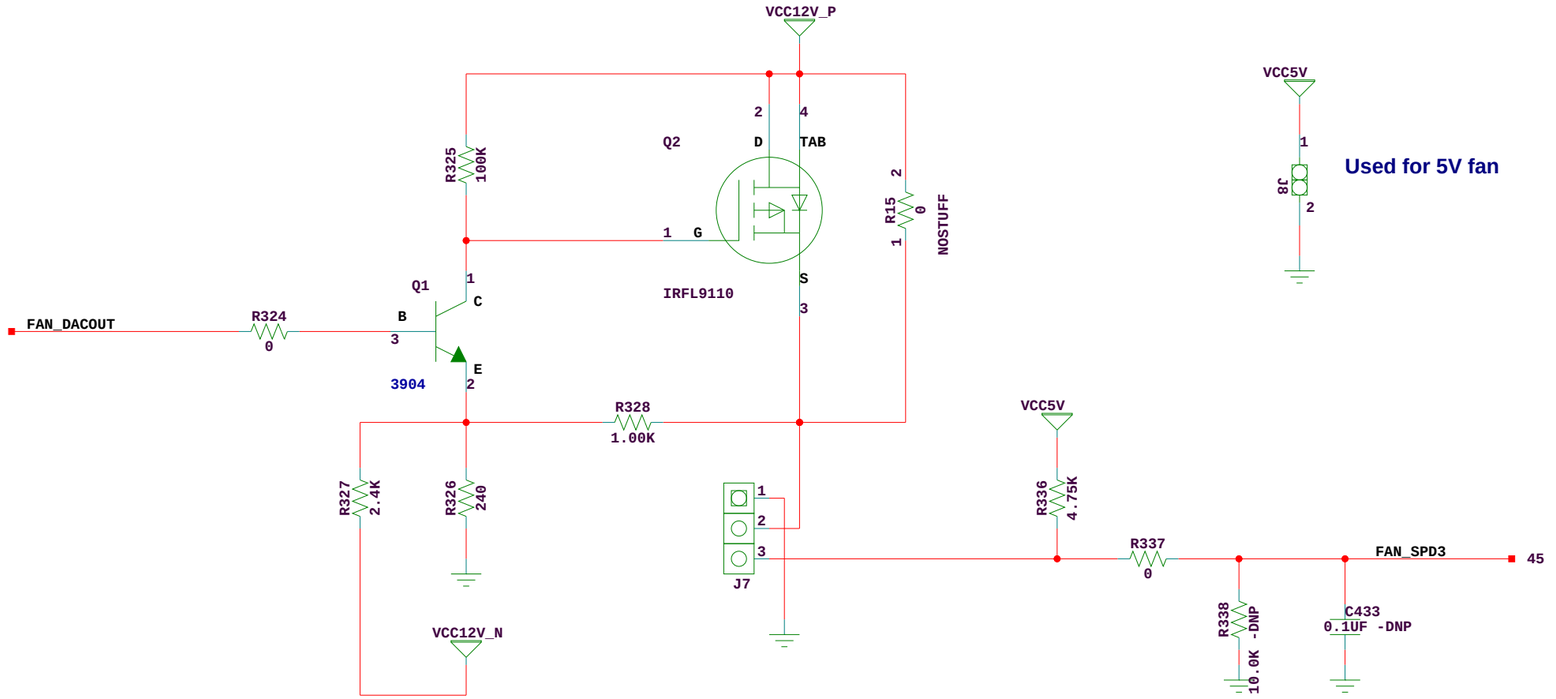
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

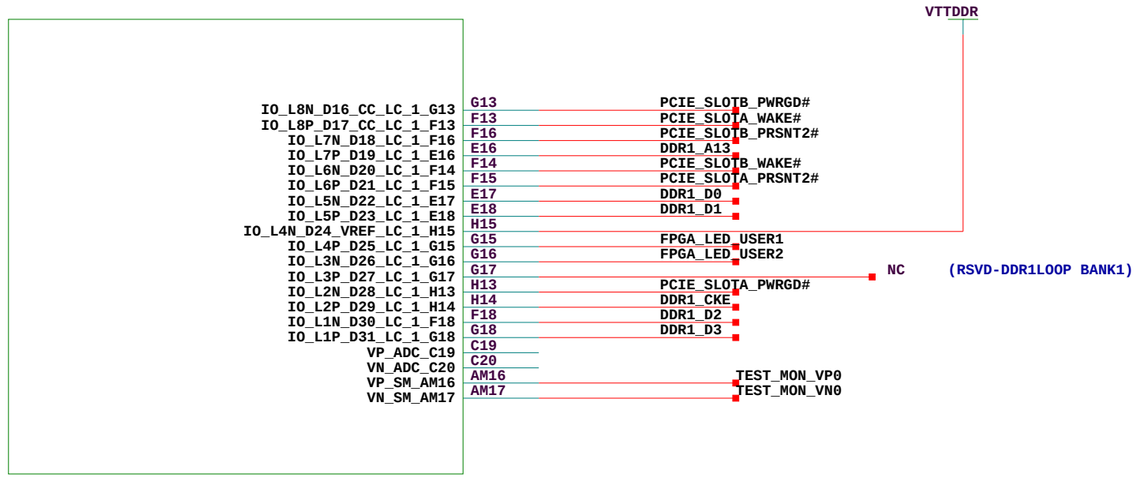
ATX MOUNTING HOLES AND TEST POINTS

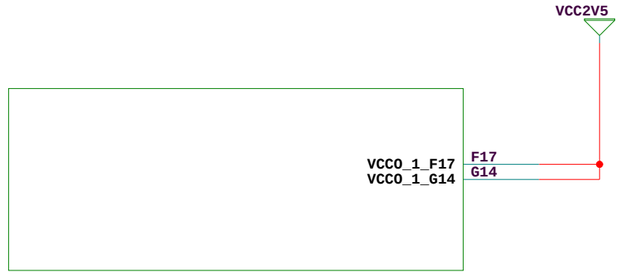
Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 37 of 72	Drawn By SS

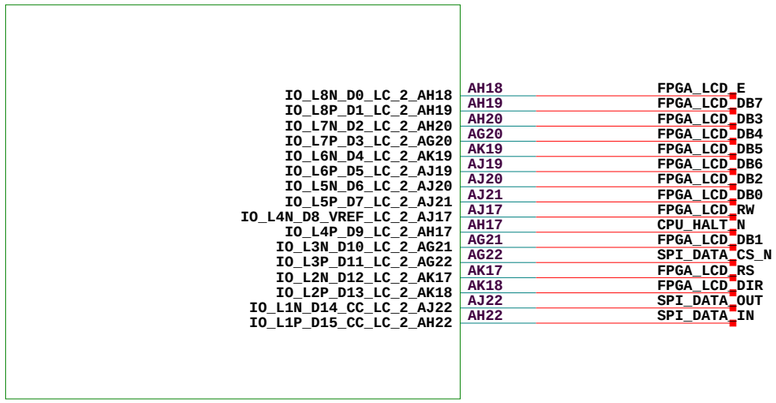


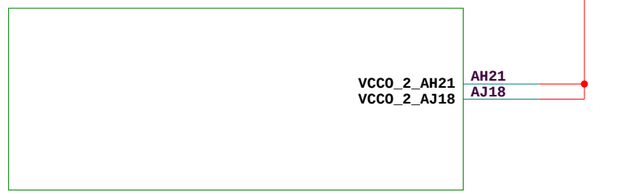
Used for 5V fan

XILINX	SCH P/N 0381203 ART P/N 0531499 FAB P/N 1280372		
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM FPGA FAN SWITCH AND TACH			
Date: 8-22-2006_9:52		Ver: 03	
Sheet Size: B		Rev: E	
Sheet 38 of 72		Drawn By SS	









XILINX		SCH P/N	0381203
		ART P/N	0531499
		FAB P/N	1280372
Title:	SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM FPGA - BANK1,2 - PCI-E CTRL, DDR1, LCD		
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	39 of 72	Drawn By	SS

Should be length matched to DDR_PLL_CLKIN

IO_L8N_GC_LC_3_L14	L14	PHY_TXER	
IO_L8P_GC_LC_3_L15	L15	USER_CLK2	
IO_L7N_GC_LC_3_H18	H18	PHY_RXER	
IO_L7P_GC_LC_3_H19	H19	DDR2_CLK_FB	(FEEDBACK)
IO_L6N_GC_LC_3_K14	K14	DDR2_CLK_FB	
IO_L6P_GC_LC_3_J14	J14	PHY_TXCLK	
IO_L5N_GC_LC_3_J19	J19	PHY_GTXCLK	
IO_L5P_GC_LC_3_K19	K19	PHY_RXC_RXCLK	
IO_L4N_GC_VREF_LC_3_J15	J15	FPGA_ATX_POW_TOG	
IO_L4P_GC_LC_3_J16	J16	USER_CLKSYS	
IO_L3N_GC_LC_3_K17	K17	PHY_INT_SGMII	
IO_L3P_GC_LC_3_K18	K18	DDR1_CK1_P	(FEEDBACK)
IO_L2N_GC_VRP_LC_3_L16	L16		
IO_L2P_GC_VRN_LC_3_K16	K16	PM_CLK_TOP	
IO_L1N_GC_CC_LC_3_J17	J17	PHY_RESET_SGMII	
IO_L1P_GC_CC_LC_3_H17	H17	PCI_P_CLK5	
			(FEEDBACK)

U37

VCC2V5

VCCO_3_J18	J18	
VCCO_3_K15	K15	

CU37

Feedback nets should be length matched

IO_L8N_GC_CC_LC_4_AG18	AG18	USER_SMA_CLK_N	
IO_L8P_GC_CC_LC_4_AF18	AF18	USER_SMA_CLK_P	
IO_L7N_GC_VRP_LC_4_AE19	AE19	PHY1_MDIO	
IO_L7P_GC_VRN_LC_4_AD19	AD19	PHY1_MDC	
IO_L6N_GC_LC_4_AG16	AG16	CLK_SEL0	
IO_L6P_GC_LC_4_AG17	AG17	CLK_SEL1	
IO_L5N_GC_LC_4_AF19	AF19	DBG_LED_0	
IO_L5P_GC_LC_4_AF20	AF20		
IO_L4N_GC_VREF_LC_4_AE17	AE17	SBR_RSM_RSTJ	
IO_L4P_GC_LC_4_AE18	AE18	SBR_PWG	
IO_L3N_GC_LC_4_AF21	AF21	SPI_CLK	
IO_L3P_GC_LC_4_AE21	AE21	SBR_INTR	
IO_L2N_GC_LC_4_AE16	AE16	SBR_IDE_RST_N	
IO_L2P_GC_LC_4_AF16	AF16	SYSACE_FPGA_CLK	
IO_L1N_GC_LC_4_AD20	AD20	SBR_NMI	
IO_L1P_GC_LC_4_AD21	AD21	PM_CLK_BOT	

U37

U37

VCC2V5

VCCO_4_AE20	AE20	
VCCO_4_AF17	AF17	

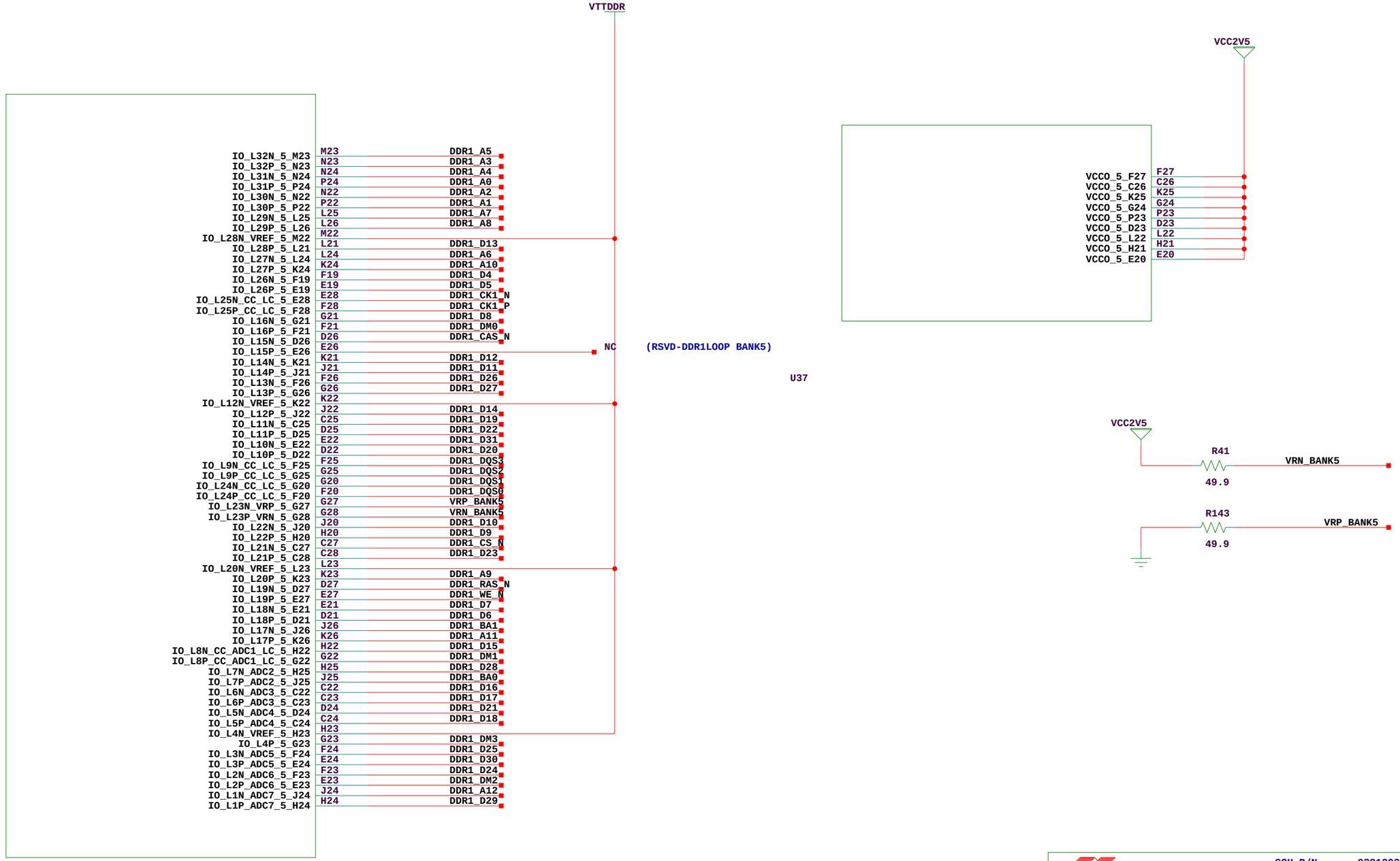
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK3,4 - PHY_CTL,USR CLKS, SBR

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 40 of 72	Drawn By SS



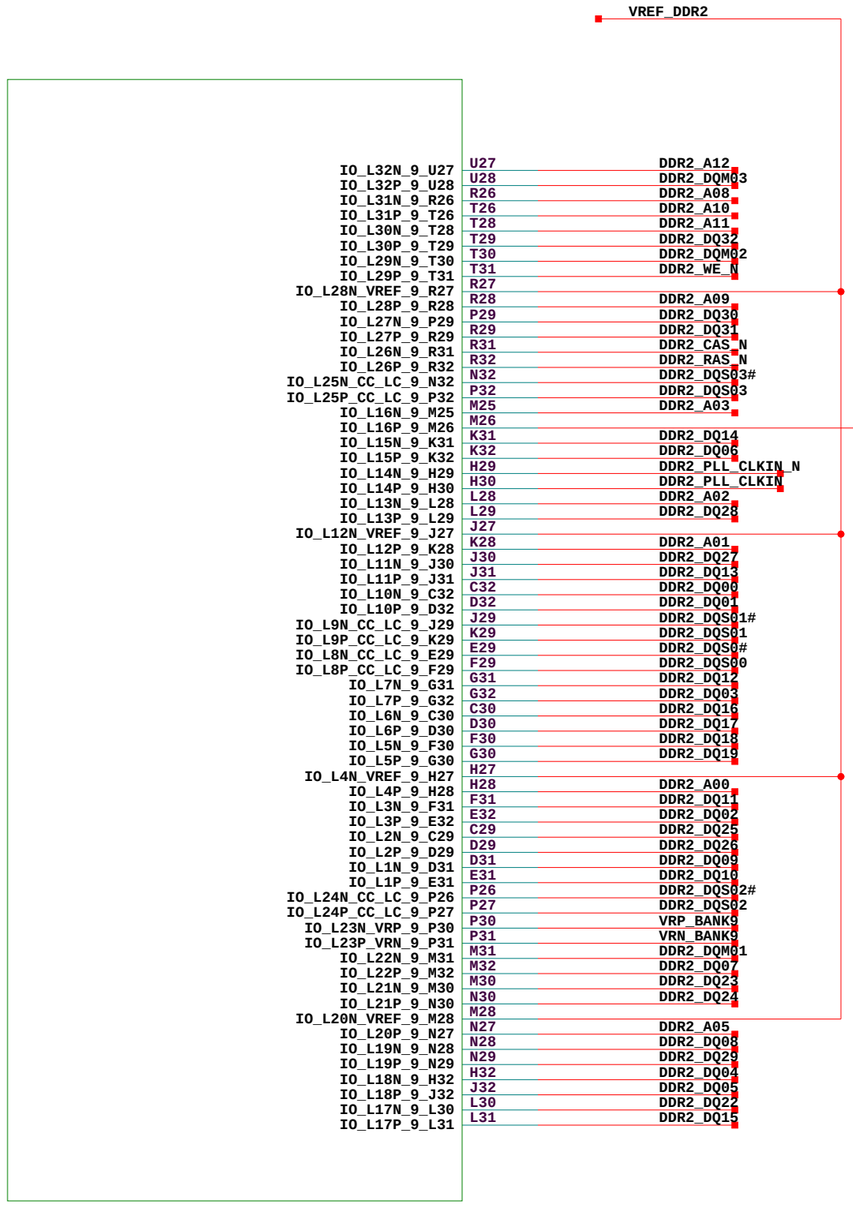
XILINX

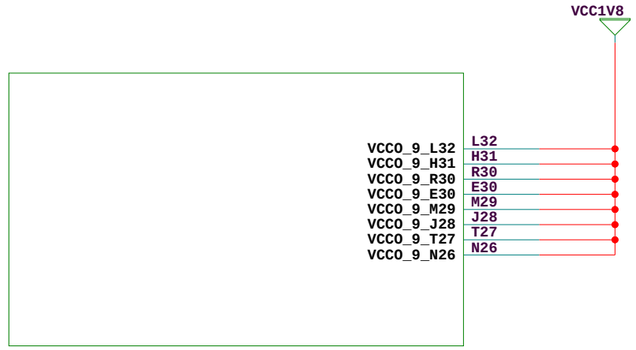
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

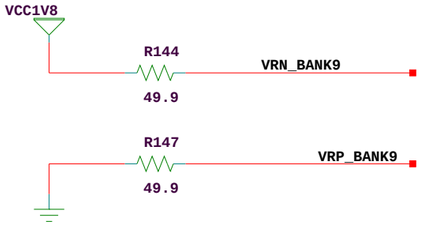
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK5 - DDR1

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 41 of 72	Drawn By SS







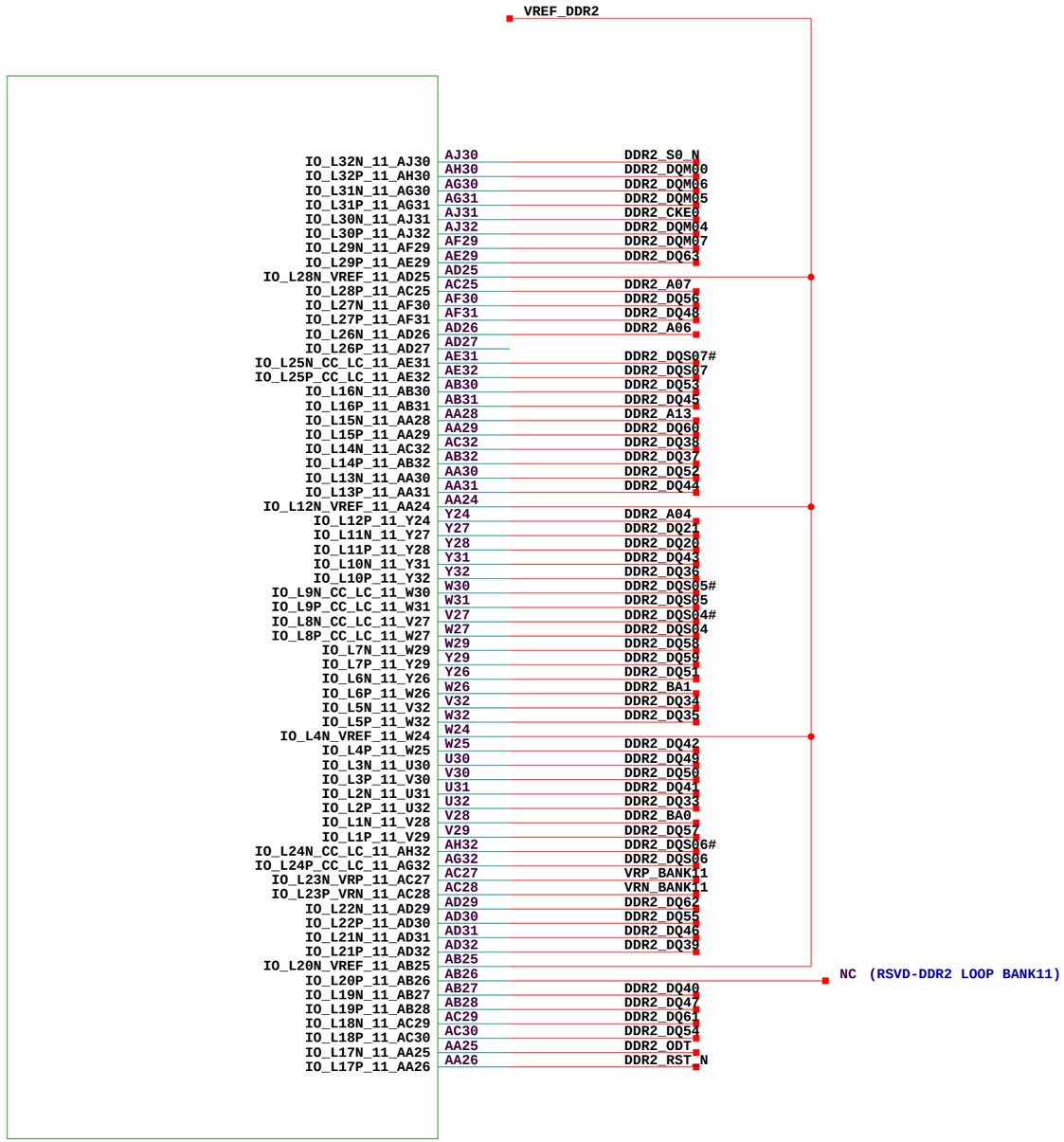
XILINX

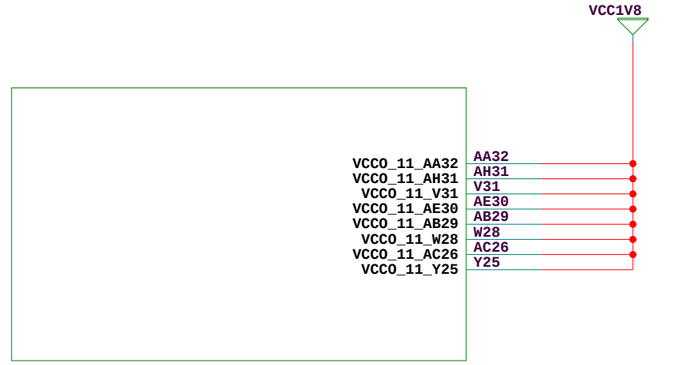
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

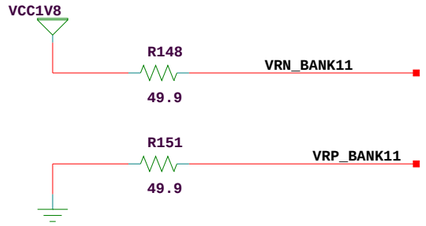
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK9 - DDR2

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet 42 of 72		Drawn By	SS







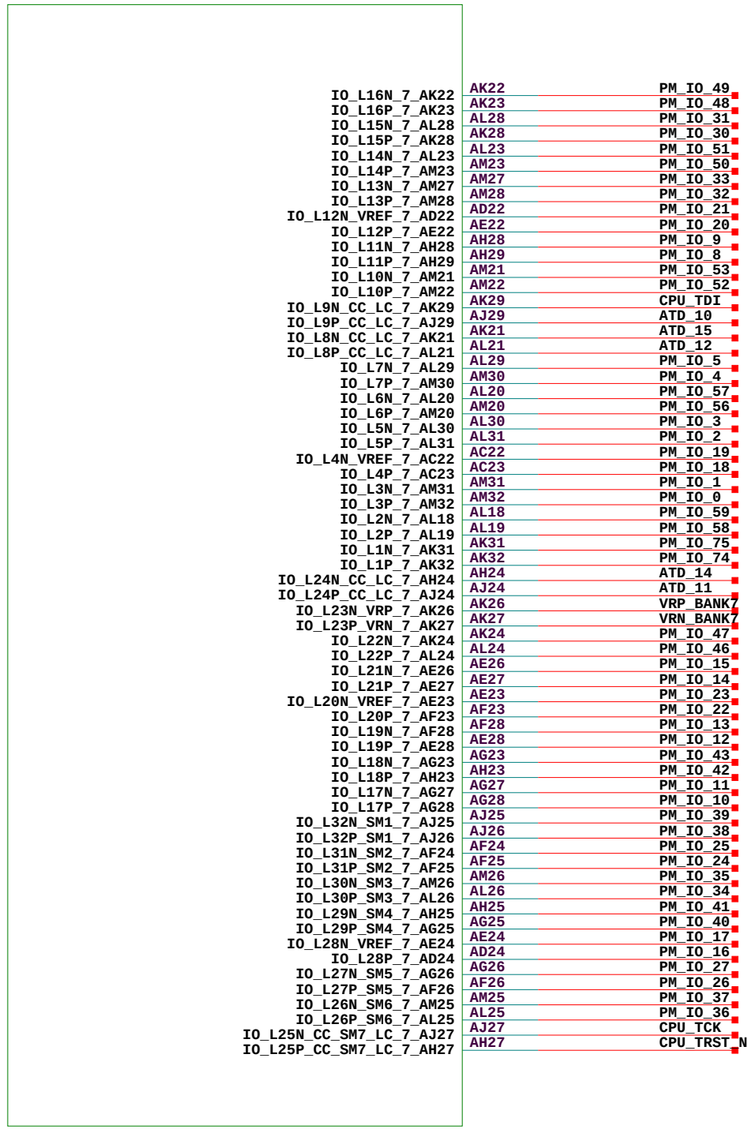
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

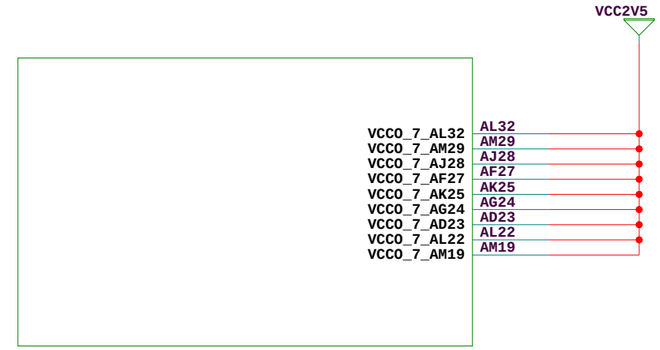
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

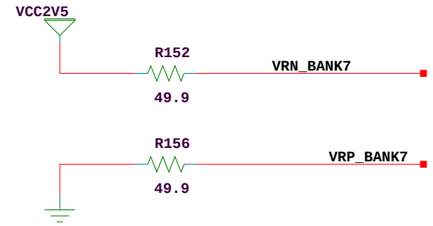
FPGA - BANK11 - DDR2

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 43 of 72	Drawn By SS



U37





U37

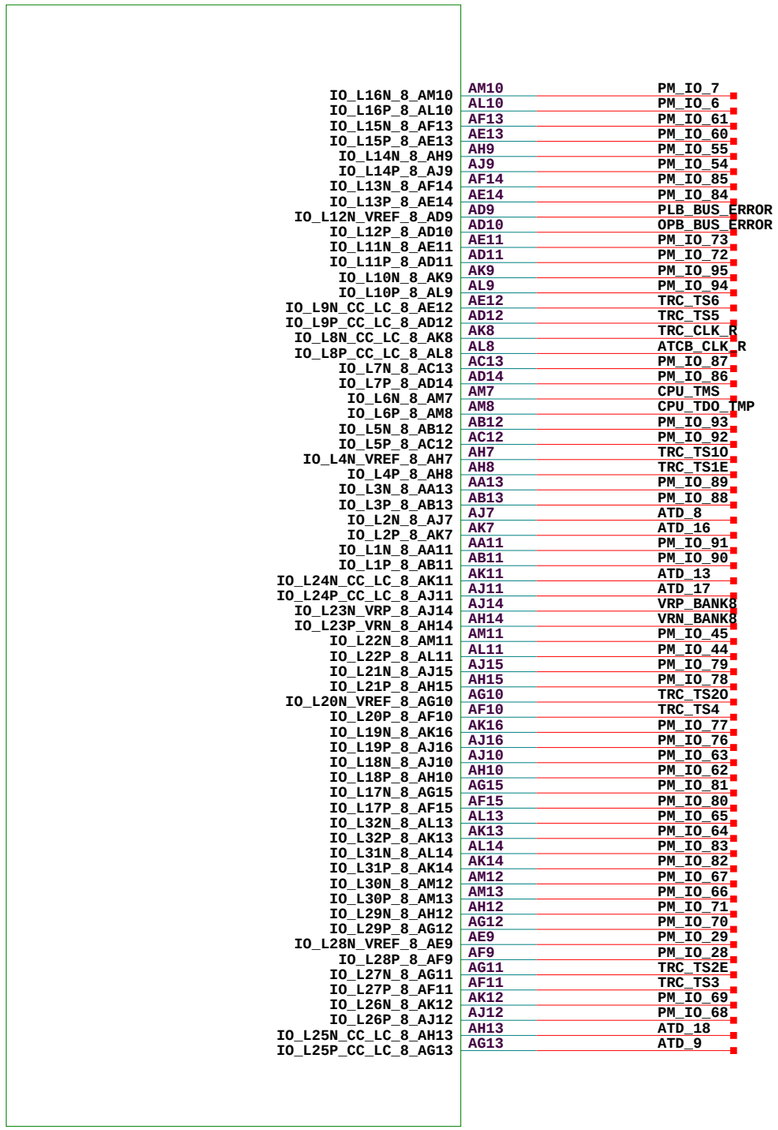
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

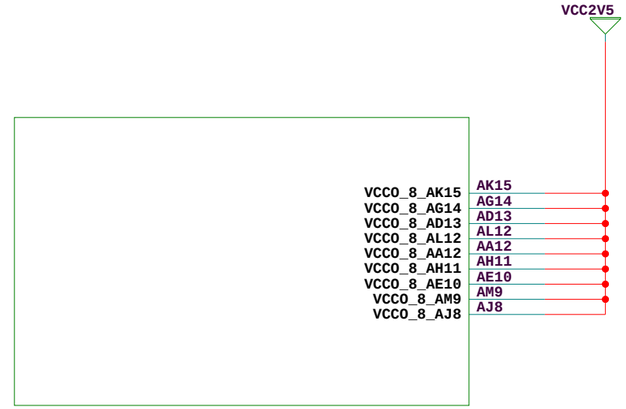
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK7- PM_IO_*

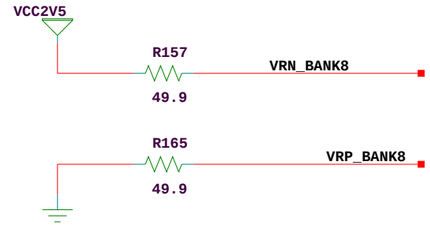
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet 44 of 72		Drawn By	SS



U37



U37



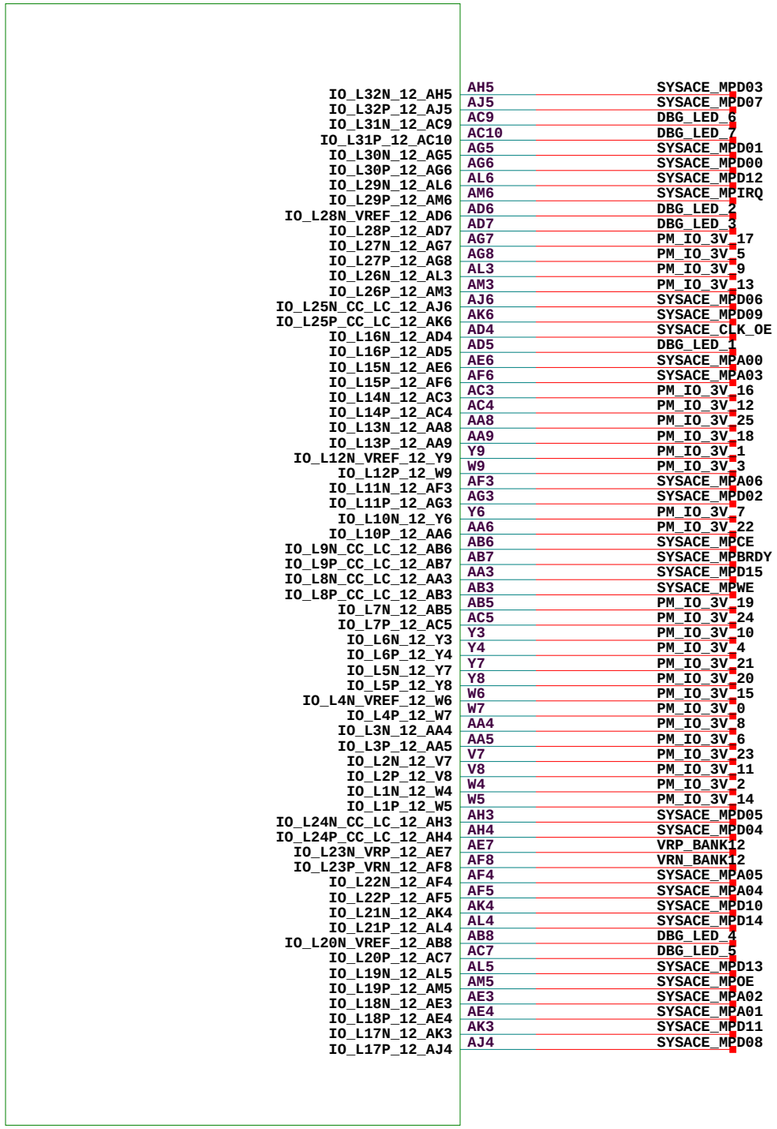
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

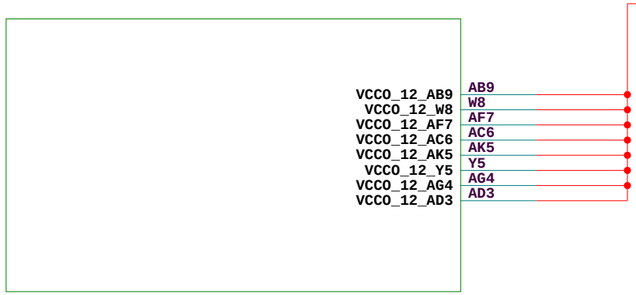
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK8 - PM_IO,MICTOR, CPU_DEBUG

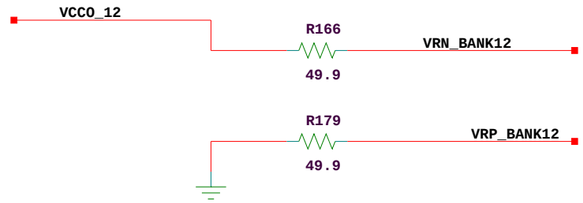
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	45 of 72	Drawn By	SS

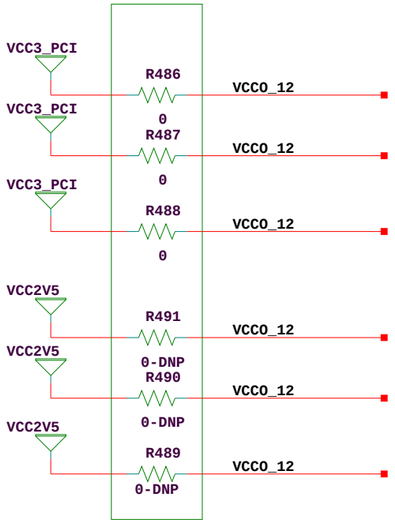


U37



U37





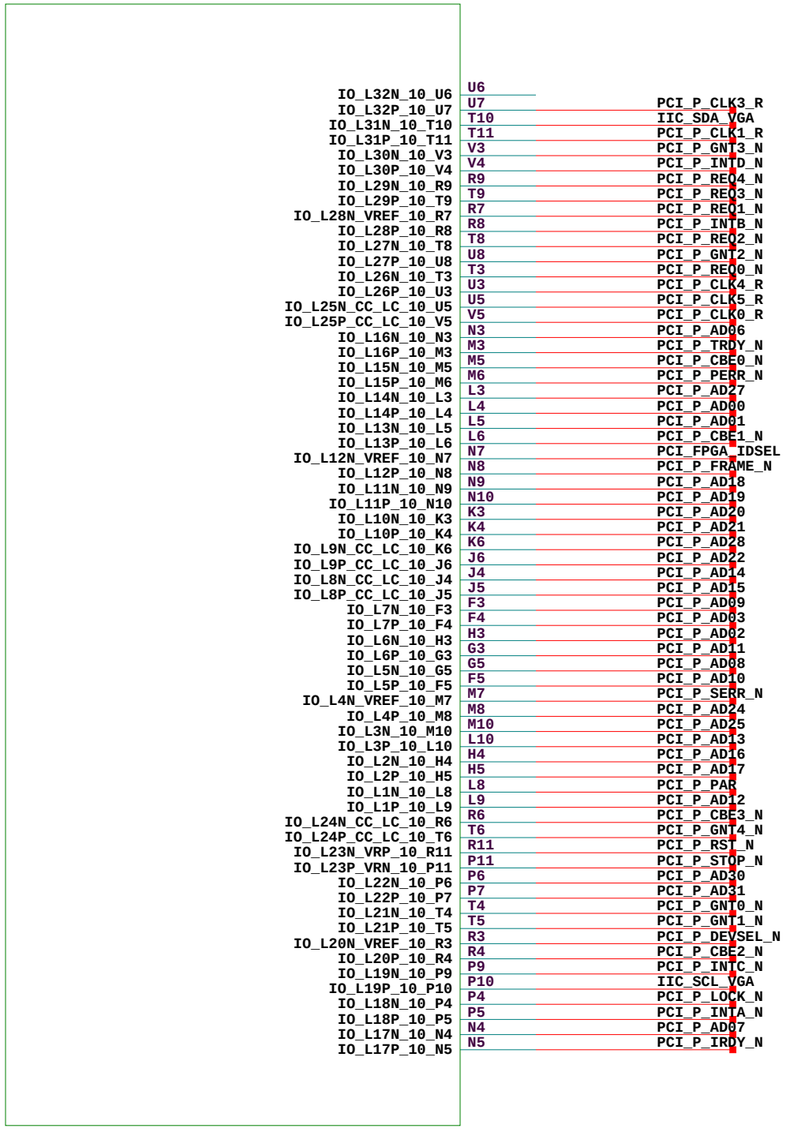
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

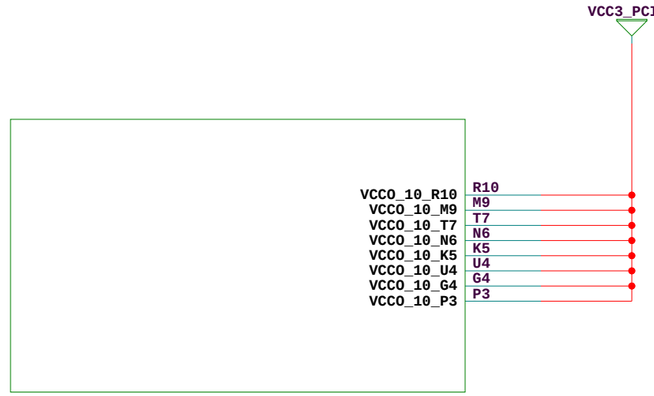
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK12 - SYSACE, PM_IO_3,DBG_LED

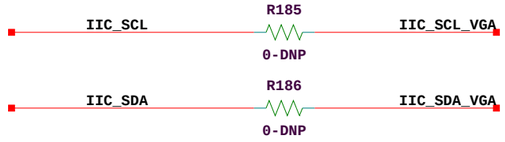
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	46 of 72	Drawn By	SS



U37



U37



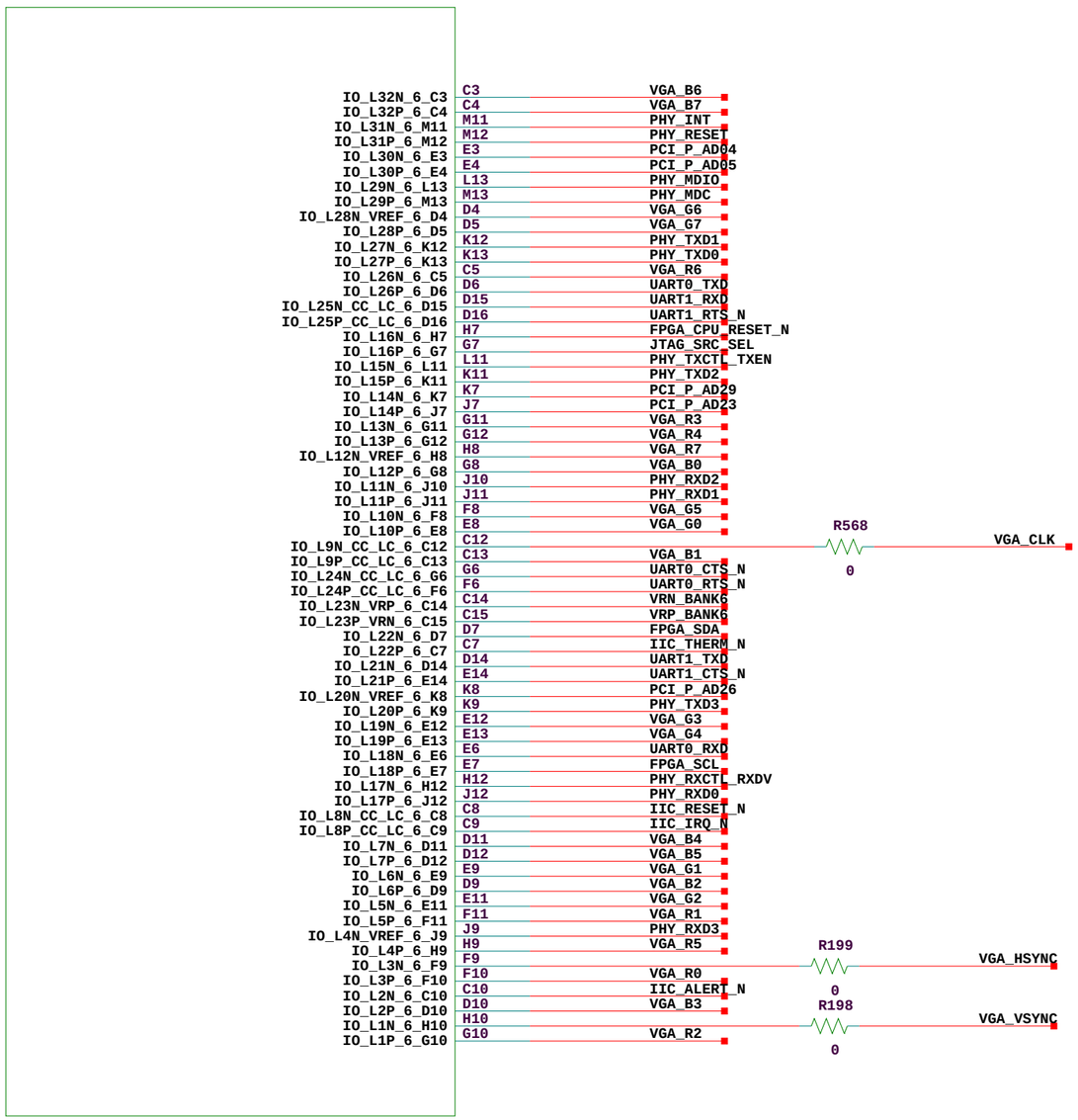
XILINX

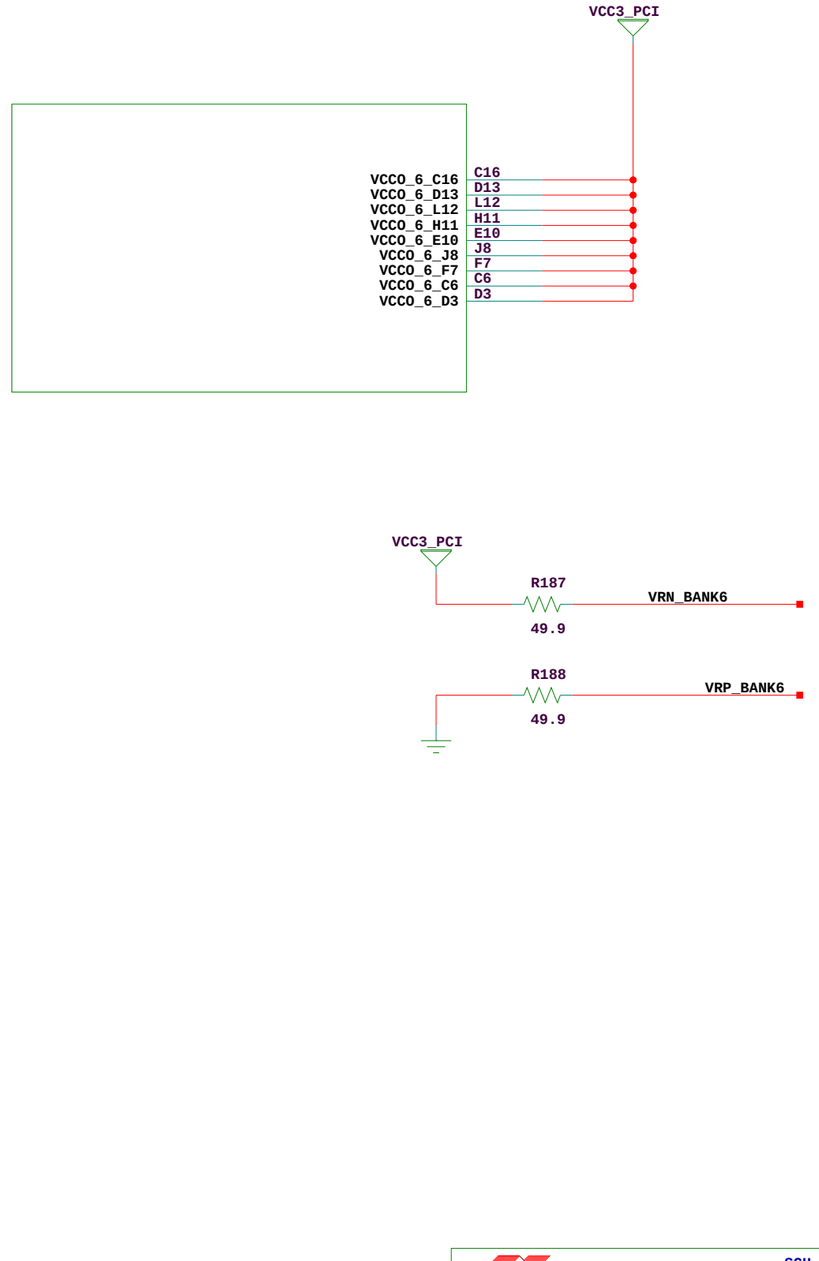
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK10 - PCI

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	47 of 72	Drawn By	SS





U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA-BANK6, VGA, UART, PHY

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet 48 of 72		Drawn By	SS

U37

VTRXB_101_A27	A27	MGT_101_VTRXB
AVCCAUXRXB_101_B30	B30	MGT_101_AVCCAUXRXB
VTTXB_101_B26	B26	MGT_101_VTTXB
AVCCAUXMGT_101_B28	B28	MGT_101_AVCCAUX
AVCCAUXTX_101_B25	B25	MGT_101_AVCCAUXTX
VTTXA_101_B23	B23	MGT_101_VTTXA
AVCCAUXRXA_101_B21	B21	MGT_101_AVCCAUXRXA
VTRXA_101_A22	A22	MGT_101_VTRXA

U37

VTRXB_102_H34	H34	MGT_102_VTRXB
AVCCAUXRXB_102_K33	K33	MGT_102_AVCCAUXRXB
VTTXB_102_G33	G33	MGT_102_VTTXB
AVCCAUXMGT_102_J33	J33	MGT_102_AVCCAUX
AVCCAUXTX_102_F33	F33	MGT_102_AVCCAUXTX
VTTXA_102_D33	D33	MGT_102_VTTXA
AVCCAUXRXA_102_B32	B32	MGT_102_AVCCAUXRXA
VTRXA_102_C34	C34	MGT_102_VTRXA

U37

VTRXB_103_AB34	AB34	MGT_103_VTRXB
AVCCAUXRXB_103_AE33	AE33	MGT_103_AVCCAUXRXB
VTTXB_103_AA33	AA33	MGT_103_VTTXB
AVCCAUXMGT_103_AC33	AC33	MGT_103_AVCCAUX
AVCCAUXTX_103_Y33	Y33	MGT_103_AVCCAUXTX
VTTXA_103_V33	V33	MGT_103_VTTXA
AVCCAUXRXA_103_T33	T33	MGT_103_AVCCAUXRXA
VTRXA_103_U34	U34	MGT_103_VTRXA

U37

TXNPADA_101_C	C8181 10NF	2	TXNPADA_101	
TXPPADA_101_C	C8191 10NF	2	TXPPADA_101	
TXNPADB_101_C	C8161 10NF	2	TXNPADB_101	
TXPPADB_101_C	C8171 10NF	2	TXPPADB_101	
TXNPADA_102_C	C8101 10NF	2	TXNPADA_102	
TXPPADA_102_C	C8111 10NF	2	TXPPADA_102	
TXNPADA_103_C	C8121 10NF	2	TXNPADA_103	
TXPPADA_103_C	C8131 10NF	2	TXPPADA_103	
TXNPADB_103_C	C8141 10NF	2	TXNPADB_103	
TXPPADB_103_C	C8151 10NF	2	TXPPADB_103	

Available only on FX100

4x PCIE_SLOTB

U37

RXNPADB_101_A29	A29	RXNPADB_101
RXPPADB_101_A28	A28	RXPPADB_101
TXNPADB_101_A26	A26	TXNPADB_101_C
TXPPADB_101_A25	A25	TXPPADB_101_C
TXNPADA_101_A24	A24	TXNPADA_101_C
TXPPADA_101_A23	A23	TXPPADA_101_C
RXNPADA_101_A21	A21	RXNPADA_101
RXPPADA_101_A20	A20	RXPPADA_101

U37

MGTCLK_N_102_N34	N34	SGMIICLK_NQO
MGTCLK_P_102_M34	M34	SGMIICLK_QO
RXNPADB_102_K34	K34	RXNPADB_102
RXPPADB_102_J34	J34	RXPPADB_102
TXNPADB_102_G34	G34	TXNPADB_102
TXPPADB_102_F34	F34	TXPPADB_102
TXNPADA_102_E34	E34	TXNPADA_102_C
TXPPADA_102_D34	D34	TXPPADA_102_C
RXNPADA_102_A32	A32	RXNPADA_102
RXPPADA_102_A31	A31	RXPPADA_102

SGMII

1X PCIE_SLOTB

U37

4X PCIE_SLOTA

RXNPADB_103_AD34	AD34	RXNPADB_103
RXPPADB_103_AC34	AC34	RXPPADB_103
TXNPADB_103_AA34	AA34	TXNPADB_103_C
TXPPADB_103_Y34	Y34	TXPPADB_103_C
TXNPADA_103_W34	W34	TXNPADA_103_C
TXPPADA_103_V34	V34	TXPPADA_103_C
RXNPADA_103_T34	T34	RXNPADA_103
RXPPADA_103_R34	R34	RXPPADA_103

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

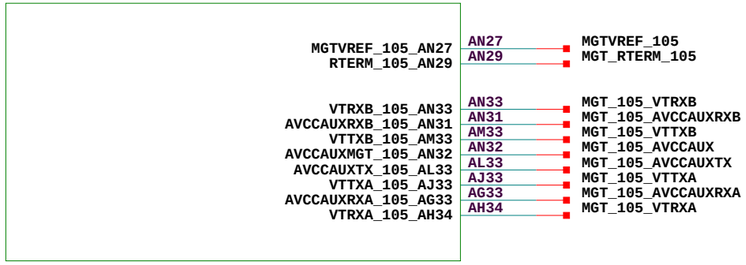
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

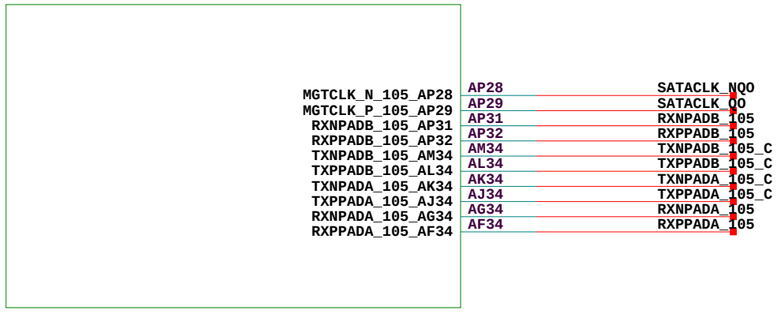
MGT 101, 102 AND 103 - SGMII, PCIE-A & B

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 49 of 72	Drawn By SS

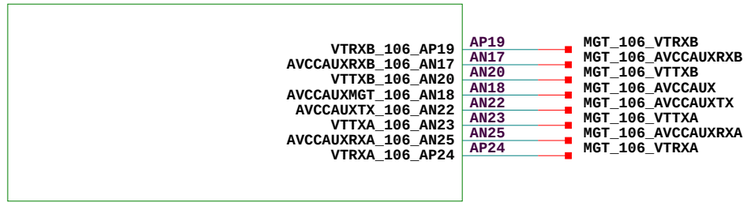
SATA Clock

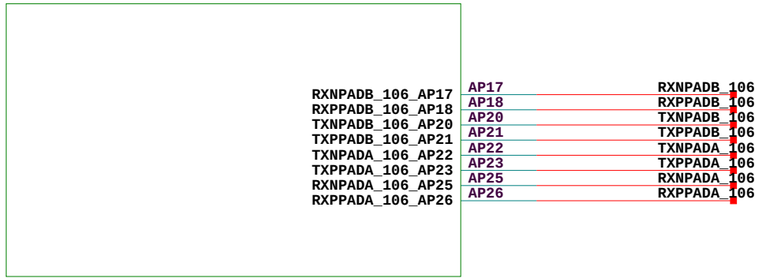
4X PCIE_SLOTA



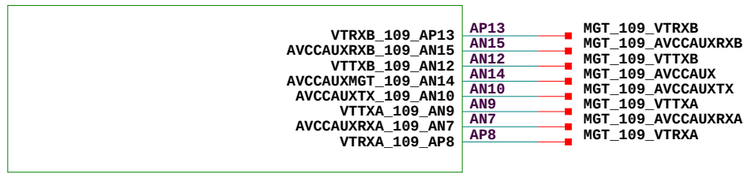


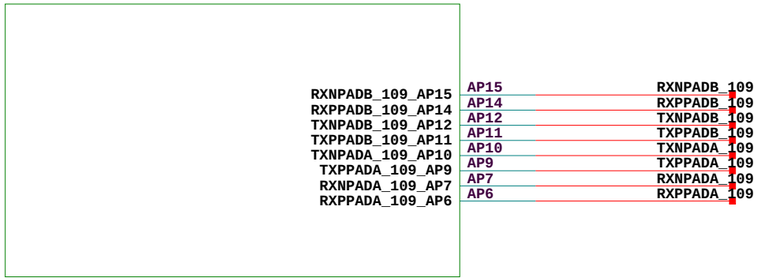
SATA





PM





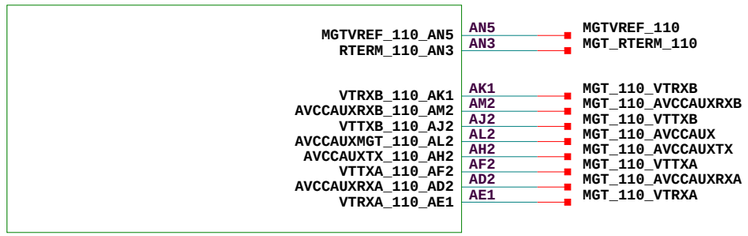
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

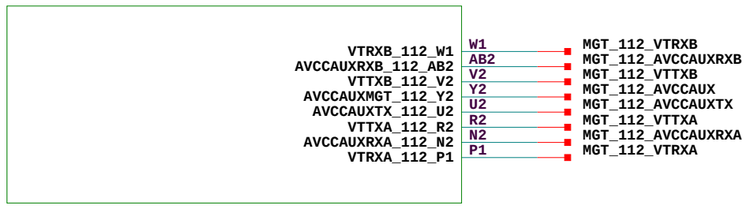
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT 105, 106 AND 109 - PM, SATA+CLK, PCIE

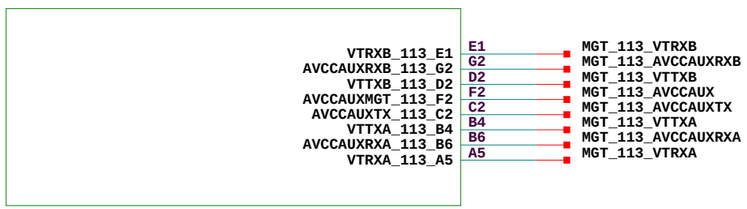
Date: 8-22-2006_9:52		Ver: 03
Sheet Size: B		Rev: E
Sheet 50 of 72		Drawn By SS



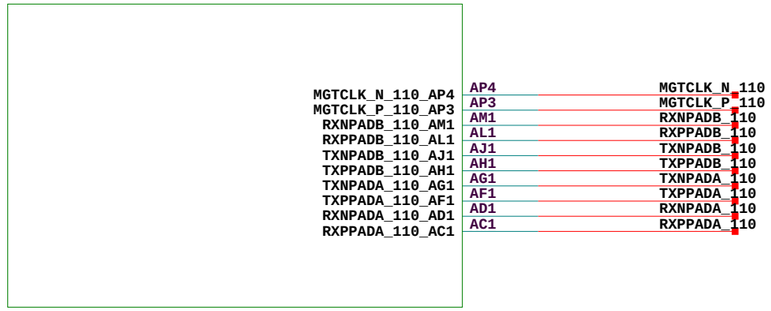
U37



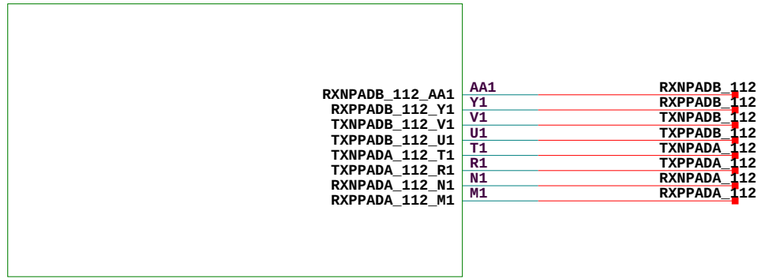
U37



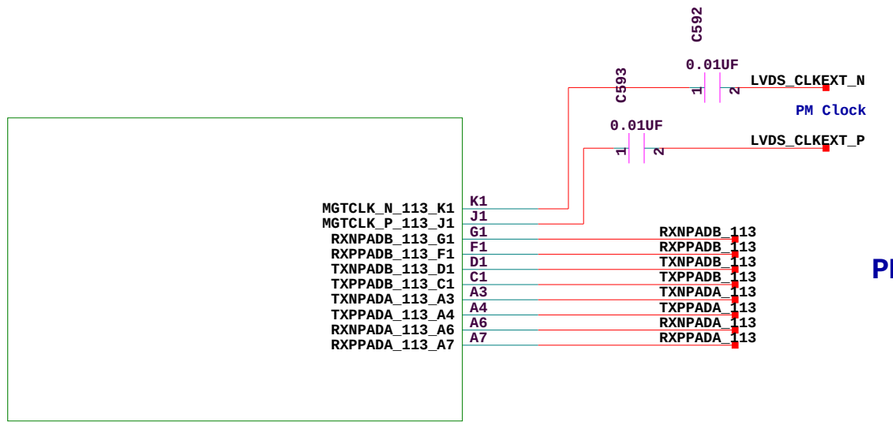
U37



U37



U37



U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT - 110 , 112 AND 113

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	51 of 72	Drawn By	SS

Available only on FX100

4x PCIE_SLOTB

U37

RXNPADB_114_A9 A9 RXNPADB_114
RXPPADB_114_A10 A10 RXPPADB_114
TXNPADB_114_A12 A12 TXNPADB_114_C
TXPPADB_114_A13 A13 TXPPADB_114_C
TXNPADA_114_A14 A14 TXNPADA_114
TXPPADA_114_A15 A15 TXPPADA_114
RXNPADA_114_A17 A17 RXNPADA_114
RXPPADA_114_A18 A18 RXPPADA_114

Unused

U37

VTRXB_114_A11 A11 MGT_114_VTRXB
AVCCAUXRXB_114_B8 B8 MGT_114_AVCCAUXRXB
VTTXB_114_B12 B12 MGT_114_VTTXB
AVCCAUXMGT_114_B10 B10 MGT_114_AVCCAUX
AVCCAUXTX_114_B13 B13 MGT_114_AVCCAUXTX
VTTXA_114_B15 B15 MGT_114_VTTXA
AVCCAUXRXA_114_B17 B17 MGT_114_AVCCAUXRXA
VTRXA_114_A16 A16 MGT_114_VTRXA

U37

TXNPADB_114_C — C8241 10NF — TXNPADB_114

TXPPADB_114_C — C8251 10NF — TXPPADB_114

U37

VCC2V5

VCCO_0_R20 R20
VCCO_0_W18 W18
VCCO_0_T17 T17
VCCO_0_Y15 Y15

U37

AVSS_ADC_C18 C18
AVDD_ADC_D18 D18
VREFP_ADC_D19 D19
VREFN_ADC_D20 D20
AVSS_SM_AM15 AM15
AVDD_SM_AL15 AL15
VREFP_SM_AL16 AL16
VREFN_SM_AL17 AL17

TEST_MON_AVDD
TEST_MON_VREFP

U37

Should be routed differentially

TDP_0_C17 C17 FPGA_DXP
TDN_0_D17 D17 FPGA_DXN
TDI_0_AA15 AA15 FPGA_TDI
DOUT_BUSY_0_Y18 Y18
M1_0_W19 W19 FPGA_MODE_1
TCK_0_AA14 AA14 FPGA_TCK
TDO_0_W17 W17 FPGA_TDO
M0_0_V18 V18 FPGA_MODE_0
TMS_0_Y14 Y14 FPGA_TMS
PWRDWN_B_0_AA16 AA16 FPGA_PWRDWN_B
M2_0_T20 T20 FPGA_MODE_2
VBATT_0_R21 R21 FPGA_VBATT
RDWR_B_0_W15 W15
DONE_0_R19 R19 FPGA_DONE
CS_B_0_T16 T16
INIT_0_P19 P19 FPGA_INIT
PROGRAM_B_0_P21 P21 FPGA_PROG_B
D_IN_0_R17 R17
CCLK_0_T18 T18 FPGA_CCLK
HSWAPEN_0_P20 P20 FPGA_HSWAP

R206 4.7K
R244 4.7K
R257 4.7K

FPGA_VBATT — C534 0.1UF

U37

XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT_114, VCCO_0, CONFIG,MISC

Date: 8-22-2006_9:52 Ver: 03

Sheet Size: B Rev: E

Sheet 52 of 72 Drawn By SS

VCC2V5

VCCAUX_K27	K27
VCCAUX_U26	U26
VCCAUX_N25	N25
VCCAUX_V24	V24
VCCAUX_AB22	AB22
VCCAUX_W21	W21
VCCAUX_AC19	AC19
VCCAUX_V19	V19
VCCAUX_N19	N19
VCCAUX_L19	L19
VCCAUX_AD16	AD16
VCCAUX_AB16	AB16
VCCAUX_U16	U16
VCCAUX_M16	M16
VCCAUX_T14	T14
VCCAUX_N13	N13
VCCAUX_U11	U11
VCCAUX_AB10	AB10
VCCAUX_V9	V9
VCCAUX_AE8	AE8

U37

VCC1V2

VCCINT_M27	M27
VCCINT_V25	V25
VCCINT_T25	T25
VCCINT_P25	P25
VCCINT_AC24	AC24
VCCINT_U24	U24
VCCINT_R24	R24
VCCINT_AB23	AB23
VCCINT_Y23	Y23
VCCINT_V23	V23
VCCINT_T23	T23
VCCINT_AA22	AA22
VCCINT_W22	W22
VCCINT_U22	U22
VCCINT_R22	R22
VCCINT_AB21	AB21
VCCINT_Y21	Y21
VCCINT_V21	V21
VCCINT_T21	T21
VCCINT_M21	M21
VCCINT_AC20	AC20
VCCINT_AA20	AA20
VCCINT_W20	W20
VCCINT_U20	U20
VCCINT_N20	N20
VCCINT_L20	L20
VCCINT_AB19	AB19
VCCINT_Y19	Y19
VCCINT_T19	T19
VCCINT_M19	M19
VCCINT_AC18	AC18
VCCINT_AA18	AA18
VCCINT_U18	U18
VCCINT_R18	R18
VCCINT_N18	N18
VCCINT_L18	L18
VCCINT_AD17	AD17
VCCINT_AB17	AB17
VCCINT_Y17	Y17
VCCINT_V17	V17
VCCINT_P17	P17
VCCINT_M17	M17
VCCINT_AC16	AC16
VCCINT_W16	W16
VCCINT_R16	R16
VCCINT_N16	N16
VCCINT_AD15	AD15
VCCINT_AB15	AB15
VCCINT_V15	V15
VCCINT_T15	T15
VCCINT_P15	P15
VCCINT_M15	M15
VCCINT_AC14	AC14
VCCINT_W14	W14
VCCINT_U14	U14
VCCINT_R14	R14
VCCINT_N14	N14
VCCINT_Y13	Y13
VCCINT_V13	V13
VCCINT_T13	T13
VCCINT_P13	P13
VCCINT_W12	W12
VCCINT_U12	U12
VCCINT_R12	R12
VCCINT_N12	N12
VCCINT_Y11	Y11
VCCINT_V11	V11
VCCINT_AA10	AA10
VCCINT_W10	W10
VCCINT_U10	U10
VCCINT_AC8	AC8

U37

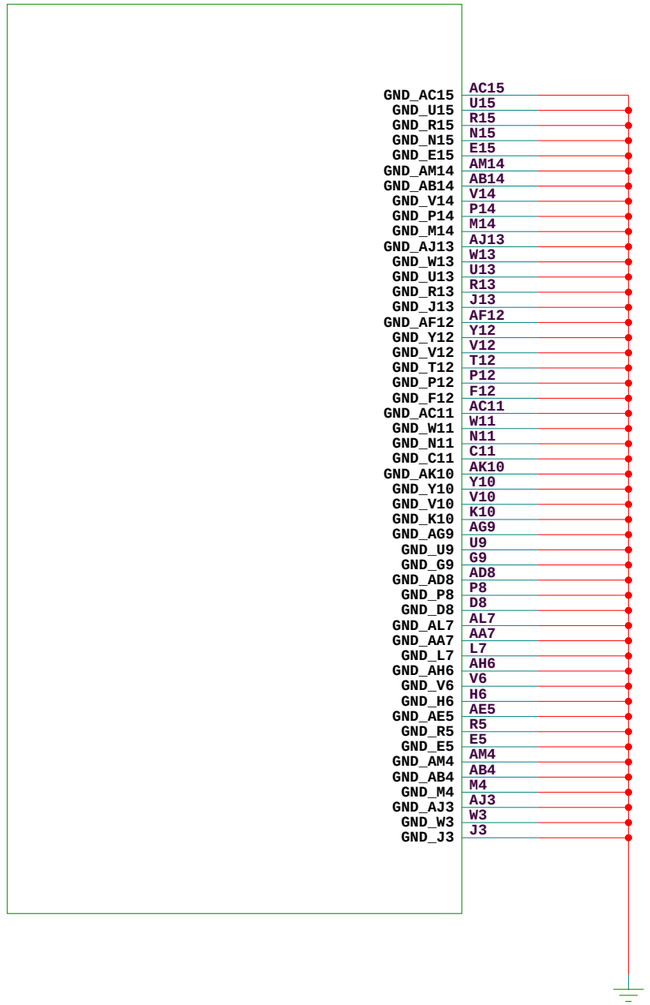
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

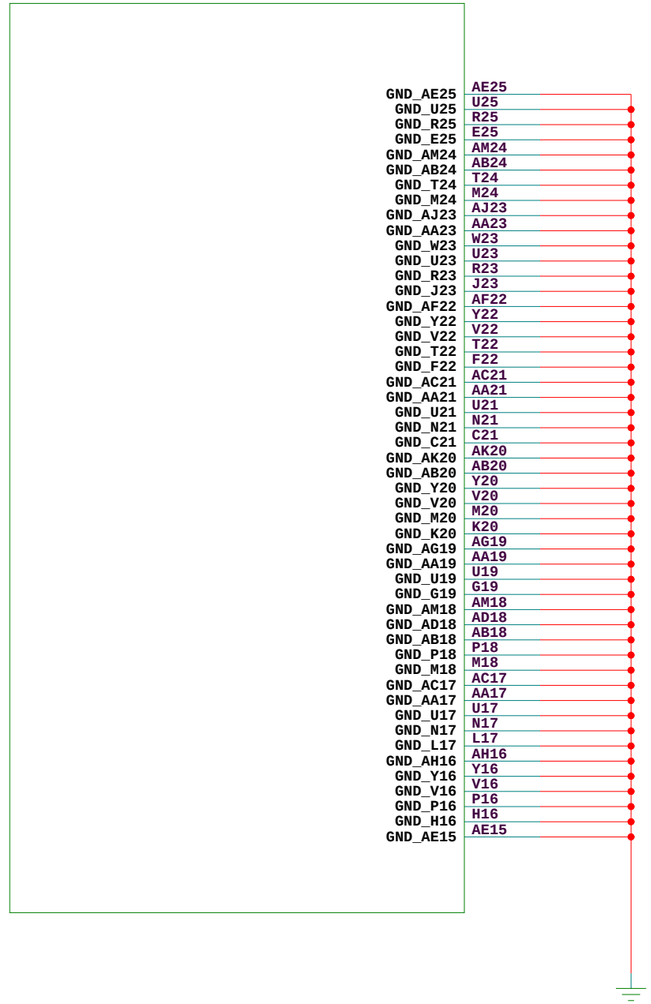
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA CORE AND VCCAUX PINS

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 53 of 72	Drawn By SS



U37



U37

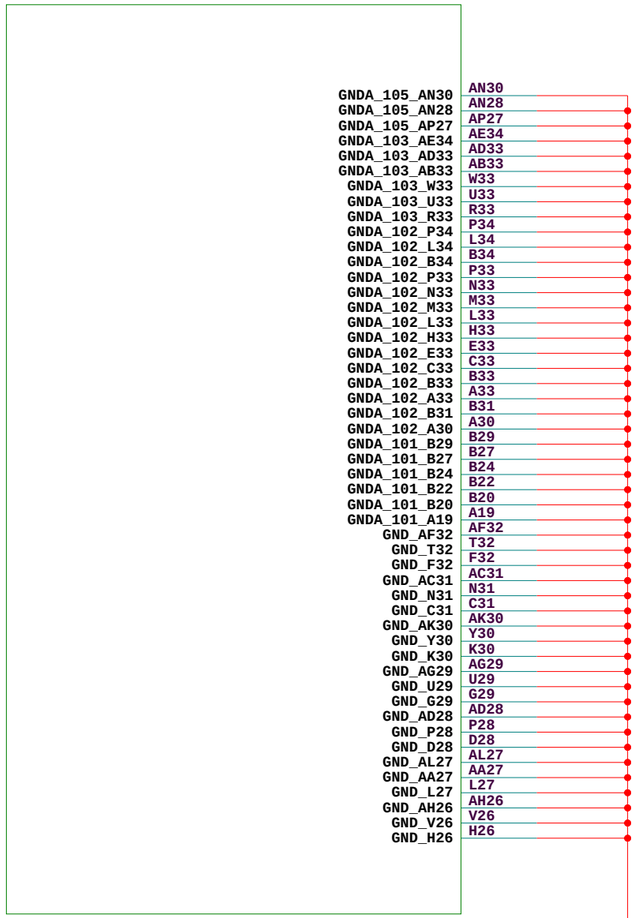
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

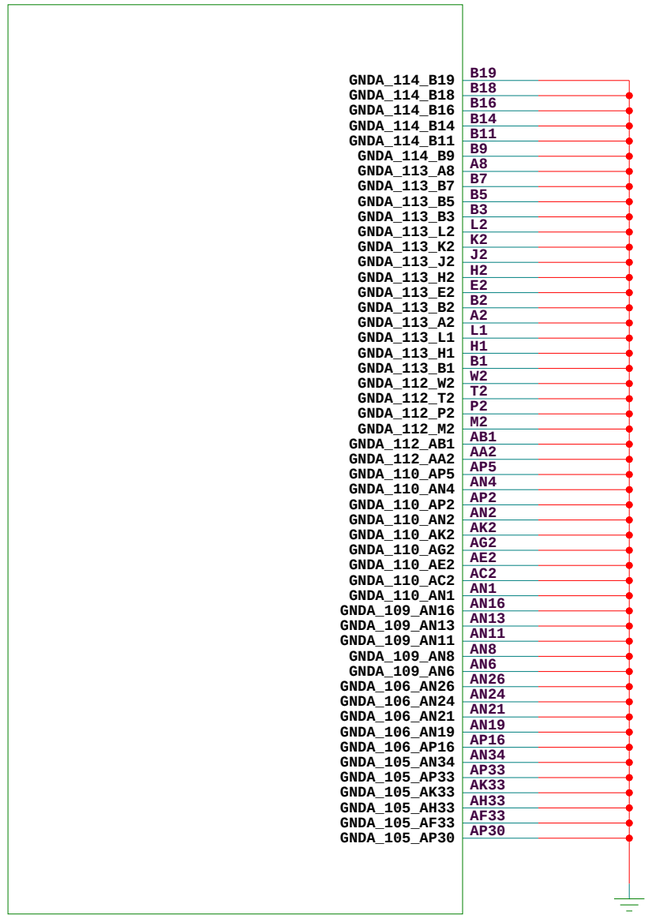
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA GROUND PINS

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 54 of 72	Drawn By SS



U37



U37

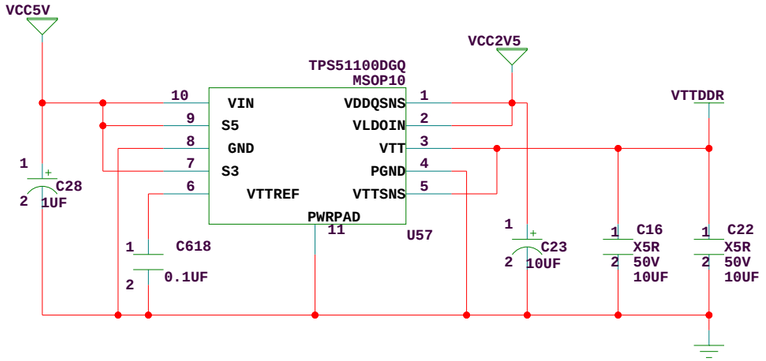
XILINX

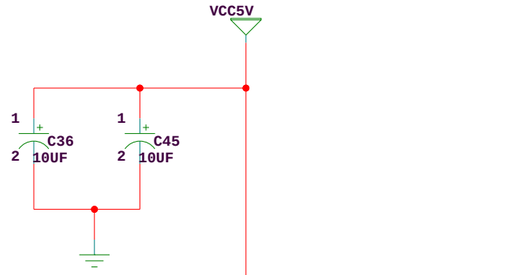
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

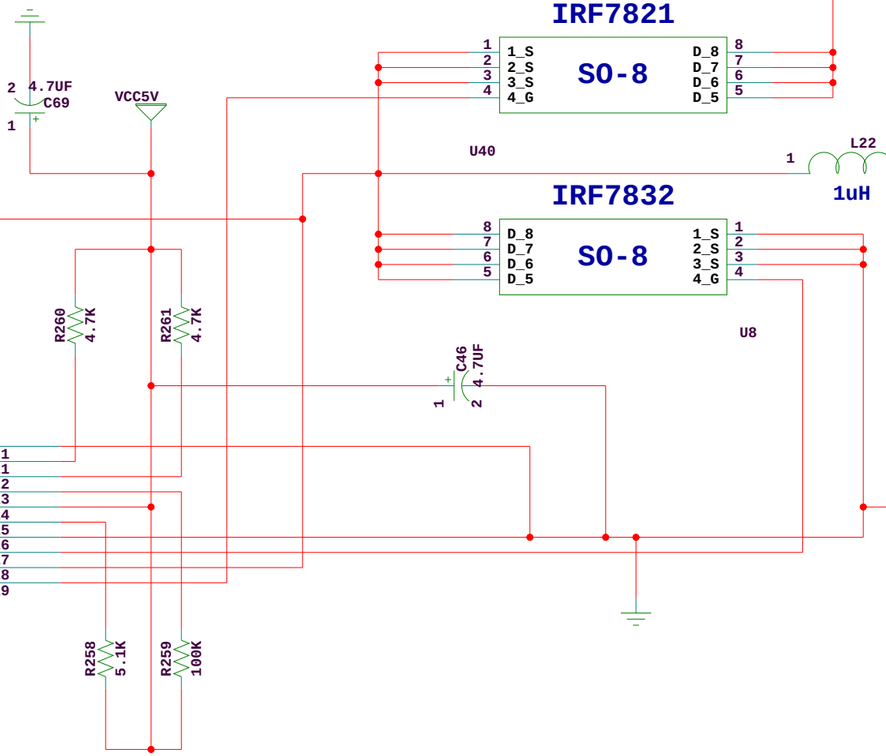
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

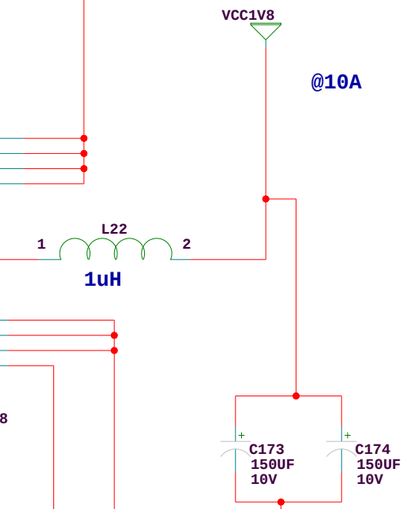
FPGA GROUND PINS

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 55 of 72	Drawn By SS









SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

DDR1 AND DDR2 POWER SUPPLIES

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 56 of 72	Drawn By SS

Matched Length Nets

DDR1_A3
DDR1_A2
DDR1_A1
DDR1_A0
DDR1_A10
DDR1_BA1
DDR1_BA0
DDR1_CS_N

DDR1_RAS_N
DDR1_CAS_N
DDR1_WE_N
DDR1_DM2
DDR1_A13
DDR1_DQS2
DDR1_D23
DDR1_D22

DDR1_D20
DDR1_D19
DDR1_D18
DDR1_D17
DDR1_D16

DDR1_DM3

DDR1_DQS3
DDR1_D24
DDR1_D25
DDR1_D26
DDR1_D27
DDR1_D28
DDR1_D29
DDR1_D30

DDR1_A7
DDR1_A6
DDR1_A5
DDR1_A4
DDR1_A12
DDR1_A11
DDR1_A9
DDR1_A8

DDR1_DM1
DDR1_CK1_N
DDR1_CK1_P
DDR1_CKE
DDR1_D10
DDR1_D9
DDR1_D8
DDR1_DQS1

DDR1_D14
DDR1_D13
DDR1_D12
DDR1_D11
DDR1_D7
DDR1_DQS0
DDR1_DM0
DDR1_D15

DDR1_D3
DDR1_D4
DDR1_D5
DDR1_D6
DDR1_D31
DDR1_D0
DDR1_D1
DDR1_D2
DDR1_D21

RP52 RP53 RP54 RP66 RP65 RP64 RP62 RP58 RP59 RP60 RP61 RP55 RP67 RP56 RP57 — 47R

NC
NC

VTTDDR
VCC2V5

C619 C636 C620 C623 C621 C635 C622 C624 — 0.1UF
C182 C183 C185 C186 C196 C197 — 100UF

R277 — 47R

64Mx16x4
DDR SDRAM
HYB25D256160BT-7F
TSOP66

U42
U43

C626 C625 — 0.1UF

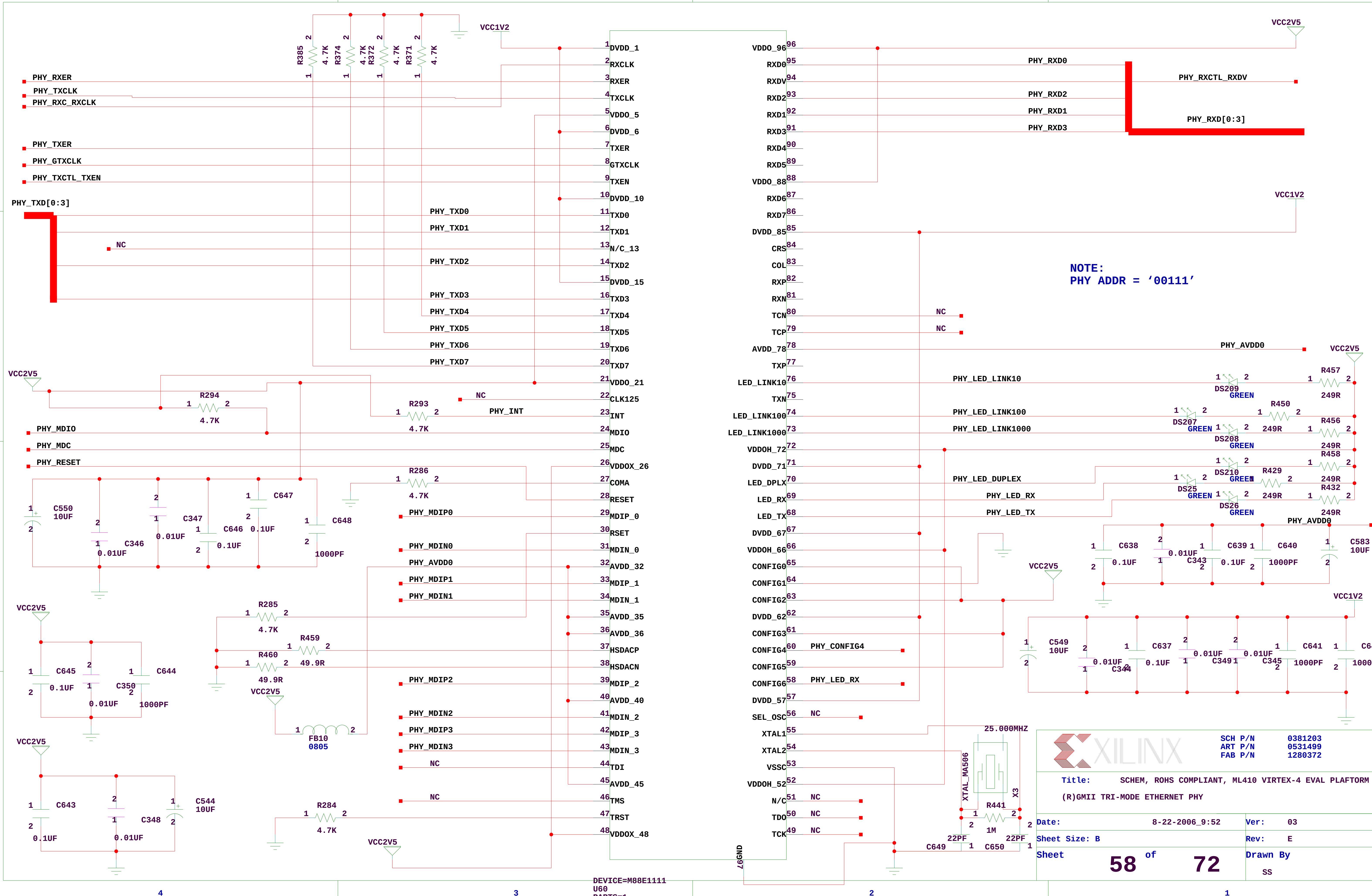
C627 C628 C630 C629 C631 C632 C633 C634 — 0.1UF

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

DDR1 DISCRETES AND TERMINATION

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	57 of 72	Drawn By	SS



VCC1V2
VCC2V5
R385 4.7K
R374 4.7K
R372 4.7K
R371 4.7K
PHY_RXER
PHY_TXCLK
PHY_RXC_RXCLK
PHY_TXER
PHY_GTXCLK
PHY_TXCTL_TXEN
PHY_TXD[0:3]
PHY_TXD0
PHY_TXD1
NC
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
R294 4.7K
R293 4.7K
PHY_INT
PHY_MDIO
PHY_MDC
PHY_RESET
R286 4.7K
C550 10UF
C346 0.01UF
C347 0.01UF
C646 0.1UF
C647 0.1UF
C648 1000PF
PHY_MDIP0
PHY_MDIN0
PHY_AVDD0
PHY_MDIP1
PHY_MDIN1
R285 4.7K
R459 49.9R
R460 49.9R
C645 0.1UF
C350 0.01UF
C644 1000PF
PHY_MDIP2
PHY_MDIN2
PHY_MDIP3
PHY_MDIN3
FB10 0805
C643 0.1UF
C348 0.01UF
C544 10UF
R284 4.7K
DVDD_1
RXCLK
RXER
TXCLK
VDDO_5
DVDD_6
TXER
GTXCLK
TXEN
DVDD_10
TXD0
TXD1
N/C_13
TXD2
DVDD_15
TXD3
TXD4
TXD5
TXD6
TXD7
VDDO_21
CLK125
INT
MDIO
MDC
VDDOX_26
COMA
RESET
MDIP_0
RSET
MDIN_0
AVDD_32
MDIP_1
MDIN_1
AVDD_35
AVDD_36
HSDACP
HSDACN
MDIP_2
AVDD_40
MDIN_2
MDIP_3
MDIN_3
TDI
AVDD_45
TMS
TRST
VDDOX_48
VDDO_96
RXD0
RXDV
RXD2
RXD1
RXD3
RXD4
RXD5
VDDO_88
RXD6
RXD7
DVDD_85
CRS
COL
RXP
RXN
TCN
TCP
AVDD_78
TXP
LED_LINK10
TXN
LED_LINK100
LED_LINK1000
VDDOH_72
DVDD_71
LED_DPLX
LED_RX
LED_TX
DVDD_67
VDDOH_66
CONFIG0
CONFIG1
CONFIG2
DVDD_62
CONFIG3
CONFIG4
CONFIG5
CONFIG6
DVDD_57
SEL_OSC
XTAL1
XTAL2
VSSC
VDDOH_52
N/C
TDO
TCK
GND97
DEVICE=M88E1111
U60
PARTS=1
PHY_RXD0
PHY_RXCTL_RXDV
PHY_RXD2
PHY_RXD1
PHY_RXD3
PHY_RXD[0:3]
NOTE:
PHY ADDR = '00111'
PHY_AVDD0
PHY_LED_LINK10
PHY_LED_LINK100
PHY_LED_LINK1000
PHY_LED_DUPLEX
PHY_LED_RX
PHY_LED_TX
DS209 GREEN
DS207 GREEN
DS208 GREEN
DS210 GREEN
DS25 GREEN
DS26 GREEN
R457 249R
R450 249R
R456 249R
R458 249R
R429 249R
R432 249R
C638 0.1UF
C343 0.01UF
C639 0.1UF
C640 1000PF
C583 10UF
PHY_CONFIG4
PHY_LED_RX
C549 10UF
C344 0.01UF
C637 0.1UF
C349 0.01UF
C345 0.01UF
C641 1000PF
C642 1000PF
25.000MHZ
XTAL_MA506
X3
R441 1M
C649 22PF
C650 22PF

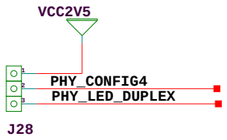
XILINX

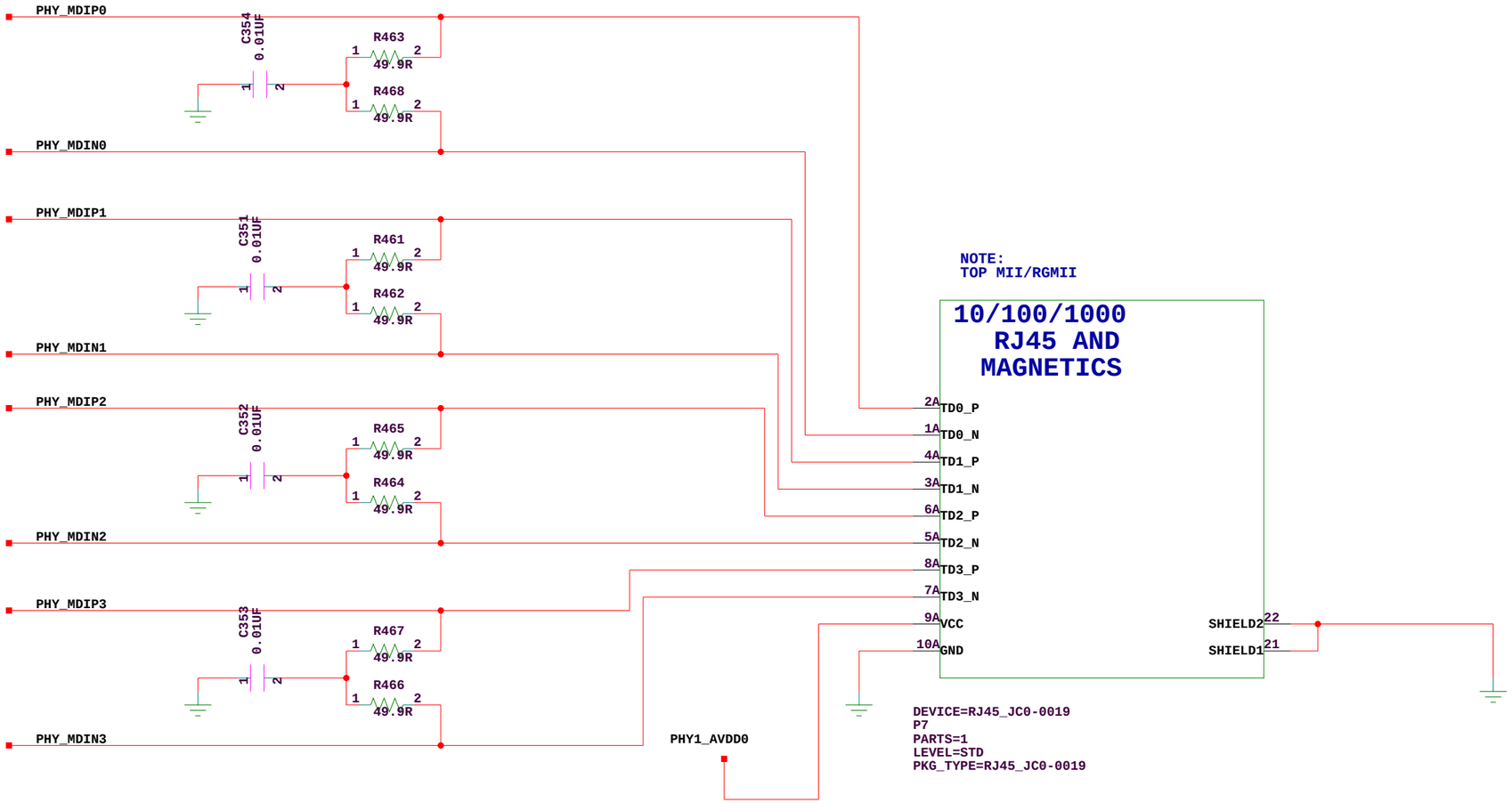
SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
(R)GMII TRI-MODE ETHERNET PHY

Date: 8-22-2006_9:52
Ver: 03
Sheet Size: B
Rev: E
Sheet 58 of 72
Drawn By SS

1-2: MII to Cu
2-3: RGMII to Cu



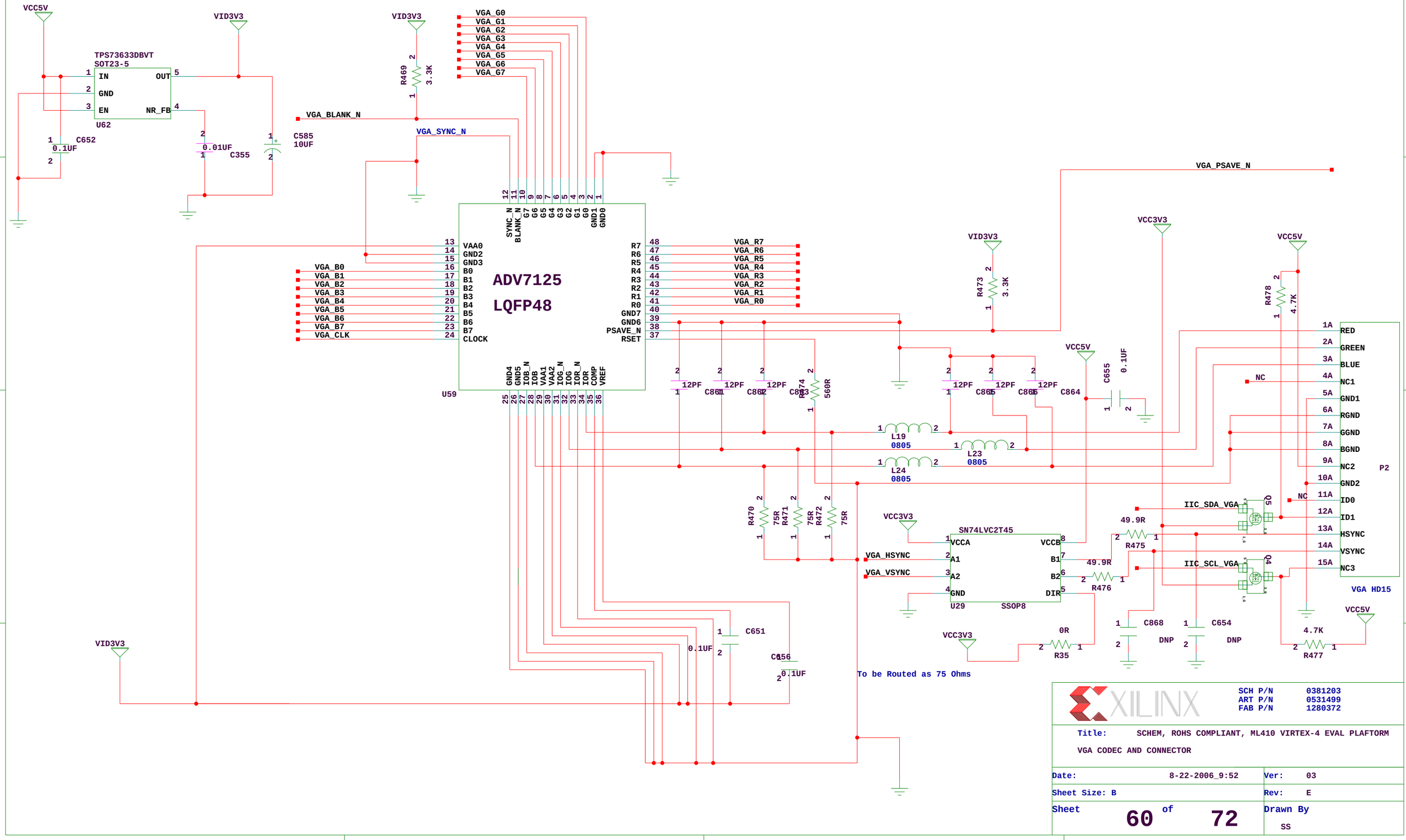


XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

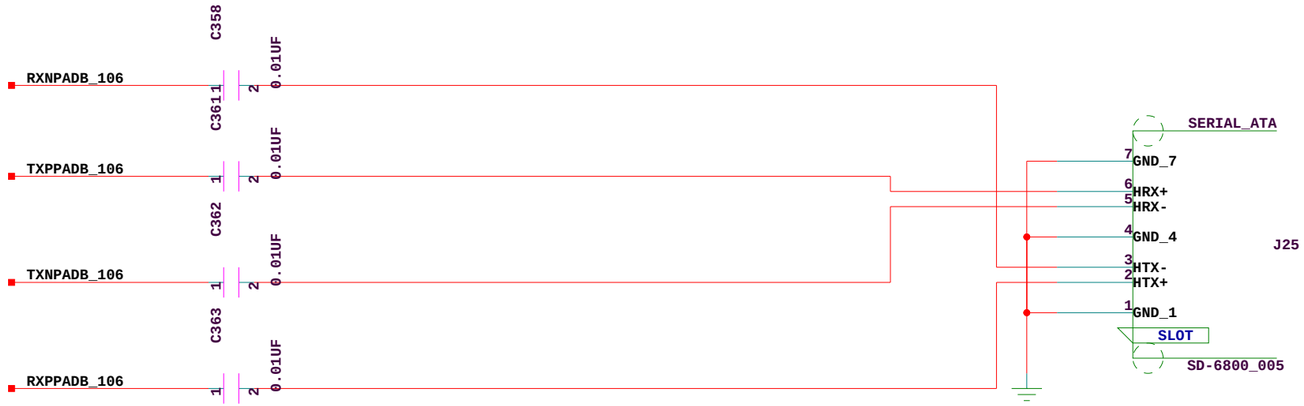
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
(R)GMII RJ-45

Date: 8-22-2006_9:52 Ver: 03
Sheet Size: B Rev: E
Sheet 59 of 72 Drawn By SS


VCC5V
VID3V3
TPS73633DBVT
SOT23-5
IN
GND
EN
OUT
NR_FB
U62
C652
0.1UF
C355
0.01UF
C585
10UF
R469
3.3K
VGA_G0
VGA_G1
VGA_G2
VGA_G3
VGA_G4
VGA_G5
VGA_G6
VGA_G7
VGA_BLANK_N
VGA_SYNC_N
VGA_PSAVE_N
SYNC_N
BLANK_N
G7
G6
G5
G4
G3
G2
G1
G0
GND1
GND0
VAA0
GND2
GND3
B0
B1
B2
B3
B4
B5
B6
B7
CLOCK
ADV7125
LQFP48
VGA_B0
VGA_B1
VGA_B2
VGA_B3
VGA_B4
VGA_B5
VGA_B6
VGA_B7
VGA_CLK
R7
R6
R5
R4
R3
R2
R1
R0
GND7
GND6
PSAVE_N
RSET
VGA_R7
VGA_R6
VGA_R5
VGA_R4
VGA_R3
VGA_R2
VGA_R1
VGA_R0
U59
GND4
GND5
IOB_N
IOB
VAA1
VAA2
IOG_N
IOG
IOR_N
IOR
COMP
VREF
12PF
C861
C862
C863
C864
R474
560R
L19
0805
L23
0805
L24
0805
R470
75R
R471
R472
C651
0.1UF
C656
0.1UF
To be Routed as 75 Ohms
VCC3V3
SN74LVC2T45
VCCA
A1
A2
GND
VCCB
B1
B2
DIR
U29
SSOP8
VGA_HSYNC
VGA_VSYNC
R473
3.3K
C655
0.1UF
R478
4.7K
NC
IIC_SDA_VGA
IIC_SCL_VGA
49.9R
R475
R476
C868
DNP
C654
DNP
0R
R35
4.7K
R477
1A
2A
3A
4A
5A
6A
7A
8A
9A
10A
11A
12A
13A
14A
15A
RED
GREEN
BLUE
NC1
GND1
RGND
GGND
BGND
NC2
GND2
ID0
ID1
HSYNC
VSYNC
NC3
P2
VGA HD15
XILINX
SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
VGA CODEC AND CONNECTOR
Date: 8-22-2006_9:52
Ver: 03
Sheet Size: B
Rev: E
Sheet 60 of 72
Drawn By
SS

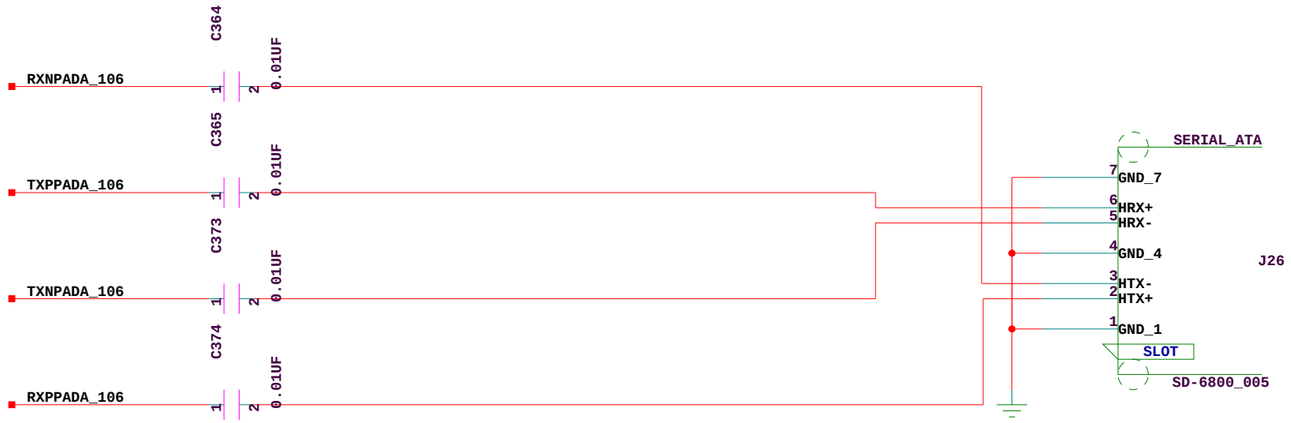
SATA Host 1

MGT 106B



SATA Host 2

MGT 106A



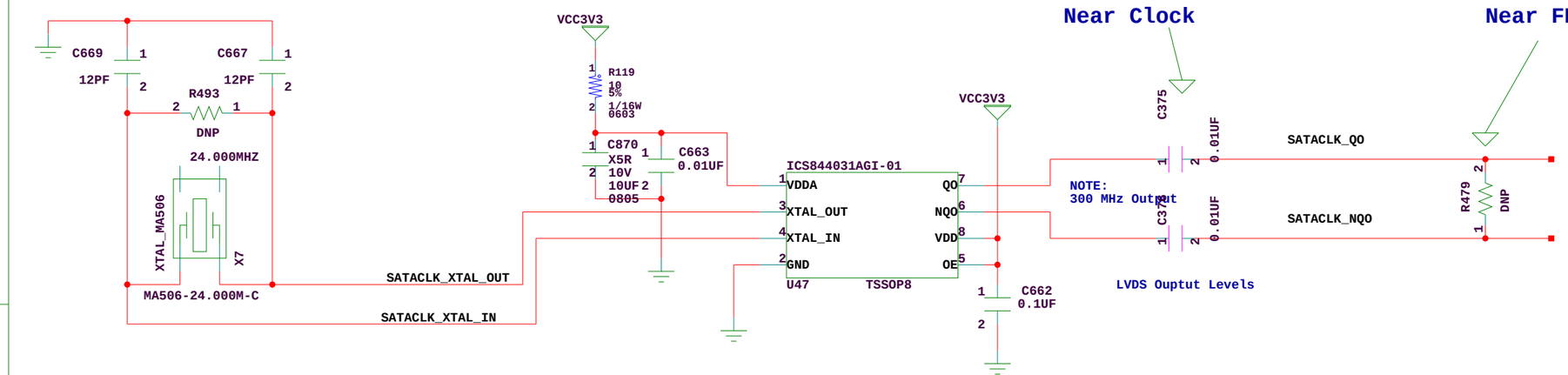
XILINX

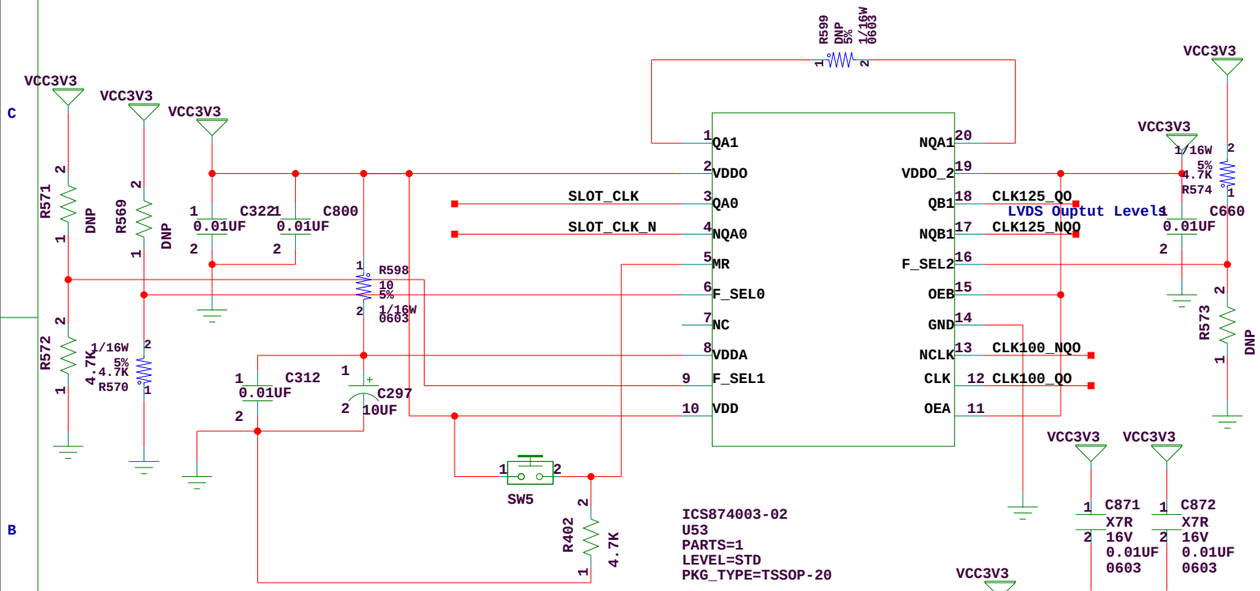
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

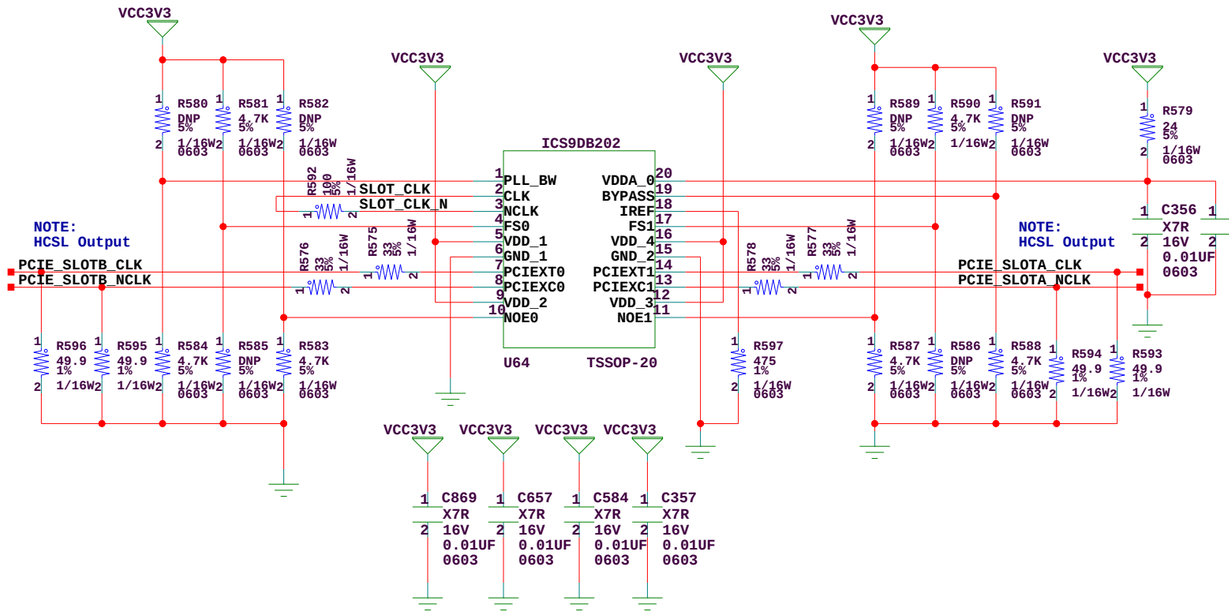
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

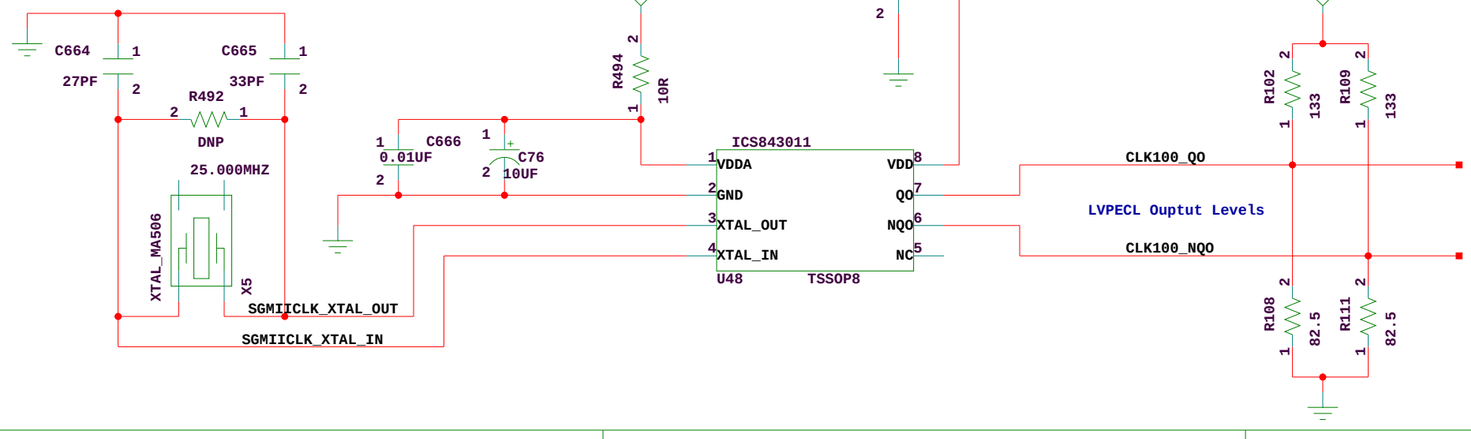
SATA INTERFACE

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet 61 of 72		Drawn By	SS









XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
SATA, 125MHZ AND PCIEXPRESS CLKS

Date: 8-22-2006_11:34 Ver: 03
Sheet Size: B Rev: E
Sheet 62 of 72 Drawn By SS

MGT 102B

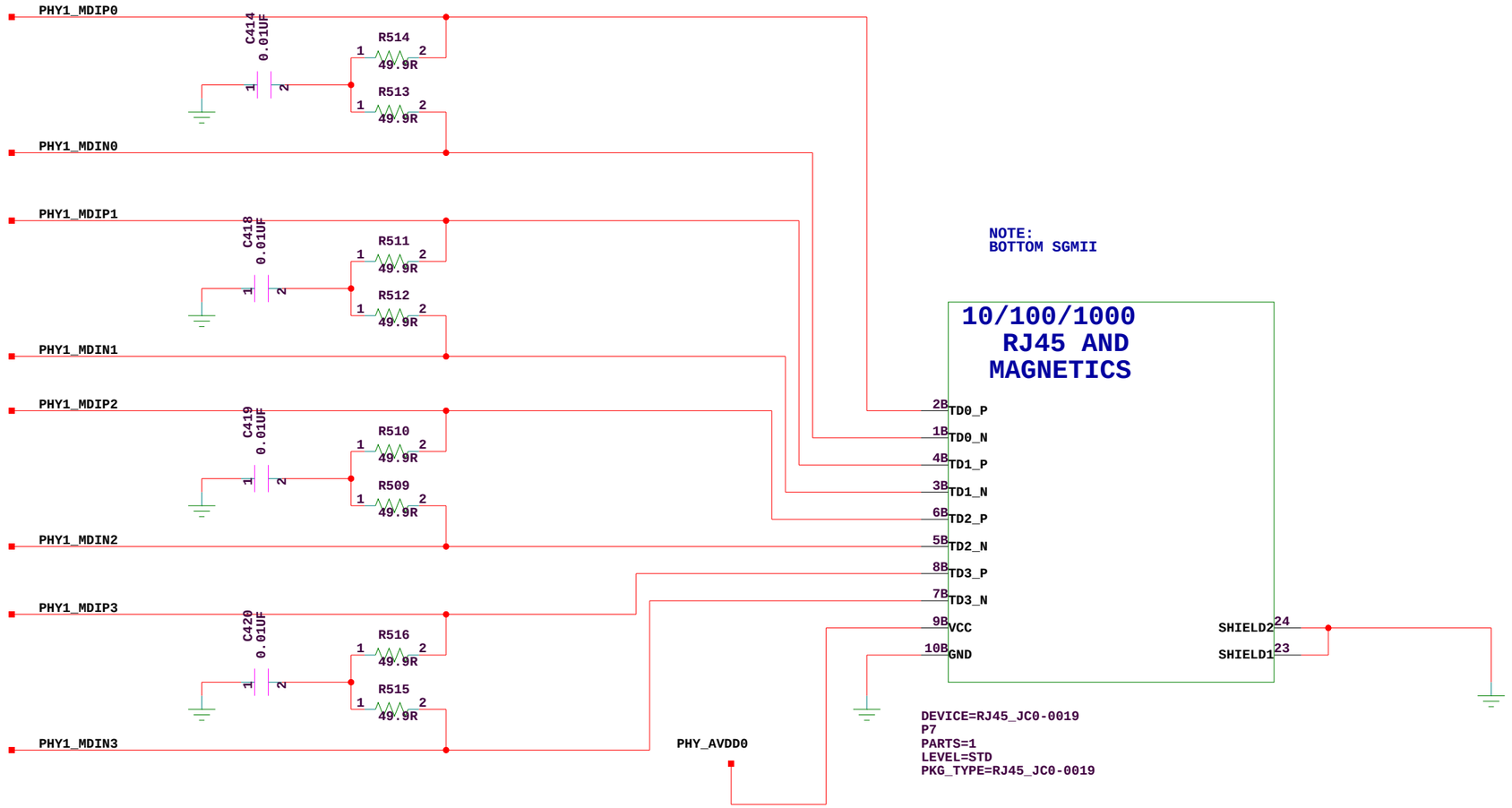
NOTE:
PHY ADDR = ‘00111’

DEVICE=M88E1111
U61
PARTS=1

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
SGMII TRI-MODE ETHERNET PHY

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	63 of 72	Drawn By	SS

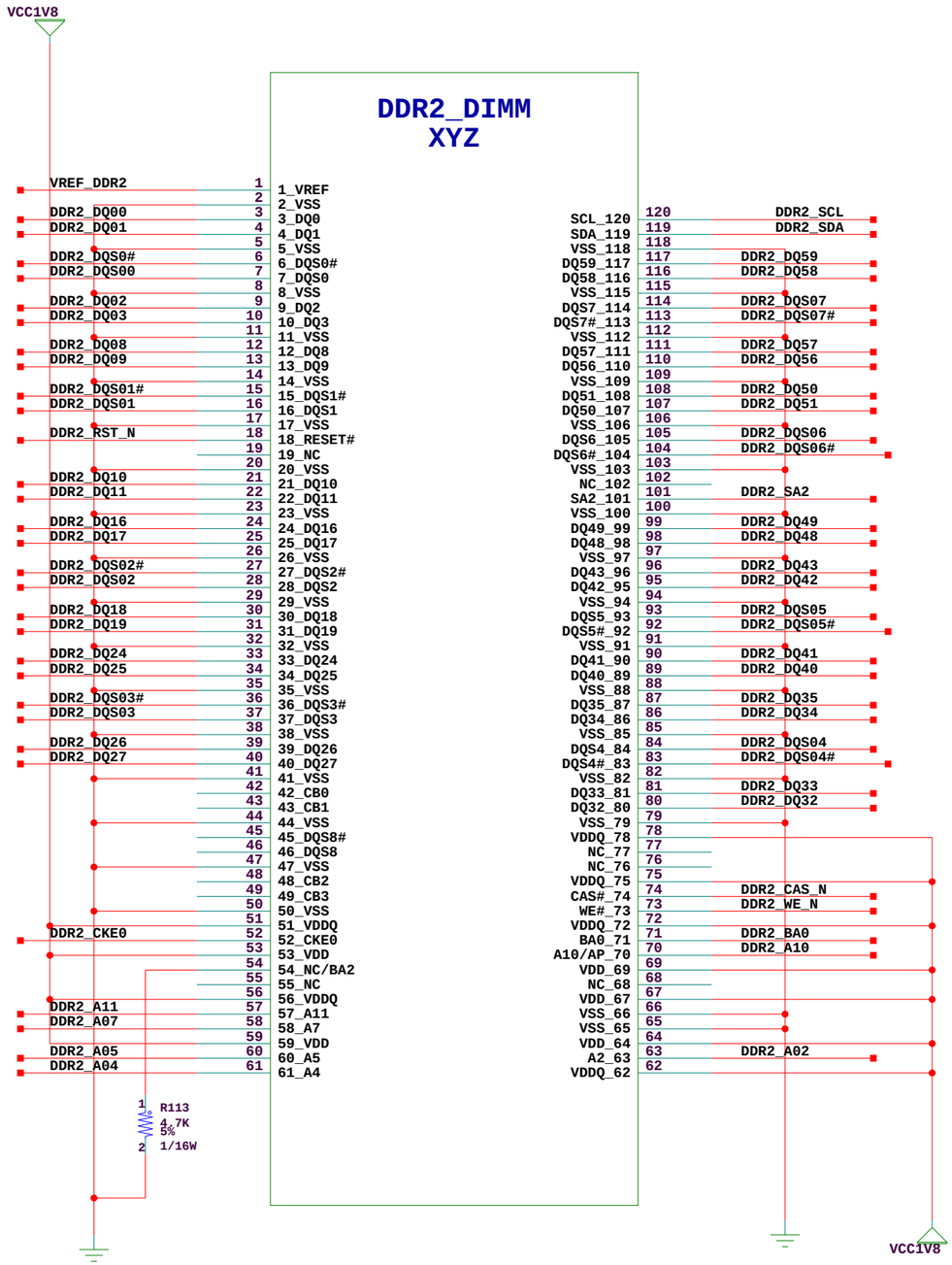


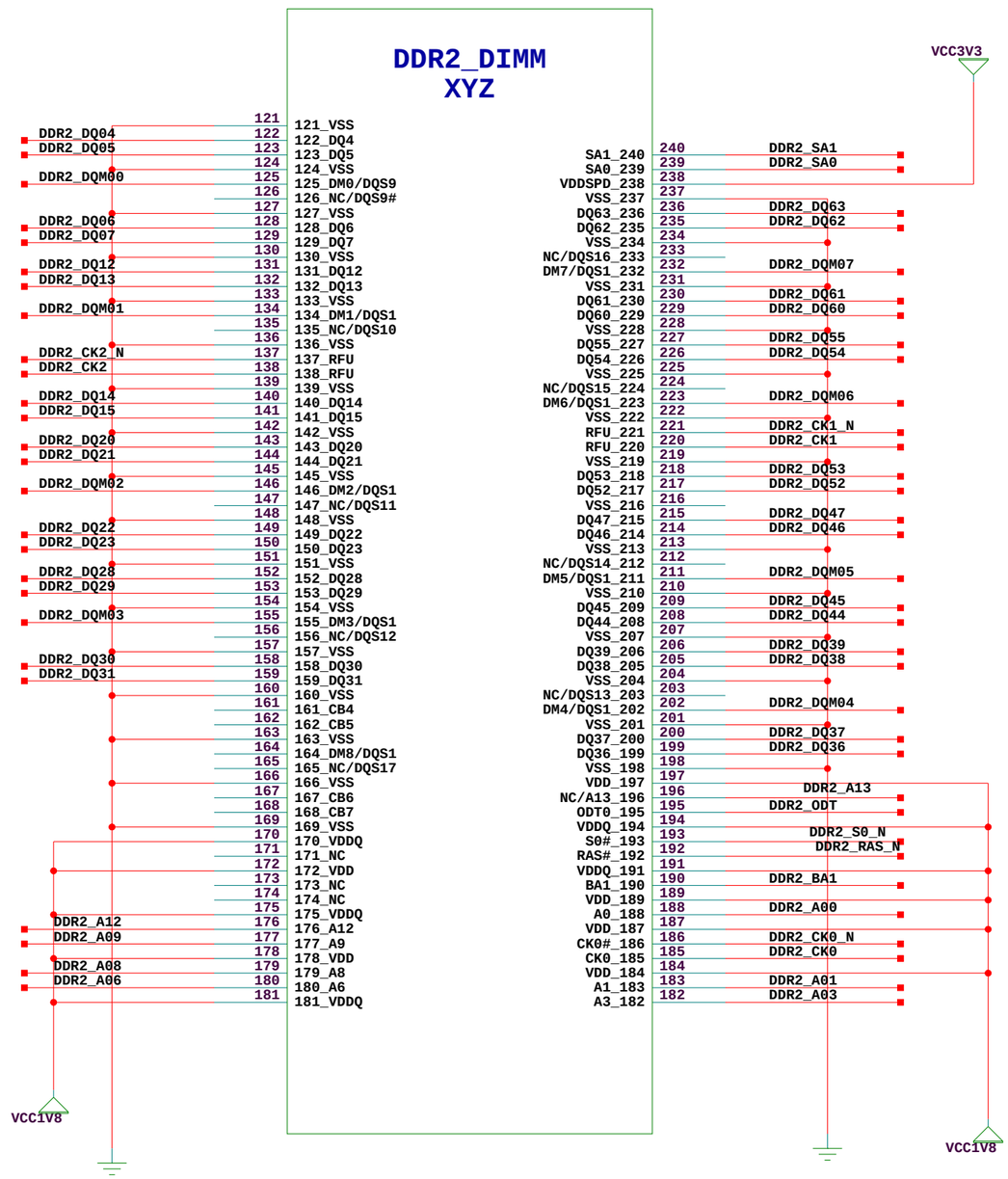
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

SGMII RJ-45

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	64 of 72	Drawn By	SS





XILINX

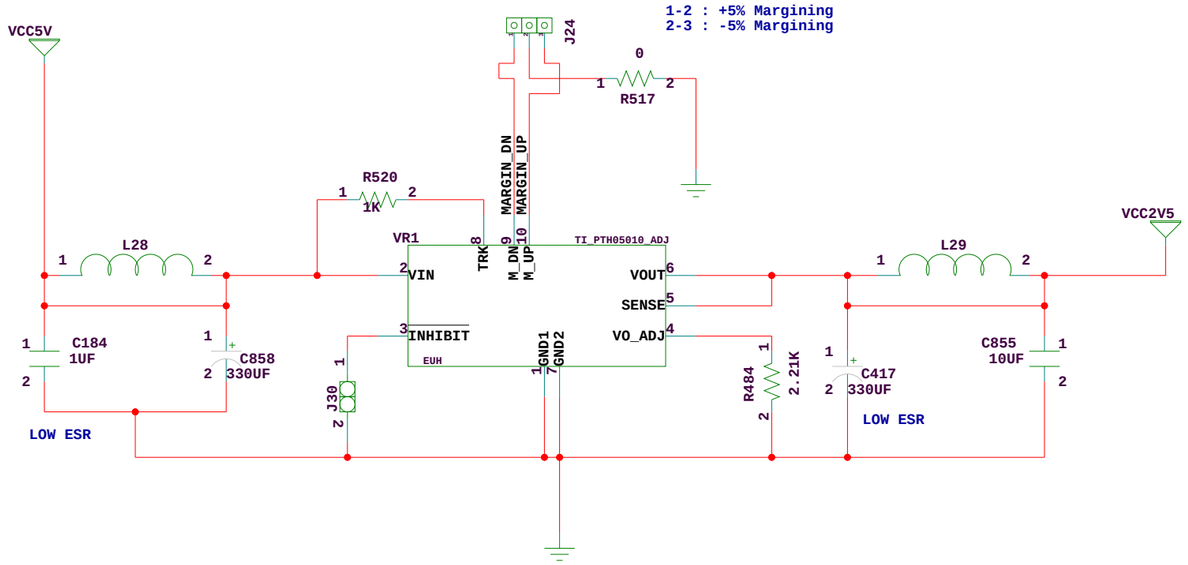
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

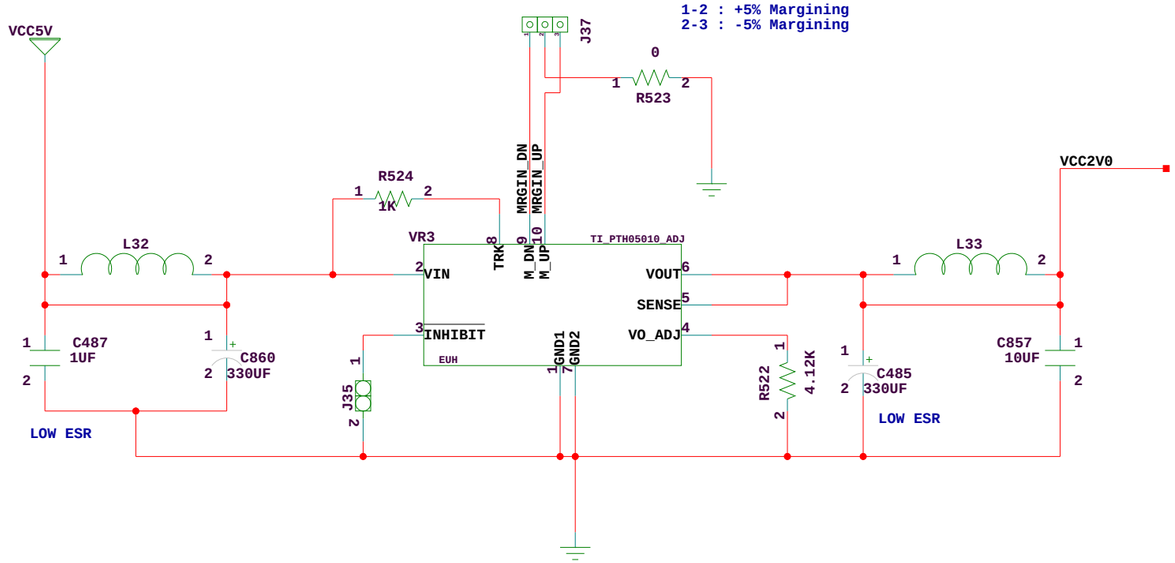
DDR2 DIMM CONNECTOR

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	65 of 72	Drawn By	SS

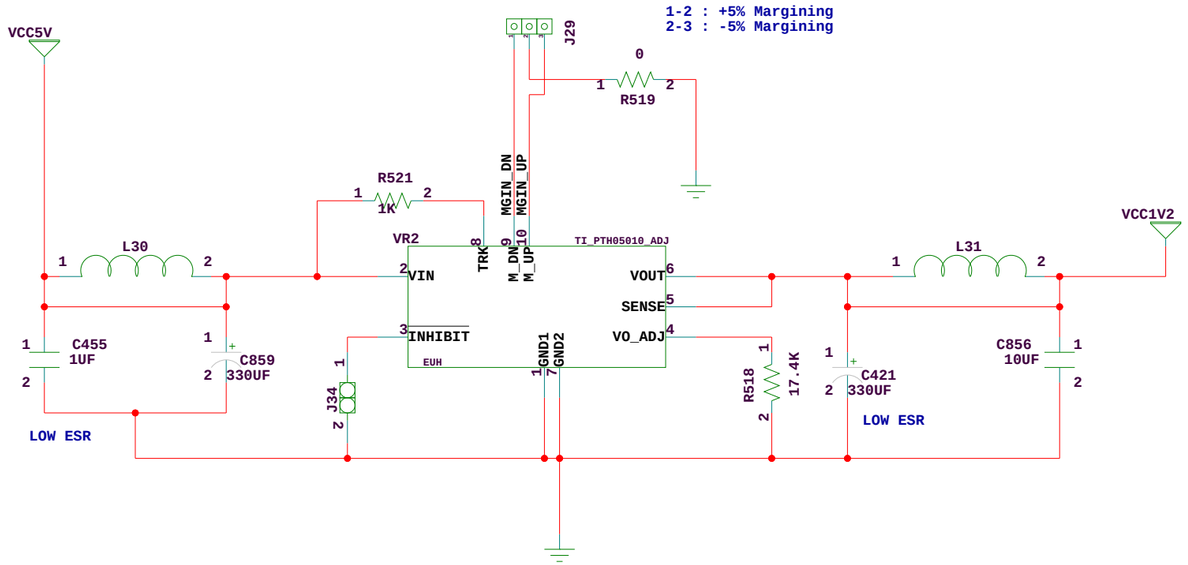
2.5V Supply @15A

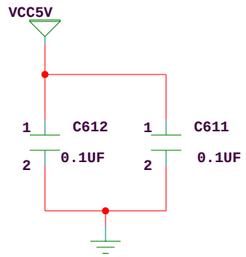


2.0V Supply @15A



1.2V Supply @15A





RSET=10K*(0.8V/(VOUT-0.8V)-2.49K
Vout=(8K/(RSET+2.49K))+0.8V

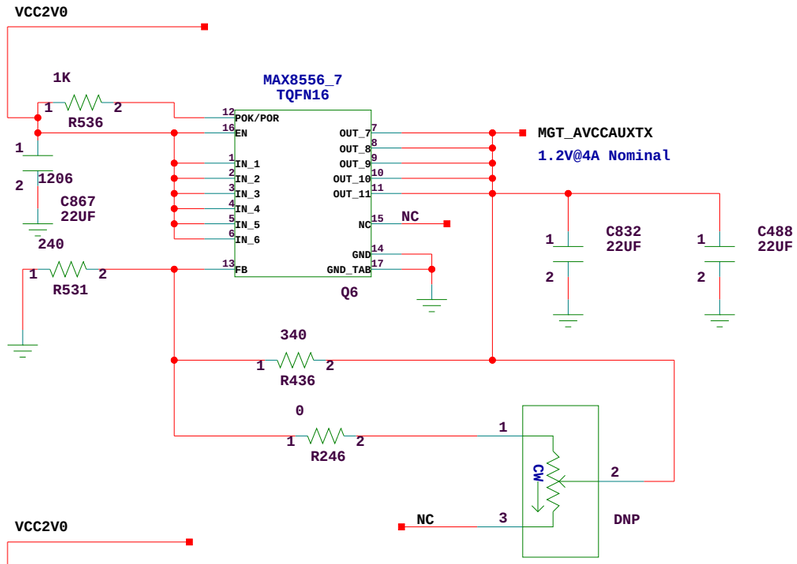
For 2.0V, R29 = 4.176K

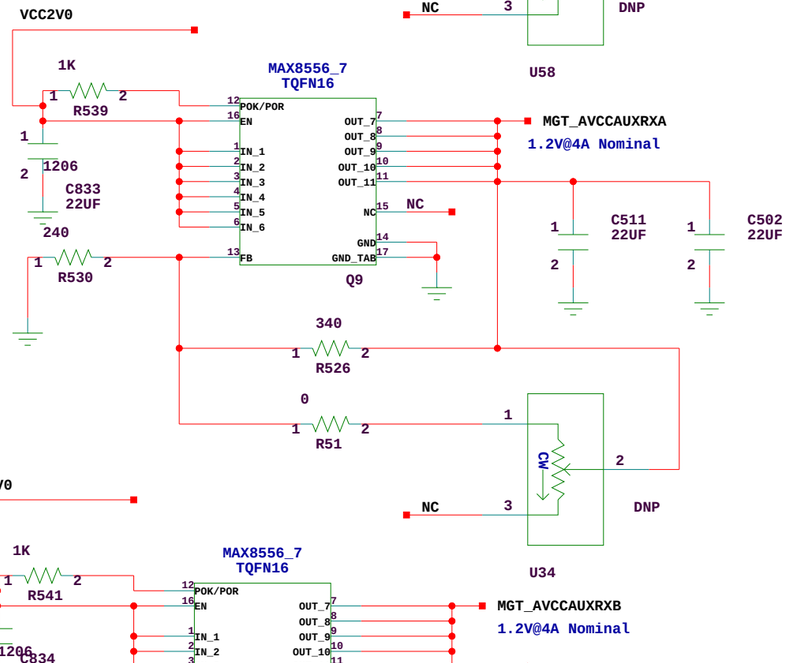
XILINX

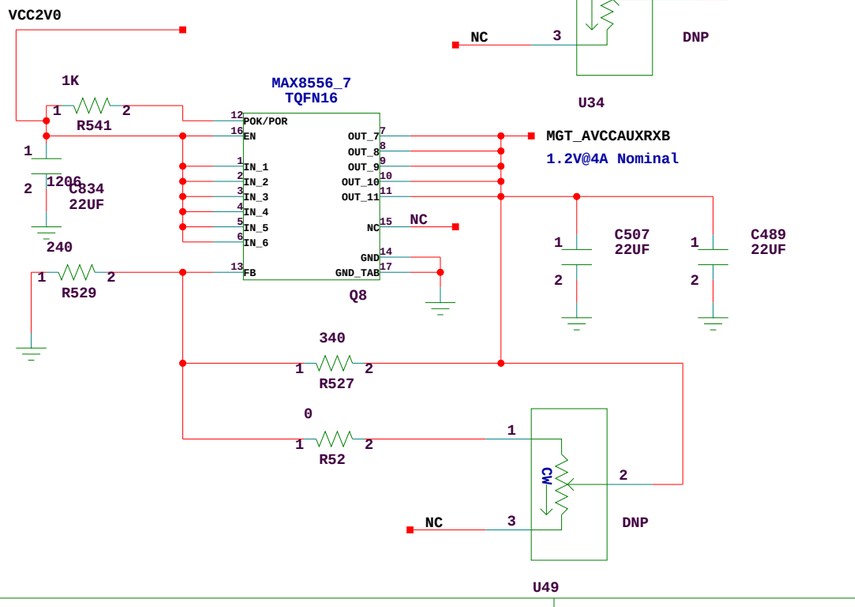
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

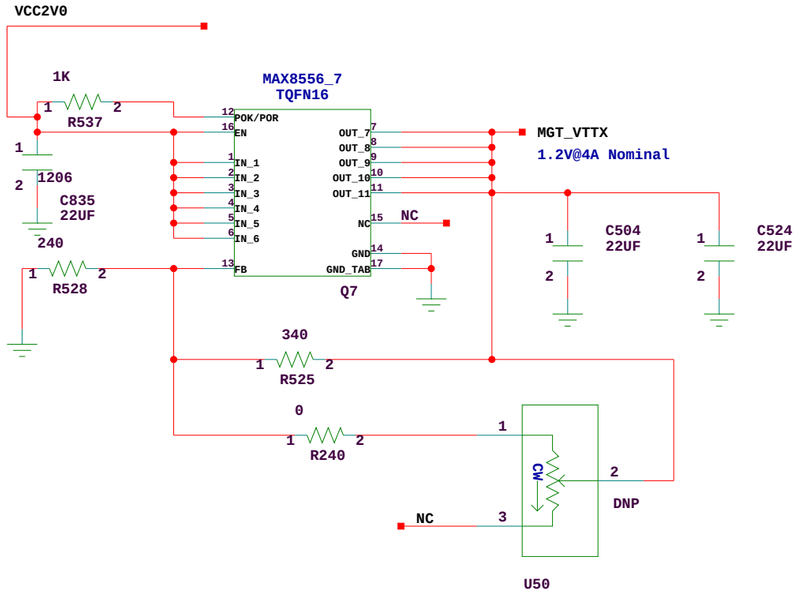
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
FPGA CORE AND IO VOLTAGE

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	66 of 72	Drawn By	SS

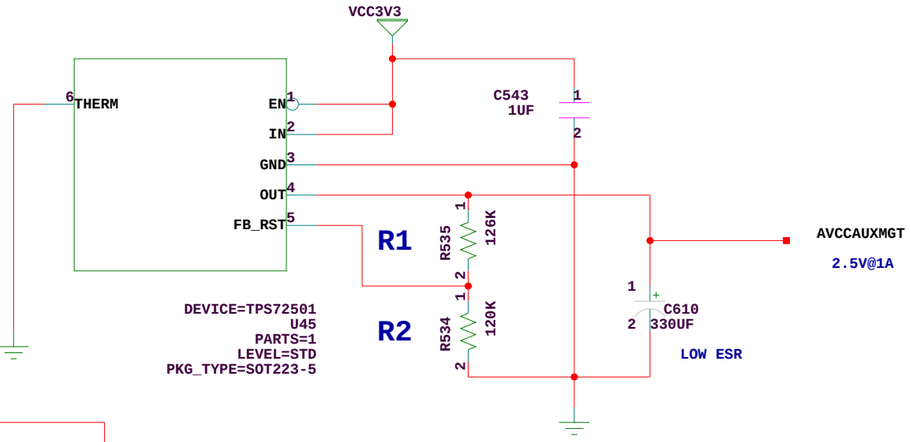


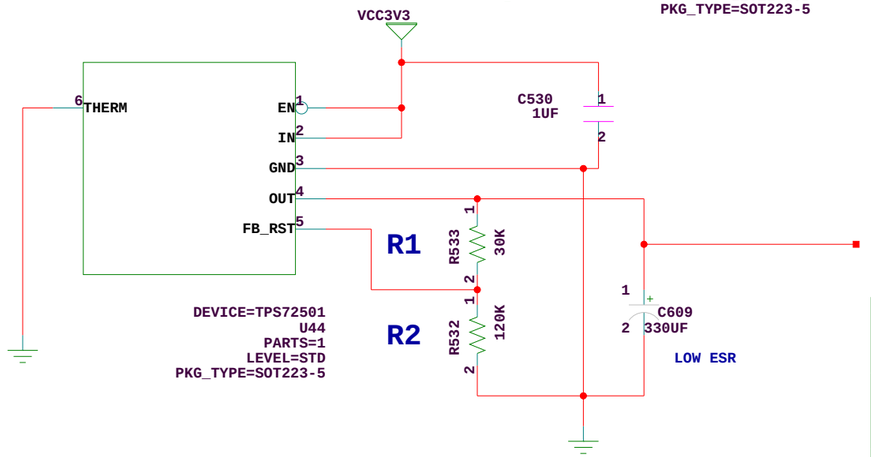






R2 = R1*{(Vout/0.5)-1}





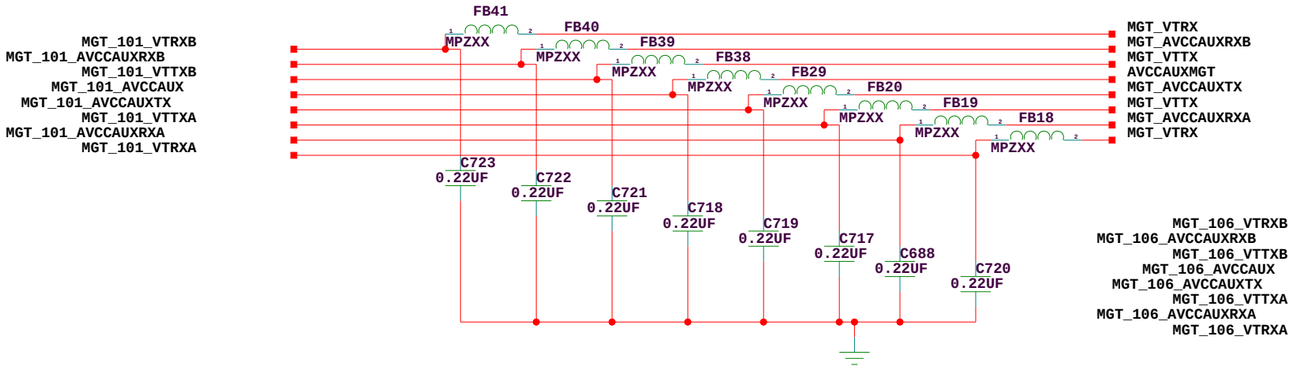
XILINX

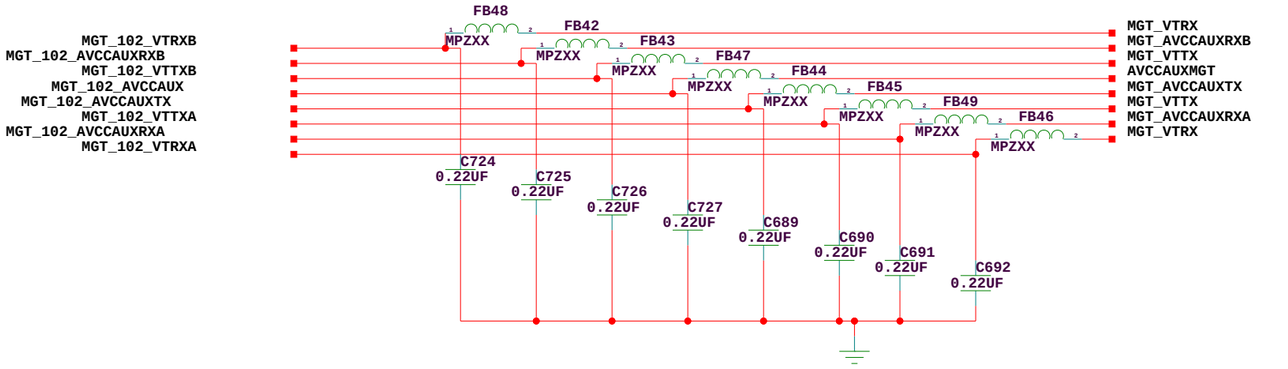
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

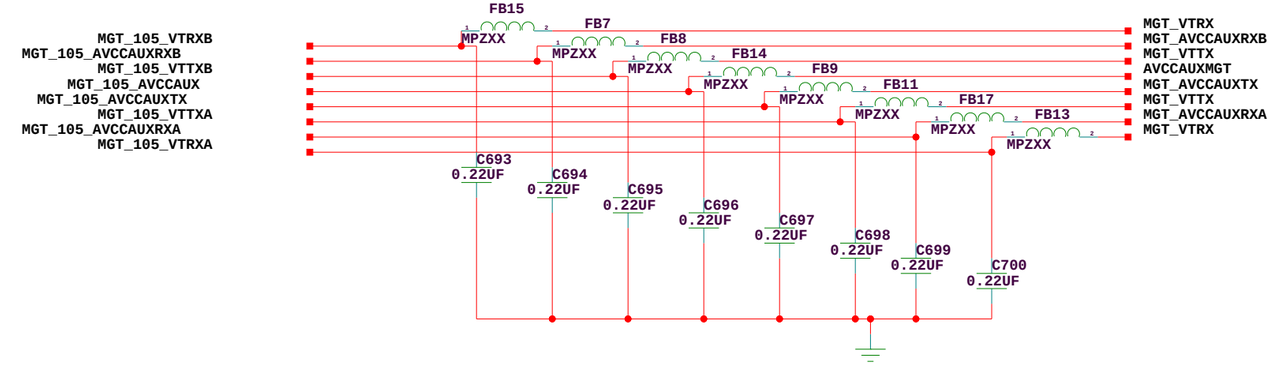
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

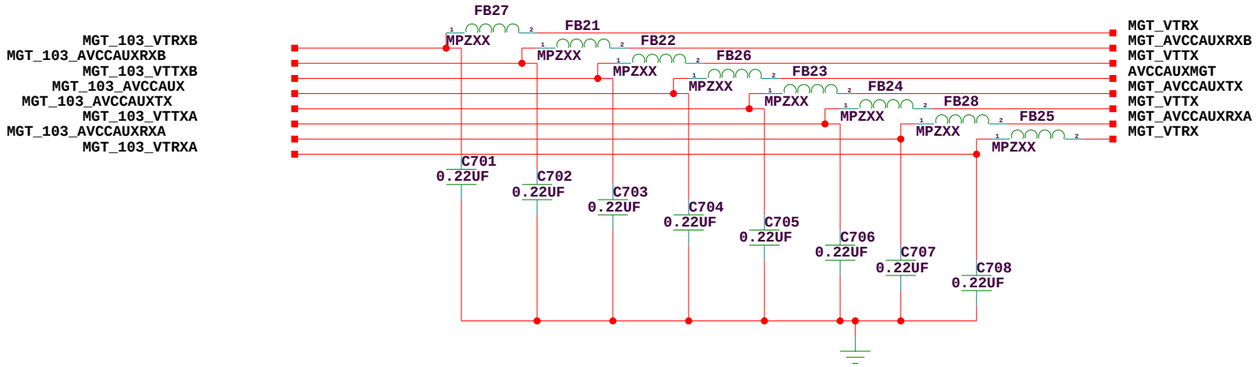
MGT POWER SUPPLIES

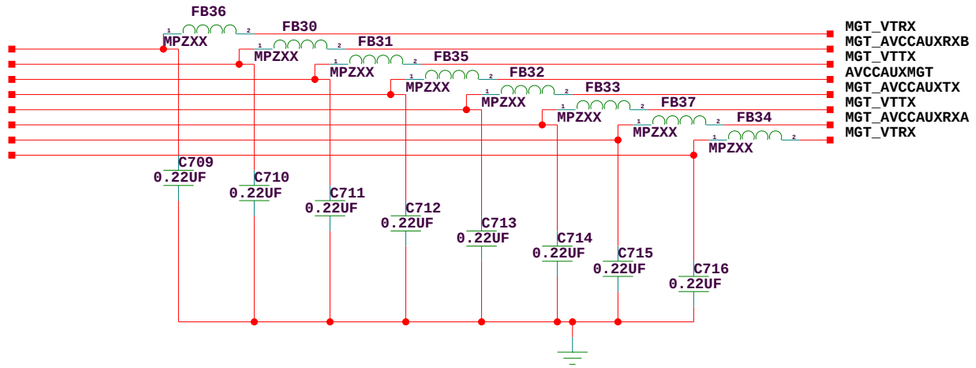
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	67 of 72	Drawn By	SS

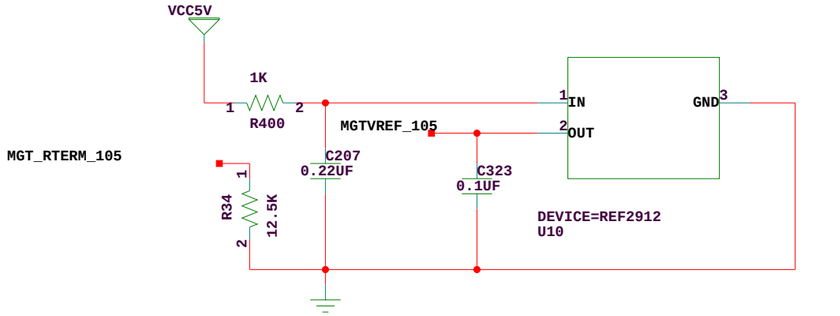


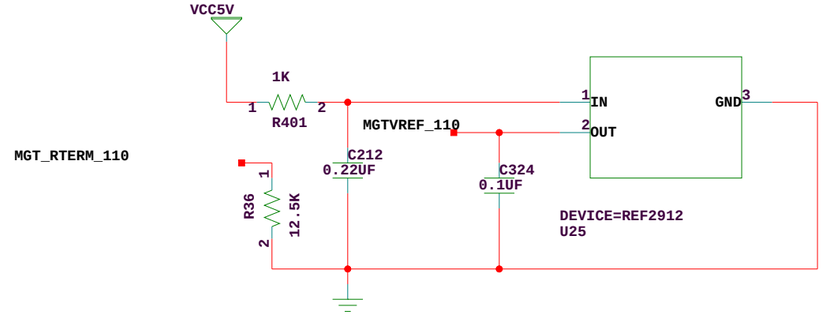












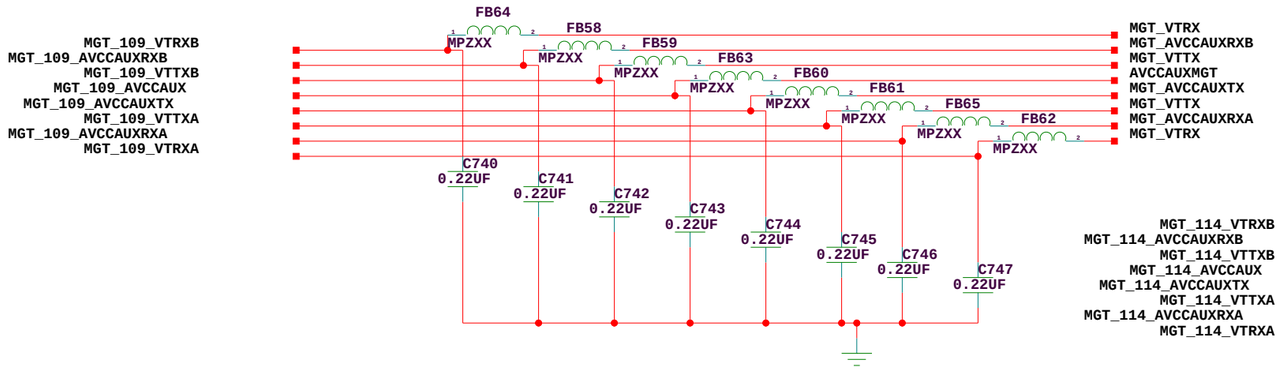
XILINX

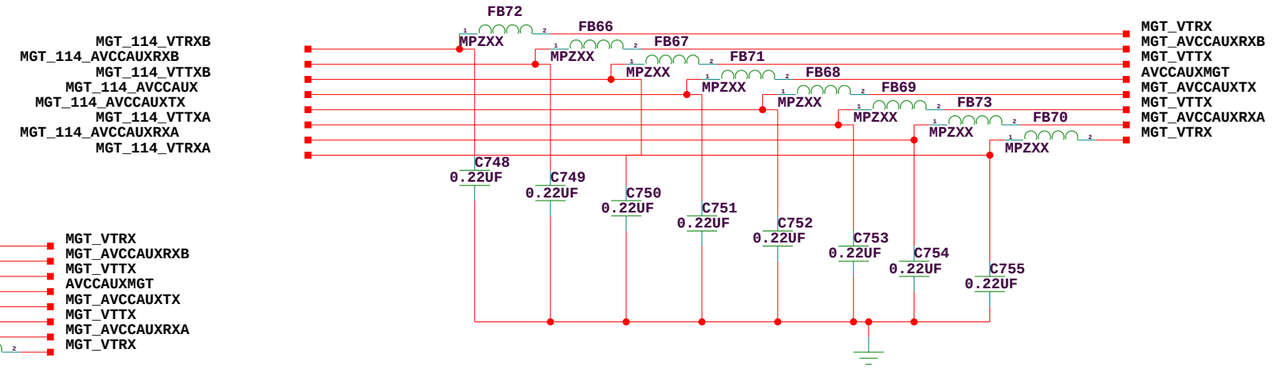
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

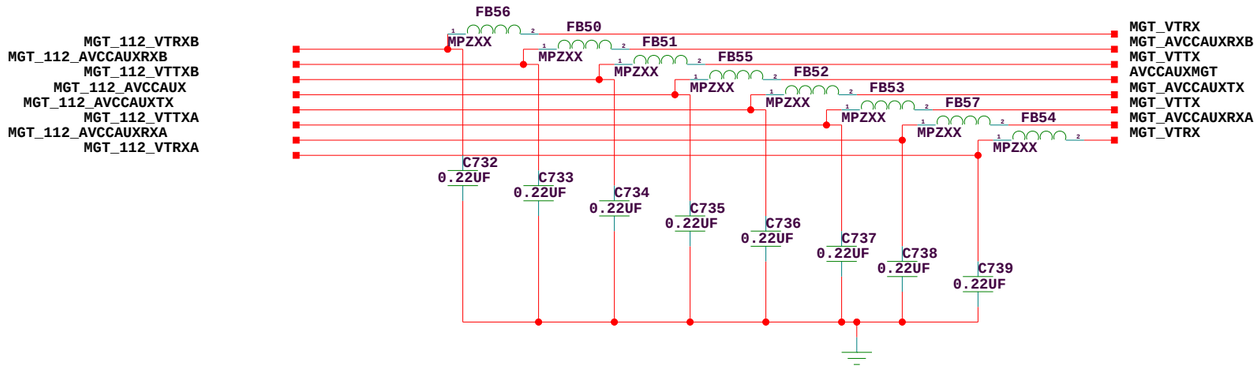
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

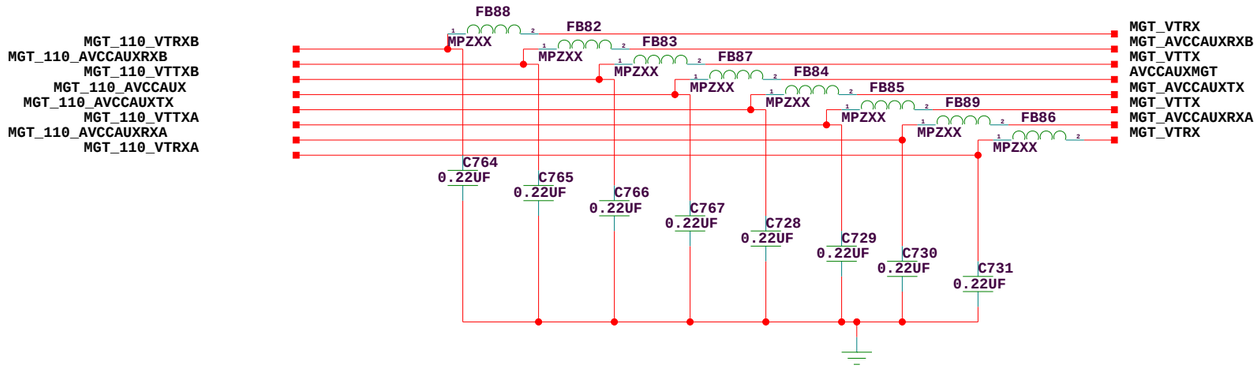
MGT POWER FILTER-1, VTERM AND RTERM

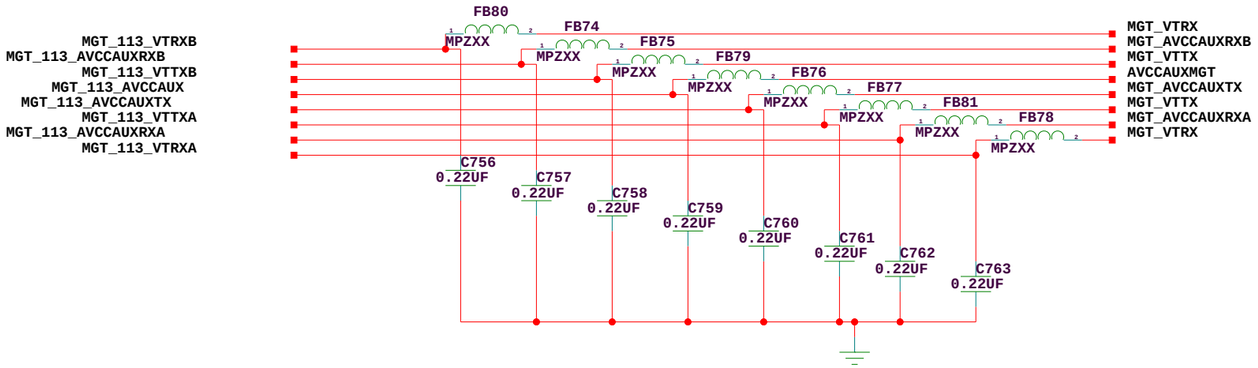
Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	68 of 72	Drawn By	SS











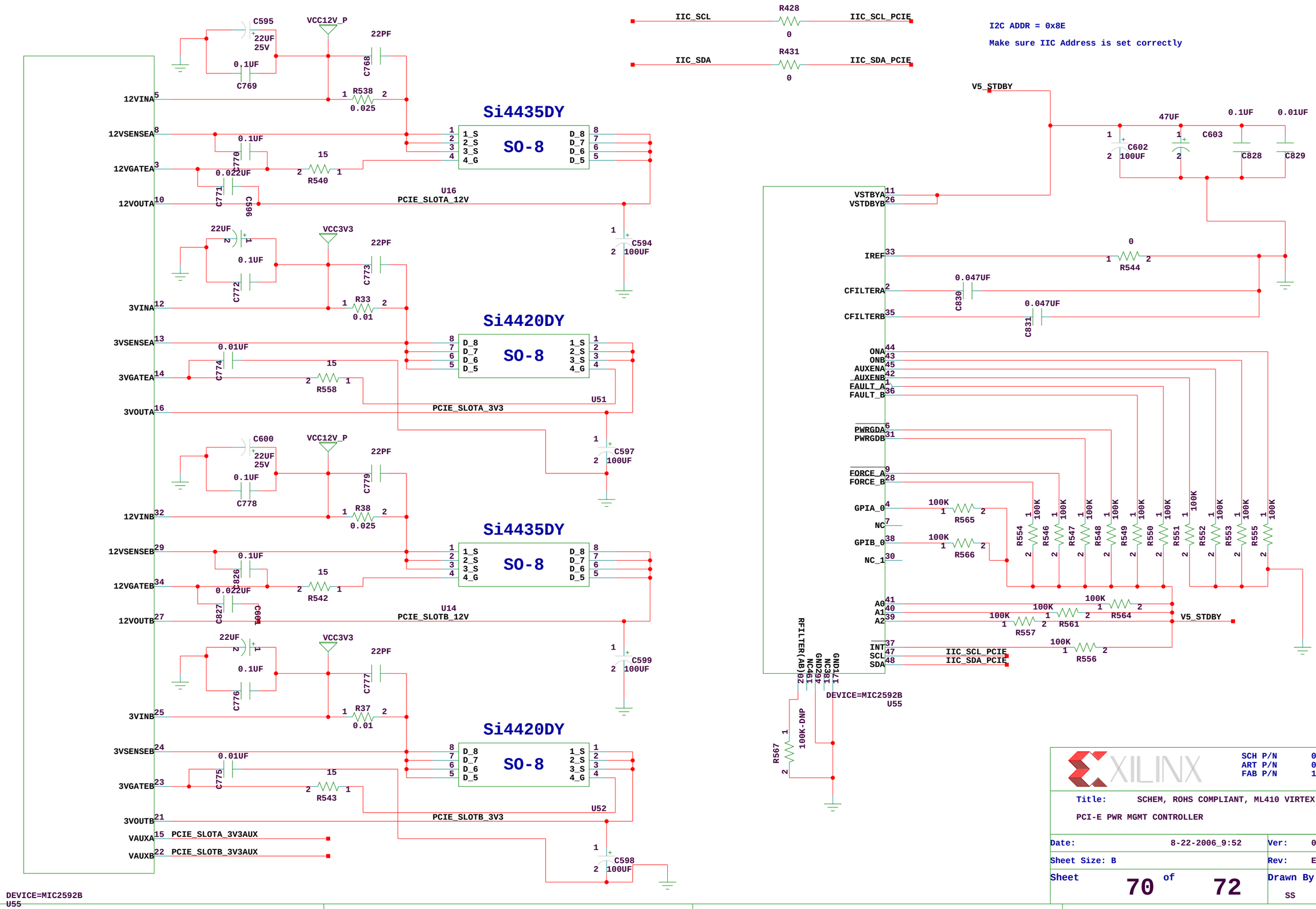
XILINX

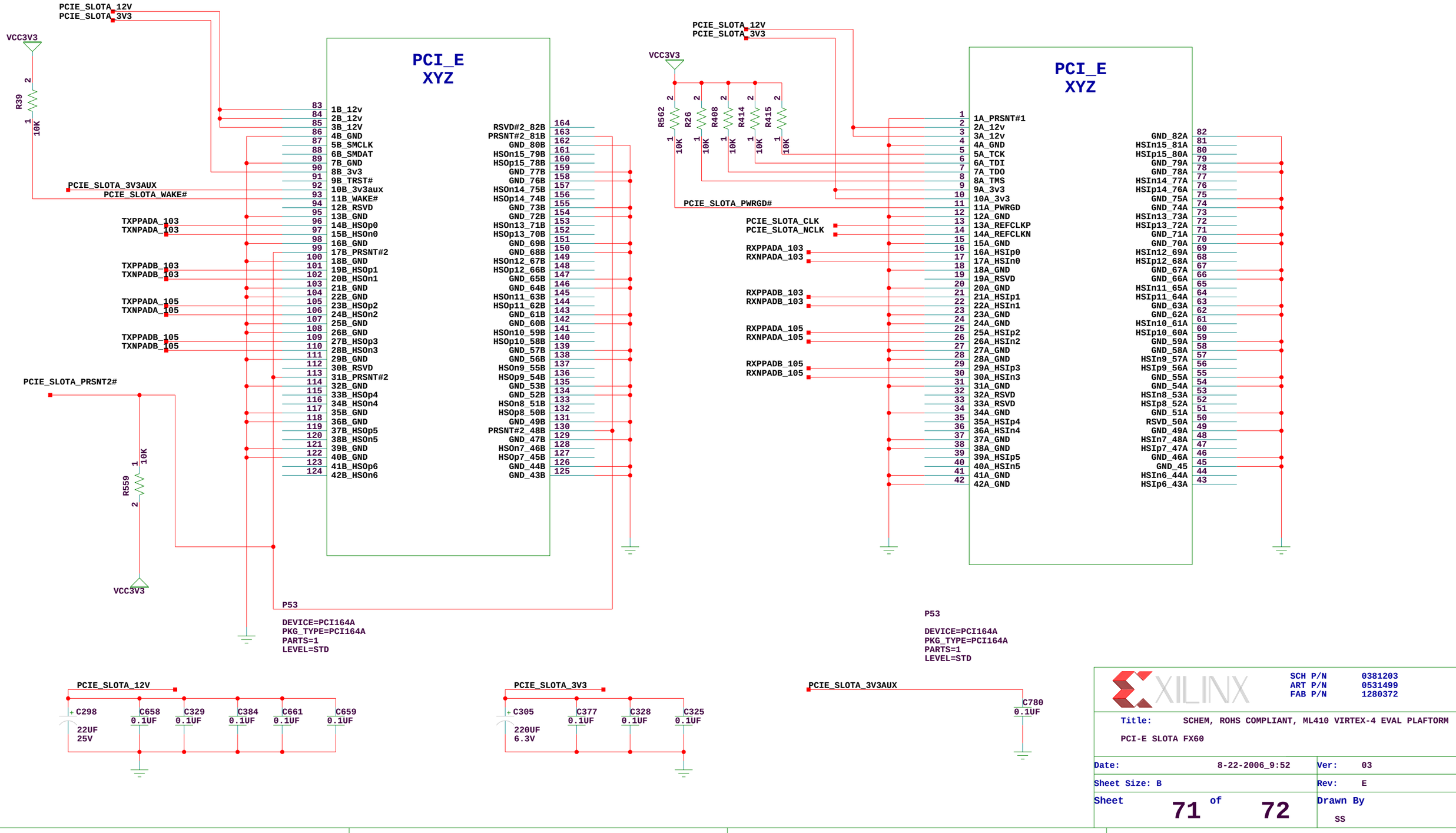
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT POWER FILTER-2

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	69 of 72	Drawn By	SS


C595
22UF
25V
0.1UF
C769
VCC12V_P
22PF
C768
12VINA
R538
0.025
Si4435DY
SO-8
12VSENSEA
0.1UF
C770
12VGATEA
15
R540
0.022UF
C771
C596
12VOUTA
U16
PCIE_SLOTA_12V
C594
100UF
22UF
0.1UF
C772
VCC3V3
22PF
C773
3VINA
R33
0.01
Si4420DY
SO-8
3VSENSEA
0.01UF
C774
3VGATEA
15
R558
U51
3VOUTA
PCIE_SLOTA_3V3
C597
100UF
C600
22UF
25V
0.1UF
C778
VCC12V_P
22PF
C779
12VINB
R38
0.025
Si4435DY
SO-8
12VSENSEB
0.1UF
C826
12VGATEB
15
R542
0.022UF
C827
C603
12VOUTB
U14
PCIE_SLOTB_12V
C599
100UF
22UF
0.1UF
C776
VCC3V3
22PF
C777
3VINB
R37
0.01
Si4420DY
SO-8
3VSENSEB
0.01UF
C775
3VGATEB
15
R543
U52
3VOUTB
PCIE_SLOTB_3V3
VAUXA
PCIE_SLOTA_3V3AUX
VAUXB
PCIE_SLOTB_3V3AUX
C598
100UF
DEVICE=MIC2592B
U55
IIC_SCL
R428
0
IIC_SCL_PCIE
IIC_SDA
R431
0
IIC_SDA_PCIE
I2C ADDR = 0x8E
Make sure IIC Address is set correctly
V5_STDBY
47UF
0.1UF
0.01UF
C602
100UF
C603
C828
C829
VSTBYA
VSTDBYB
IREF
R544
0
CFILTERA
0.047UF
C830
CFILTERB
0.047UF
C831
ONA
ONB
AUXENA
AUXENB
FAULT_A
FAULT_B
PWRGDA
PWRGDB
FORCE_A
FORCE_B
GPIA_0
R565
100K
NC
GPIB_0
R566
100K
NC_1
R554
R546
R547
R548
R549
R550
R551
R552
R553
R555
A0
A1
A2
R557
R561
R564
V5_STDBY
INT
SCL
SDA
IIC_SCL_PCIE
IIC_SDA_PCIE
R556
RFILTER(AB)
R567
100K-DNP
DEVICE=MIC2592B
U55
XILINX
SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
PCI-E PWR MGMT CONTROLLER
Date: 8-22-2006_9:52
Ver: 03
Sheet Size: B
Rev: E
Sheet 70 of 72
Drawn By
SS

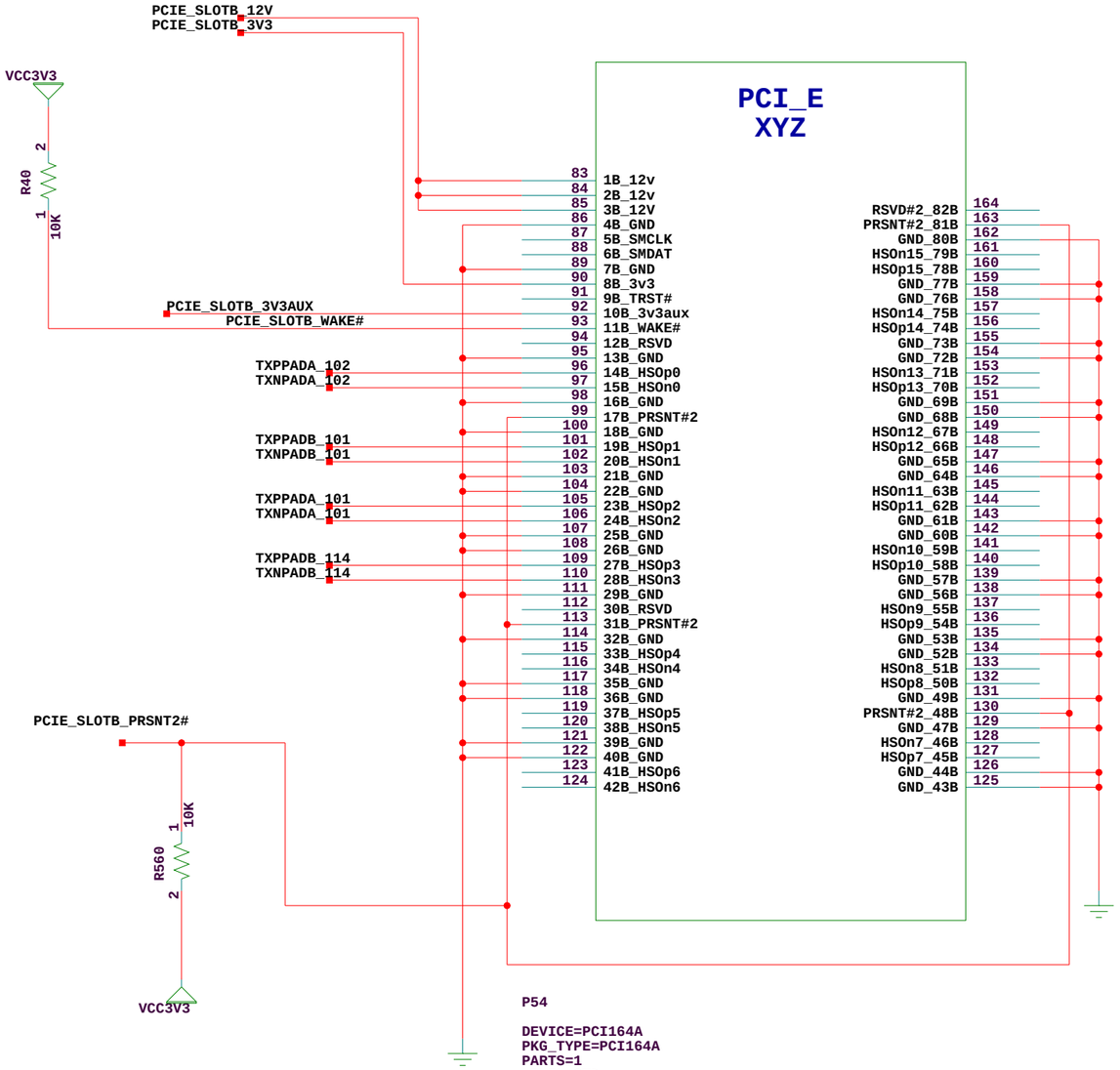


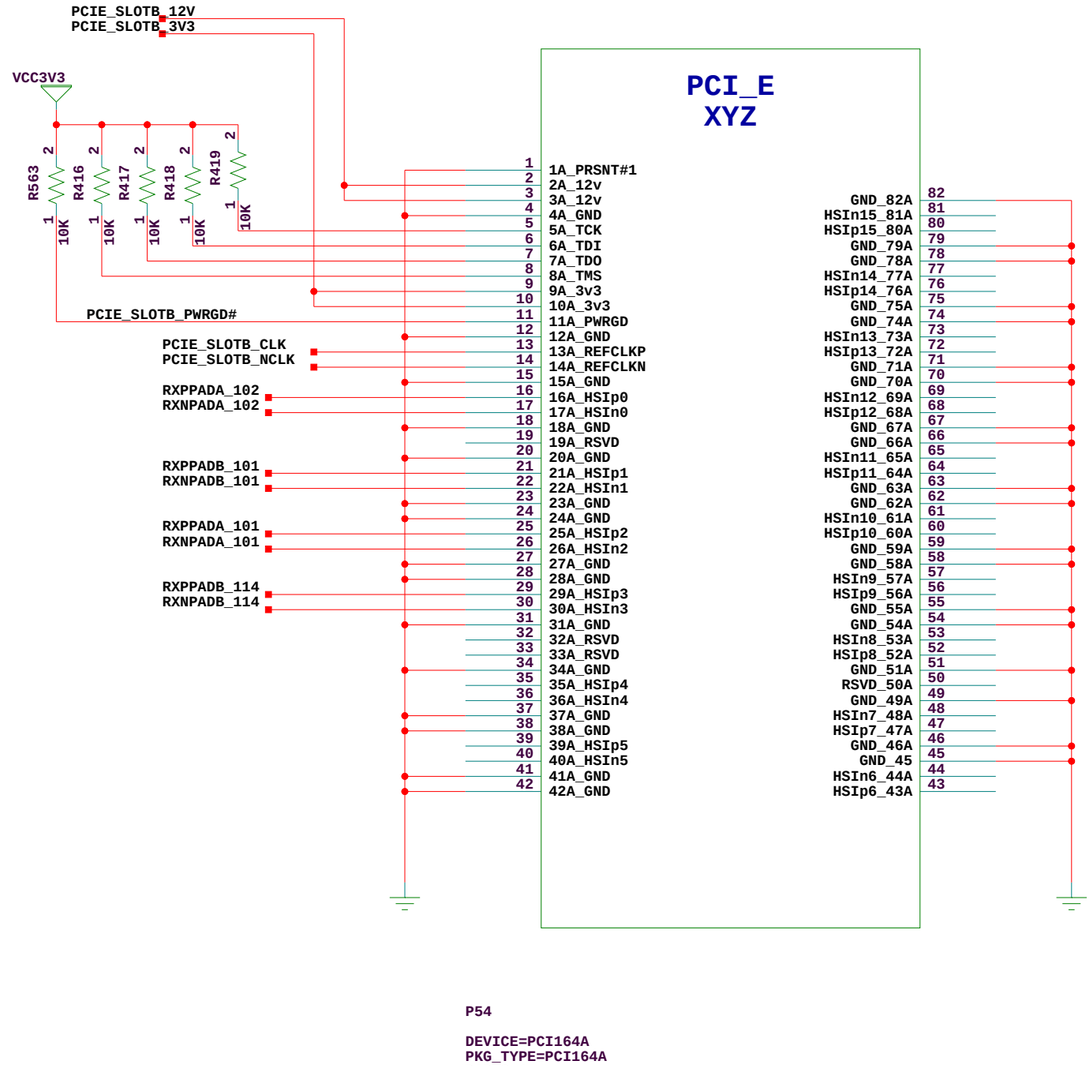
SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

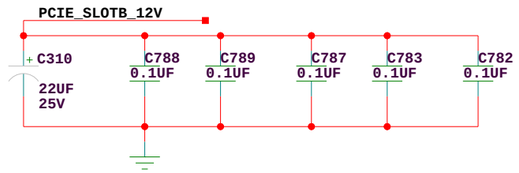
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

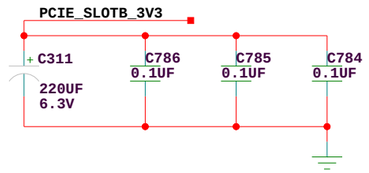
PCI-E SLOTA FX60

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	71 of 72	Drawn By	SS









XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOTB FX100

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	72 of 72	Drawn By	SS