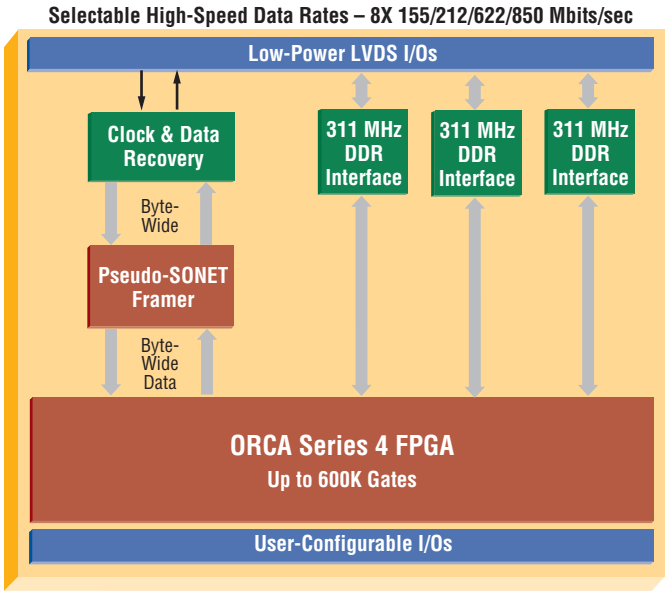
ORCA ORT8850

8-Channel High-Speed Serial Backplane Driver

Lattice has developed a solution for designers who need the many advantages of FPGA-based design implementation, coupled with high-speed serial backplane data transfer. Built on the ORCA® Series 4 reconfigurable embedded system-on-a-chip (SoC) architecture, the ORT8850 family is made up of backplane transceivers containing eight channels, each operating at up to 850 Mbits/s (6.8 Gbits/s when all eight channels are used) full-duplex synchronous interface, with built-in clock and data recovery (CDR) in standard-cell logic, along with up to 600K usable FPGA system gates.

The ORT8850 family offers a clockless high-speed interface for inter-device communication, on a board or across a backplane. The built-in clock recovery of the ORT8850 allows higher system performance, easier- to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will also benefit from the backplane transceiver as a network termination device. The backplane transceiver offers SONET scrambling/descrambling of data and streamlined SONET framing, pointer moving, and transport overhead handling, plus the programmable logic to terminate the network into proprietary systems. For non-SONET applications, all SONET functionality is hidden from the user and no prior networking knowledge is required.

ORCA ORT8850 Block Diagram



Also included on the device are three full-duplex, high-speed parallel interfaces, consisting of 8-bit data, control (such as start-of-cell), and clock. The interface delivers double data rate (DDR) data at rates up to 311 MHz (622 Mbits/s per pin), and converts this data internal to the device into 32-bit wide data running at half rate on one clock edge. Functions such as centering the transmit clock in the transmit data eye are done automatically by the interface. Applications delivered by this interface include a parallel backplane interface similar to the RapidIO packet-based interface.

Key Features and Benefits

- **High Performance ORCA Series 4 FPGA Gates:**
  - Internal performance of > 250 MHz.
  - Up to 600K usable system gates (with ORT8850H).
  - 1.5 V operation (30% less power than 1.8 V operation)
  - Comprehensive I/O selections including LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL3/2, HSTL, ZBT, DDR, LVDS, bused-LVDS, and LVPECL.
- **Ease of Design**
  - Supported by ORCA Foundry 2001 design software
  - Complete ORT8850 design kit supplies simulation models for embedded core, configuration tool, and integrates with ORCA Foundry 2001

ORCA ORT8850 Attributes

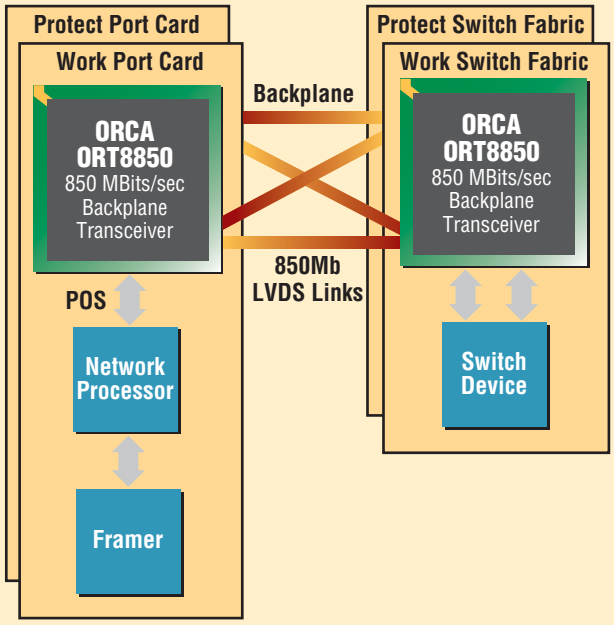
Device	Usable Gates	PFUs	LUTs	Registers	PFU RAM Bits	EBR RAM Bits	Available User I/O 352PBGA	Available User I/O 680PBGAM	I/O Compatibility	PLLs	SERDES Channels	Maximum Data Rate
ORT8850L	360-470K	624	4,992	6,504	154K	74K	161	278	1.8 / 2.5 / 3.3V	4	8	850 Mbits/sec
ORT8850H	530-600K	2,024	16,192	19,824	406K	147K	N/A	297	1.8 / 2.5 / 3.3V	4	8	850 Mbits/sec

Key Features and Benefits (cont.)

- **Easy System Integration**
  - Supports wide range of SONET-based backplane applications as well as generic data moving for high-speed backplane data transfer. No knowledge of SONET/SDH needed in generic applications: simply supply data, 63 MHz-106 MHz clock, and a frame pulse.
  - High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
  - Eight-channel HSI function provides 850 Mbits/s serial interface per channel for a total chip bandwidth of 6.8 Gbits/s (full duplex). Rates from 126 Mbits/s to 850 Mbits/s are supported directly (lower rates directly supported through decimation and interpolation).
  - Powerdown option of HSI receiver on a per-channel basis.
  - SONET scrambler/descrambler.
  - Three full-duplex, double data rate (DDR) I/O groups include 8-bit data, one control, and one clock. Each interface is implemented with LVDS I/Os that include on-board termination to allow long-haul driving of backplanes, such as those similar to the industry standard RapidIO interface.
  - Redundant outputs and multiplexed redundant inputs for CDR I/Os allow implementation of eight channels with redundancy on a single device.
  - On-chip, phase-lock loop (PLL) clock meets B jitter tolerance specification of ITU-T recommendation G.958.
  - FIFOs align incoming data across all eight channels (two groups of four channels or four groups of two channels). Optional ability to bypass alignment FIFOs.
  - 1 + 1 protection supports STS-12/STS-48 redundancy by either software or hardware control for protection switching applications. STS-192 and above rates are supported through multiple devices.

ORT8850 Application – 4 Gbits/sec Serial Backplane for Switching

- SERDES operates at up to 850 Mbits/sec. With one ORT8850 on port-card and one on switch-card, 4 Gbits/sec throughput achieved
- 850 Mbits/sec with SONET scrambling (3.3% overhead) allows > 800 Mbits/sec raw data transfer
- Packet-Over-SONET (POS) or RapidIO-like interface to Network Processor on port card



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