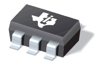


36V, SINGLE-SUPPLY, GENERAL-PURPOSE OPERATIONAL AMPLIFIER

Check for Samples: OPA171-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3A**
- **Supply Range: +2.7V to +36V, ±1.35V to ±18V**
- **Low Noise: 14nV/$\sqrt{Hz}$**
- **Low Offset Drift: ±0.3μV/°C (typ)**
- **RFI Filtered Inputs**
- **Input Range Includes the Negative Supply**
- **Input Range Operates to Positive Supply**
- **Rail-to-Rail Output**
- **Gain Bandwidth: 3MHz**
- **Low Quiescent Current: 475μA per Amplifier**
- **High Common-Mode Rejection: 120dB (typ)**
- **Low Input Bias Current: 8pA**
- **Industry-Standard Package:**
  - **5-Pin Small Outline Transistor [SOT (SOT-23) - DBV] Package**

APPLICATIONS

- **Tracking Amplifier in Power Modules**
- **Merchant Power Supplies**
- **Transducer Amplifiers**
- **Bridge Amplifiers**
- **Temperature Measurements**
- **Strain Gauge Amplifiers**
- **Precision Integrators**
- **Battery-Powered Instruments**
- **Test Equipment**

Product Family

DEVICE	PACKAGE
OPA171-Q1	SOT (SOT-23) - DBV

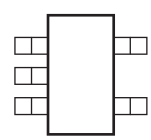
DESCRIPTION

The OPA171-Q1 is a 36V, single-supply, low-noise operational amplifier with the ability to operate on supplies ranging from +2.7V (±1.35V) to +36V (±18V). This device is available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

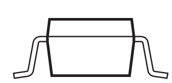
Unlike most op amps, which are specified at only one supply voltage, the OPA171-Q1 is specified from +2.7V to +36V. Input signals beyond the supply rails do not cause phase reversal. The OPA171-Q1 is stable with capacitive loads up to 300pF. The input can operate 100mV below the negative rail and within 2V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail.

The OPA171-Q1 op amp is specified from –40°C to +125°C.

Package Footprint



Package Height



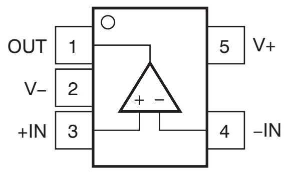
DBV (SOT23-5)

Smallest Packaging for 36V Op Amp

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DBV PACKAGE: OPA171-Q1
SOT23-5
(TOP VIEW)



ORDERING INFORMATION(1)

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	OPA171AQDBVRQ1	OULQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Supply voltage			±20	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		±10	mA
Output short circuit(2)		Continuous		
Operating temperature		–55	+150	°C
Storage temperature		–65	+150	°C
Junction temperature			+150	°C
ESD Ratings	Human body model (HBM) classification level H2		4	kV
	Charged device model (CDM) classification level C3A		500	V
	Latch-up per JESD78D	Class 1		

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA171-Q1	UNITS
		DBV (SOT-23)	
		5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	277.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	193.3	
θ_{JB}	Junction-to-board thermal resistance	121.2	
ψ_{JT}	Junction-to-top characterization parameter	51.8	
ψ_{JB}	Junction-to-board characterization parameter	109.5	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +2.7V to +36V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.25	±1.8	mV
Over temperature				**0.3**	**±2**	**mV**
Drift	**dV_{OS}/dT**			**0.3**	**±2**(1)	**µV/°C**
vs power supply	**PSRR**	**V_S = +4V to +36V**		**1**	**±3**	**µV/V**
Channel separation, dc		dc		5		µV/V
INPUT BIAS CURRENT						
Input bias current	I_B			±8	±15	pA
Over temperature					**±3.5**	**nA**
Input offset current	I_{OS}			±4		pA
Over temperature					**±3.5**	**nA**
NOISE						
Input voltage noise		f = 0.1Hz to 10Hz		3		$µV_{PP}$
Input voltage noise density	e_n	f = 100Hz		25		nV/√Hz
		f = 1kHz		14		nV/√Hz
INPUT VOLTAGE						
Common-mode voltage range(2)	V_{CM}		(V–) – 0.1V		(V+) – 2V	V
Common-mode rejection ratio	**CMRR**	**V_S = ±2V, (V–) – 0.1V < V_{CM} < (V+) – 2V**	**90**	**104**		**dB**
		V_S = ±18V, (V–) – 0.1V < V_{CM} < (V+) – 2V	**104**	**120**		**dB**
INPUT IMPEDANCE						
Differential				100 || 3		MΩ || pF
Common-mode				6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain	**A_{OL}**	**V_S = +4V to +36V, (V–) + 0.35V < V_O < (V+) – 0.35V**	**110**	**130**		**dB**
FREQUENCY RESPONSE						
Gain bandwidth product	GBP			3.0		MHz
Slew rate	SR	G = +1		1.5		V/µs
Settling time	t_S	To 0.1%, V_S = ±18V, G = +1, 10V step		6		µs
		To 0.01% (12 bit), V_S = ±18V, G = +1, 10V step		10		µs
Overload recovery time		V_{IN} × Gain > V_S		2		µs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$		0.0002		%
OUTPUT						
Voltage output swing from rail	**V_O**	**R_L = 10kΩ, A_{OL} ≥ 110dB**	**(V–) + 0.35**		**(V+) – 0.35**	**V**
Short-circuit current	I_{SC}			+25/–35		mA
Capacitive load drive	C_{LOAD}			See Typical Characteristics		pF
Open-loop output resistance	R_O	f = 1MHz, I_O = 0A		150		Ω
POWER SUPPLY						
Specified voltage range	V_S		+2.7		+36	V
Quiescent current per amplifier	I_Q	I_O = 0A		475	595	µA
Over temperature		**I_O = 0A**			**650**	**µA**
TEMPERATURE						
Specified range			–40		+125	°C
Operating range			–55		+150	°C

(1) Not production tested.
(2) The input range can be extended beyond (V+) – 2V up to V+. See the *Typical Characteristics* and *Application Information* sections for additional information.

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TYPICAL CHARACTERISTICS

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

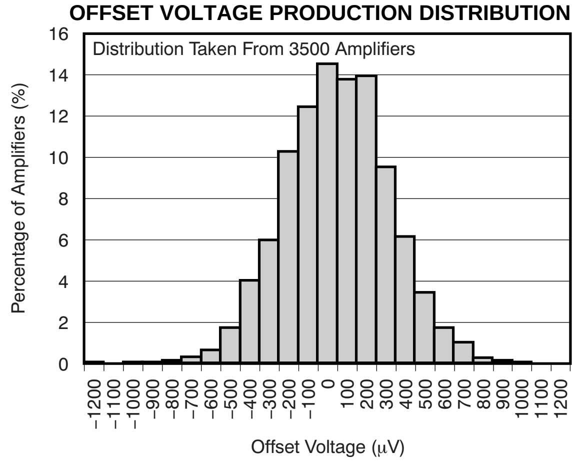

Figure 1.

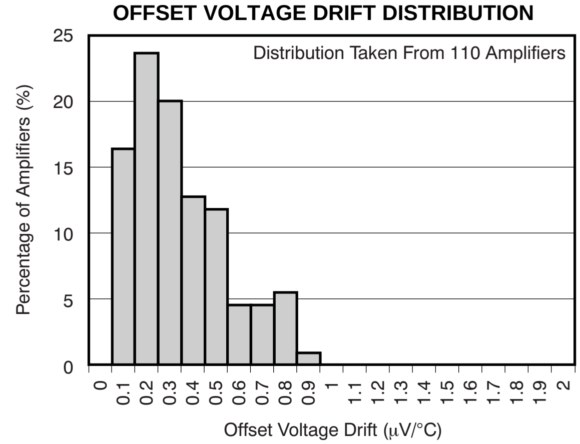

Figure 2.

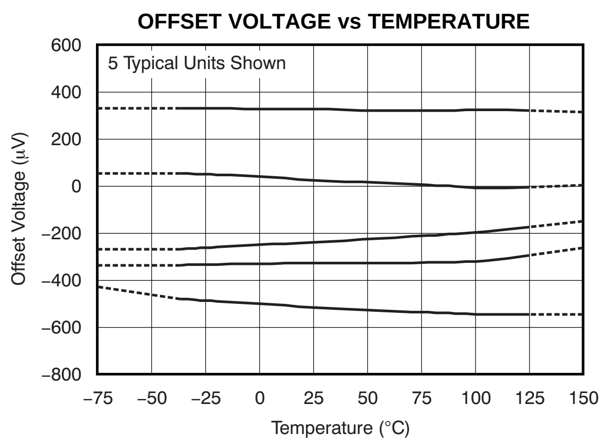

Figure 3.

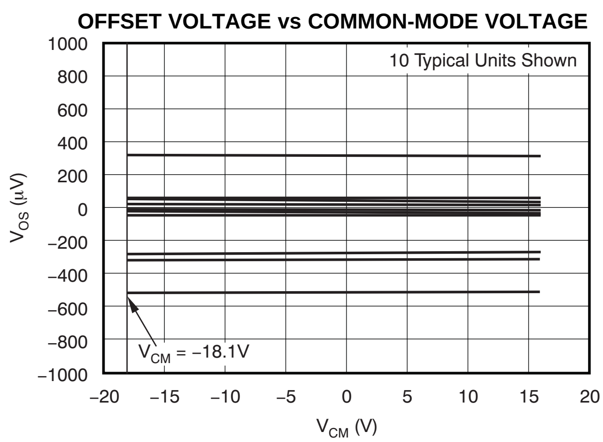

Figure 4.

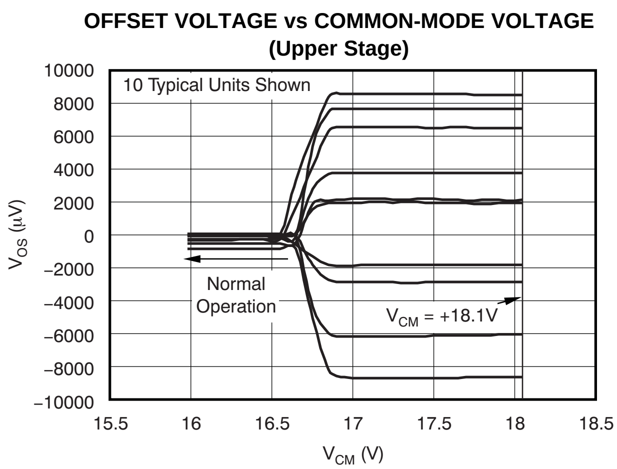

Figure 5.

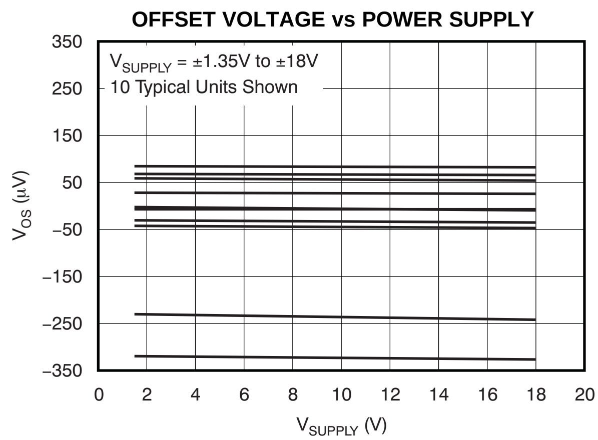

Figure 6.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

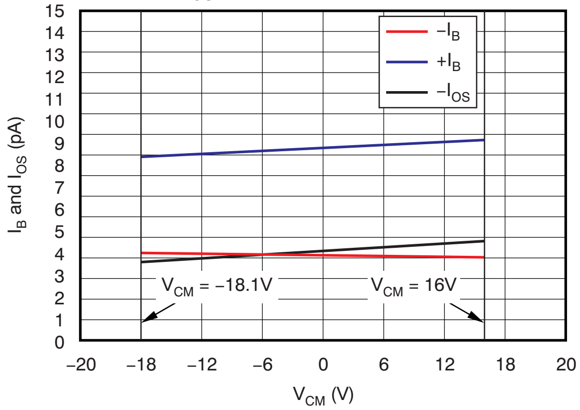

Figure 7.

INPUT BIAS CURRENT vs TEMPERATURE

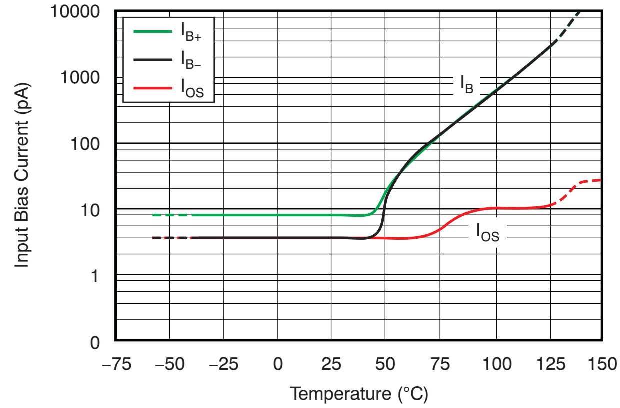

Figure 8.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

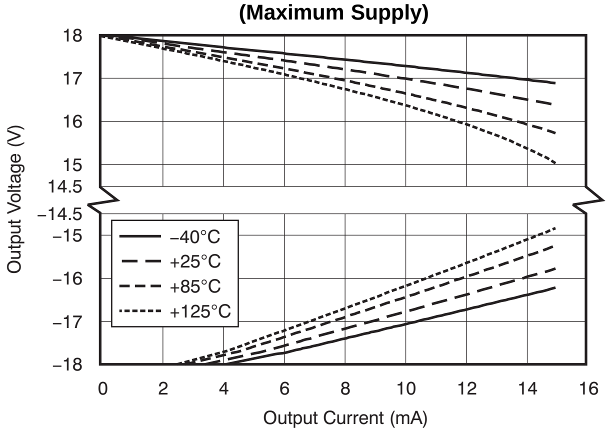

Figure 9.

CMRR AND PSRR vs FREQUENCY (Referred-to Input)

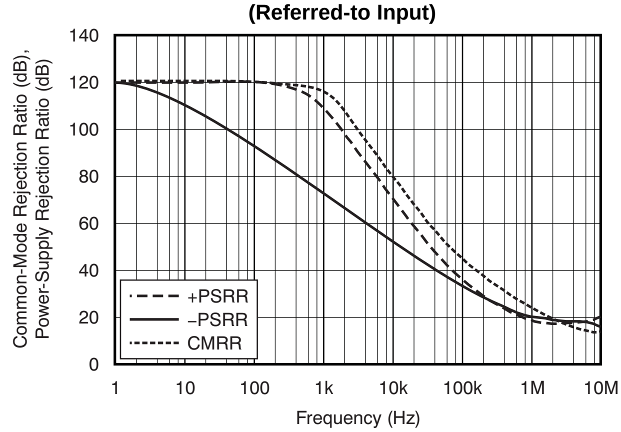

Figure 10.

CMRR vs TEMPERATURE

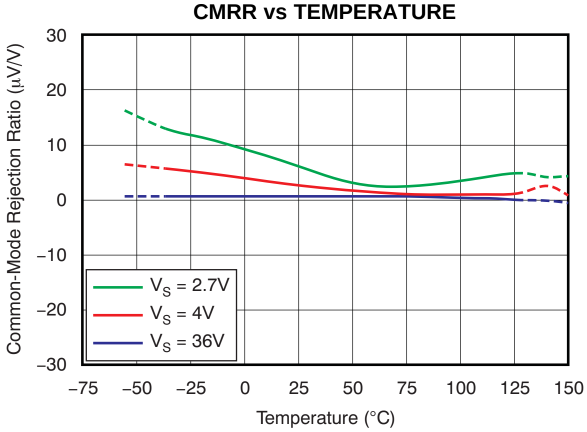

Figure 11.

PSRR vs TEMPERATURE

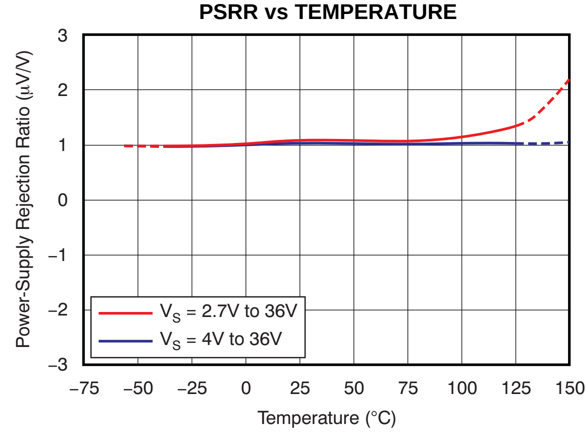

Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

0.1Hz TO 10Hz NOISE

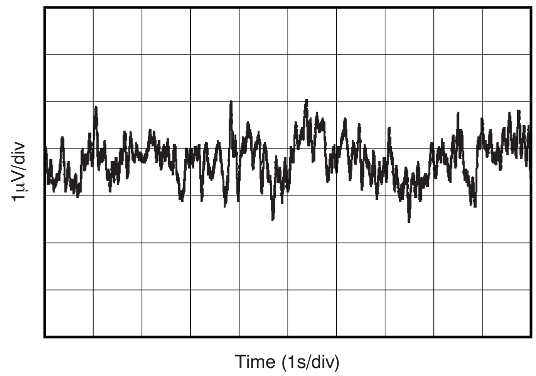

Figure 13.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

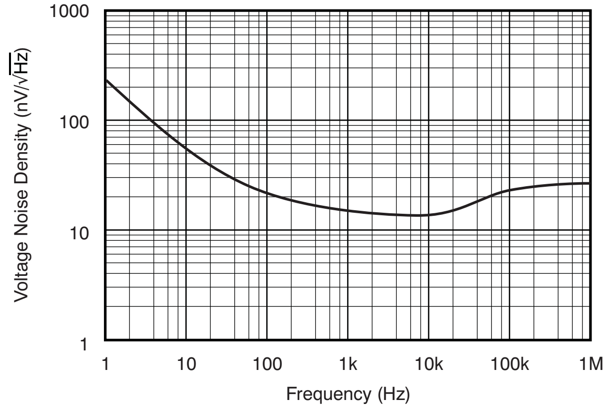

Figure 14.

THD+N RATIO vs FREQUENCY

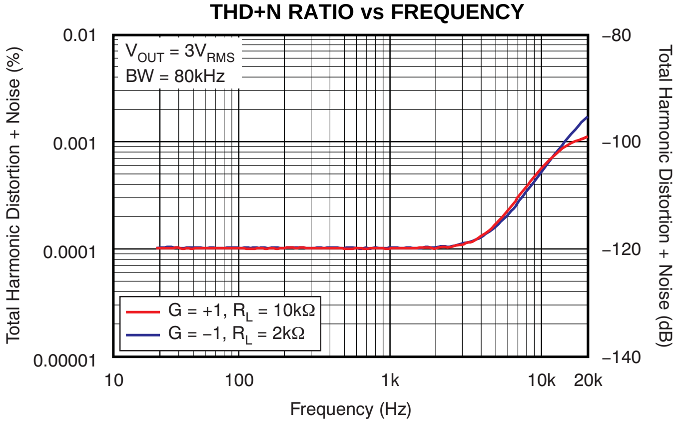

Figure 15.

THD+N vs OUTPUT AMPLITUDE

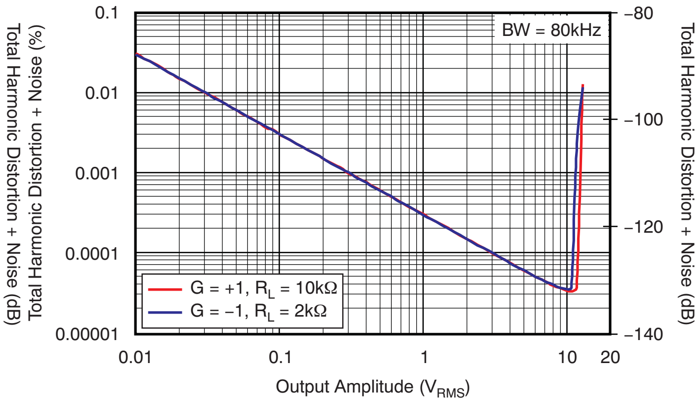

Figure 16.

QUIESCENT CURRENT vs TEMPERATURE

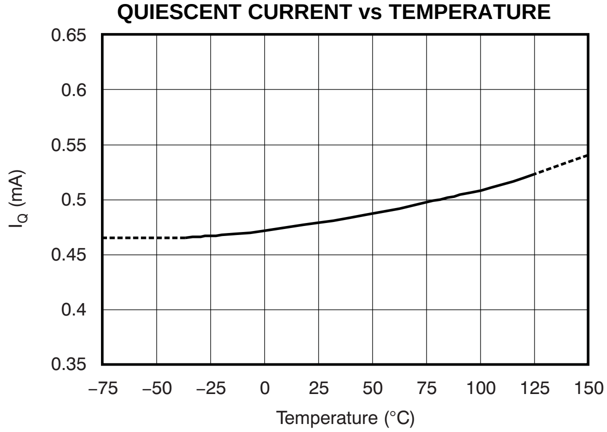

Figure 17.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

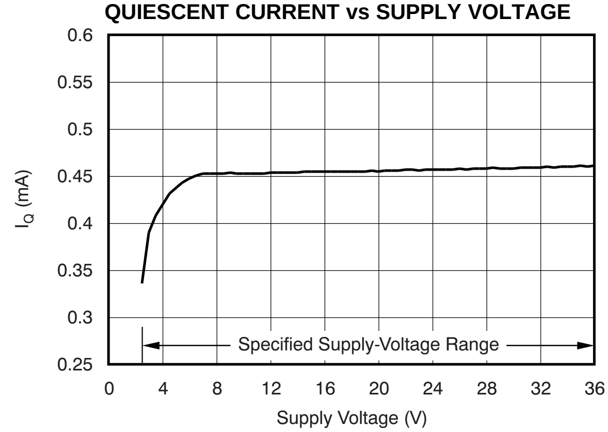

Figure 18.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

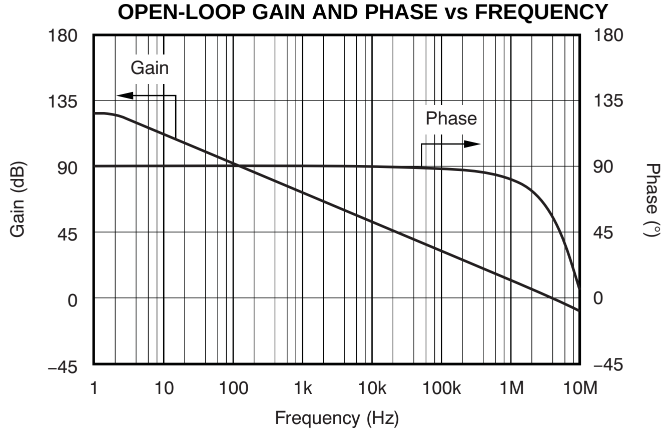

Figure 19.

CLOSED-LOOP GAIN vs FREQUENCY

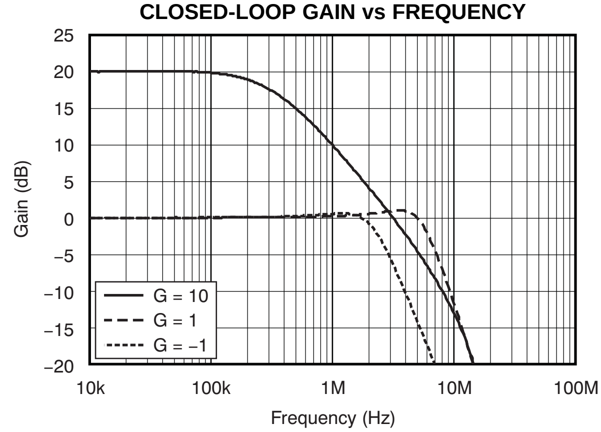

Figure 20.

OPEN-LOOP GAIN vs TEMPERATURE

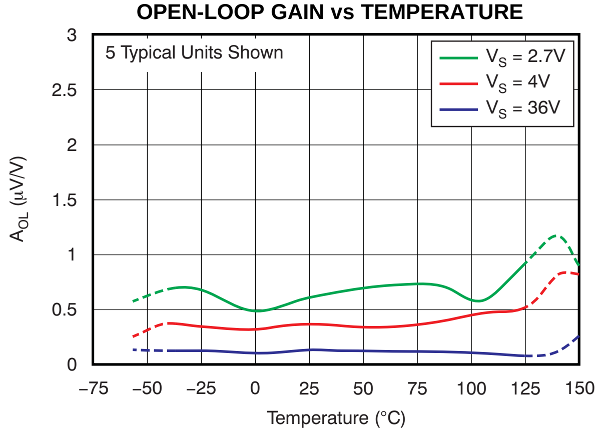

Figure 21.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

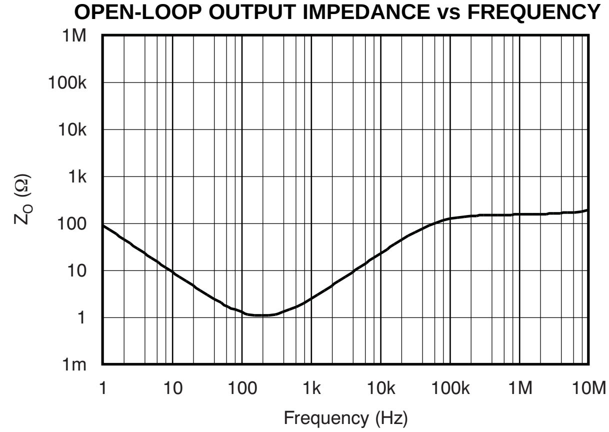

Figure 22.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

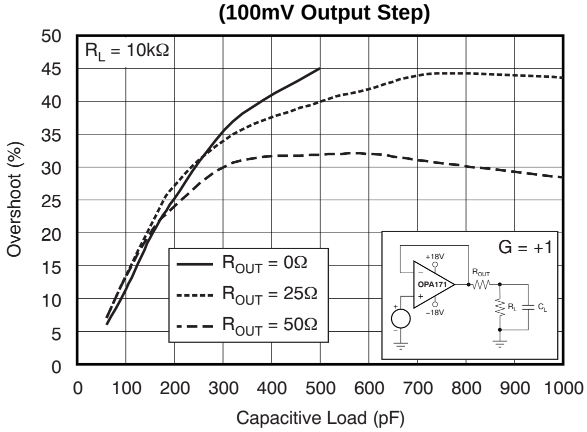

Figure 23.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

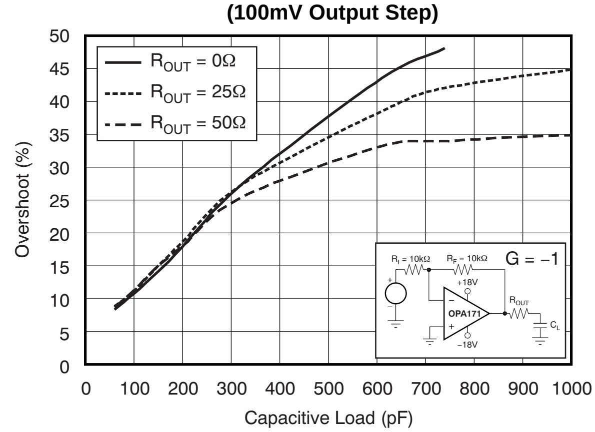

Figure 24.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

NO PHASE REVERSAL

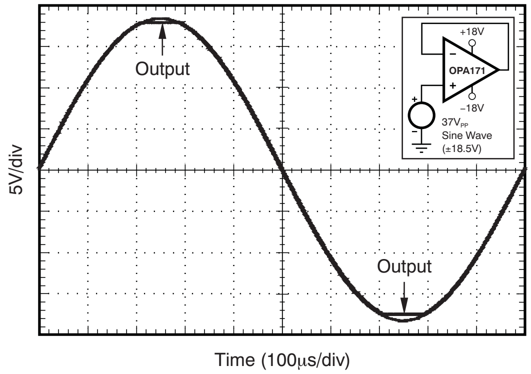

Figure 25.

POSITIVE OVERLOAD RECOVERY

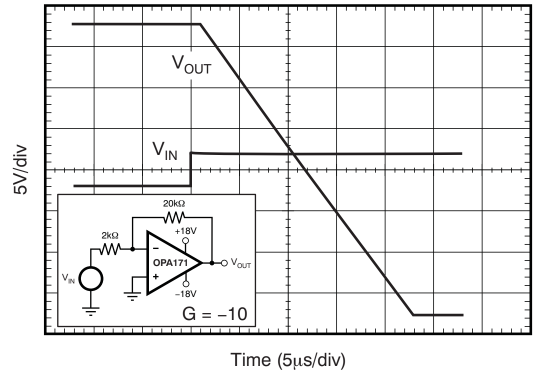

Figure 26.

NEGATIVE OVERLOAD RECOVERY

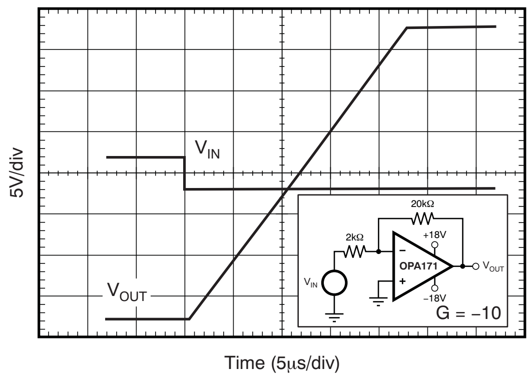

Figure 27.

SMALL-SIGNAL STEP RESPONSE (100mV)

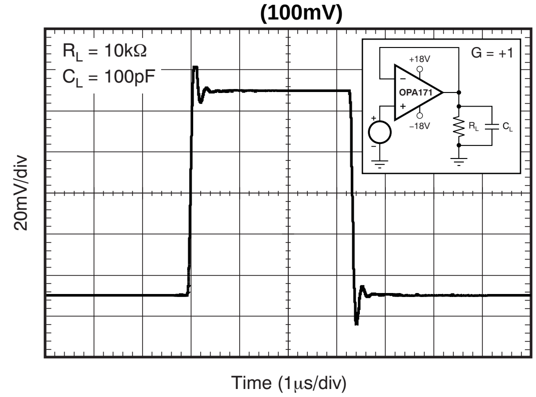

Figure 28.

SMALL-SIGNAL STEP RESPONSE (100mV)

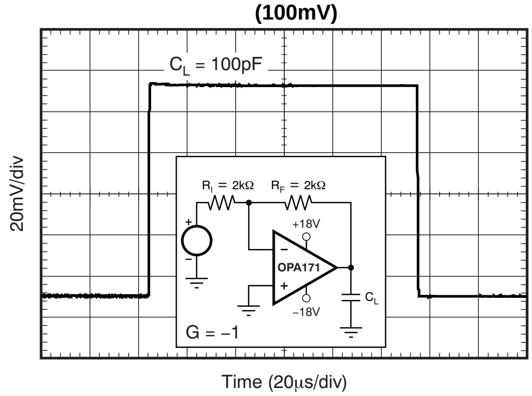

Figure 29.

LARGE-SIGNAL STEP RESPONSE

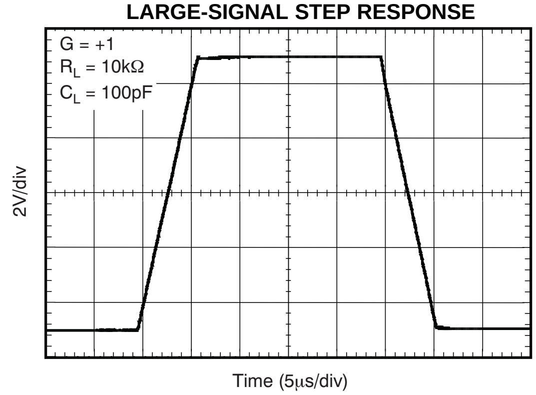

Figure 30.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

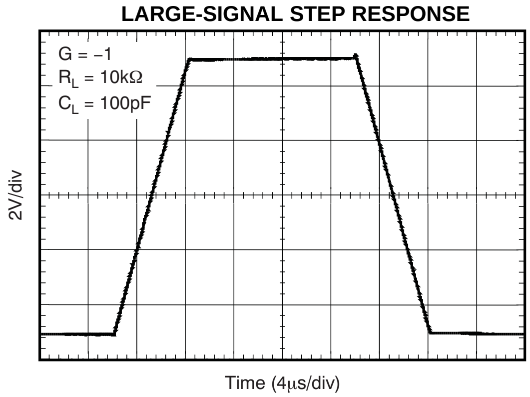

Figure 31.

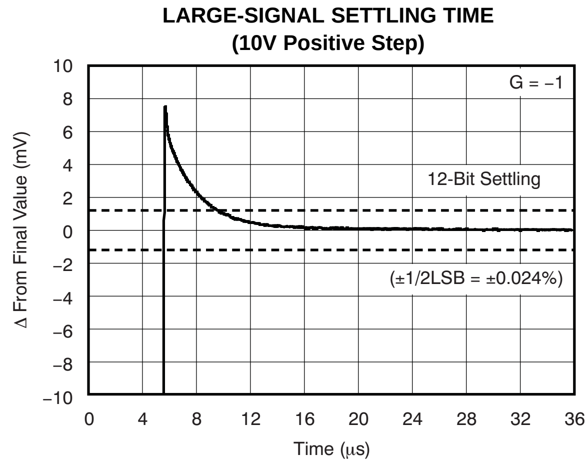

Figure 32.

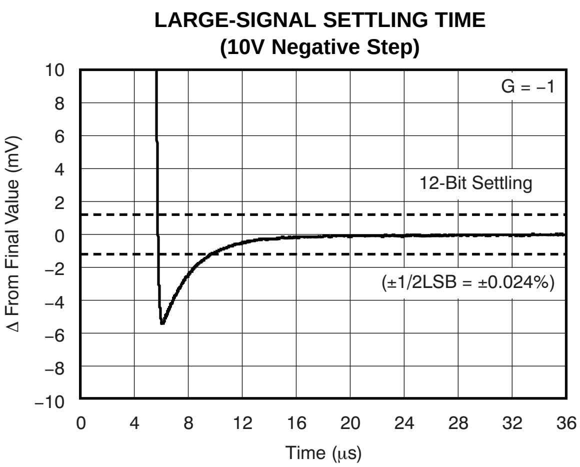

Figure 33.

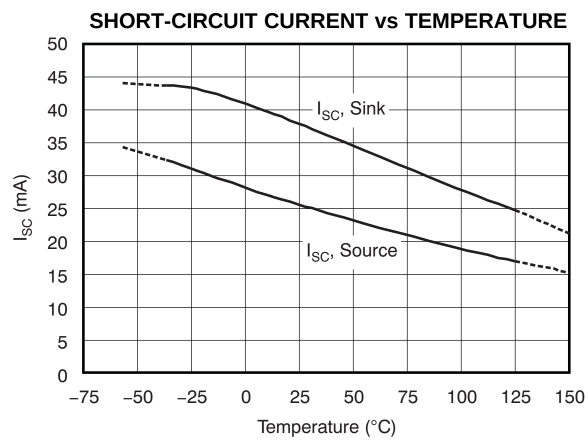

Figure 34.

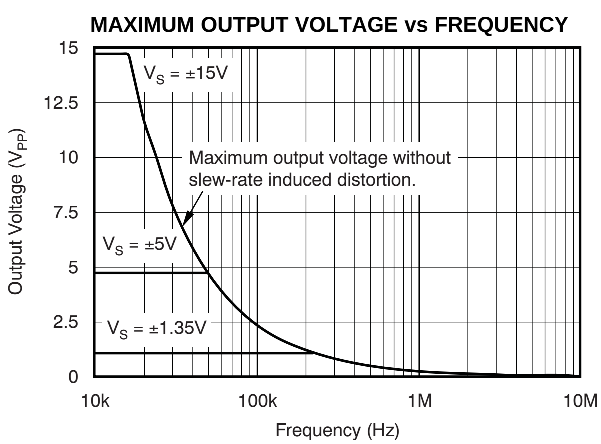

Figure 35.

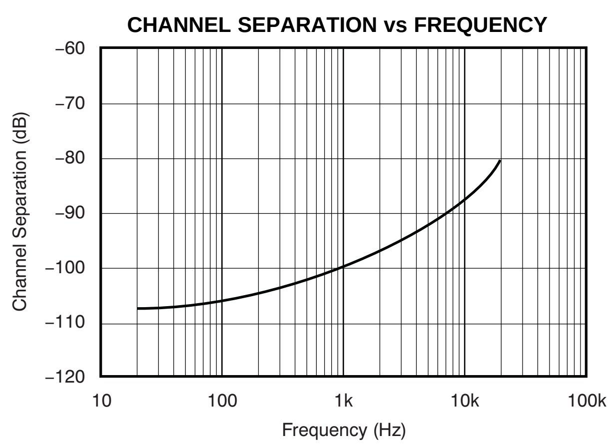

Figure 36.

APPLICATION INFORMATION

The OPA171-Q1 operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only 2µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate.

OPERATING CHARACTERISTICS

The OPA171-Q1 is specified for operation from 2.7V to 36V (±1.35V to ±18V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPAx171 series extends 100mV below the negative rail and within 2V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail. The typical performance in this range is summarized in Table 2.

PHASE-REVERSAL PROTECTION

The OPA171-Q1 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 37.

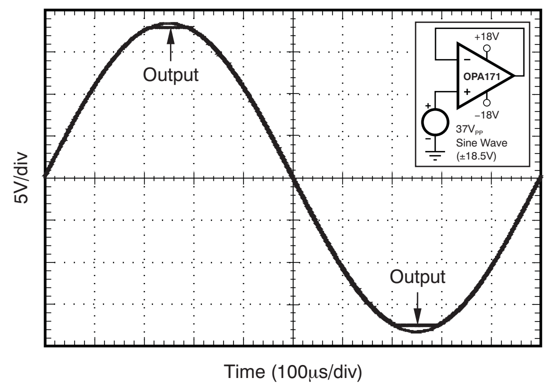

Figure 37. No Phase Reversal

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	**(V+) – 2**		**(V+) + 0.1**	**V**
Offset voltage		7		mV
vs Temperature		**12**		**µV/°C**
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1kHz		30		nV/√Hz

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPA171-Q1 have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50Ω) in series with the output. Figure 38 and Figure 39 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to Applications Bulletin AB-028 (*SBOA015*), available for download from the TI website for details of analysis techniques and application circuits.

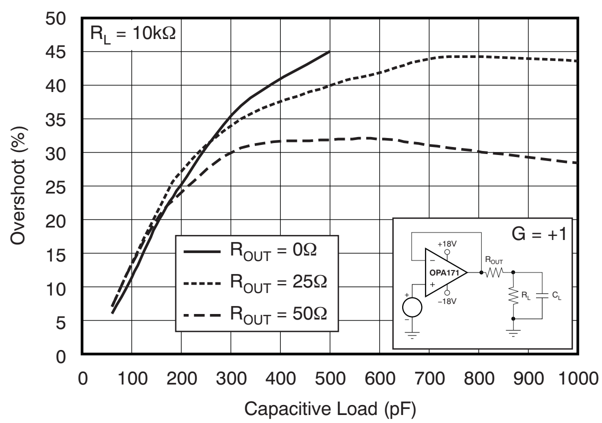

Figure 38. Small-Signal Overshoot versus Capacitive Load (100mV Output Step)

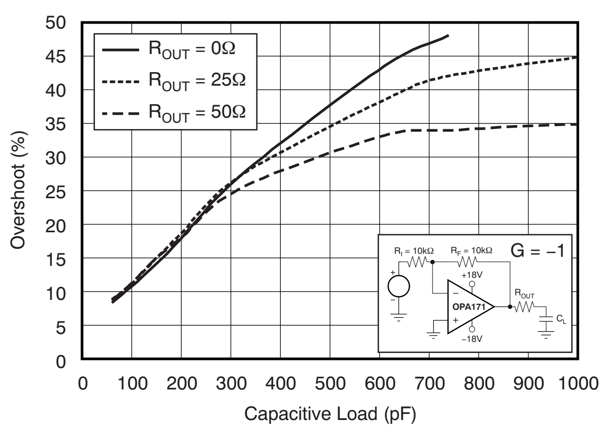

Figure 39. Small-Signal Overshoot versus Capacitive Load (100mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the Absolute Maximum Ratings. Figure 40 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

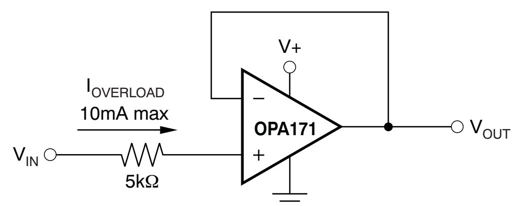

Figure 40. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

REVISION HISTORY

Changes from Original (June, 2011) to Revision A **Page**

- Added second bullet to Features: AEC-Q100 Test Guidance With the Following Results: –Device Temperature Grade1: -40°C to 125°C Ambient Operating Temperature Range –Device HBM ESD Classification Level H2 –Device CDM ESD Classification Level C3A 1
- Removed package column in Ordering Information table. 2
- Added classification levels to ESD ratings in Absolute Maximum Ratings table. 2
- Added row to Absolute Maximum Ratings table: Latch-up per JESD78D with Class 1 value. 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA171AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OULQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF OPA171-Q1 :

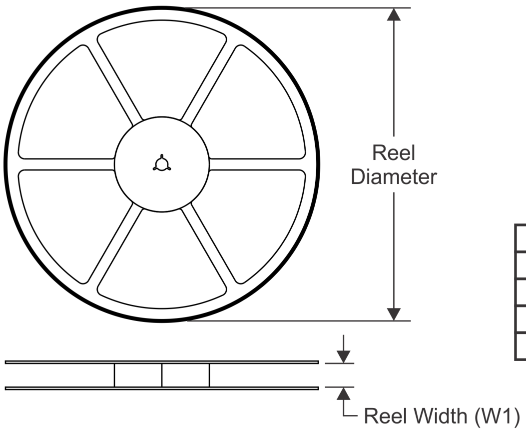
- Catalog: OPA171

NOTE: Qualified Version Definitions:

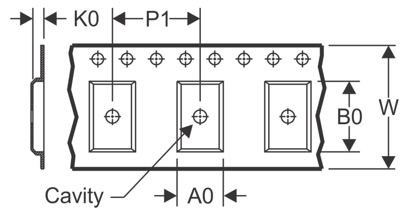
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

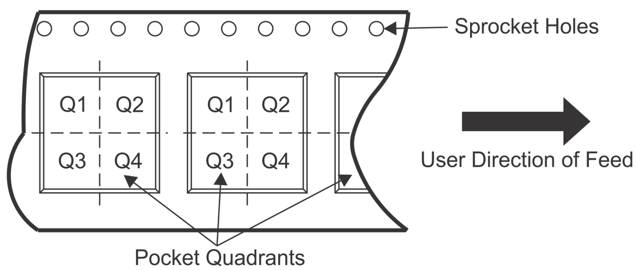


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

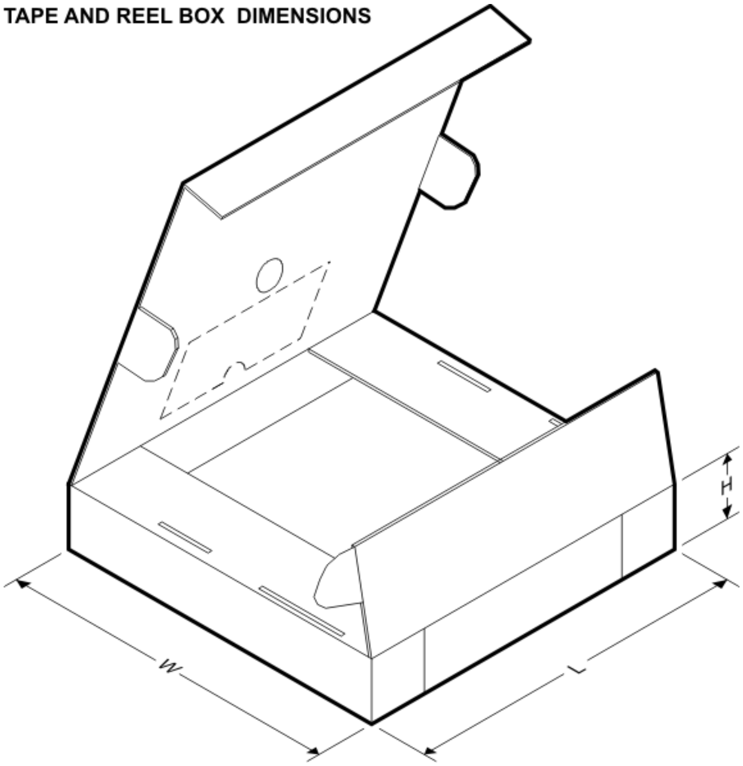
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

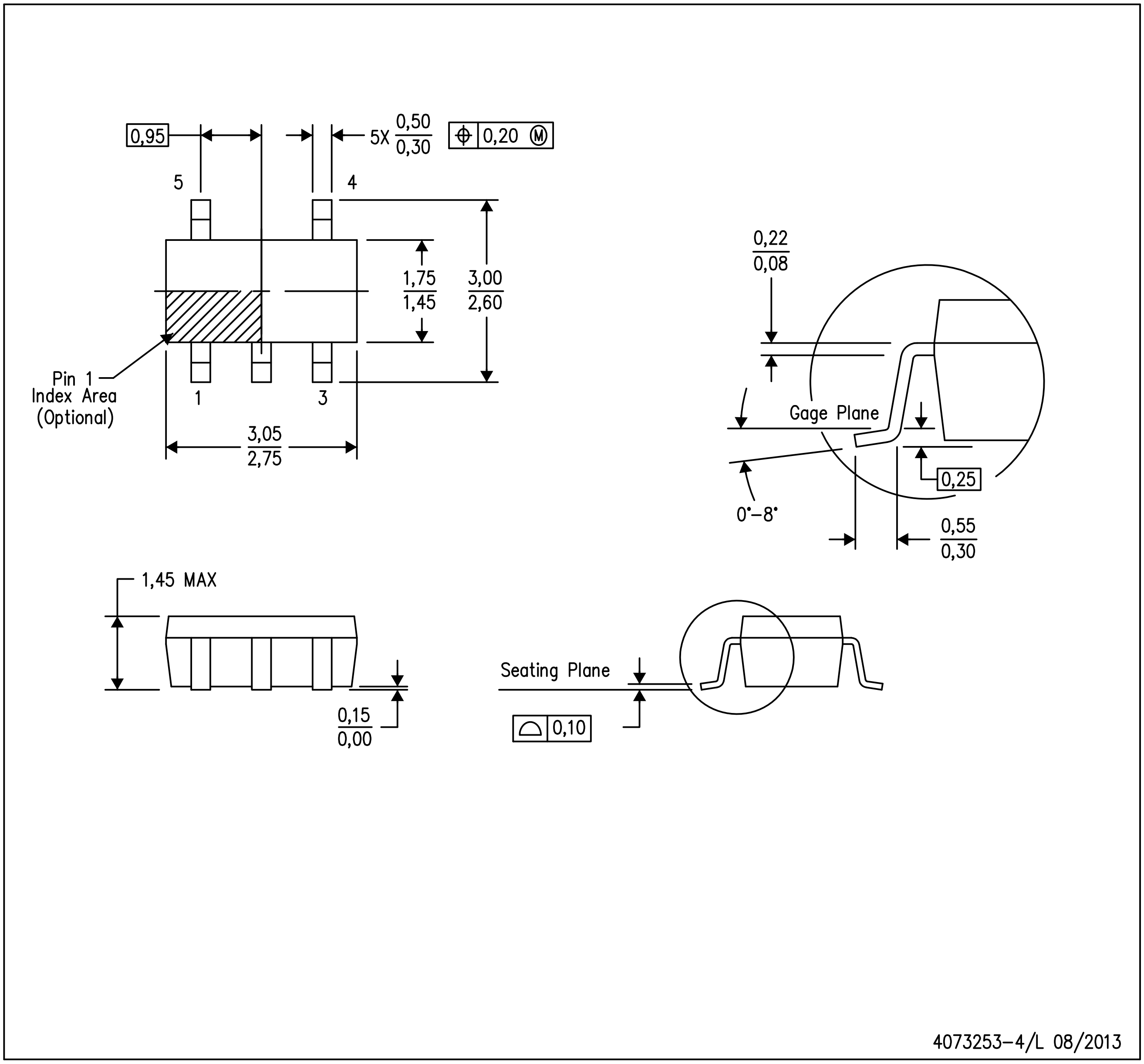
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

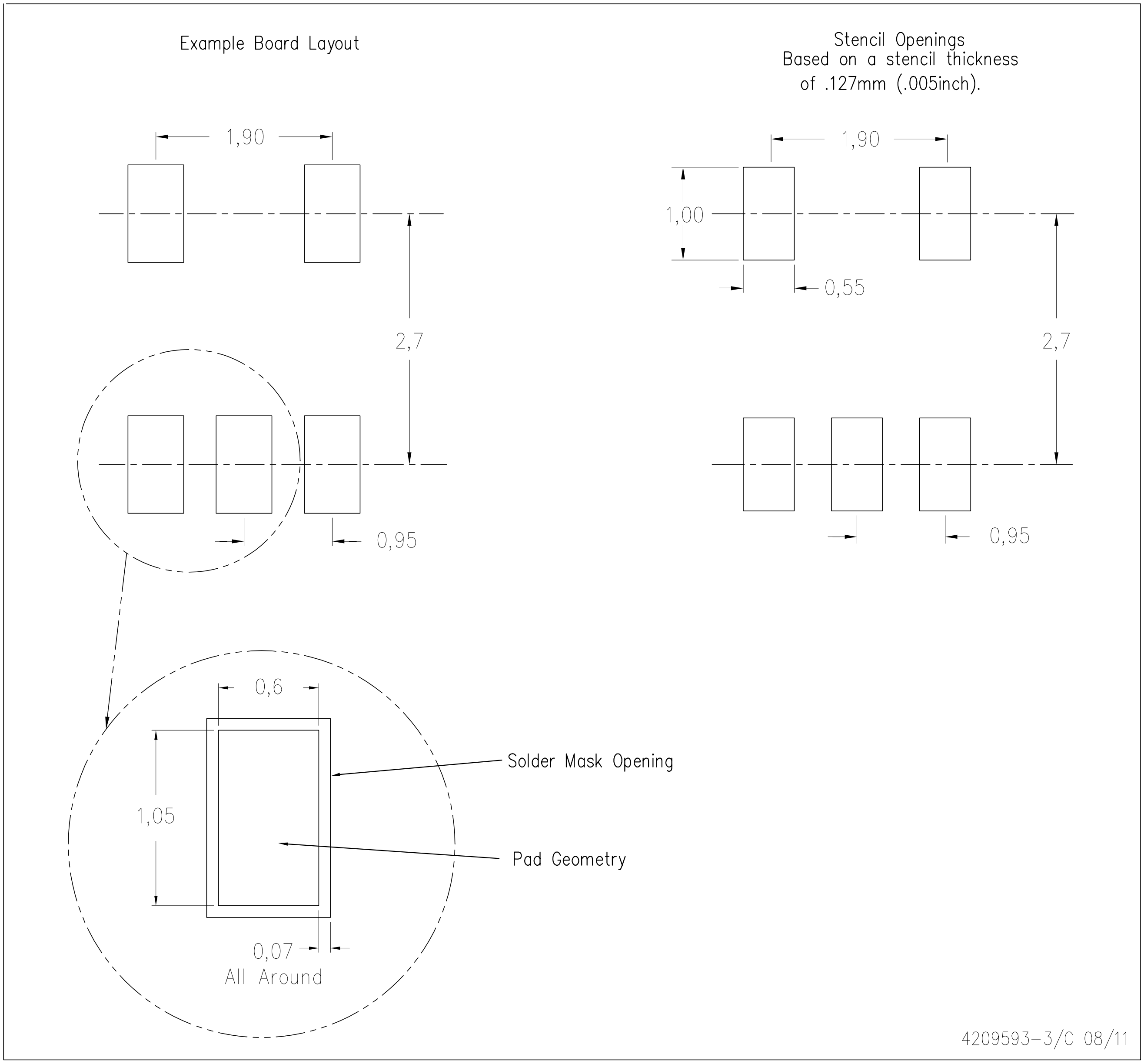
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AQDBVRQ1	SOT-23	DBV	5	3000	202.0	201.0	28.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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