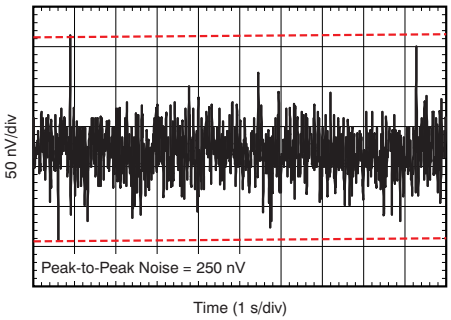
0.1-μV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift OPERATIONAL AMPLIFIERS

Check for Samples: OPA2180, OPA4180

FEATURES

- **Low Offset Voltage: 75 μV (max)**
- **Zero-Drift: 0.1 μV/°C**
- **Low Noise: 10 nV/√Hz**
- **Very Low 1/f Noise**
- **Excellent DC Precision:**
  - **PSRR: 126 dB**
  - **CMRR: 114 dB**
  - **Open-Loop Gain (A_{OL}): 120 dB**
- **Quiescent Current: 525 μA (max)**
- **Wide Supply Range: ±2 V to ±18 V**
- **Rail-to-Rail Output:**
  Input Includes Negative Rail
- **Low Bias Current: 250 pA (typ)**
- **RFI Filtered Inputs**
- ***Micro*SIZE Packages**



APPLICATIONS

- **Bridge Amplifiers**
- **Strain Gauges**
- **Test Equipment**
- **Transducer Applications**
- **Temperature Measurement**
- **Electronic Scales**
- **Medical Instrumentation**
- **Resister Thermal Detectors**
- **Precision Active Filters**

DESCRIPTION

The OPA2180 and OPA4180 operational amplifiers use zero-drift techniques to simultaneously provide low offset voltage (75 μV), and near zero-drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 18 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of +4.0 V to +36 V (±2 V to ±18 V).

The dual version is offered in MSOP-8 and SO-8 packages. The quad is offered in SO-14 and TSSOP-14 packages. All versions are specified for operation from –40°C to +105°C.

Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV)	OFFSET VOLTAGE DRIFT (μV/°C)	BANDWIDTH (MHz)
Single	OPA188 (4 V to 36 V)	25	0.085	2
	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188 (4 V to 36 V)	25	0.085	2
	OPA2180 (4 V to 36 V)	75	0.35	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
	OPA4180 (4 V to 36 V)	75	0.35	2
	OPA4330 (5 V)	50	0.25	0.35

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DUAL				
OPA2180	SO-8	D	–40°C to +105°C	2180
	MSOP-8	DGK	–40°C to +105°C	2180
QUAD				
OPA4180	SO-14	D	–40°C to +105°C	OPA4180
	TSSOP-14	PW	–40°C to +105°C	OPA4180

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		OPA2180, OPA4180	UNIT
Supply voltage		±20, 40 (single supply)	V
Signal input terminals	Voltage	(V–) – 0.5 to (V+) + 0.5	V
	Current	±10	mA
Output short-circuit(2)		Continuous	
Operating temperature		–55 to +125	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
ESD ratings	Human body model (HBM)	1.5	kV
	Charged device model (CDM)	1	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = ±2 V to ±18 V (V_S = +4 V to +36 V)

At T_A = +25°C, R_L = 10 kΩ connected to $V_S/2$, and $V_{COM} = V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER			CONDITIONS	OPA2180, OPA4180 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				15	75	µV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +105°C		0.1	0.35	µV/°C
PSRR	Power-supply rejection ratio		V_S = 4 V to 36 V, $V_{CM} = V_S/2$		0.1	0.5	µV/V
			T_A = –40°C to +105°C, V_S = 4 V to 36 V, $V_{CM} = V_S/2$			0.5	µV/V
	Long-term stability				See note (1)		µV
	Channel separation, dc				1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		OPA2180		±0.25	±1	nA
			OPA2180, T_A = –40°C to +105°C			±5	nA
			OPA4180		±0.25	±1.7	nA
			OPA4180, T_A = –40°C to +105°C			±6	nA
I_{OS}	Input offset current		OPA2180		±0.5	±2	nA
			OPA2180, T_A = –40°C to +105°C			±2.5	nA
			OPA4180			±3.4	nA
			OPA4180, T_A = –40°C to +105°C			±3	nA
NOISE							
	Input voltage noise		f = 0.1 Hz to 10 Hz		0.25		μV_{PP}
e_n	Input voltage noise density		f = 1 kHz		10		$nV/\sqrt{Hz}$
i_n	Input current noise density		f = 1 kHz		10		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio		(V–) < V_{CM} < (V+) – 1.5 V	104	114		dB
			T_A = –40°C to +105°C, (V–) + 0.5 V < V_{CM} < (V+) – 1.5 V	100	104		dB
INPUT IMPEDANCE							
	Differential				100/6		MΩ/pF
	Common-mode				6/9.5		10^{12} Ω/pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	110	120		dB
			T_A = –40°C to +105°C, (V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	104	114		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				2		MHz
SR	Slew rate		G = +1		0.8		V/µs
	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		22		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		30		µs
	Overload recovery time		$V_{IN} \times G = V_S$		1		µs
THD+N	Total harmonic distortion + noise		f = 1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits, or approximately 4 µV.

ELECTRICAL CHARACTERISTICS: V_S = ±2 V to ±18 V (V_S = +4 V to +36 V) (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA2180, OPA4180 MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		8	18	mV
		R_L = 10 kΩ		250	300	mV
		T_A = –40°C to +105°C, R_L = 10 kΩ		325	360	mV
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 2 MHz, I_O = 0 mA		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		±2 (or 4)		±18 (or 36)	V
I_Q	Quiescent current (per amplifier)			450	525	µA
		T_A = –40°C to +105°C, I_O = 0 mA			600	µA
TEMPERATURE						
	Specified range		–40		+105	°C
	Operating range		–40		+125	°C
	Storage range		–65		+150	°C

THERMAL INFORMATION: OPA2180

THERMAL METRIC(1)		OPA2180 D (SO) 8 PINS	OPA2180 DGK (MSOP) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	111.0	159.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	54.9	37.4	
θ_{JB}	Junction-to-board thermal resistance	51.7	48.5	
ψ_{JT}	Junction-to-top characterization parameter	9.3	1.2	
ψ_{JB}	Junction-to-board characterization parameter	51.1	77.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

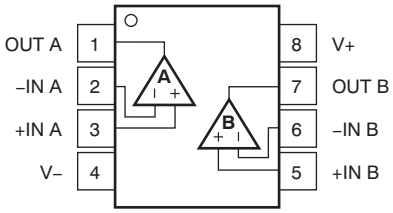
THERMAL INFORMATION: OPA4180

THERMAL METRIC(1)		OPA4180 D (SO) 14 PINS	OPA4180 PW (TSSOP) 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.8	24.4	
θ_{JB}	Junction-to-board thermal resistance	49.4	59.3	
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

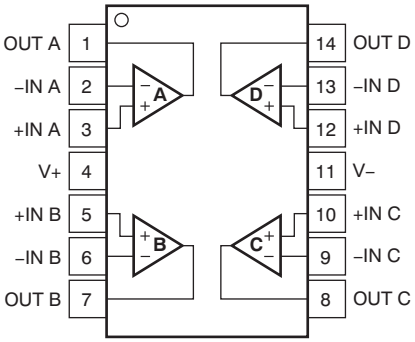
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

OPA2180
D, DGK PACKAGES (SO-8, MSOP-8)
(TOP VIEW)



OPA4180
D, PW PACKAGES (SO-14, TSSOP-14)
(TOP VIEW)



TYPICAL CHARACTERISTICS

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
I_B and I_{OS} vs Common-Mode Voltage	Figure 1
Input Bias Current vs Temperature	Figure 2
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 3
CMRR vs Temperature	Figure 4
0.1-Hz to 10-Hz Noise	Figure 5
Input Voltage Noise Spectral Density vs Frequency	Figure 6
Open-Loop Gain and Phase vs Frequency	Figure 7
Open-Loop Gain vs Temperature	Figure 8
Open-Loop Output Impedance vs Frequency	Figure 9
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 10, Figure 11
No Phase Reversal	Figure 12
Positive Overload Recovery	Figure 13
Negative Overload Recovery	Figure 14
Small-Signal Step Response (100 mV)	Figure 15, Figure 16
Large-Signal Step Response	Figure 17, Figure 18
Large-Signal Settling Time (10-V Positive Step)	Figure 19
Large-Signal Settling Time (10-V Negative Step)	Figure 20
Short-Circuit Current vs Temperature	Figure 21
Maximum Output Voltage vs Frequency	Figure 22
Channel Separation vs Frequency	Figure 23
EMIRR IN+ vs Frequency	Figure 24

TYPICAL CHARACTERISTICS

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

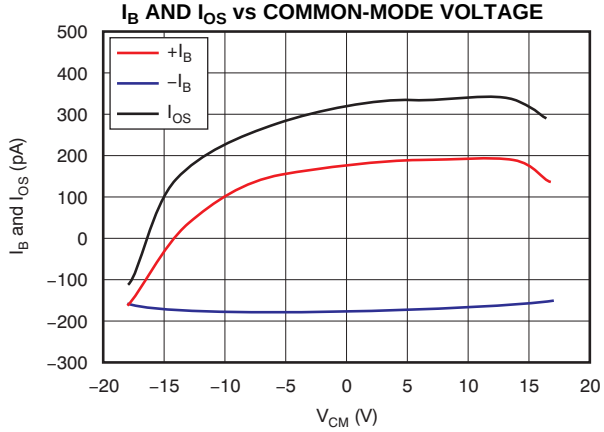


Figure 1.

INPUT BIAS CURRENT vs TEMPERATURE

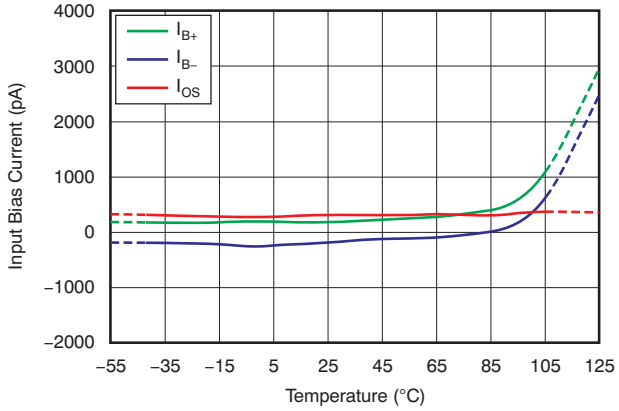


Figure 2.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

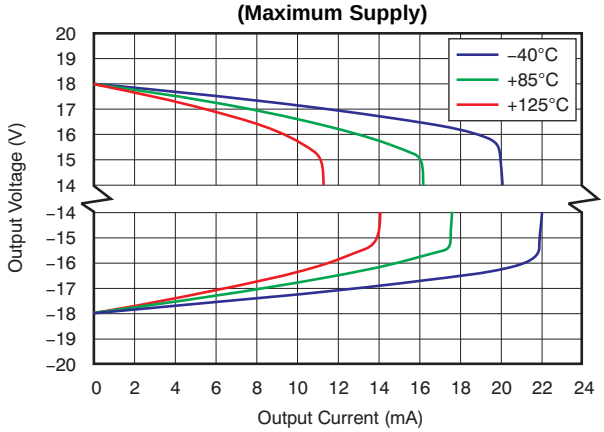


Figure 3.

CMRR vs TEMPERATURE

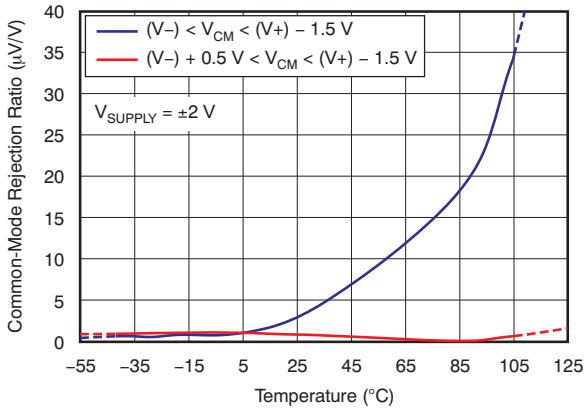


Figure 4.

0.1-Hz TO 10-Hz NOISE

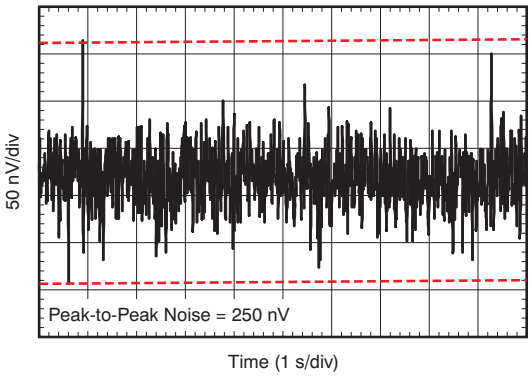


Figure 5.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

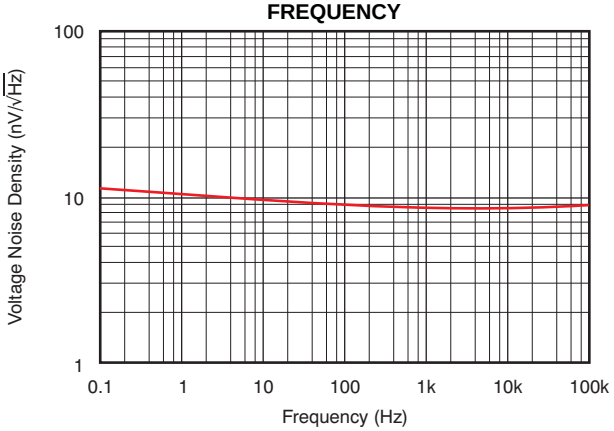


Figure 6.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

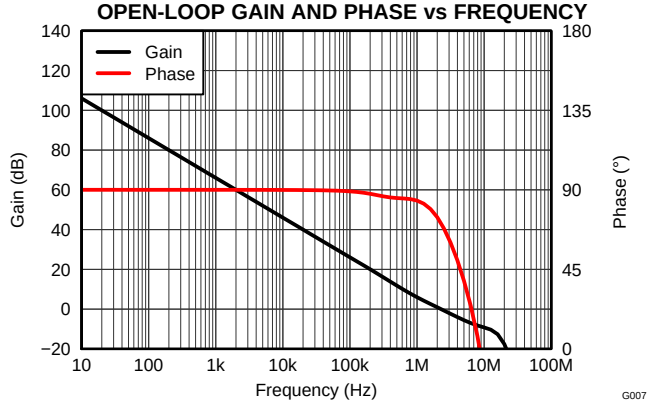


Figure 7.

OPEN-LOOP GAIN vs TEMPERATURE

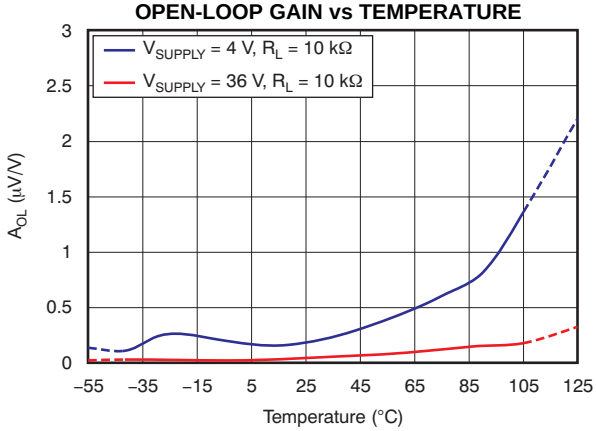


Figure 8.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

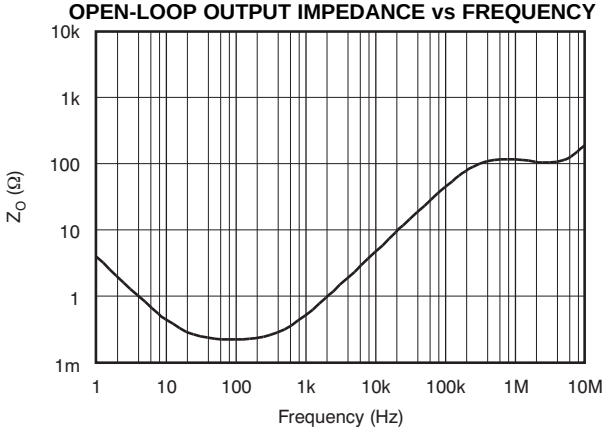


Figure 9.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

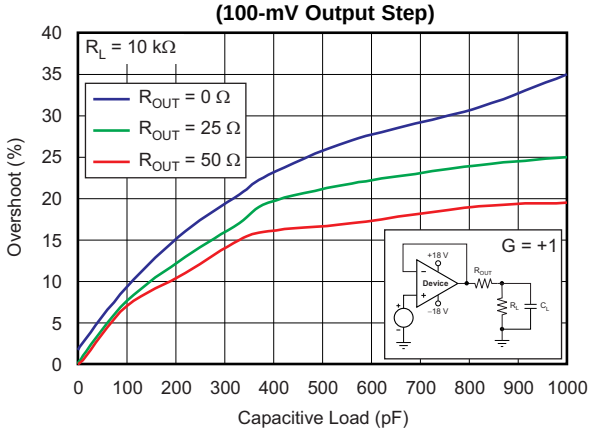


Figure 10.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

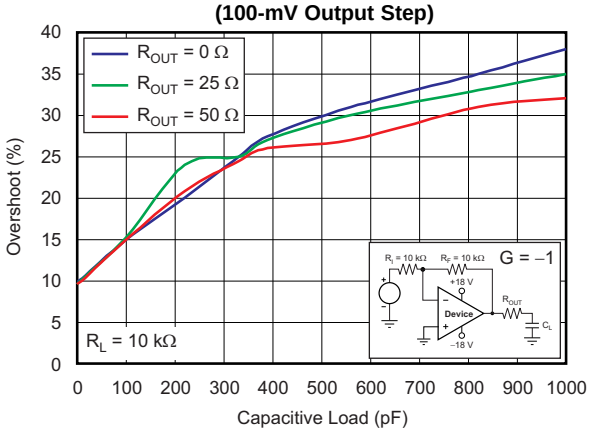


Figure 11.

NO PHASE REVERSAL

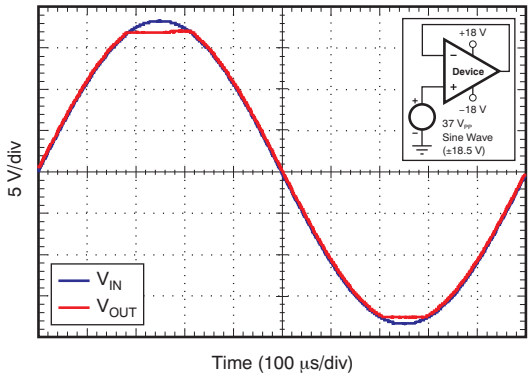


Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

POSITIVE OVERLOAD RECOVERY

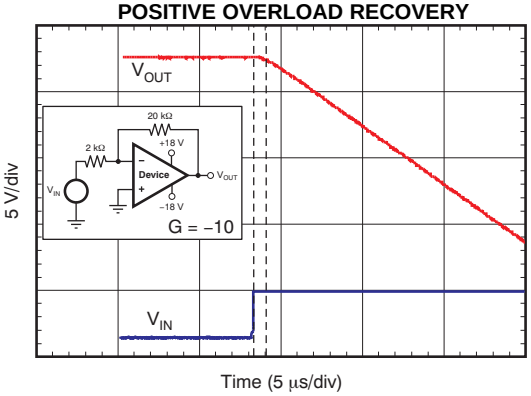


Figure 13.

NEGATIVE OVERLOAD RECOVERY

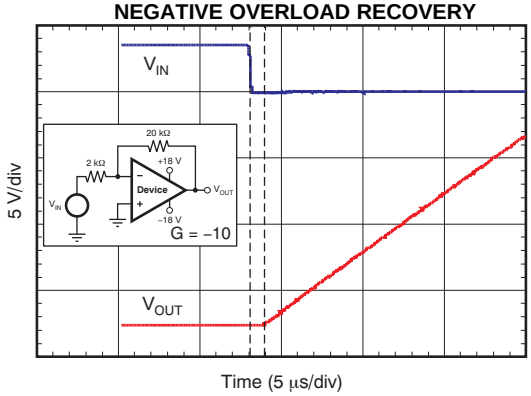


Figure 14.

SMALL-SIGNAL STEP RESPONSE (100 mV)

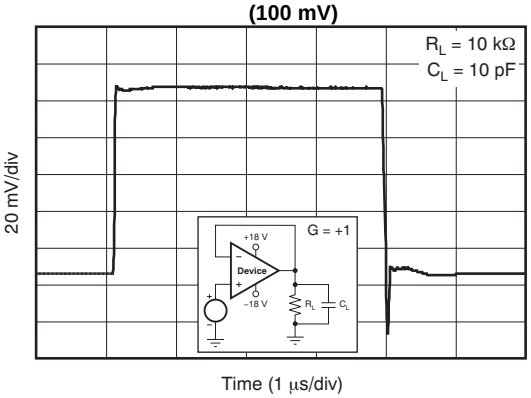


Figure 15.

SMALL-SIGNAL STEP RESPONSE (100 mV)

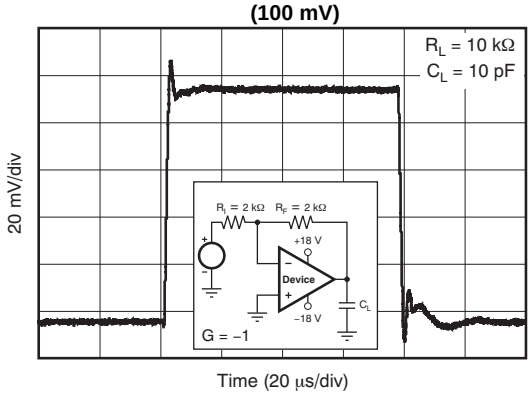


Figure 16.

LARGE-SIGNAL STEP RESPONSE

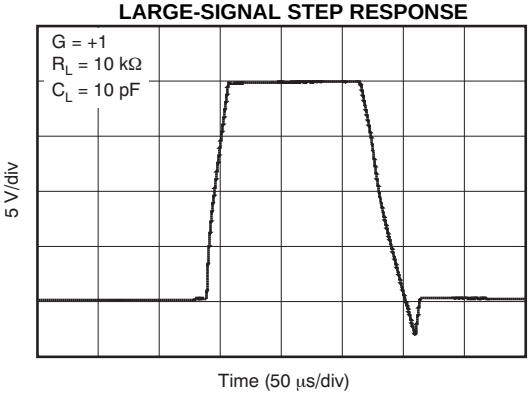


Figure 17.

LARGE-SIGNAL STEP RESPONSE

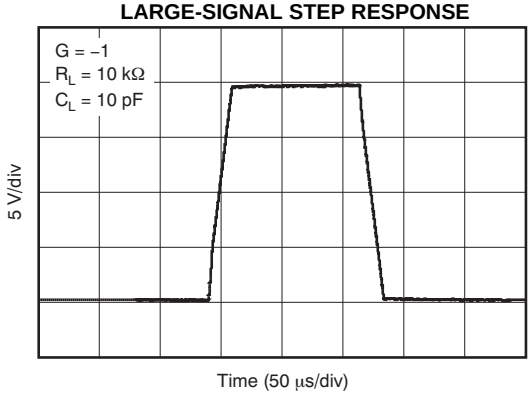


Figure 18.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

LARGE-SIGNAL SETTLING TIME (10-V Positive Step)

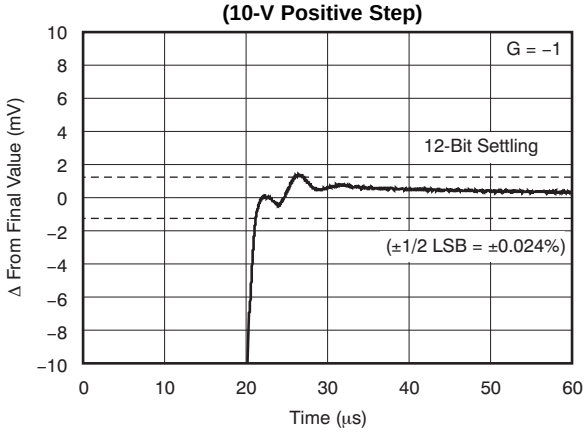


Figure 19.

LARGE-SIGNAL SETTLING TIME (10-V Negative Step)

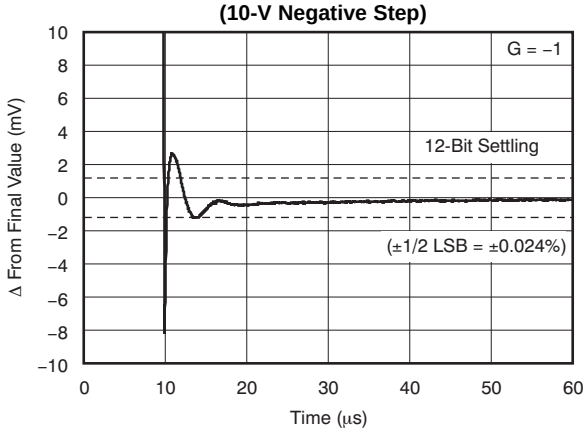


Figure 20.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

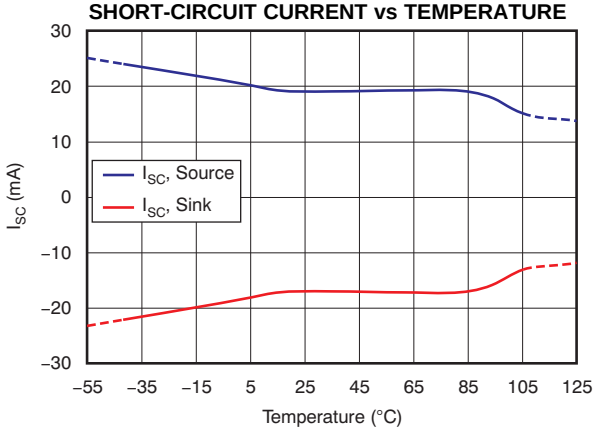


Figure 21.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

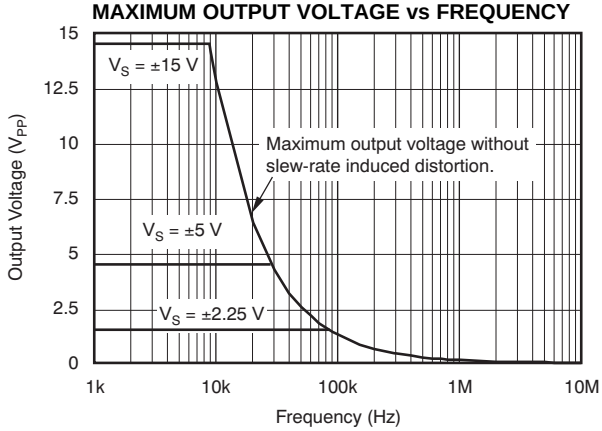


Figure 22.

CHANNEL SEPARATION vs FREQUENCY

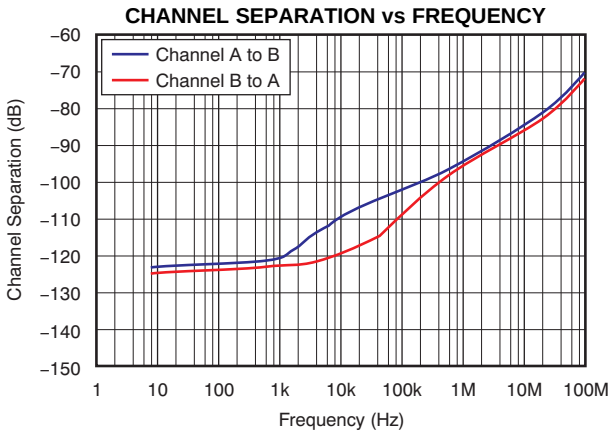


Figure 23.

EMIRR IN+ vs FREQUENCY

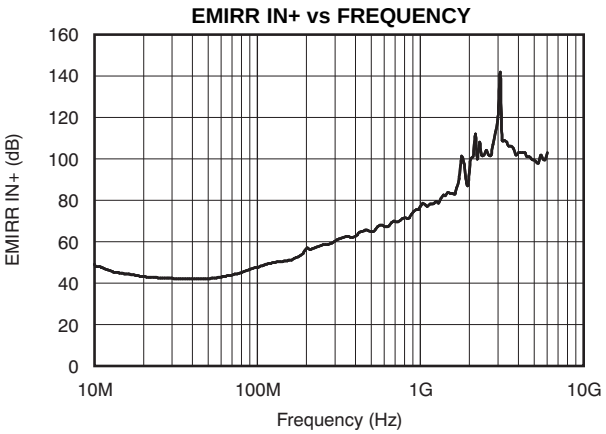


Figure 24.

APPLICATION INFORMATION

The OPAx180 family of operational amplifiers combine precision offset and drift with excellent overall performance, making them ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

OPERATING CHARACTERISTICS

The OPAx180 family of amplifiers is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to +105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

EMI REJECTION

The OPAx180 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx180 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 25 shows the results of this testing on the OPAx180. Detailed information can also be found in the Application Report EMI Rejection Ratio of Operational Amplifiers (*SBOA128*), available for download from the TI website.

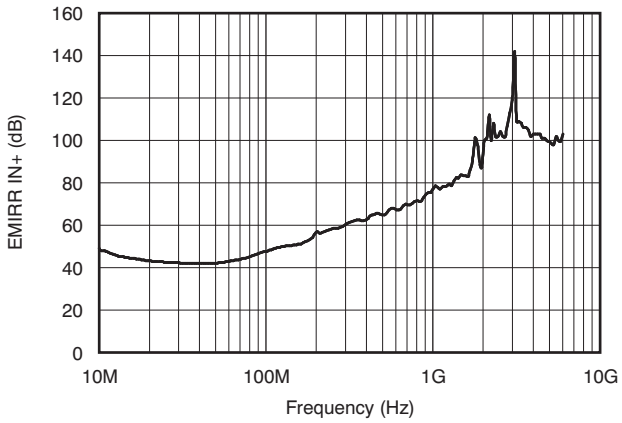


Figure 25. OPAx180 EMIRR Testing

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1-µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

PHASE-REVERSAL PROTECTION

The OPAx180 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx180 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 26.

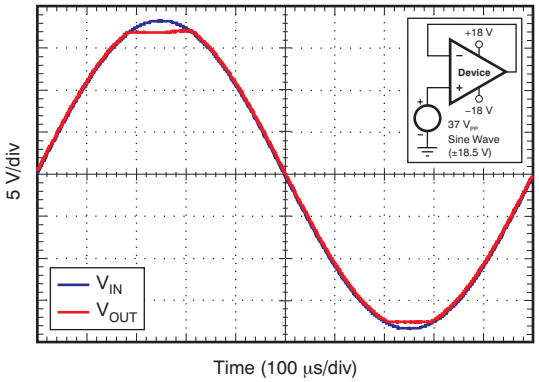


Figure 26. No Phase Reversal

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx180 have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 27 and Figure 28 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to the Applications Report, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI website, for details of analysis techniques and application circuits.

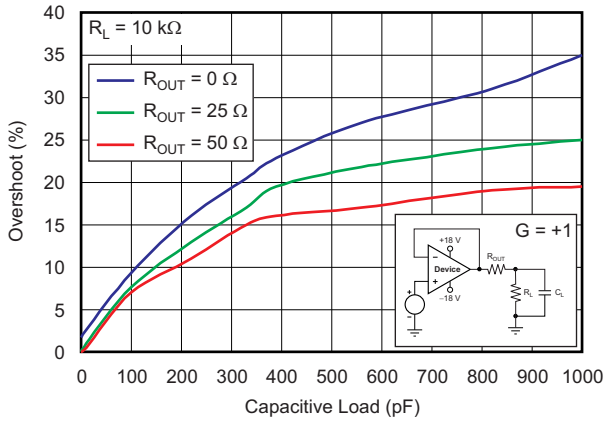


Figure 27. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

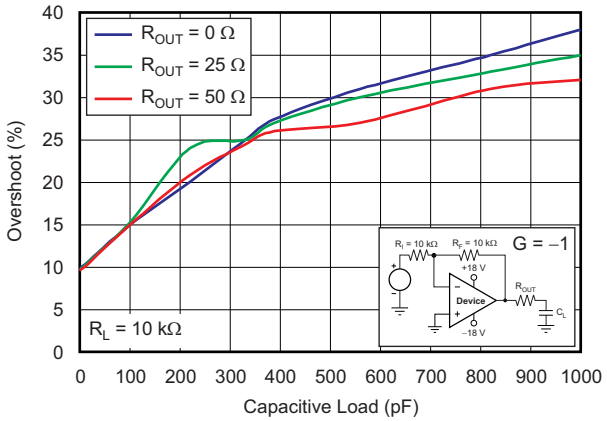


Figure 28. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 29 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

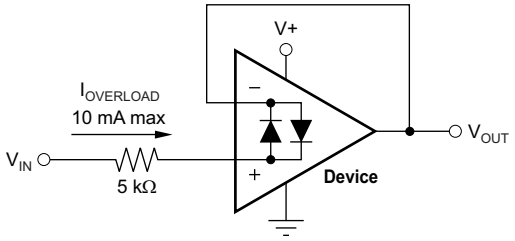


Figure 29. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

APPLICATION EXAMPLES

The application examples of Figure 30 and Figure 31 highlight only a few of the circuits where the OPAx180 family of devices can be used.

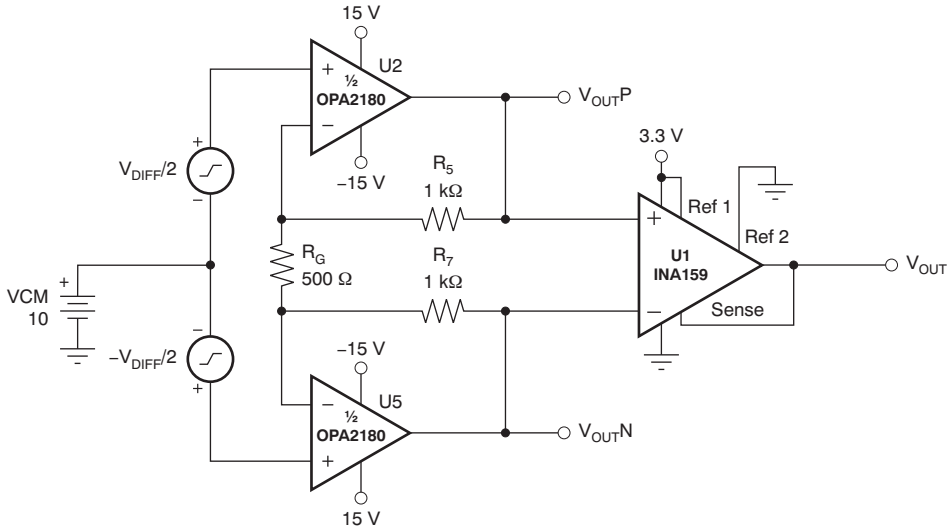
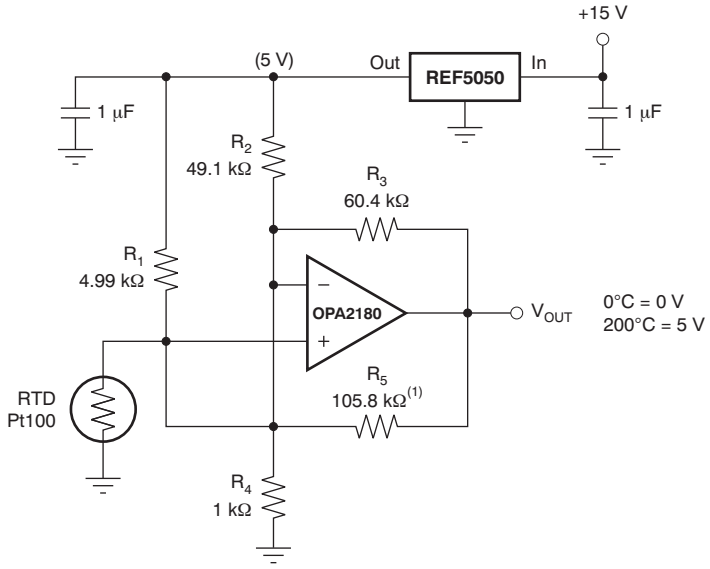


Figure 30. Discrete INA + Attenuation for ADC with 3.3-V Supply



(1) R_5 provides positive-varying excitation to linearize output.

Figure 31. RTD Amplifier with Linearization

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2011) to Revision C **Page**

- Changed product status from Mixed Status to Production Data 1
- Changed OPA4180 status to Production Data 1
- Added package marking to OPS2180 MSOP-8 row in Package Information table 2
- Deleted ordering number and transport media columns from Package Information table 2
- Changed Input Bias Current section in Electrical Characteristics (V_S = +4 V to +36 V) table 3

Changes from Revision A (November 2011) to Revision B **Page**

- Changed footnote 1 of Electrical Characteristics table 3
- Updated Figure 7 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2180ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2180	Samples
OPA2180IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	2180	Samples
OPA2180IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	2180	Samples
OPA2180IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2180	Samples
OPA4180ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	OPA4180	Samples
OPA4180IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	OPA4180	Samples
OPA4180IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	OPA4180	Samples
OPA4180IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	OPA4180	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

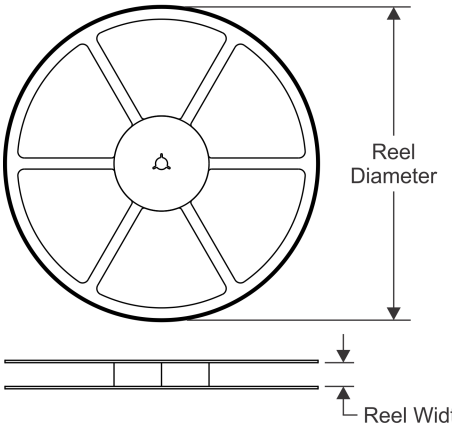
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

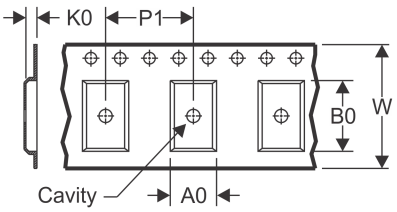
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

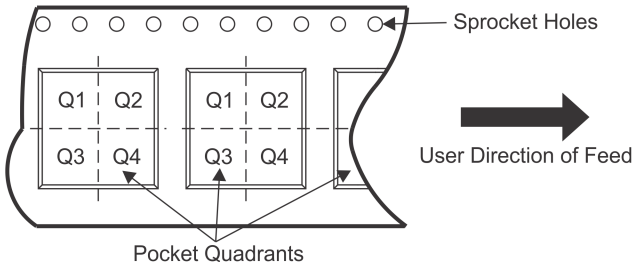


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

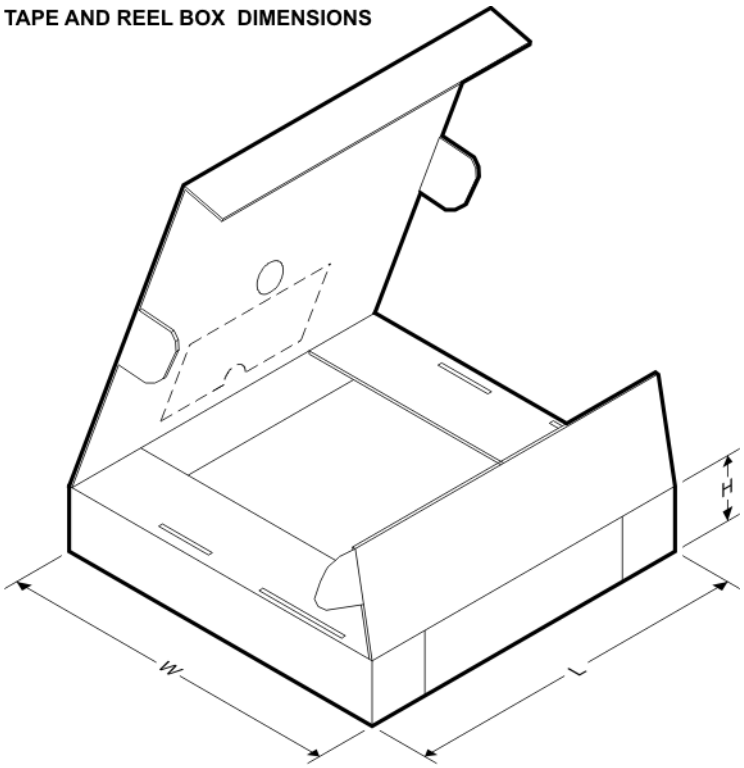
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2180IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA4180IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

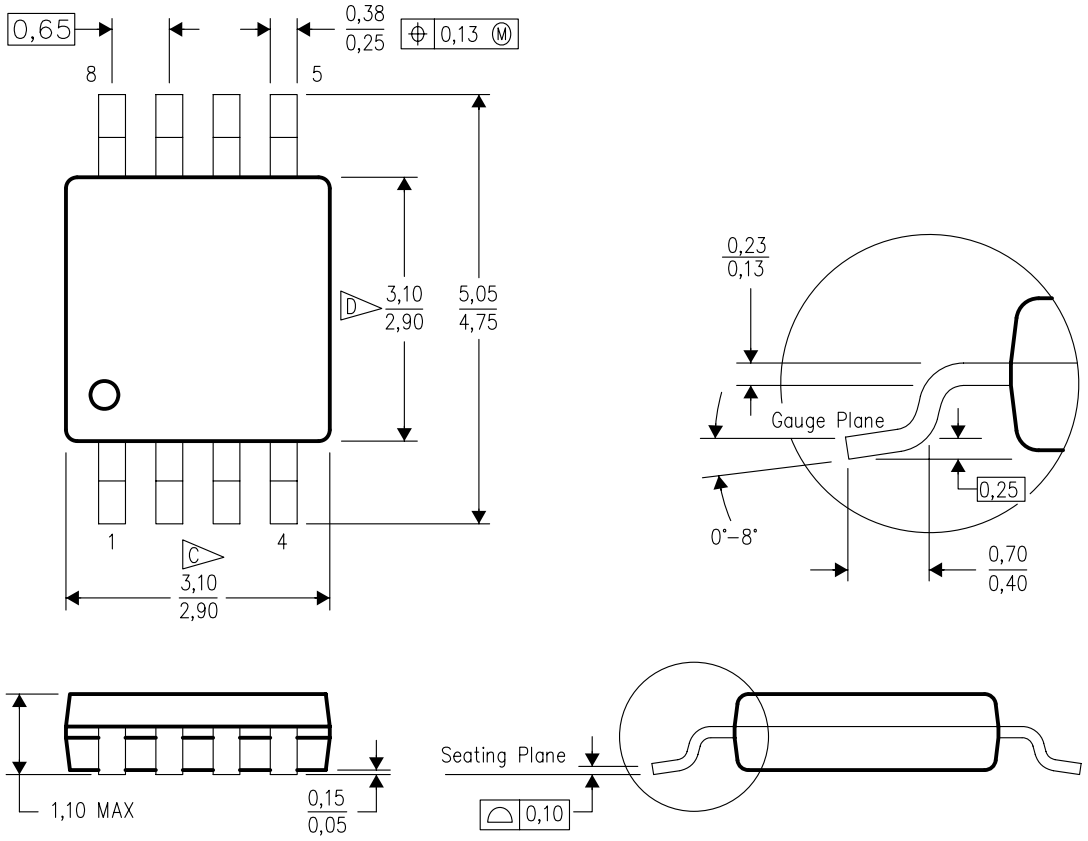
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2180IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA4180IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

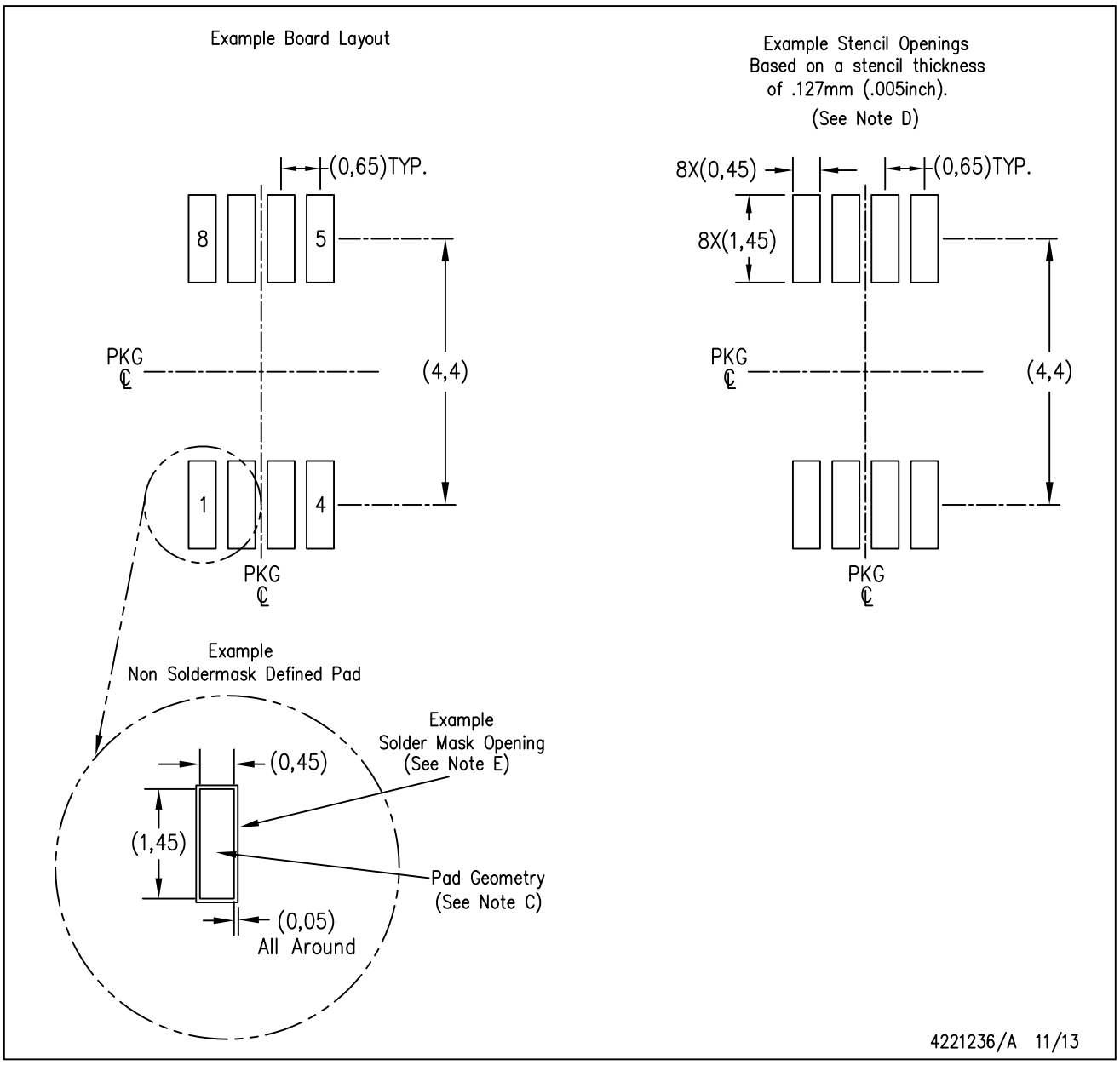
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

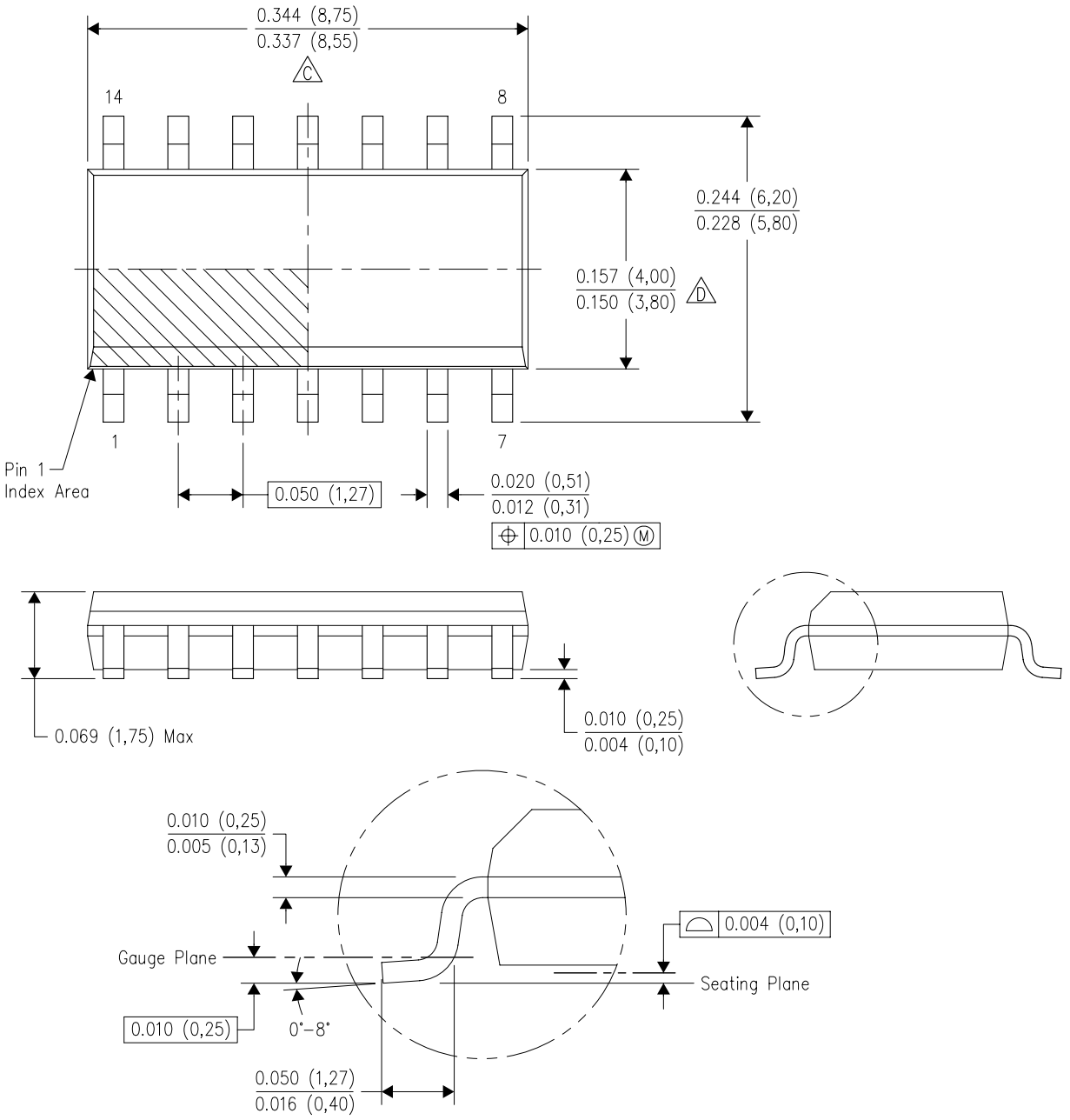
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

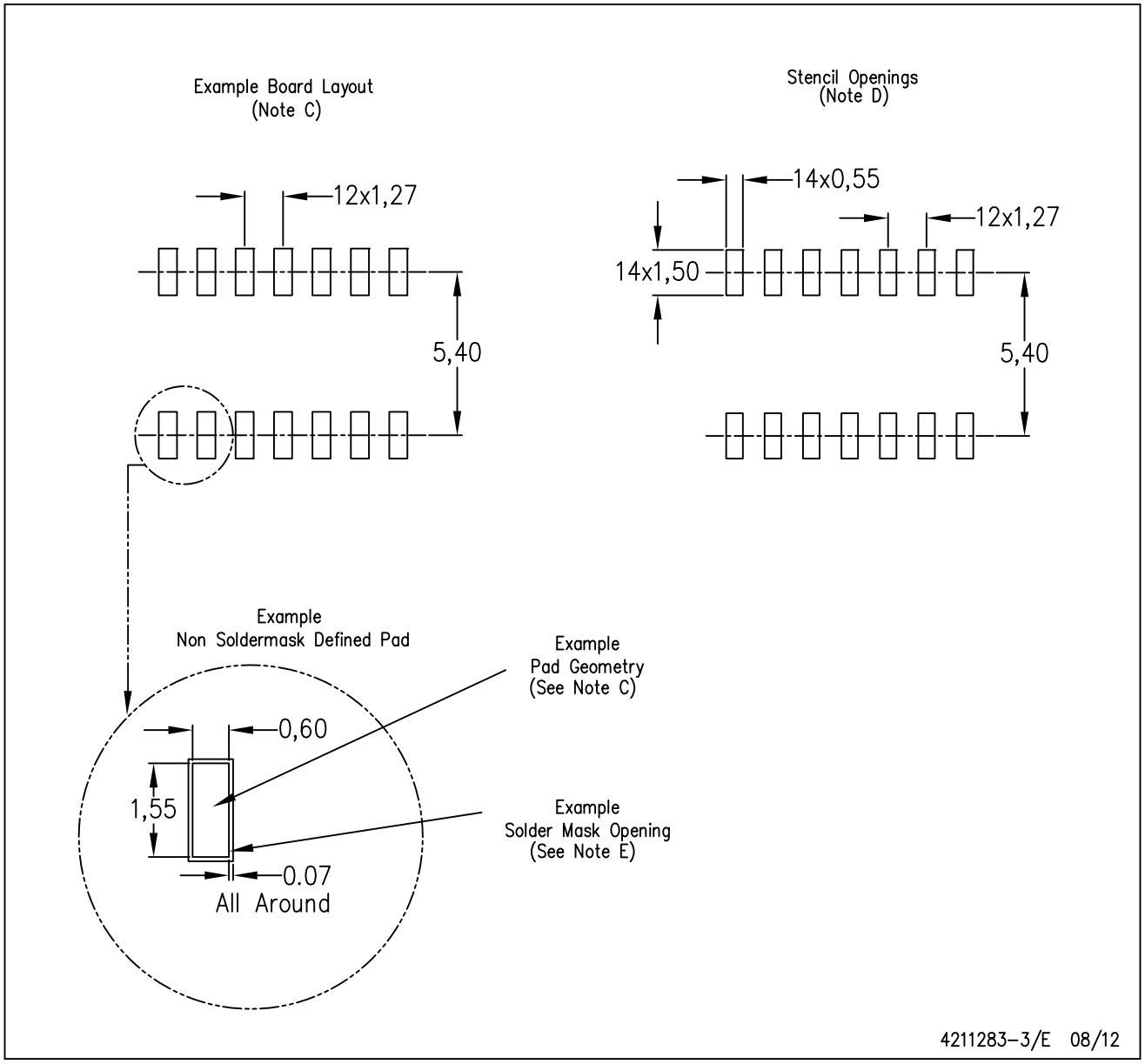
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

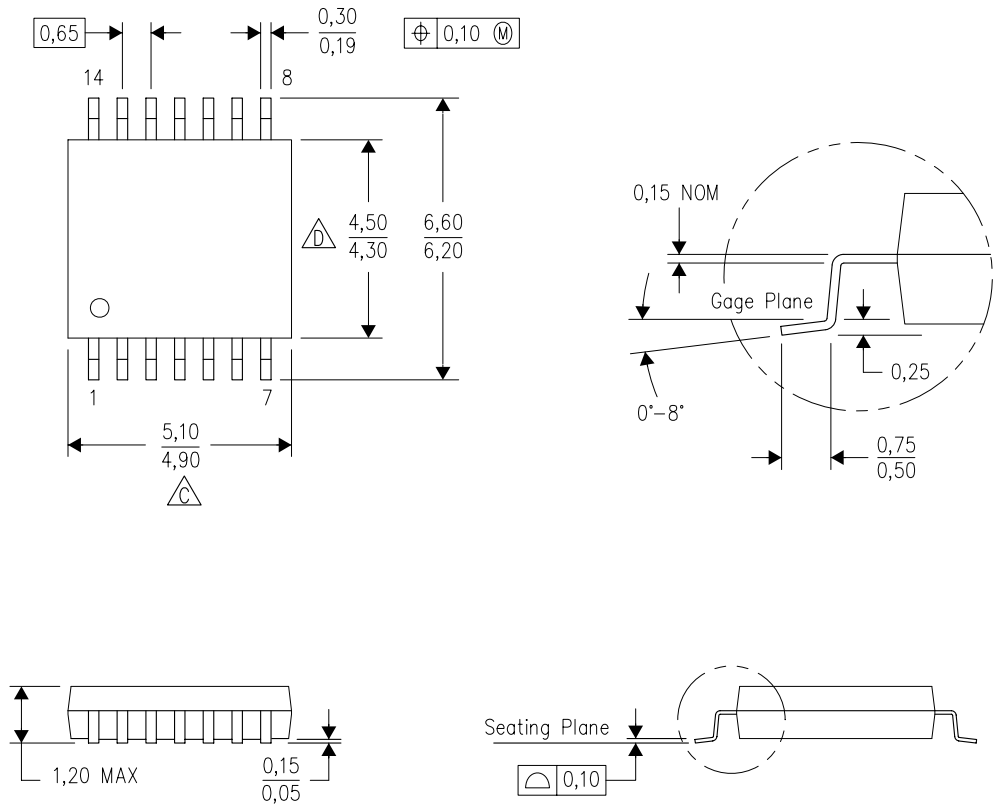
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

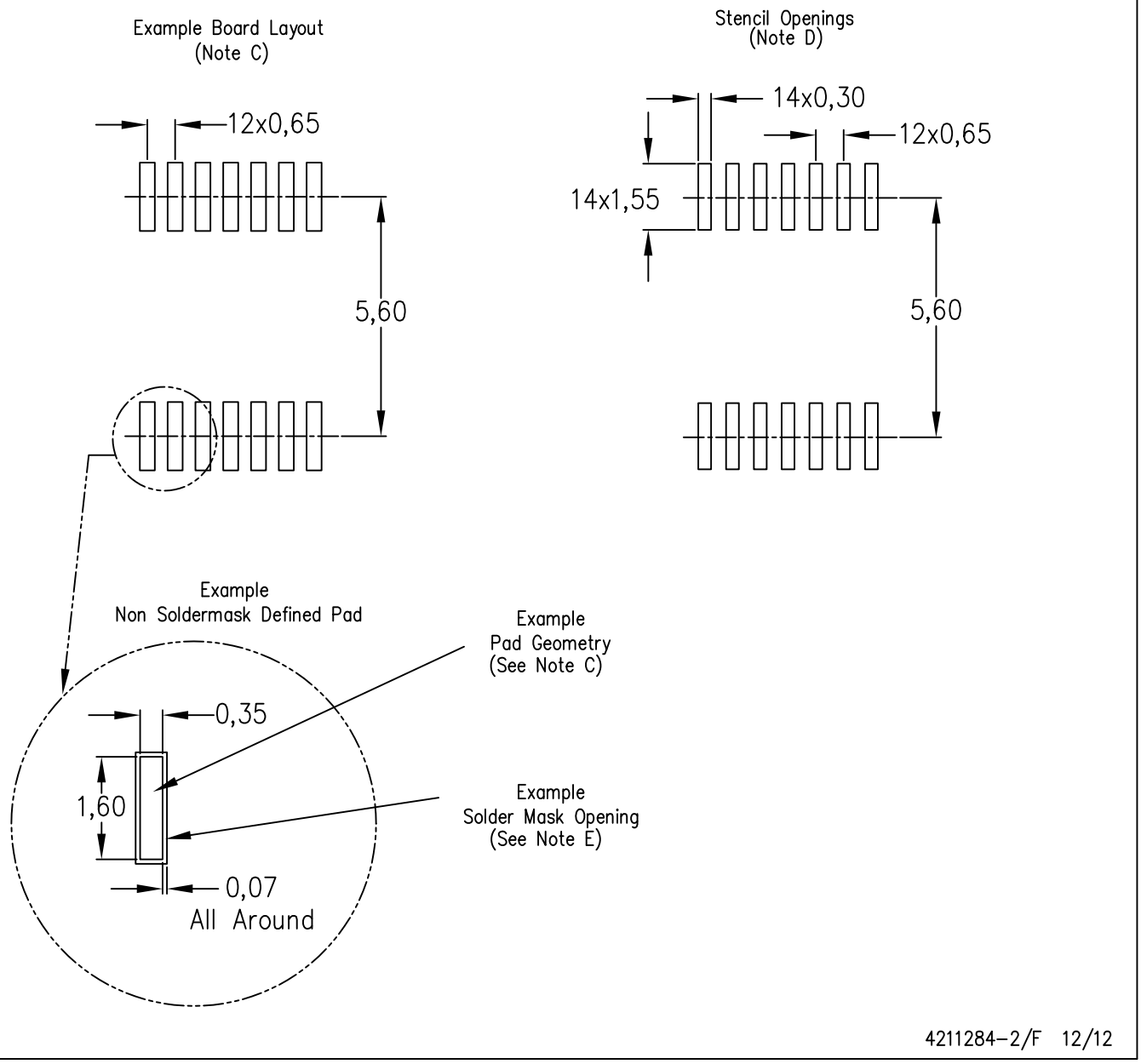
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

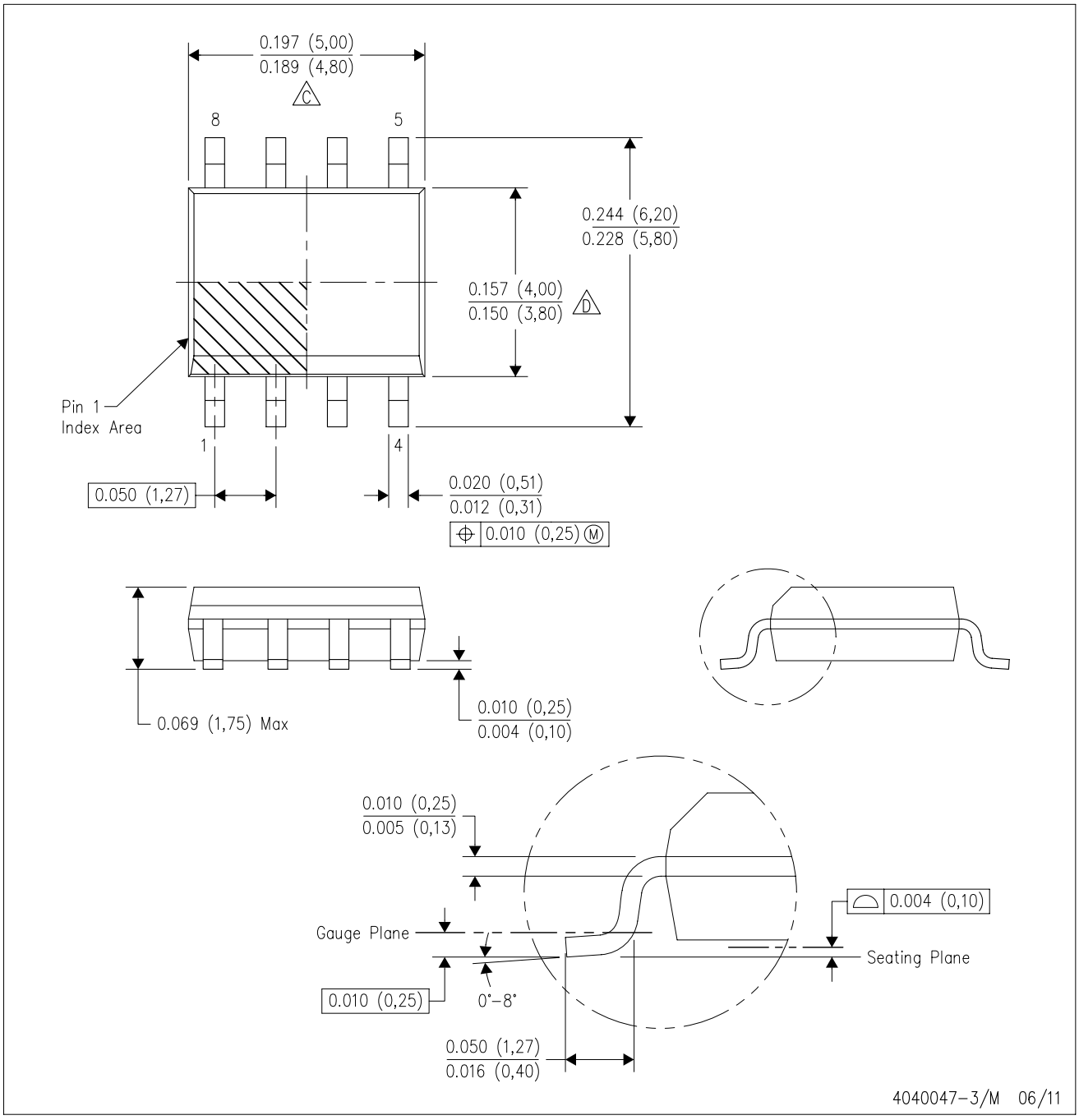
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



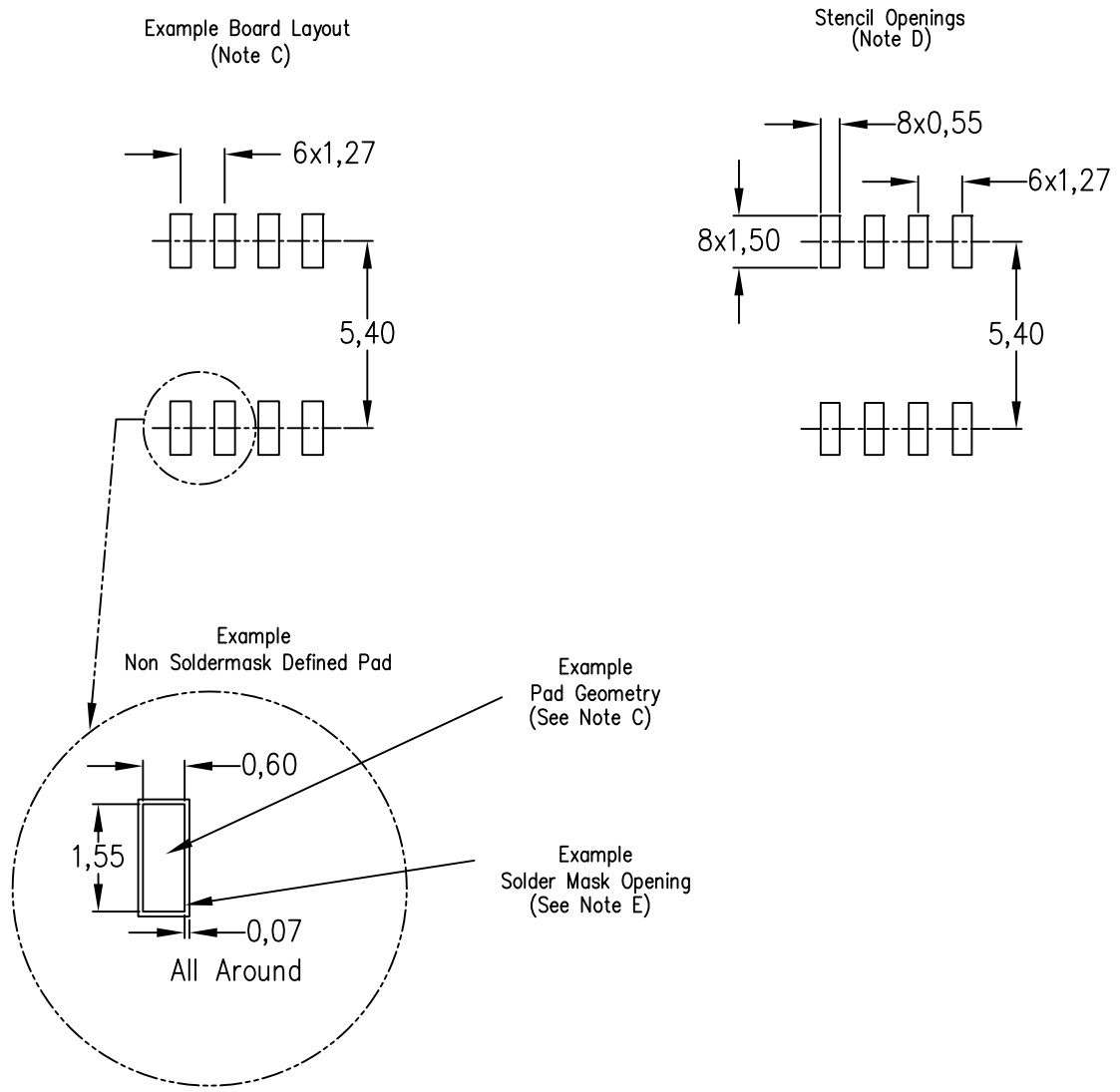
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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