SBOS282B − DECEMBER 2003 − REVISED FEBRUARY 2005

0.05μV/°C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zer∅-Drift Series

FEATURES

- **LOW OFFSET VOLTAGE: 5μV (max)**
- **ZERO DRIFT: 0.05μV/°C max**
- **QUIESCENT CURRENT: 750μA (max)**
- **SINGLE-SUPPLY OPERATION**
- **LOW BIAS CURRENT: 200pA (max)**
- **SHUTDOWN**
- ***Micro*SIZE PACKAGES**
- **WIDE SUPPLY RANGE: 2.7V to 12V**

APPLICATIONS

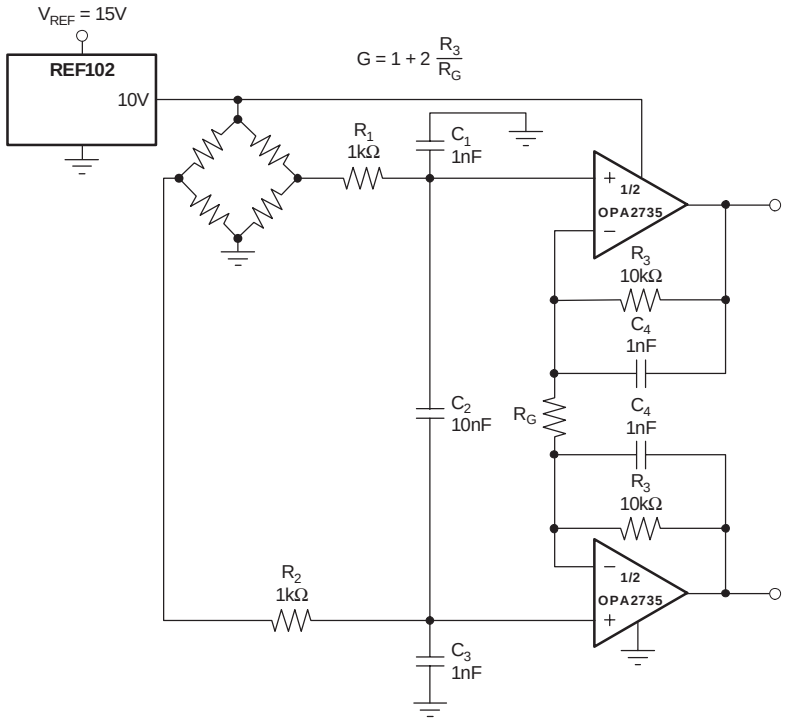
- **TRANSDUCER APPLICATIONS**
- **TEMPERATURE MEASUREMENTS**
- **ELECTRONIC SCALES**
- **MEDICAL INSTRUMENTATION**
- **BATTERY-POWERED INSTRUMENTS**
- **HANDHELD TEST EQUIPMENT**

DESCRIPTION

The OPA734 and OPA735 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide low offset voltage (5μV max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 50mV of the rails. Either single or bipolar supplies can be used in the range of +2.7V to +12V (±1.35V to ±6V). They are optimized for low-voltage, single-supply operation.

The OPA734 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is 9μA (max) and the output placed in a high-impedance state.

The single version is available in the MicroSIZE SOT23-5 (SOT23-6 for shutdown version) and the SO-8 packages. The dual version is available in the MSOP-8 and SO-8 packages (MSOP-10 only for the shutdown version). All versions are specified for operation from −40°C to +85°C.



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+13.2V
Signal Input Terminals, Voltage(2)	(V−) − 0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short Circuit(3)	Continuous
Operating Temperature	−40°C to +150°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model), OPA734	1000V
ESD Rating (Human Body Model), OPA735, OPA2734, OPA2735	2000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA734	SOT23-6	DBV	−40°C to +85°C	NSB	OPA734AIDBVT	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA734AIDBVR	Tape and Reel, 3000
OPA734	SO-8	D	−40°C to +85°C	OPA734A	OPA734AID	Rails, 100
〃	〃	〃	〃	〃	OPA734AIDR	Tape and Reel, 2500
OPA2734	MSOP-10	DGS	−40°C to +85°C	BGO	OPA2734AIDGST	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA2734AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA735	SOT23-5	DBV	−40°C to +85°C	NSC	OPA735AIDBVT	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA735AIDBVR	Tape and Reel, 3000
OPA735	SO-8	D	−40°C to +85°C	OPA735A	OPA735AID	Rails, 100
〃	〃	〃	〃	〃	OPA735AIDR	Tape and Reel, 2500
OPA2735	SO-8	D	−40°C to +85°C	OPA2735A	OPA2735AID	Rails, 100
〃	〃	〃	〃	〃	OPA2735AIDR	Tape and Reel, 2500
OPA2735	MSOP-8	DGK	−40°C to +85°C	BGN	OPA2735AIDGKT	Tape and Reel, 250
〃	〃	〃	〃	〃	OPA2735AIDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (V_S = +10V)

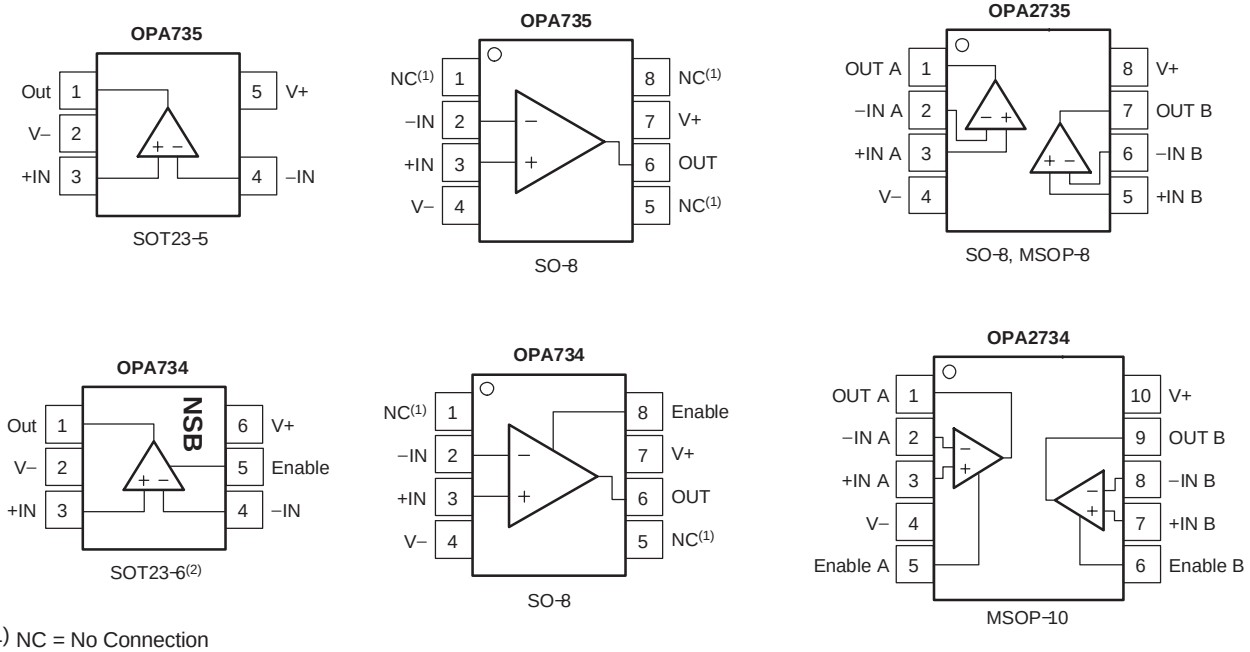
Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C.**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA734, OPA2734, OPA735, OPA2735 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}			1	5	µV
vs Temperature	**dV_{OS}/dT**			**0.01**	**0.05**	**µV/°C**
vs Power Supply	**PSRR**	**V_S = 2.7V to 12V, V_{CM} = 0V**		**0.2**	**1.8**	**µV/V**
Long-Term Stability				Note (1)		
Channel Separation, dc				0.1		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S/2		±100	±200	pA
over Temperature				**See Typical Characteristics**		**pA**
Input Offset Current	I_{OS}	V_{CM} = V_S/2		±200	±300	pA
NOISE						
Input Voltage Noise, f = 0.01Hz to 1Hz	e_n			0.8		μV_{PP}
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n			2.5		μV_{PP}
Input Voltage Noise Density, f = 1kHz	e_n			135		$nV/\sqrt{Hz}$
Input Current Noise Density, f = 1kHz	i_n			40		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	**V_{CM}**		**(V−) − 0.1**		**(V+) − 1.5**	**V**
Common-Mode Rejection Ratio	**CMRR**	**(V−) − 0.1V < V_{CM} < (V+) − 1.5V**	**115**	**130**		**dB**
INPUT CAPACITANCE						
Differential				2		pF
Common-Mode				10		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**(V−) + 100mV < V_O < (V+) − 100mV**	**115**	**130**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			1.6		MHz
Slew Rate	SR	G = +1		1.5		V/µs
OUTPUT						
Voltage Output Swing from Rail		**R_L = 10kΩ**		**20**	**50**	**mV**
Short-Circuit Current	I_{SC}			±20		mA
Open-Loop Output Impedance		f = 1MHz, I_O = 0		125		Ω
Capacitive Load Drive	C_{LOAD}			See Typical Characteristics		
ENABLE/SHUTDOWN						
t_{OFF}				1.5		µs
t_{ON}(2)				150		µs
V_L (amplifier is shutdown)			V−		(V−) + 0.8	V
V_H (amplifier is active)			(V−) + 2		V+	V
I_{QSD} (per amplifier)				4	9	µA
Input Bias Current of Enable Pin				3		µA
POWER SUPPLY						
Operating Voltage Range	V_S			2.7 to 12 (±1.35 to ±6)		V
Quiescent Current (per amplifier)	**I_Q**	**I_O = 0**		**0.6**	**0.75**	**mA**
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range			−40		+150	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5, SOT23-6				200		°C/W
MSOP-8, MSOP-10, SO-8				150		°C/W

(1) 300-hour life test at 150°C demonstrated randomly distributed variation in the range of measurement limits—approximately 1µV.
(2) Device requires one complete auto-zero cycle to return to V_{OS} accuracy.

PIN CONFIGURATIONS

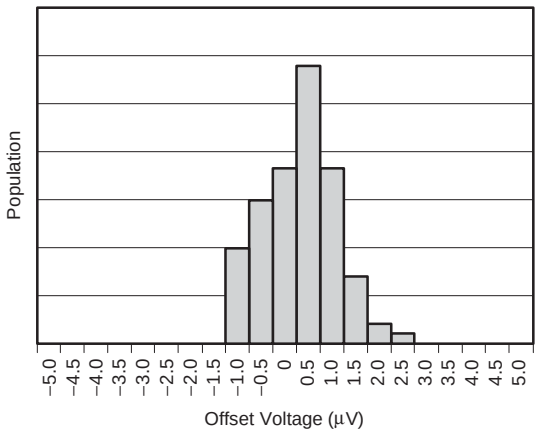


(1) NC = No Connection
(2) Pin 1 of the SOT23-6 is determined by orienting the package marking as shown in the diagram.

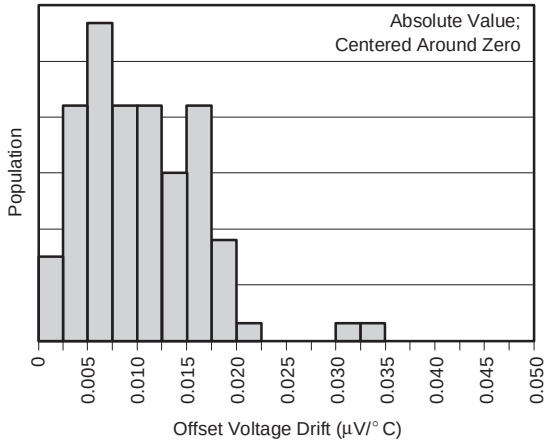
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±5V (same as +10V).

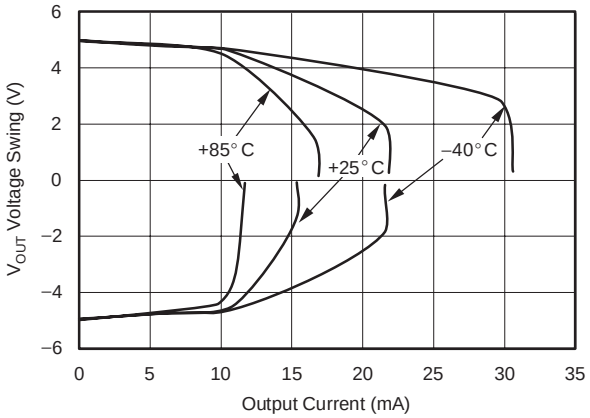
OUTPUT VOLTAGE PRODUCTION DISTRIBUTION



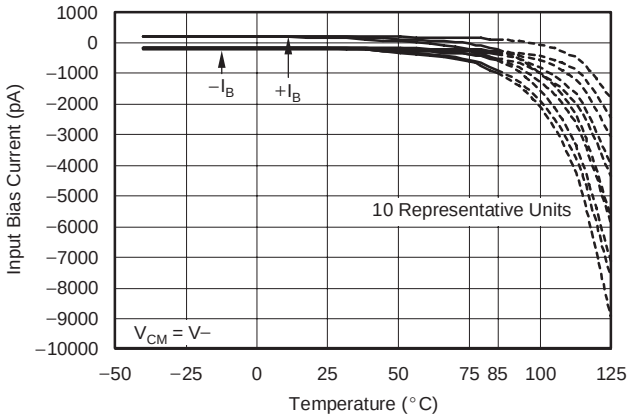
OUTPUT VOLTAGE DRIFT PRODUCTION DISTRIBUTION



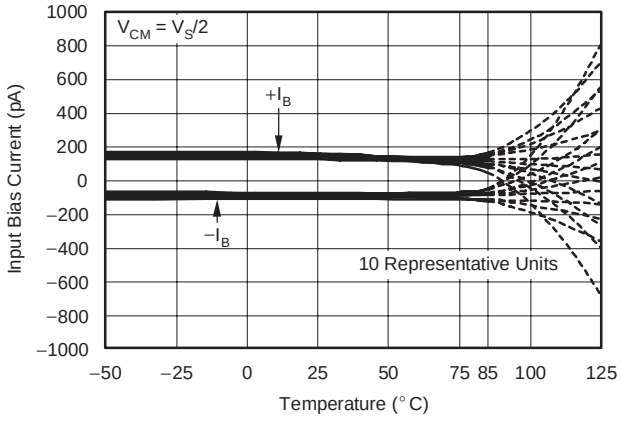
OUTPUT VOLTAGE SWING TO RAIL
vs OUTPUT CURRENT



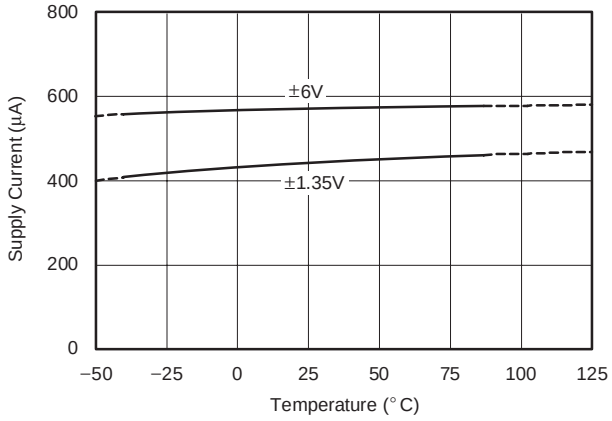
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE



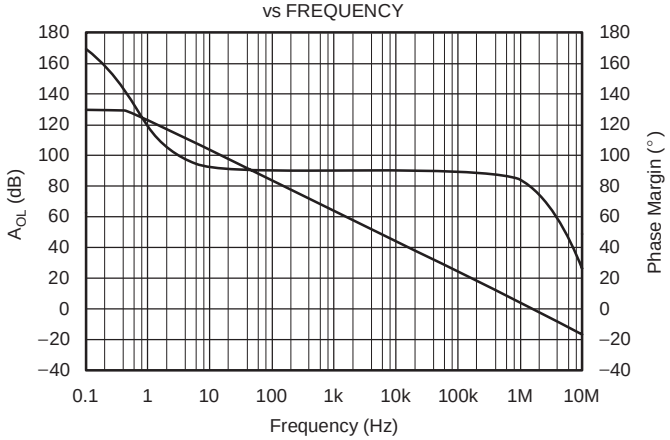
SUPPLY CURRENT vs TEMPERATURE



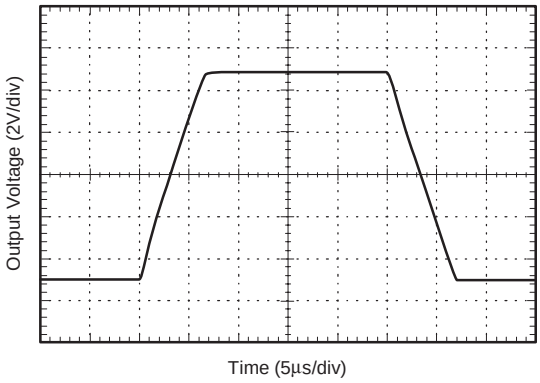
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±5V (same as +10V).

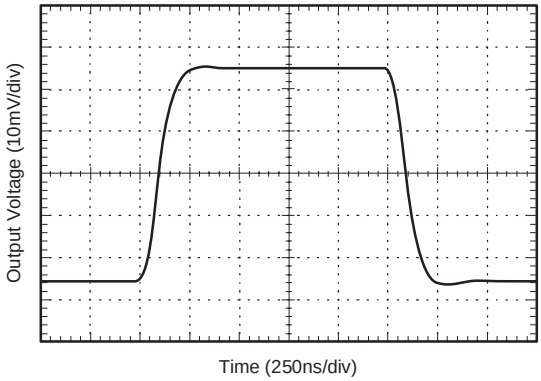
OPEN−LOOP GAIN AND PHASE MARGIN vs FREQUENCY



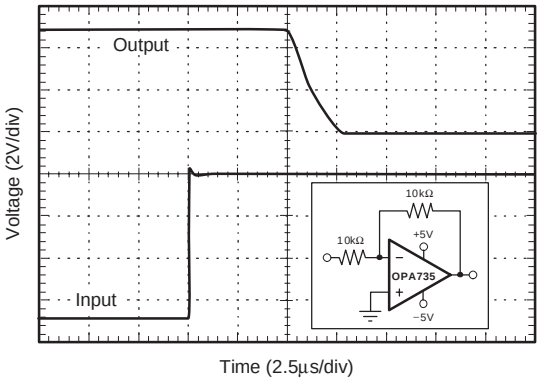
LARGE−SIGNAL RESPONSE



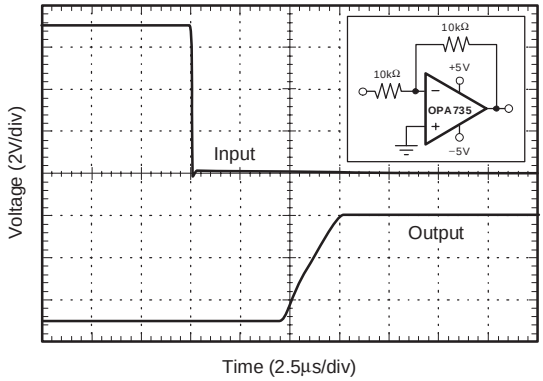
SMALL−SIGNAL RESPONSE



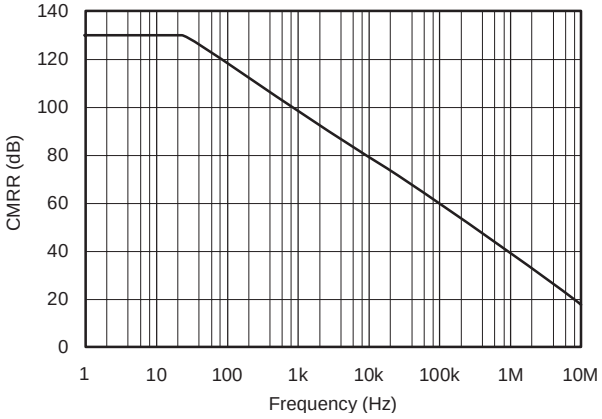
POSITIVE OVERVOLTAGE RECOVERY



NEGATIVE OVERVOLTAGE RECOVERY



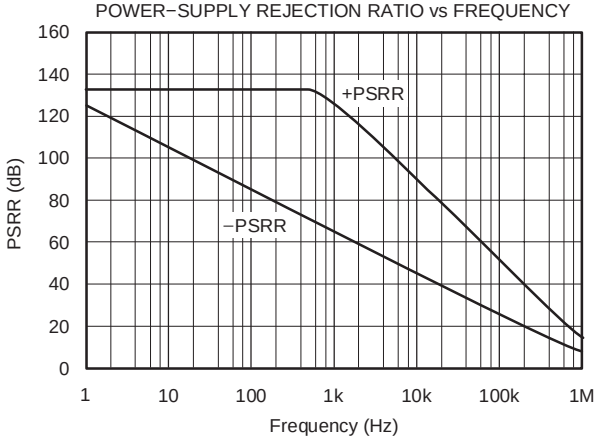
COMMON−MODE REJECTION RATIO vs FREQUENCY



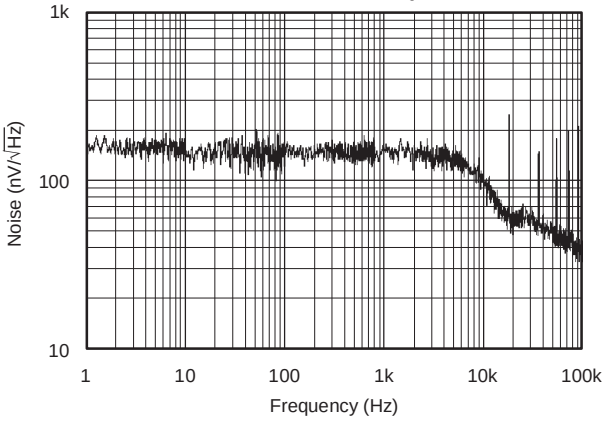
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±5V (same as +10V).

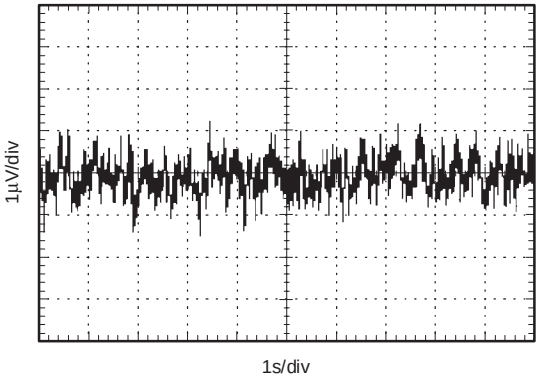
POWER−SUPPLY REJECTION RATIO vs FREQUENCY



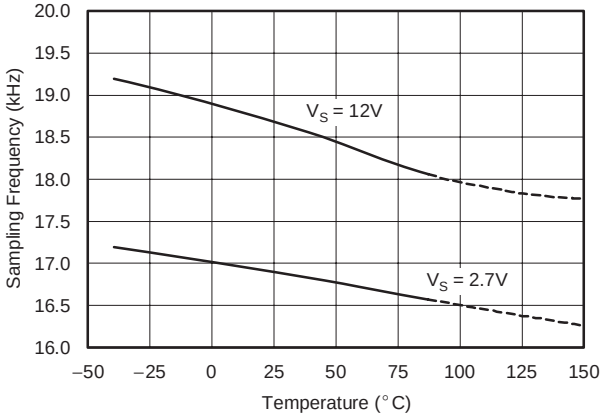
VOLTAGE NOISE vs FREQUENCY



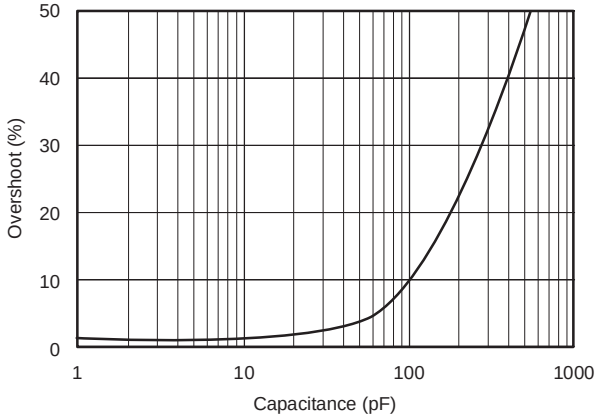
0.1Hz TO 10Hz NOISE



SAMPLING FREQUENCY vs TEMPERATURE



SMALL−SIGNAL OVERSHOOT vs CAPACITIVE LOAD



APPLICATIONS INFORMATION

The OPA734 and OPA735 series of op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and demonstrate very low drift over time and temperature.

Good layout practice mandates the use of a 0.1µF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals:

1. Use low thermoelectric-coefficient connections (avoid dissimilar metals).
2. Thermally isolate components from power supplies or other heat sources.
3. Shield op amp and input circuitry from air currents such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1µV/°C or higher, depending on the materials used.

OPERATING VOLTAGE

The OPA734 and OPA735 op amp family operates with a power-supply range of +2.7V to +12V (±1.35V to ±6V). Supply voltages higher than +13.2V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA734 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V− supply voltage of the op amp. A logic HIGH enables the op amp. A valid logic HIGH is defined as > (V−) + 2V. The valid logic HIGH signal can be up to the positive supply, independent of the negative power supply voltage. A valid logic LOW is defined as < 0.8V above the V− supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin is connected to internal pull-up circuitry and will enable the device if this pin is left open circuit.

The logic input is a CMOS input. Separate logic inputs are provided for each op amp on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is 150µs, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to returning to full accuracy, the amplifier may function properly, but with unspecified offset voltage.

Disable time is 1.5µs. When disabled, the output assumes a high-impedance state. The disable state allows the OPA734 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from (V−) − 0.1V to (V+) − 1.5V. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the specified input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 100pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

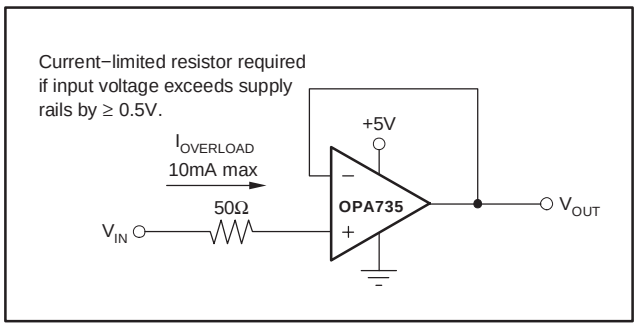


Figure 1. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA734 and OPA735 series of op amps use an auto-zero topology with a time-continuous 1.6MHz op amp in the signal path. This amplifier is zero-corrected every 100µs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100µs in addition to the start-up time for the bias circuitry to achieve specified V_{OS} accuracy. Prior to this time, the amplifier may function properly but with unspecified offset voltage.

Low-gain (< 20) operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.1% of a full-scale input step change, one calibration cycle (100µs) can be required to achieve full accuracy.

The term *clock feedthrough* describes the presence of the clock frequency in the output spectrum. In auto-zeroed op amps, clock feedthrough may result from the settling of the internal sampling capacitor, or from the small amount of charge injection that occurs during the sample-and-hold of the op amp offset voltage. Feedthrough can be minimized by keeping the source impedance relatively low (< 1kΩ) and matching the source impedance on both input terminals. If the source resistance is high (> 1kΩ) feedthrough can generally be reduced with a capacitor of 1nF or greater in parallel with the source or feedback resistors. See the circuit application examples.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

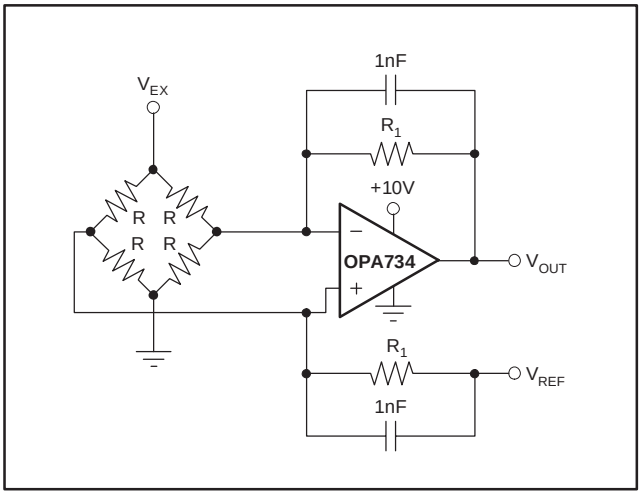


Figure 2. Single Op Amp Bridge Amplifier Circuit

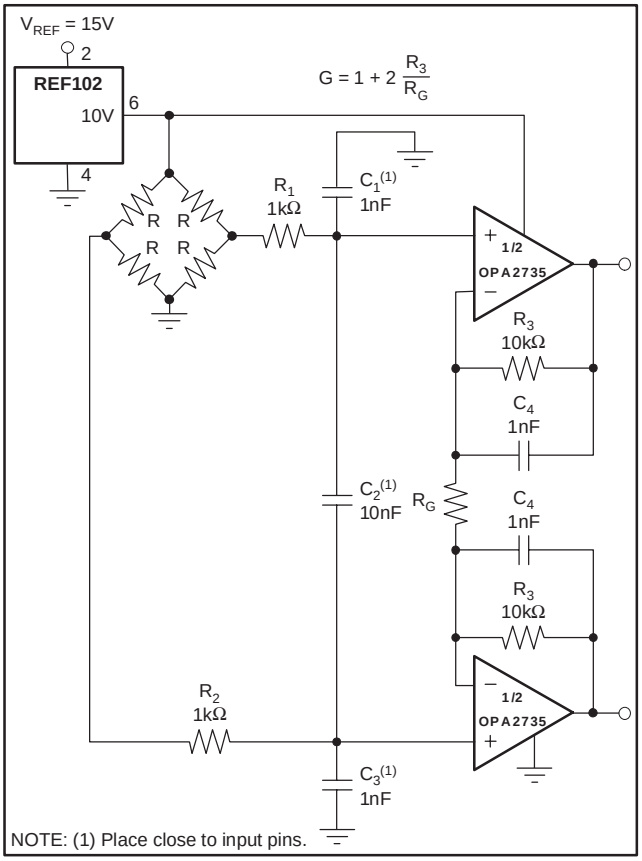
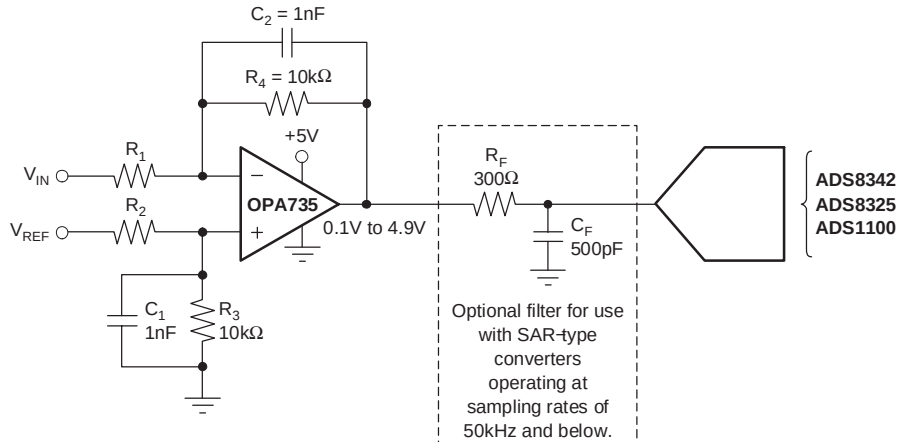
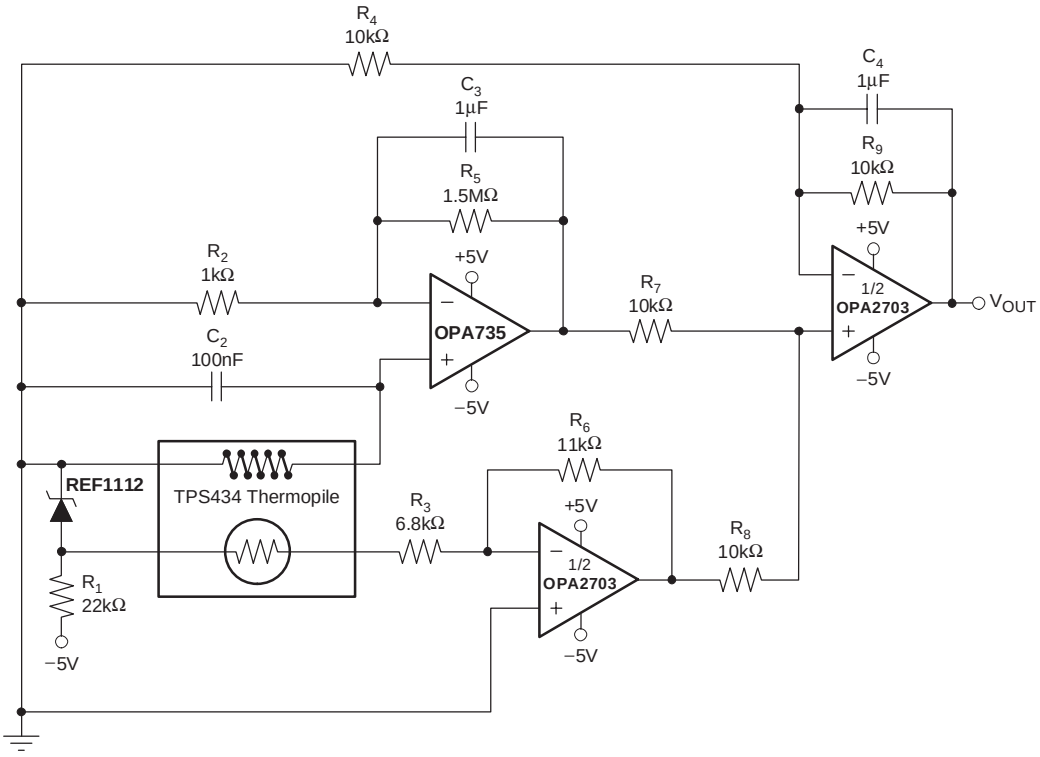


Figure 3. Differential Output Bridge Amplifier



V_{IN}	V_{REF}	R_1	R_2
±10V	5V	42.2kΩ	14.7kΩ
±5V	5V	20.8kΩ	19.6kΩ
0V to 10V	5V	20.8kΩ	5.11kΩ
0V to 5V	5V	10.5kΩ	10kΩ

Figure 4. Driving ADC



NOTE: The TPS434, by Perkin Elmer Optoelectronics, is a thermopile detector with integrated thermistor for cold-junction reference.

Figure 5. Thermopile Non-Contact Surface Temperature Measurement

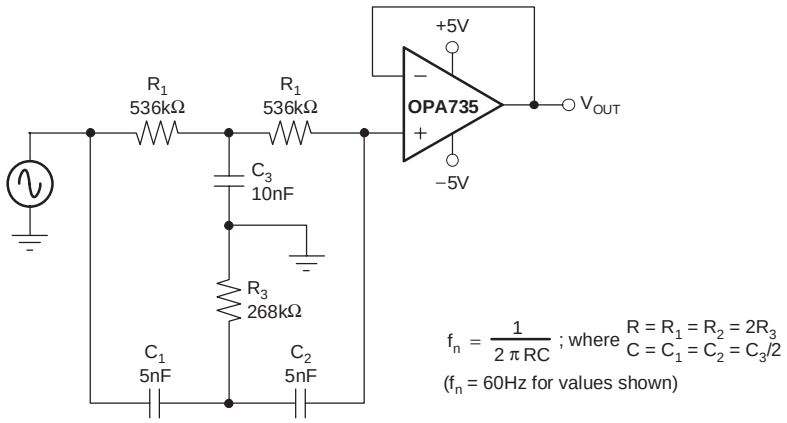
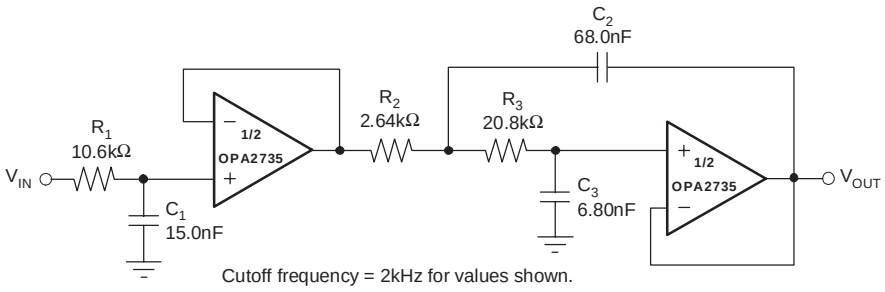
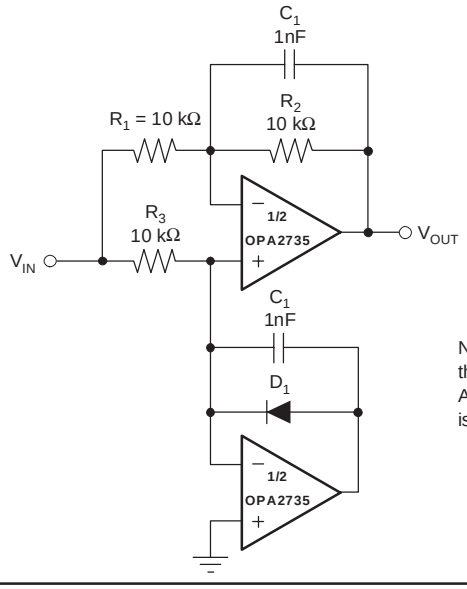


Figure 6. Twin-T Notch Filter



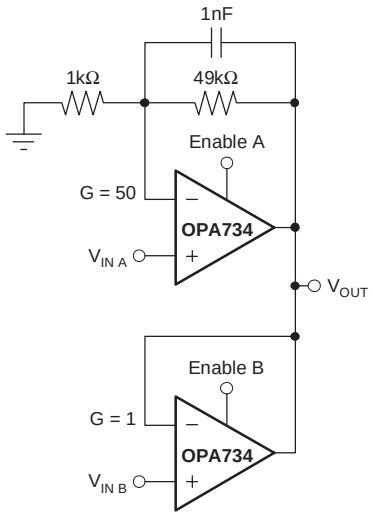
NOTE: FilterPro is a low-pass filter design program available for download at no cost from TI's web site (www.ti.com). The program can be used to easily determine component values for other cutoff frequencies or filter types.

Figure 7. High DC Accuracy, 3-Pole Low-Pass Filter



NOTE: Dynamic range of the circuit is not reduced by the diode voltage drop since the diode is not in the signal path. Application Bulletin *Precision Absolute Value Circuits* (SBOA068) is available at www.ti.com and provides further information about rectifier circuits.

Figure 8. Precision Full-Wave Rectifier with Full Dynamic Range



Enable inputs are CMOS logic compatible.

Figure 9. High-Precision 2-Input MUX for Programmable Gain

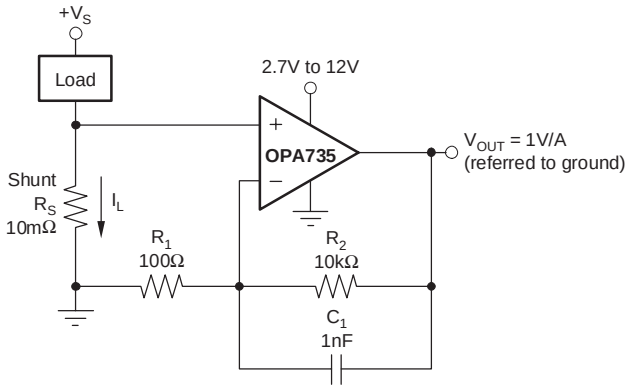


Figure 10. Low-Side Power-Supply Current Sensing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2734AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2734AIDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2734AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2734AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2735AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA734AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A	Samples
OPA734AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA734AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A	Samples
OPA735AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

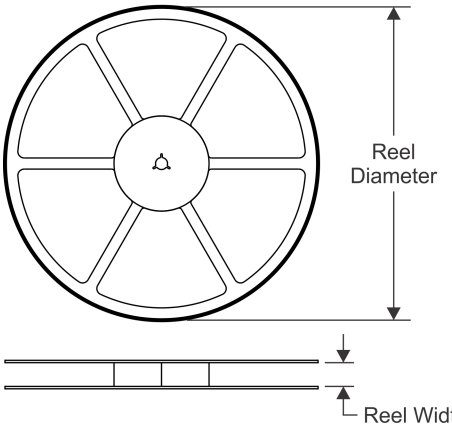
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

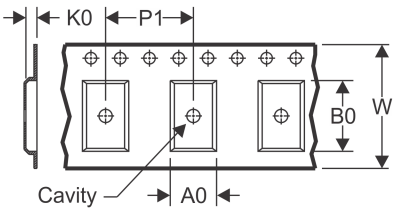
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

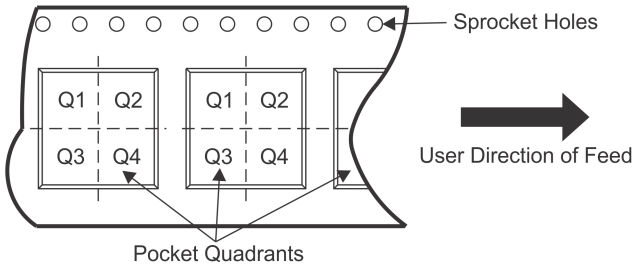


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

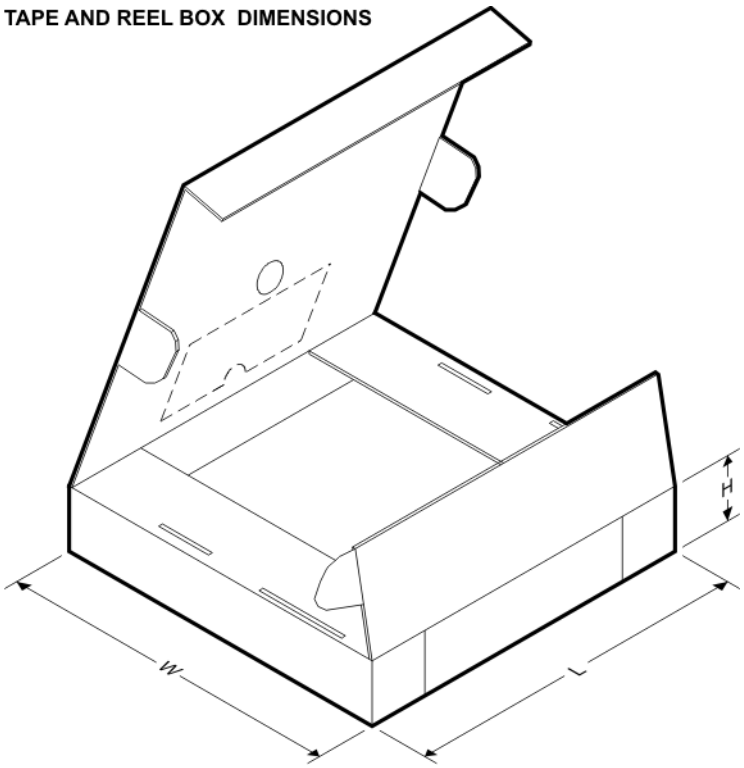
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2734AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2734AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

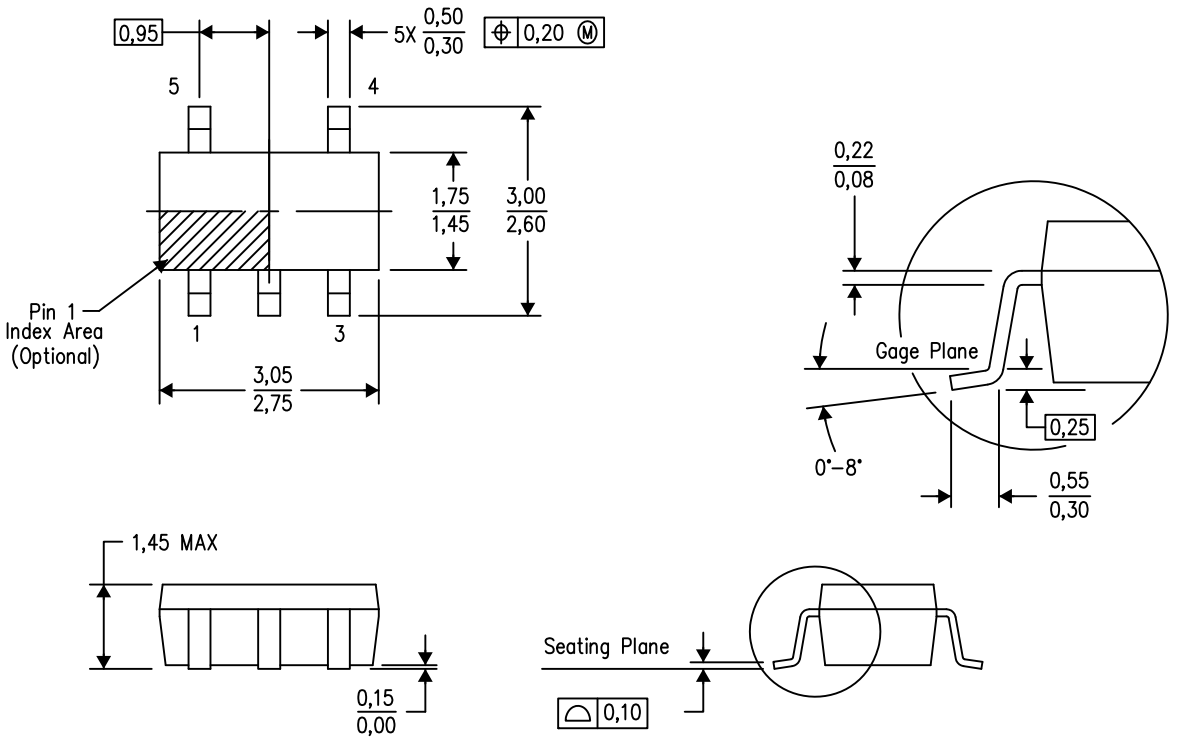
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2734AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2734AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2735AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2735AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2735AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA735AIDR	SOIC	D	8	2500	367.0	367.0	35.0

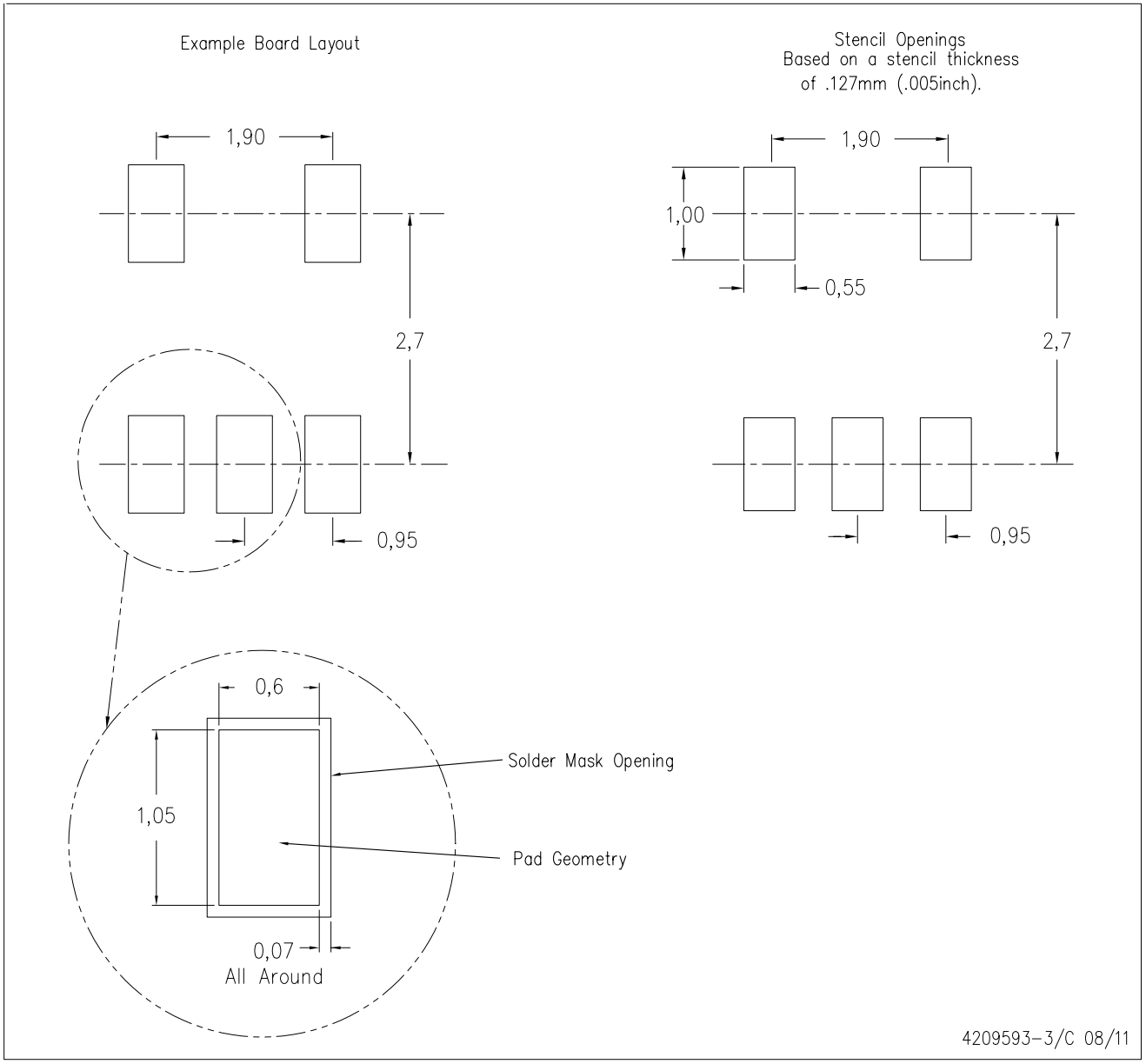
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

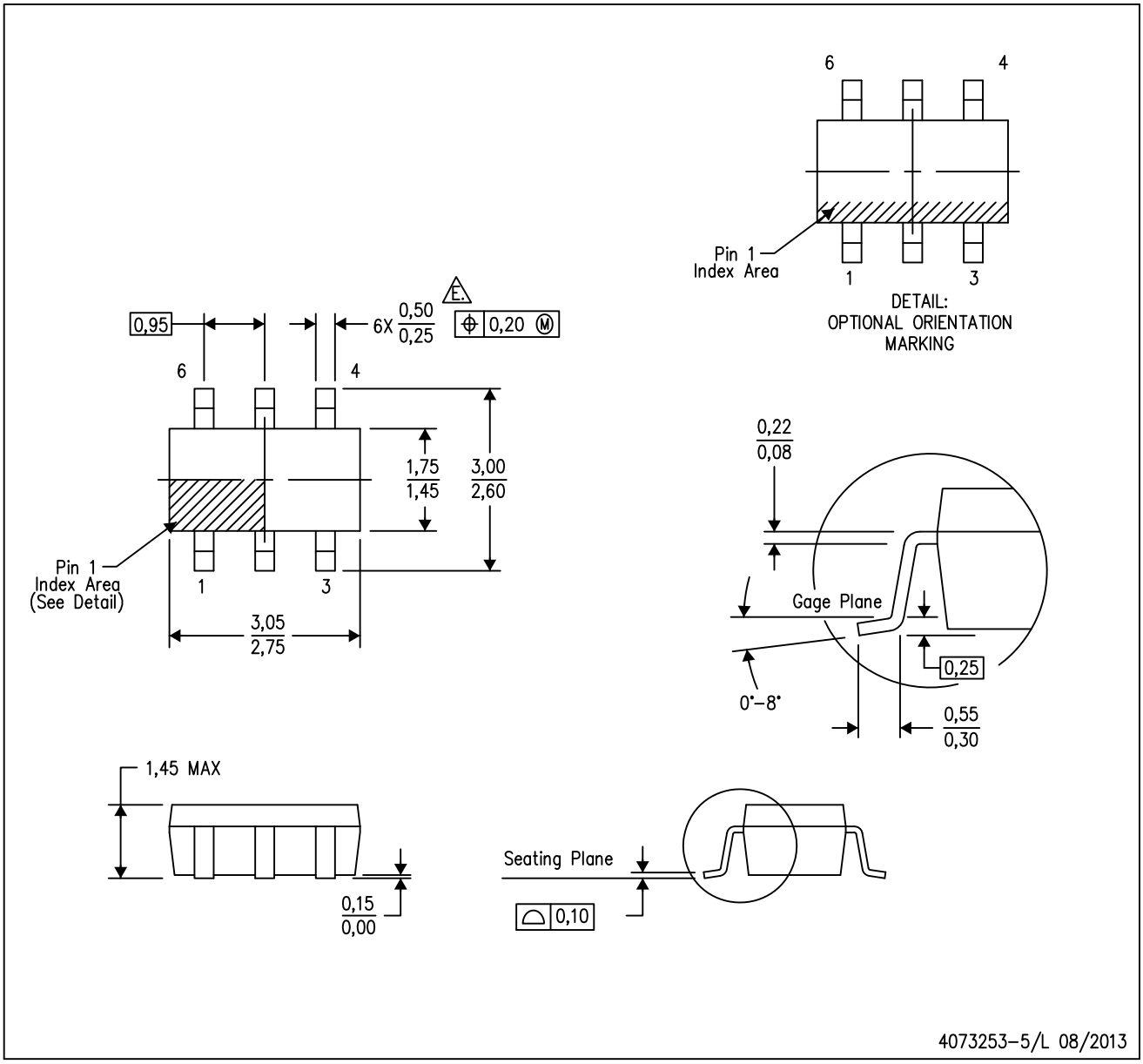
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



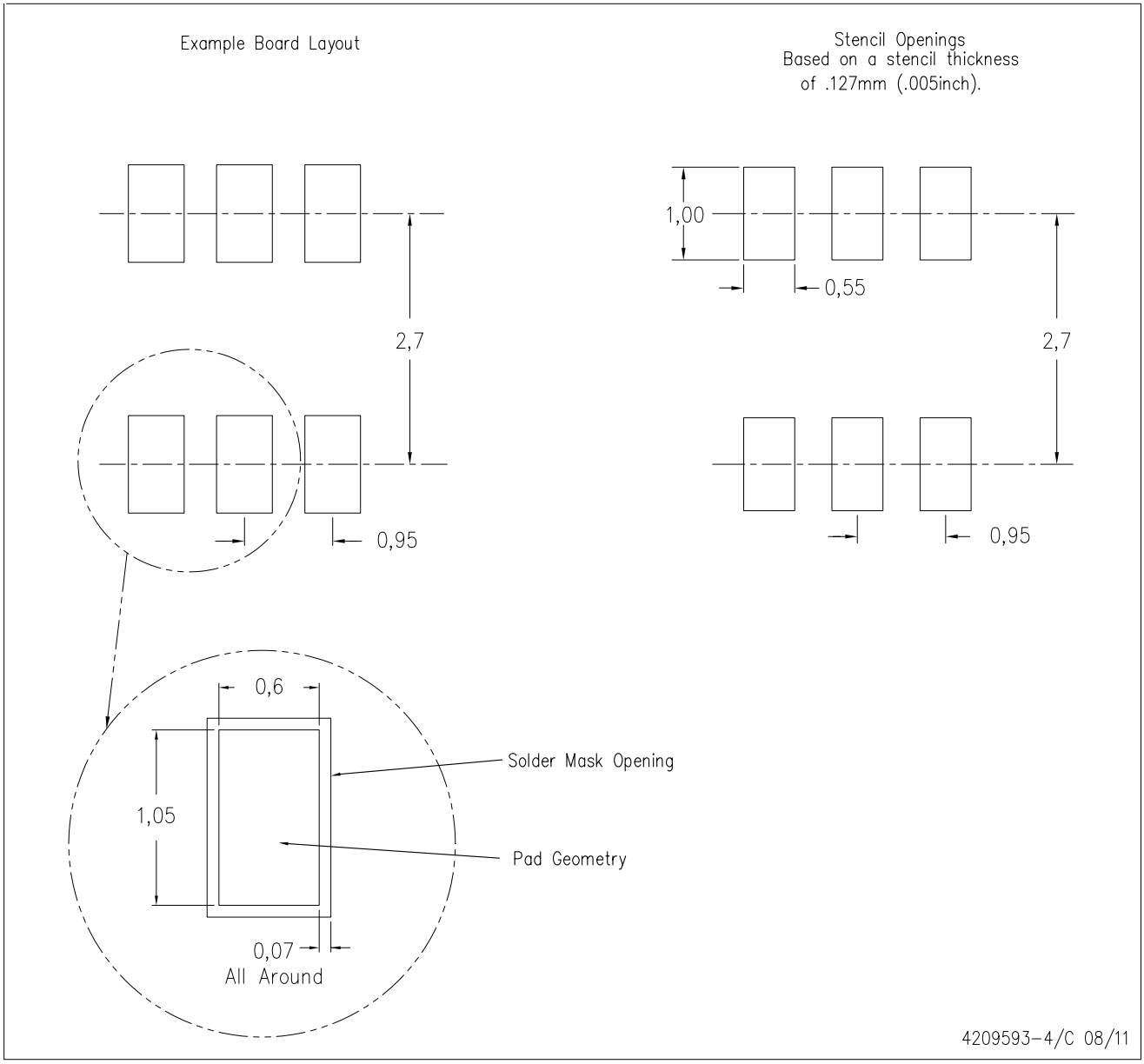
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



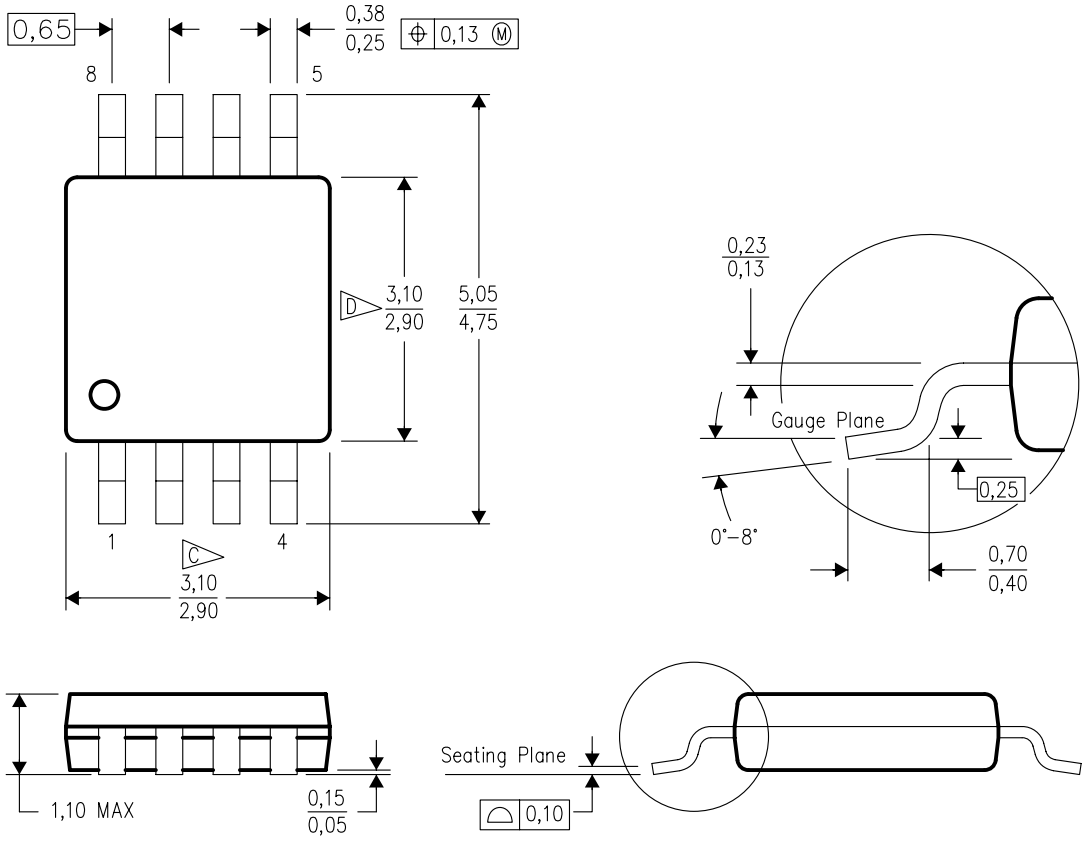
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

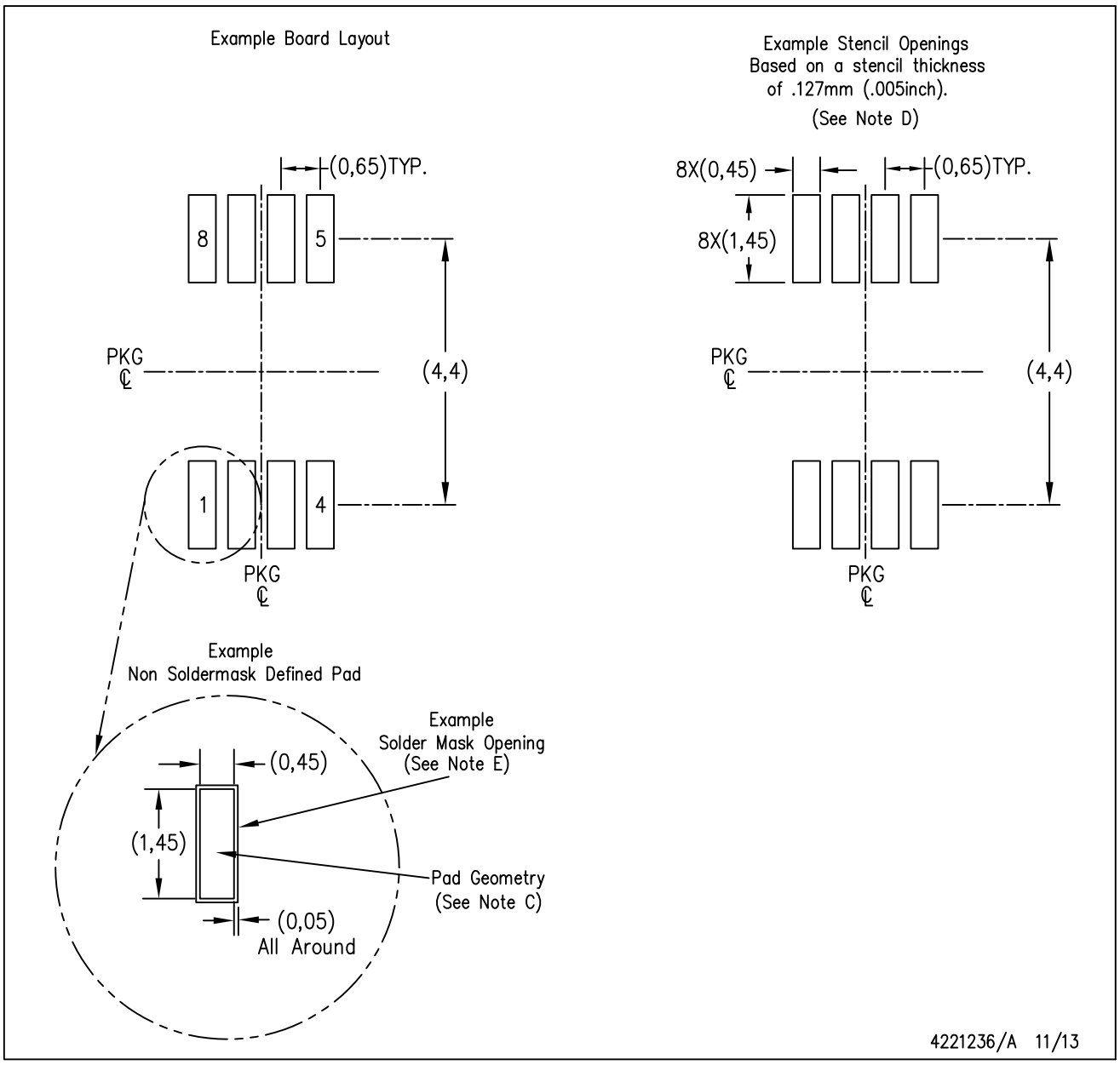
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

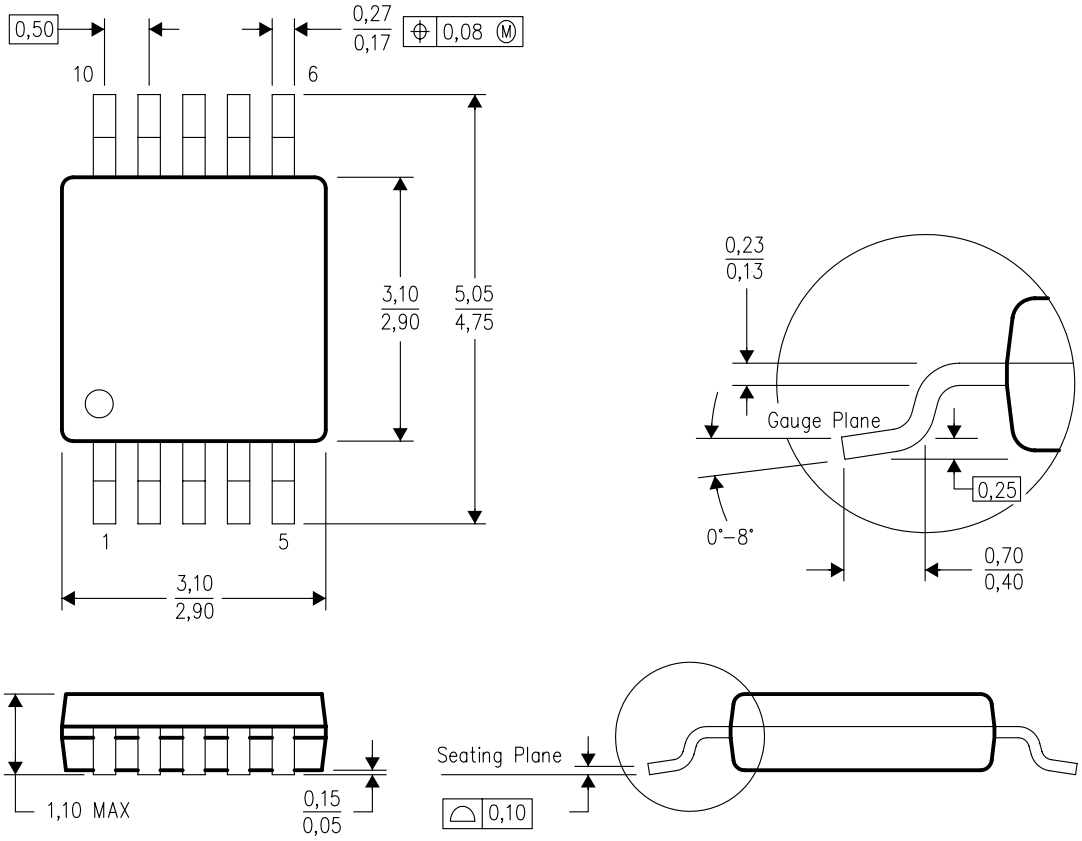
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

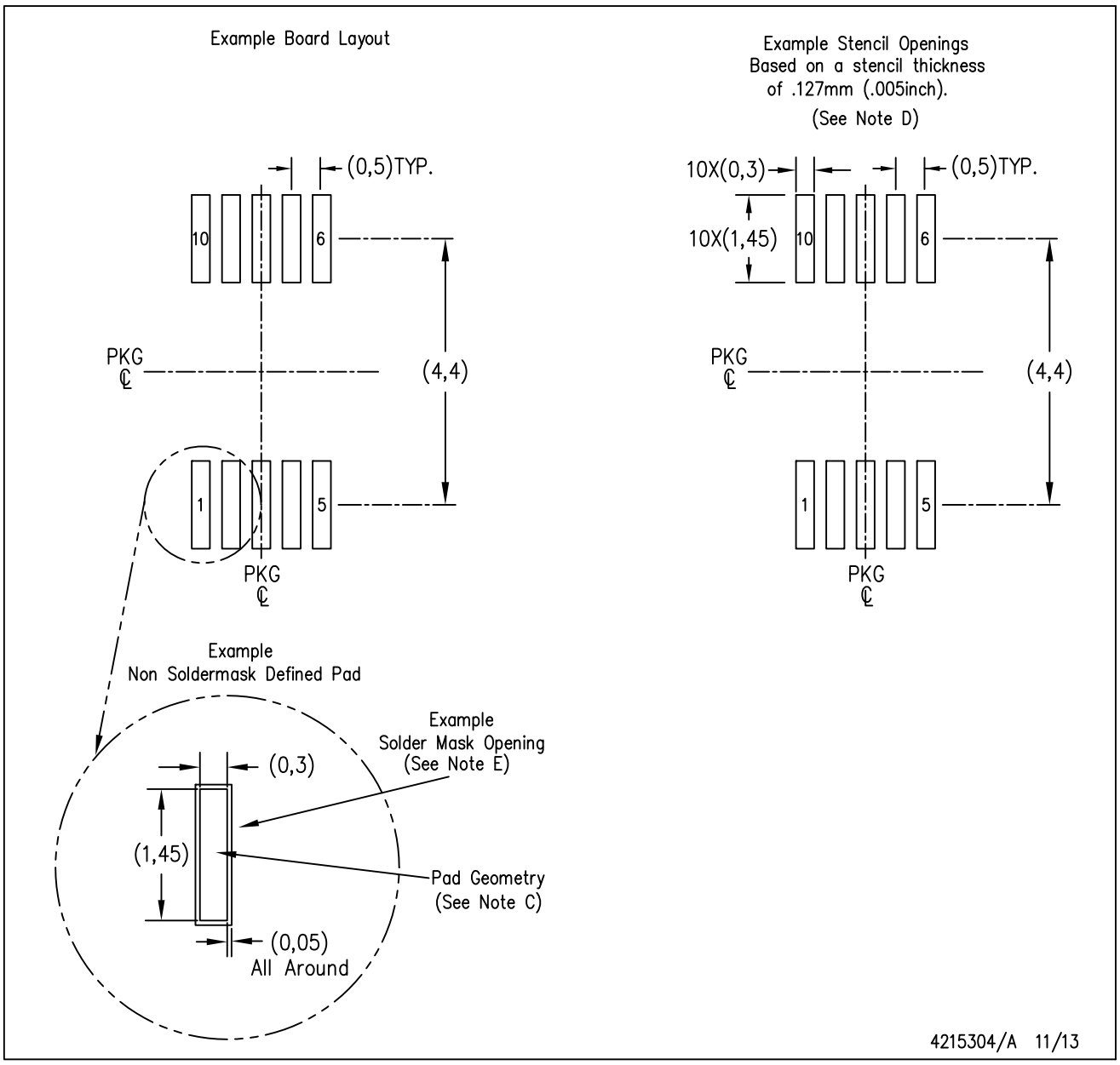
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

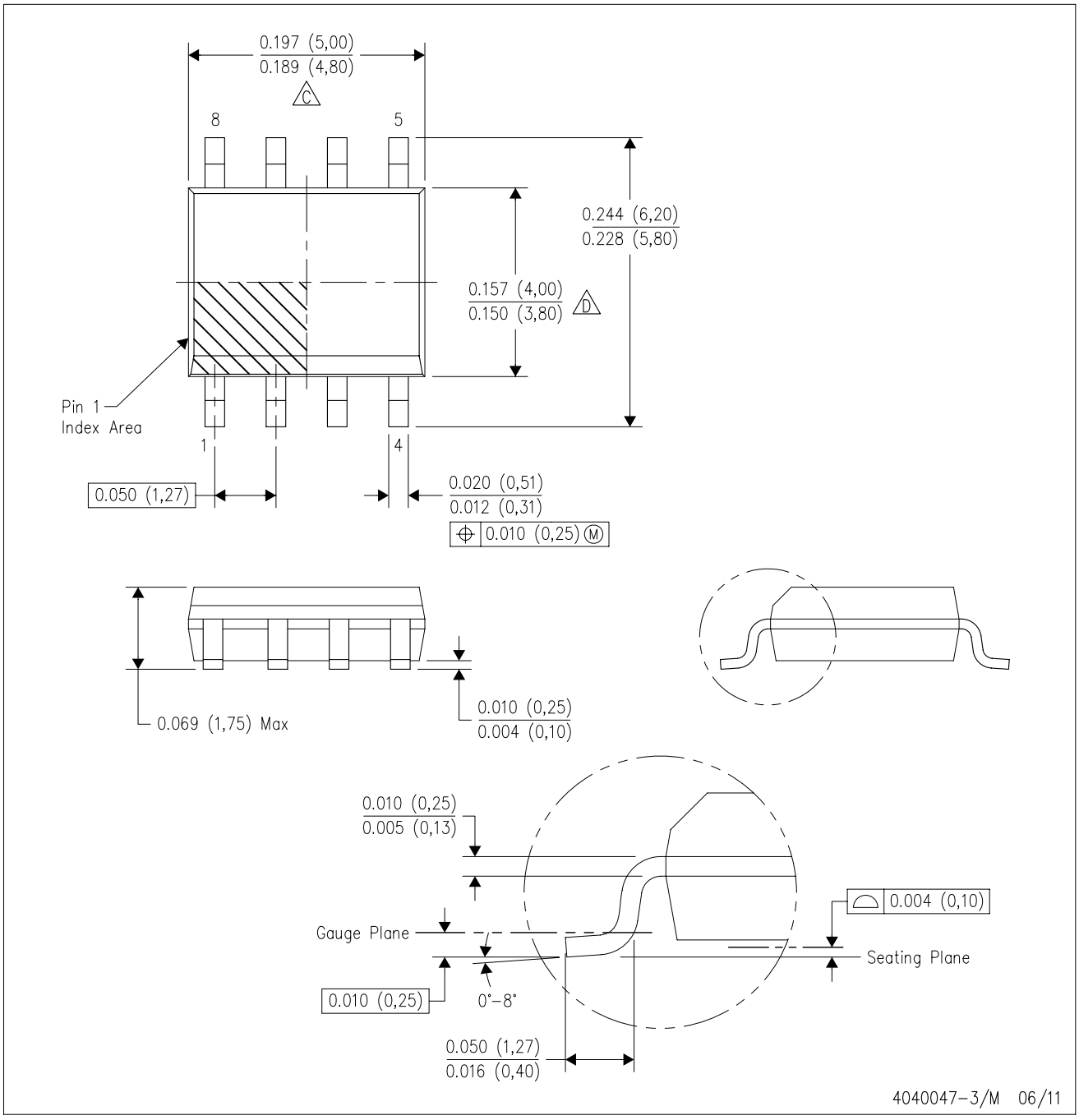
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



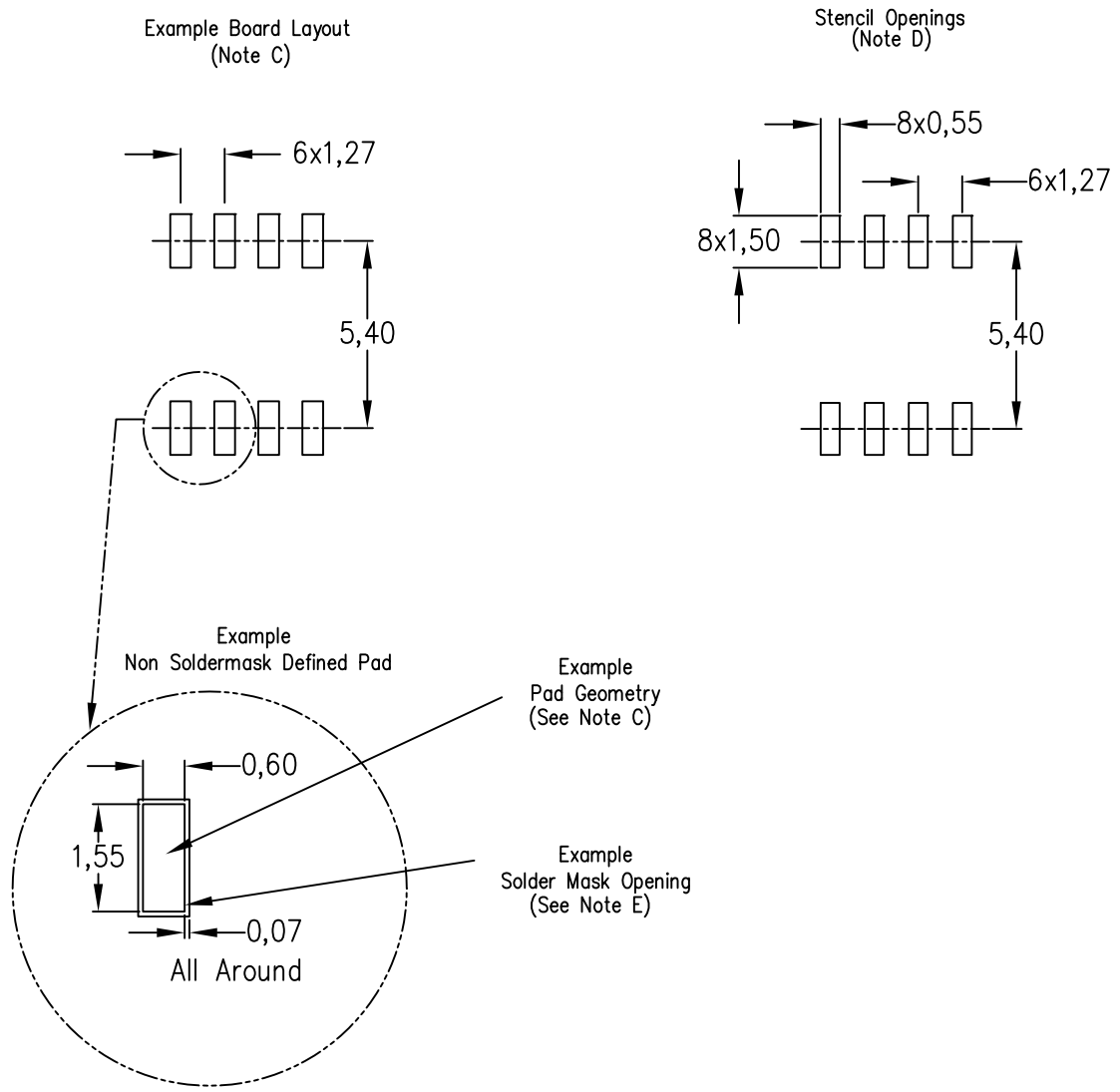
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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