ORCA ORSPI4

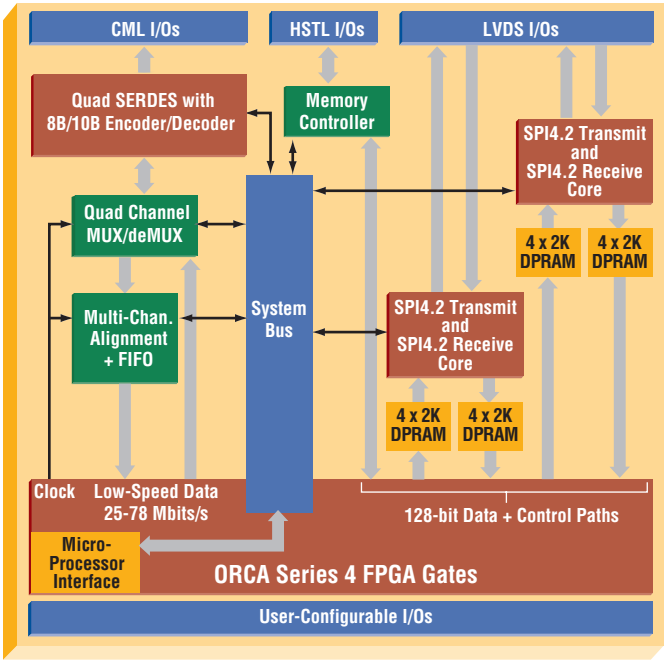
Embedded SPI4.2 Core, 3.7Gbps SERDES, High-Speed Memory Controller + FPGA

Introducing the ORCA® ORSPI4, the next-generation FPSC from Lattice Semiconductor. The ORSPI4 device offers a fast and flexible solution for high-speed data transmission. Built on the Series 4 reconfigurable embedded System-on-a-Chip (SoC) architecture, the ORSPI4 device contains two OIF-compliant System Packet Interface, Level 4, Phase 2 (SPI4.2) interface blocks, a high-speed memory controller, 4 channels of 600 Mbits/s to 3.7 Gbits/s SERDES with 8b/10b encoding/decoding, and over 16K programmable logic elements ... all on a single chip! The programmable logic elements can be used to implement functions (e.g. CSIX, PL3, UT3, etc.) to interface to other devices on a board.

Embedded SPI4.2 blocks provide dual 10 Gbits/s Physical-to-Link Layer interfaces in conformance to the OIF-SPI4-02.0 specification. Each SPI4.2 block provides a bi-directional interface with an aggregate bandwidth of 14.4 Gbits/s. This is achieved by using 16 LVDS pairs each for Rx and Tx operating at a data rate of 900 Mbits/s with a 450 MHz DDR clock. Both static and dynamic alignment are supported at the receive interface. Dynamic alignment is used to compensate for bit-to-bit skew at higher data rates, where it becomes difficult to meet tight setup/hold requirements. DIP-4 and DIP-2 parity generation and checking are supported. Embedded Dual-Port RAM in each SPI4.2 core provides data buffering of 8K bytes for both transmit and receive. Internal 1K deep main and shadow calendar supports scheduling of up to 256 ports. The Transmit and Receive Status FIFOs can also store flow control information for up to 256 ports, the maximum specified in the SPI4.2 standard. The embedded SPI4.2 blocks consume 3-10x lower power than equivalent soft SPI4.2 IP cores implemented solely in FPGA gates. An embedded SPI4.2 block is also far more predictable than a soft IP core implementation, thus reducing time-to-market.

The ORSPI4 includes an independent memory controller block to provide data buffering between the FPGA logic and external memory. This high-speed memory controller supports a throughput of greater than 20 Gbits/s. Data is transferred to and from memory through two sets of 36-bit unidirectional data lines operating at 200 MHz DDR. A set of 72 data signals, operating at a maximum speed of 156 MHz, is available to transfer data across the core-FPGA interface and allows the system to utilize the bandwidth of second-generation Quad Data Rate (QDR-II) SRAMs. Additionally, a soft memory controller can be implemented in FPGA gates to provide a second memory buffer interface.

ORCA ORSPI4 Block Diagram



A high-speed SERDES block supports four serial links, each operating at up to 3.7 Gbits/s (2.96 Gbits/s data rate with 8b/10b encoding and decoding). The SERDES block provides four full-duplex synchronous interfaces with built-in Rx Clock and Data Recovery (CDR) and transmitter pre-emphasis. The SERDES block is identical to that in Lattice's ORT82G5 device and supports embedded 8b/10b encoding/decoding and implements link state machines for both 10 Gbits/s Ethernet, and Fibre Channel. The state machines are IEEE P802.3ae/D4.01 XAUI compliant and also support FC (ANSI X3.230:1994) link synchronization.

Key Features and Benefits

Embedded SPI4.2 Core Features

- **OIF-SPI4-02.0 compliant interfaces**
- **Dynamic timing receive interface:**
  - Full bandwidth up to 450 MHz DDR (900 Mbits/s throughput)
  - Bit de-skewing up to 16 phases of the clock
  - Capable of aligning bit-to-bit skews as large as ±1 bit periods
- **Static timing receive interface:**
  - Speeds up to 350 MHz DDR (700 Mbits/s throughput, Quarter Rate mode supported)
  - Clock aligned or clock centered modes supported
- **DIP-4 and DIP-2 parity generation and checking**
- **Transmit interface:**
  - Speeds up to 450 MHz DDR (900 Mbits/s throughput)

ORSPI4 Attributes

Device	FPGA Usable Gates	PFUs	LUTs	EBR RAM Bits	Packaging / User I/Os	I/O Compatibility	SERDES Channels	Max SERDES Rate	SPI4.2 Cores
ORSPI4	471 - 899K	2,024	16,192	148K	1036-ball ftSBGA / 498 I/Os 1156-ball fpBGA / 356 I/Os	1.5/1.8/2.5/3.3V	4	3.7Gbits/s	2

Embedded SPI4.2 Core Features (cont.)

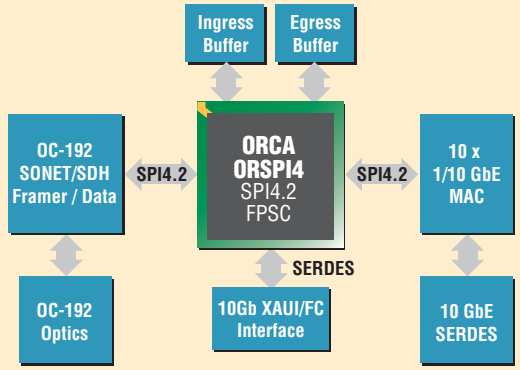
- Dedicated LVDS transmit interface for improved data eye integrity
- Automatic idle insertion

- **256 logical ports:**
  - Embedded Calendar-based sequence port polling mechanism and bandwidth allocation; shadow Calendar support for smooth transition to new Calendar
  - Up to 32 independent Tx & 32 independent Rx buffers per SPI4 interface internally; various aggregation modes to support 1 to 32 separate embedded buffers per Tx and Rx
  - Up to 4 independent Tx and 4 independent Rx clock domain transfers to the FPGA logic
- **FIFO status support modes:**
  - Quarter rate LVTTL or quarter rate LVDS
  - Automatic status handling or optionally under user control; credit calculations based on burst size and status are also handled automatically
- **Configuration options as suggested in the OIF-SPI4-02.0 standard to configure parameters such as maximum burst size, calendar length, main and shadow calendars (1K deep each), length of training sequence etc.**
- **Simple FIFO interface to the FPGA logic provides ease of design and efficient clock domain transfers**
- **Loopback modes provide system- & chip-level debug**
- **Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded core blocks. Includes built-in system registers that act as the control and status center for the device**

ORSPI4 Application

10 x 1 GbE / 10 GbE over SONET/SDH

The ORCA ORSPI4 is an excellent solution for implementing a 10x1 GbE / 10 GbE over SONET/SDH line card.



Note: One SPI4.2 block available if SERDES is used.

- **Low-power operation. Full-rate SPI4.2 interfaces running at 450MHz DDR (900Mbits/sec) consumes less than 2W of power. More efficient than FPGAs with soft-IP SPI4.2 solutions which consumes in excess of 10W**
- **Interoperability demonstrated with ORSPI4 partners (NPU and framer vendors)**

Additional Embedded Core Features

- **Quad 600 Mbits/s to 3.7 Gbits/s SERDES:**
  - IEEE 802.3ae XAUI (Link State Machine & Alignment FIFOs embedded)
  - ANSI X3.230:1994 1G/2G FC-compliant (Link State Machine & Alignment FIFOs embedded)
  - Proven performance (same SERDES used in ORT82G5 FPSC)
- **High Performance memory controller for interface to external buffer memory**
  - Required for Layer 2 data buffering
  - QDR II memory interface
    - 36-bit Input and 36-bit Output bus, 18-bit address
    - 200 MHz clock rates
    - 20+ Gbits/s bandwidth
    - Supports 2- or 4-word burst mode
    - Simple FIFO interface to FPGA
    - Integrated PLL for optimized performance
    - Proven performance with multiple memory suppliers

High-Speed ORCA Series 4 FPGA Gates

- **ORCA Series 4 FPGA gates are available for customer use beyond the embedded core**
- **Internal performance of > 250 MHz**
- **Over 16K programmable logic elements**
- **1.5V operation (30% less power than 1.8 V operation)**
- **Comprehensive I/O selections including LVTTL, LVCMOS, GTL, GTL+, PECL, SSTL3/2, HSTL, ZBT, DDR, LVDS, bused-LVDS, and LVPECL**
- **1036-pin fpSBGA package provides enough FPGA user I/Os (498) for 4 full-duplex XGMII interfaces, 4 full-duplex PL-3 interfaces, etc; a 40% smaller 1156-pin fpBGA package is available with 356 FPGA user I/Os**

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