2.5V Drive Pch+SBD MOS FET QS5U21

●Structure

Silicon P-channel MOS FET Schottky Barrier DIODE

● Features

- 1) The QS5U21 combines Pch MOS FET with a Schottky barrier diode in a TSMT5 package.
- 2) Low on-state resistance with fast switching.
- 3) Low voltage drive(2.5V)
- 4) Built-in schottky barrier diode has low forward voltage.

TSMT5 TSMT5 1,0MAX 0,095,095,095 0,7 0,01 0,00

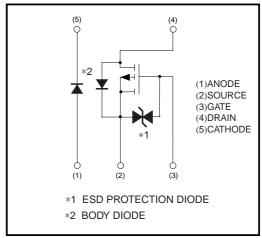
Applications

Load switch, DC/DC conversion

Packaging specifications

Туре	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS5U21		0

●Equivalent circuit



● Absolute maximum ratings (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit			
Drain-source voltage		Voss	-20	V			
Gate-source voltage		V _{GSS}	±12	V			
Drain current	Continuous	ID	±1.5	Α			
	Pulsed	I _{DP} *1	±6.0	Α			
Source current (Body diode)	Continuous	Is	-0.75	Α			
	Pulsed	Pulsed I _{SP} *1 -		Α			
Channel temperature		Tch	150	°C			
Power dissipation		P _D *3	0.9	W / ELEMENT			
<di></di>							
Repetitive peak reverse voltage		V_{RM}	25	V			
Reverse voltage		V_R	20	V			
Forward current		l _F	1.0	А			
Forward current surge peak		I _{FSM} *2	3.0	A			
Junction temperature		Tj	150	°C			
Power dissipation		P _D *3	0.7	W / ELEMENT			
<mosfet and="" di=""></mosfet>							
Total power dissipation		P _D *3	1.25	W / TOTAL			
Range of Storage temperature		Tstg	−55 to +150 °C				

^{*1} Pw≤10μs, Duty cycle≤1% *2 60Hz•1cyc. *3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

< MOSFET >

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Gate-source leakage	Igss	-	_	±10	μΑ	Vgs=±12V/ Vps=0V	
Drain-source breakdown voltage	V _{(BR)DSS}	-20	_	-	V	In=-1mA/ Vgs=0V	
Zero gate voltage drain current	IDSS	-	-	-1	μΑ	Vps=-20V/ Vgs=0V	
Gate threshold voltage	VGS(th)	-0.7	_	-2.0	V	VDS=-10V/ ID=-1mA	
		-	160	200	mΩ	In=-1.5A, Vgs=-4.5V	
Static drain–source on–state resistance	RDS(on)*	_	180	240	mΩ	In=-1.5A, Vgs=-4V	
		_	260	340	mΩ	In=-0.75A, Vgs=-2.5V	
Forward transfer admittance	Y _{fs} *	1.0	_	-	S	V _{DS} =-10V, I _D =-0.75A	
Input capacitance	Ciss	-	325	-	pF	V _{DS} =-10V	
Output capacitance	Coss	-	60	_	pF	Vgs=0V	
Reverse transfer capacitance	Crss	_	40	_	pF	f=1MHz	
Turn-on delay time	td(on) *	_	10	_	ns	$\begin{array}{l} \text{ID=-0.75A} \\ \text{VDD} \leftrightharpoons -15 \\ \text{VGS=-4.5V} \\ \text{RL=}20\Omega \\ \text{RG}=10\Omega \end{array}$	
Rise Time	tr *	-	10	-	ns		
Turn-off delay time	td(off) *	-	35	-	ns		
Fall time	t _f *	-	10	-	ns		
Total gate charge	Qg	-	4.2	-	nC	V _{DD} = −15V	
Gate-source charge	Qgs	_	1.0	-	nC	Vgs=-4.5V	
Gate-drain charge	Qgd	_	1.1	_	nC	ID=-1.5A	
*Pulsed				•			
<body (source-drain)="" diode=""></body>							
Forward voltage	VsD	-	-	-1.2	V	Is=-0.75A/ Vgs=0V	
< Di >							
Foward voltage drop	VF	_	_	0.45	V	IF=1.0A	
Reverse current	lR	-	_	200	μА	V _R =20V	



•Electrical characteristic curves

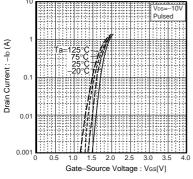


Fig.1 Typical Transfer Characteristics

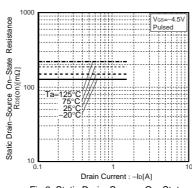


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

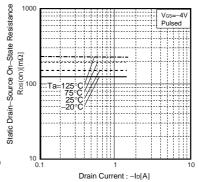


Fig.3 Static Drain-Source On-State Resistance vs.Drain Current

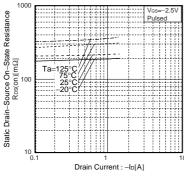


Fig.4 Static Drain-Source On-State Resistance vs.Drain-Current

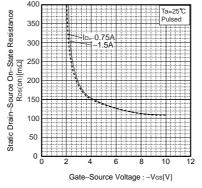


Fig.5 Static Drain-Source On-State Resistance vs.Gate-Source Voltage

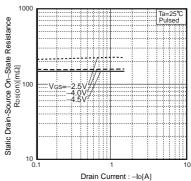


Fig.6 Static Drain-Source On-State Resistance vs.Drain Current

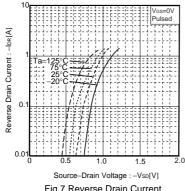


Fig.7 Reverse Drain Current vs. Source-Drain Current

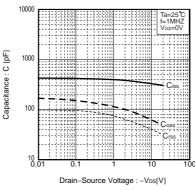


Fig.8 Typical Capactitance vs.Drain-Source Voltage

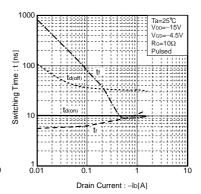


Fig.9 Switching Characteristics

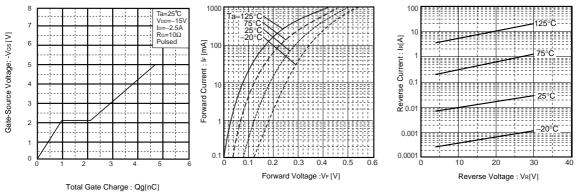


Fig.10 Dynamic Input Characteristics

Fig.11 Forward Temperature Characteristics Fig.12 Reverse Temperature Characteristics

●Measurement circuits

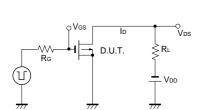


Fig.13 Switching Time Measurement Circuit

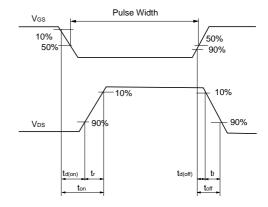


Fig.14 Switching Waveforms

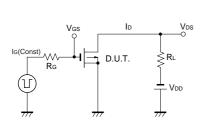


Fig.15 Gate Charge Measurement Circuit

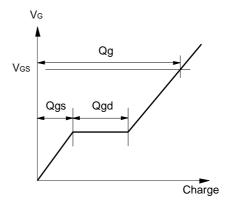


Fig.16 Gate Charge Waveforms

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