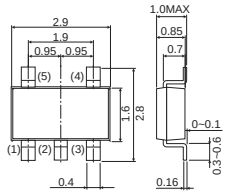
2.5V Drive Pch+SBD MOS FET

QS5U23

●Structure
Silicon P-channel MOS FET
Schottky Barrier DIODE

●External dimensions (Unit : mm)

TSMT5



Each lead has same dimensions

Abbreviated symbol : U23

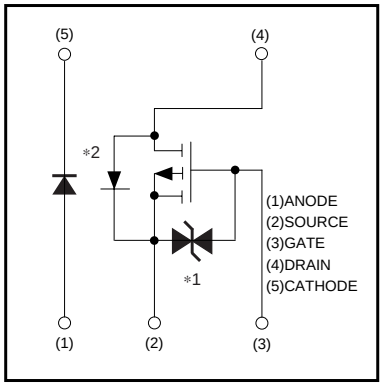
●Features
1) The QS5U23 combines Pch MOS FET with a Schottky barrier diode in a TSMT5 package.
2) Low on-state resistance with fast switching.
3) Low voltage drive(2.5V)
4) Built-in schottky barrier diode has low forward voltage.

●Applications
Load switch , DC/DC conversion

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS5U23		◯

●Equivalent circuit



*1 ESD PROTECTION DIODE
*2 BODY DIODE

●Absolute maximum ratings (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−20	V
Gate-source voltage		V_{GSS}	±12	V
Drain current	Continuous	I_D	±1.5	A
	Pulsed	I_{DP} *1	±6.0	A
Source current (Body diode)	Continuous	I_S	−0.75	A
	Pulsed	I_{SP} *1	−3.0	A
Channel temperature		Tch	150	°C
Power dissipation		P_D *3	0.9	W / ELEMENT

<Di>

Repetitive peak reverse voltage	V_{RM}	30	V
Reverse voltage	V_R	20	V
Forward current	I_F	0.5	A
Forward current surge peak	I_{FSM} *2	2.0	A
Junction temperature	Tj	150	°C
Power dissipation	P_D *3	0.7	W / ELEMENT

<MOSFET AND Di>

Total power dissipation	P_D *3	1.25	W / TOTAL
Range of Storage temperature	Tstg	−55 to +150	°C

*1 Pw≤10µs, Duty cycle≤1% *2 60Hz･1cyc. *3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

< MOSFET >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	−	−	±10	µA	V_{GS}=±12V/ V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−20	−	−	V	I_D=−1mA/ V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	−	−	−1	µA	V_{DS}=−20V/ V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	−0.7	−	−2.0	V	V_{DS}=−10V/ I_D=−1mA
Static drain−source on−state resistance	$R_{DS(on)}$ *	−	160	200	mΩ	I_D=−1.5A, V_{GS}=−4.5V
		−	180	240	mΩ	I_D=−1.5A, V_{GS}=−4V
		−	260	340	mΩ	I_D=−0.75A, V_{GS}=−2.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	1.0	−	−	S	V_{DS}=−10V, I_D=−0.75A
Input capacitance	C_{iss}	−	325	−	pF	V_{DS}=−10V
Output capacitance	C_{oss}	−	60	−	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	−	40	−	pF	f=1MHz
Turn−on delay time	$t_{d(on)}$ *	−	10	−	ns	I_D=−0.75A
Rise Time	t_r *	−	10	−	ns	V_{DD} ≒−15
Turn off delay time	$t_{d(off)}$ *	−	35	−	ns	V_{GS}=−4.5V R_L=20Ω
Fall time	t_f *	−	10	−	ns	R_G=10Ω
Total gate charge	Qg	−	4.2	−	nC	V_{DD} ≒−15V
Gate−source charge	Qgs	−	1.0	−	nC	V_{GS}=−4.5V
Gate−drain charge	Qgd	−	1.1	−	nC	I_D=−1.5A

*Pulsed

<Body diode (source−drain)>

Forward voltage	V_{SD}	−	−	−1.2	V	I_S=−0.75A/ V_{GS}=0V

< Di >

Foward voltage drop	V_F	−	−	0.36	V	I_F=0.1A
		−	−	0.47	V	I_F=0.5A
Reverse current	I_R	−	−	100	µA	V_R=20V

●Electrical characteristic curves

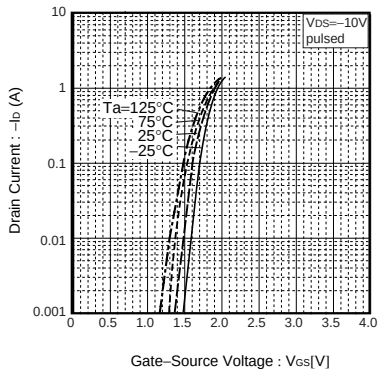


Fig.1 Typical Transfer Characteristics

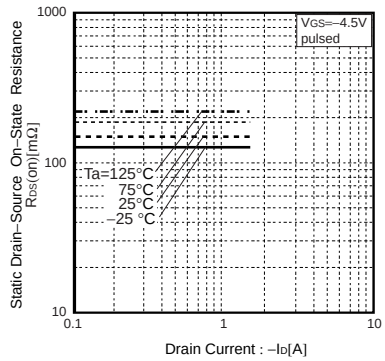


Fig.2 Static Drain−Source On−State Resistance vs. Drain Current

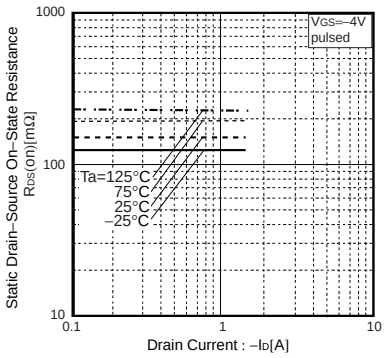


Fig.3 Static Drain−Source On−State Resistance vs. Drain Current

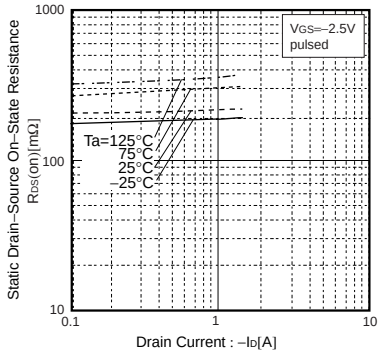


Fig.4 Static Drain−Source On−State Resistance vs. Drain−Current

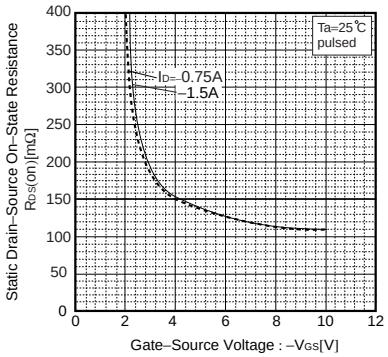


Fig.5 Static Drain−Source On−State Resistance vs.Gate−Source Voltage

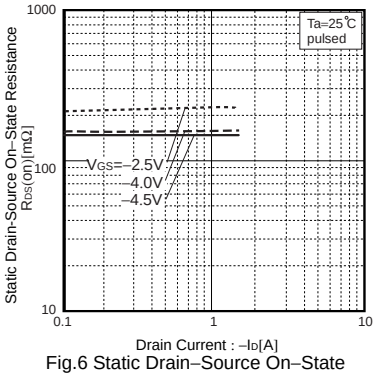


Fig.6 Static Drain−Source On−State Resistance vs. Drain Current

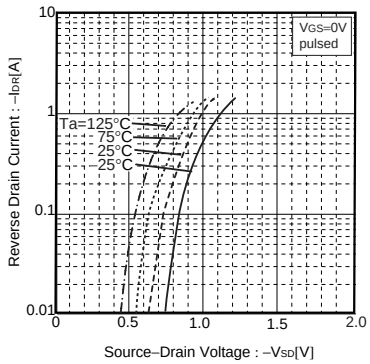


Fig.7 Reverse Drain Current VS. Source-Drain Current

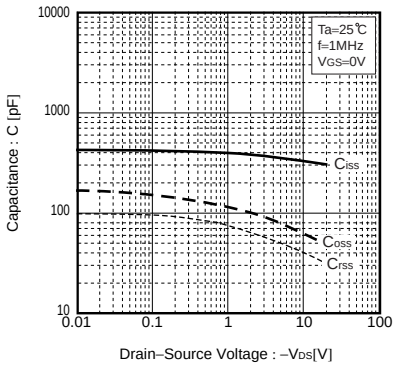


Fig.8 Typical Capactitance vs. Drain−Source Voltage

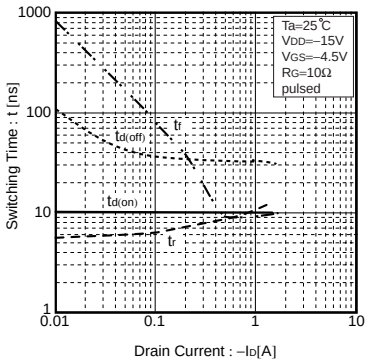


Fig.9 Switching Characteristics

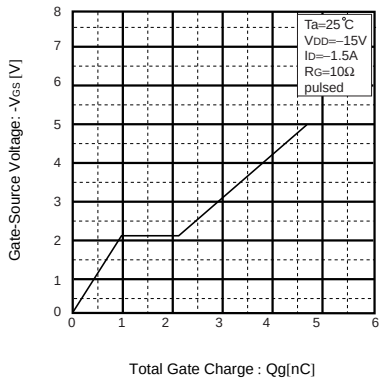


Fig.10 Dynamic Input Characteristics

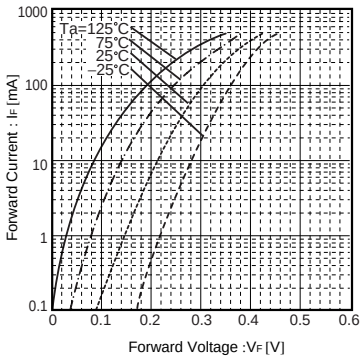


Fig.11 Forward Temperature Characteristics

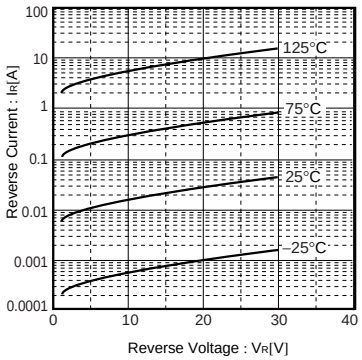


Fig.12 Reverse Temperature Characteristics

●Measurement circuits

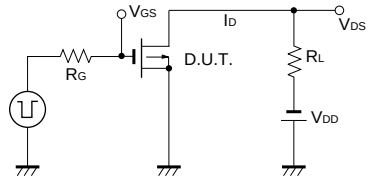


Fig.13 Switching Time Measurement Circuit

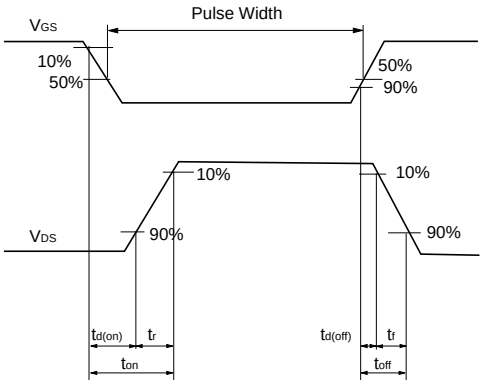


Fig.14 Switching Waveforms

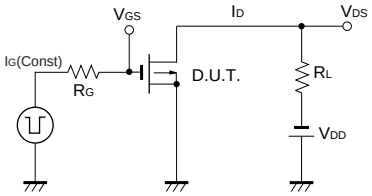


Fig.15 Gate Charge Measurement Circuit

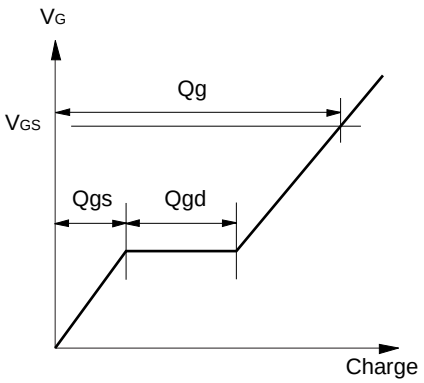


Fig.16 Gate Charge Waveforms

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