

1.5V Drive Pch MOSFET

RW1C025ZP

● Structure

Silicon P-channel MOSFET

● Features

- 1) Low On-resistance.
- 2) Small high power package.
- 3) Low voltage drive.(1.5V)

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	T2CR
	Basic ordering unit (pieces)	8000
RW1C025ZP		○

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	Continuous	I_D	±2.5	A
	Pulsed	I_{DP} *1	±10	A
Source current (Body Diode)	Continuous	I_S	-0.5	A
	Pulsed	I_{SP} *1	-10	A
Power dissipation		P_D *2	0.7	W
Channel temperature		T_{ch}	150	°C
Range of storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$

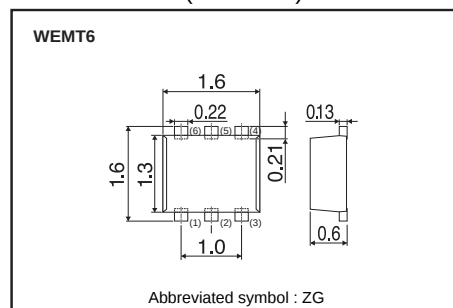
*2 Mounted on a ceramic board.

● Thermal resistance

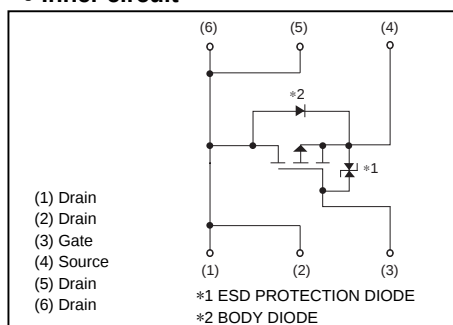
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	179	°C / W

*Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 10V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-20	-	-	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	-	-	-1	μA	$V_{DS} = -20V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	48	65	m Ω	$I_D = -2.5A, V_{GS} = -4.5V$
		-	65	90		$I_D = -1.2A, V_{GS} = -2.5V$
		-	90	135		$I_D = -1.2A, V_{GS} = -1.8V$
		-	120	240		$I_D = -0.5A, V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	2.2	-	-	S	$I_D = -2.5A, V_{DS} = -10V$
Input capacitance	C_{iss}	-	1300	-	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	-	90	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	70	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	9	-	ns	$I_D = -1.2A, V_{DD} = -10V$
Rise time	t_r^*	-	18	-	ns	$V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	110	-	ns	$R_L = 8.3\Omega$
Fall time	t_f^*	-	50	-	ns	$R_G = 10\Omega$
Total gate charge	Q_g^*	-	21	-	nC	$I_D = -2.5A$
Gate-source charge	Q_{gs}^*	-	4	-	nC	$V_{DD} = -10V$
Gate-drain charge	Q_{gd}^*	-	3	-	nC	$V_{GS} = -4.5V$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	-1.2	V	$I_S = -2.5A, V_{GS} = 0V$

*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics (I)

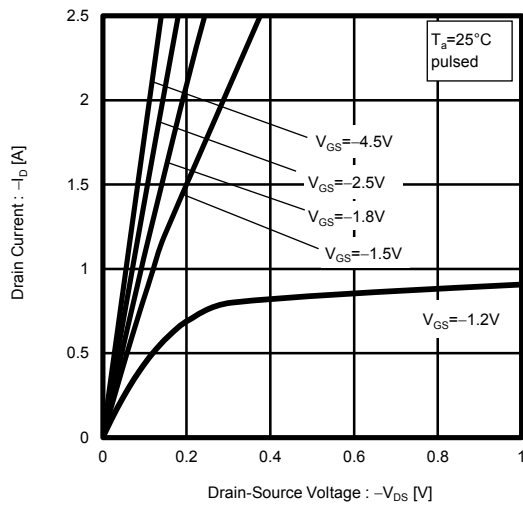


Fig.2 Typical Output Characteristics (II)

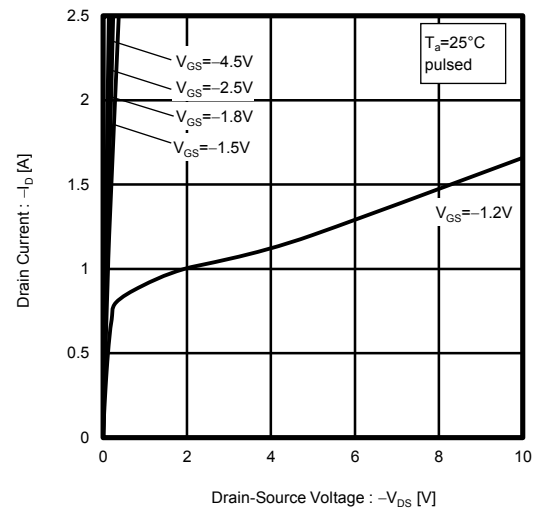


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

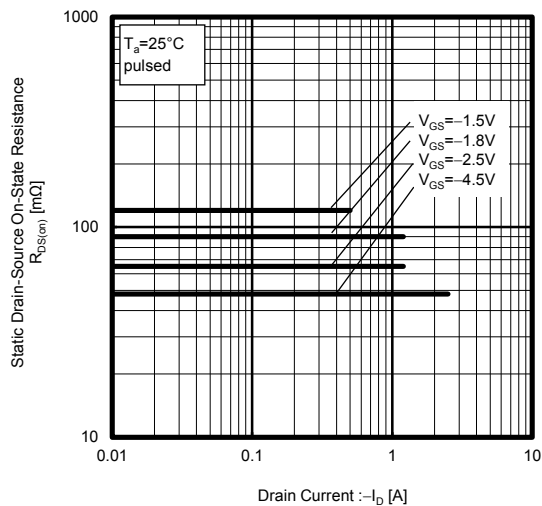


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

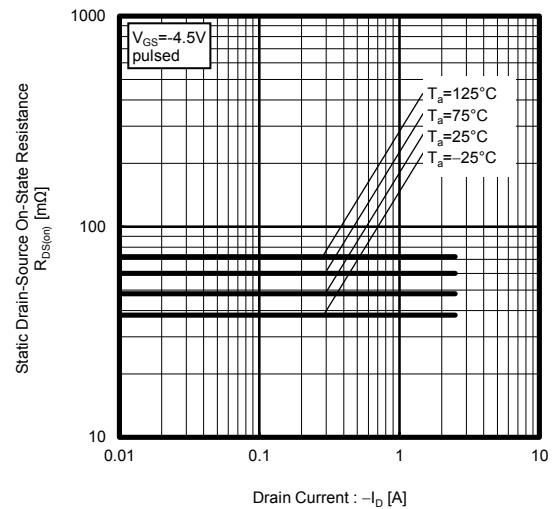


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

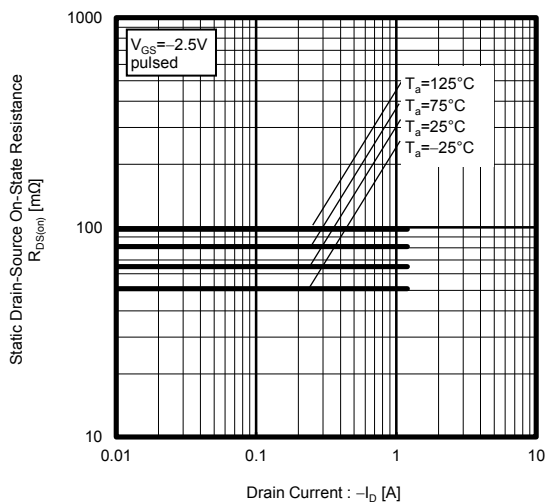


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

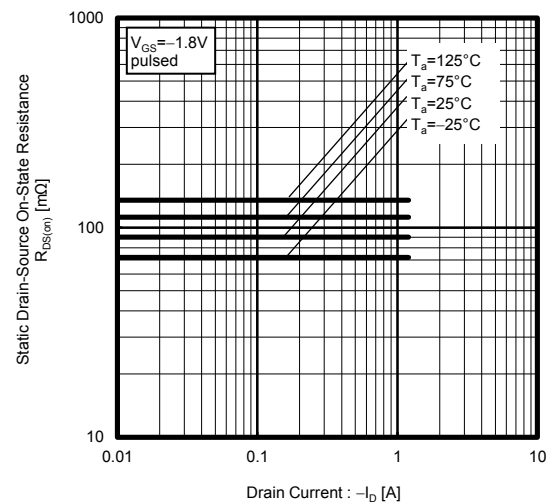


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current

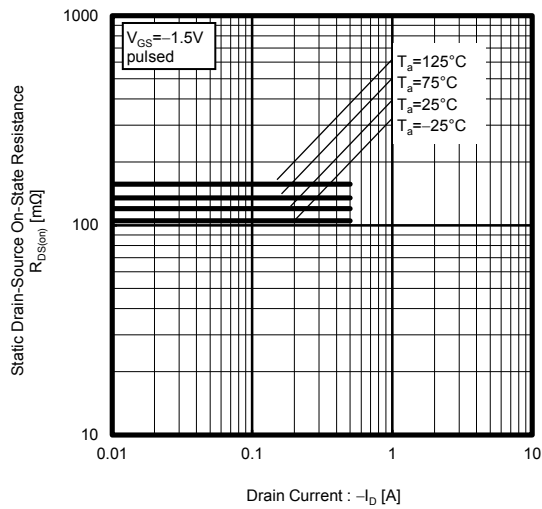


Fig.8 Forward Transfer Admittance vs. Drain Current

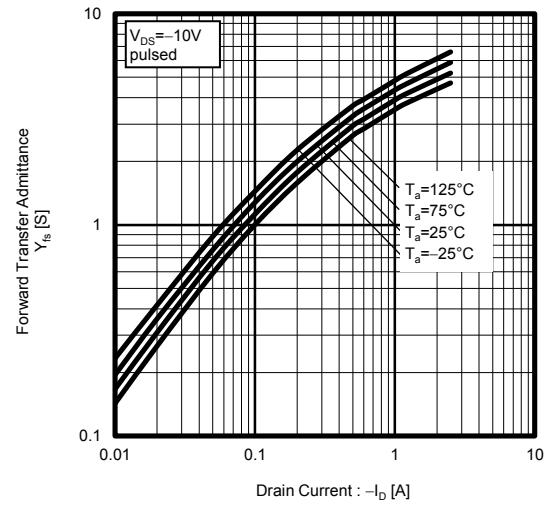


Fig.9 Typical Transfer Characteristics

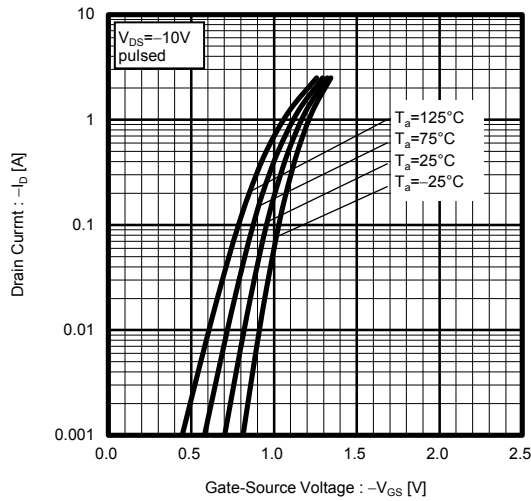


Fig.10 Source Current vs. Source-Drain Voltage

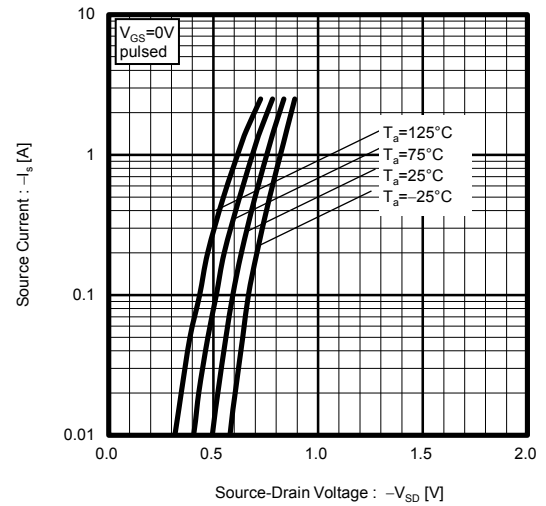


Fig.11 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

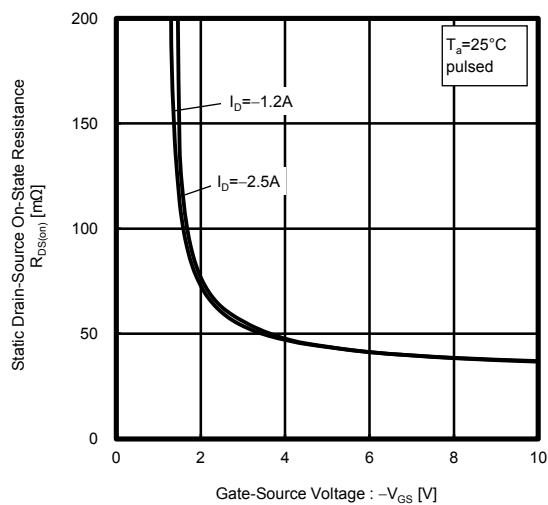


Fig.12 Switching Characteristics

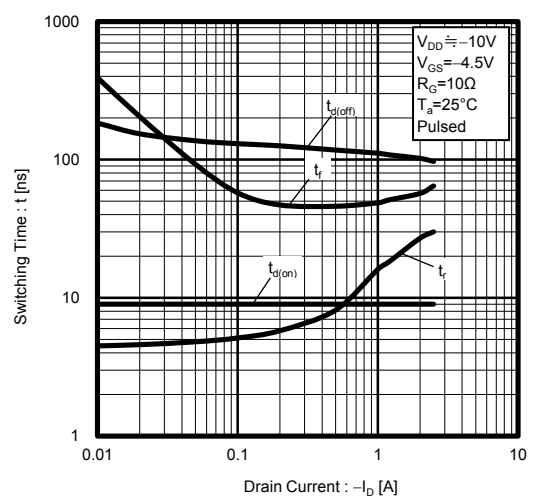


Fig.13 Dynamic Input Characteristics

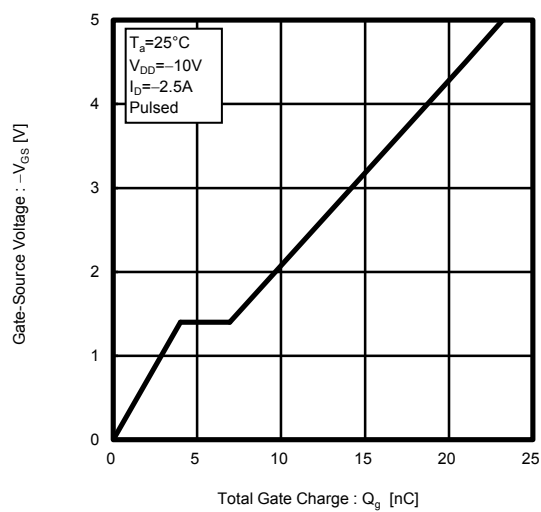
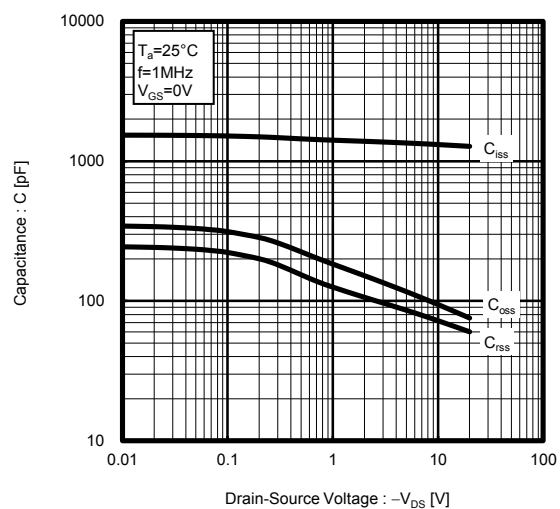


Fig.14 Typical Capacitance vs. Drain-Source Voltage



● Measurement circuits

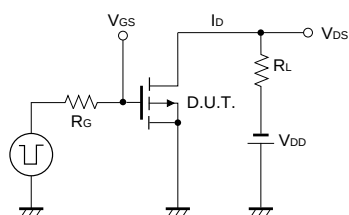


Fig.1-1 Switching Time Measurement Circuit

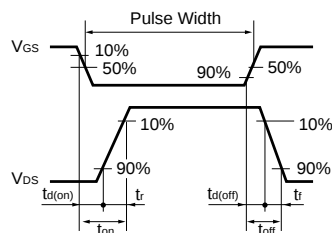


Fig.1-2 Switching Waveforms

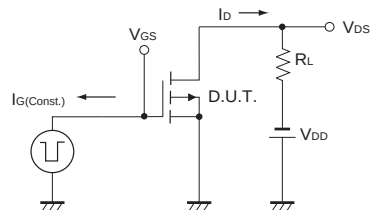


Fig.2-1 Gate Charge Measurement Circuit

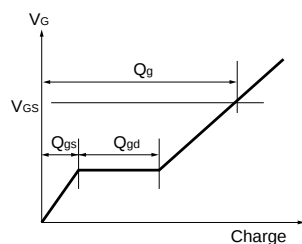


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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