PCM4204EVM User's Guide

This document provides the information needed to set up and operate the PCM4204EVM evaluation module (EVM). For a more detailed description of the PCM4204, please refer to the product datasheet available from the Texas Instruments web site at http://www.ti.com. Additional support documents are listed in the sections of this guide entitled ***Related Documentation from Texas Instruments*** and ***Additional Documentation***. Throughout this document, the acronym **EVM** and the phrase *evaluation module* are synonymous with the PCM4204EVM. This user's guide includes setup and configuration instructions, information regarding absolute operating conditions for power supplies and input/output connections, an electrical schematic, PCB layout drawings, and a bill of materials (BOM) for the EVM.

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1 Introduction

The PCM4204 is a high-performance, four-channel audio analog-to-digital (A/D) converter designed for use in professional and broadcast audio applications. The PCM4204 features simultaneous 24-bit linear PCM or 1-bit Direct Stream Digital (DSD) data output for all four channels. Sampling rates up to 216kHz are supported for PCM output formats, while 64x or 128x oversampled 1-bit data is supported for DSD output and input modes. Native support for both PCM and DSD data formats makes the PCM4204 ideal for use in a variety of audio recording and processing applications.

The PCM4204 features 1-bit delta-sigma ($\Delta\Sigma$) modulators employing a novel density modulated dithering scheme, yielding improved dynamic performance. Differential voltage inputs are utilized for the modulators, providing excellent common-mode rejection. On-chip voltage references are provided for the modulators, in addition to generating DC common-mode bias voltage outputs for use with external input circuitry. Linear phase digital decimation filtering is provided for the 24-bit PCM output, with a minimum stop band attenuation of -100dB for all sampling modes.

The PCM output mode features clipping flag outputs for each of the four channels, as well as a digital high-pass filter for DC removal. The PCM4204 is configured using dedicated input pins for sampling mode and audio data format selection, high-pass filter enable/disable, and reset/power-down operation.

A +5V power supply is required for the analog section of the device, while a +3.3V power supply is required for the digital circuitry. Figure 1 shows the functional block diagram of the PCM4204.

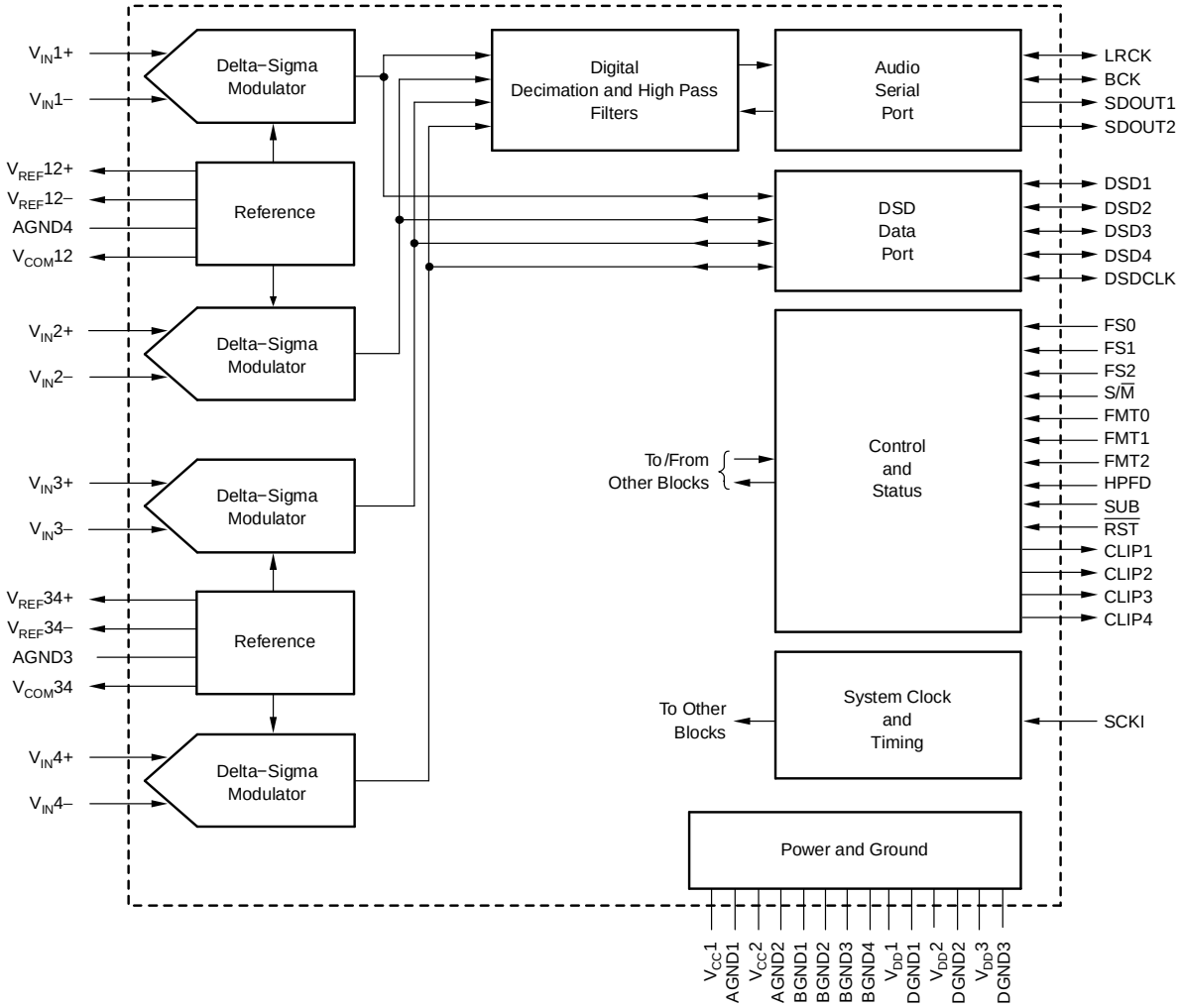

Figure 1. PCM4204 Functional Block Diagram

1.1 PCM4204EVM Features

The PCM4204EVM provides a convenient platform for evaluating the performance and functionality of the PCM4204 product. The primary EVM features include:

- Simple configuration using onboard DIP switches
- Four differential voltage inputs supporting either 3-pin XLR or Balanced TRS connections
- Low-noise input buffer circuits utilizing the OPA1632 fully differential audio amplifier
- Four 75Ω AES3-encoded outputs, supporting operation up to 216kHz sampling rates
- Buffered Audio Serial Port supports a four-channel, 24-bit linear PCM data interface for external hardware and signal processors. Sampling rates up to 216kHz are supported.
- DSD Data Port supports a four-channel, 1-bit output or input data interface at 64x or 128x data rates
- A second PCM4204 provides a test mode for 1-bit DSD to 24-bit linear PCM format conversions
- Two onboard system clock oscillators, operating at 22.5792MHz and 24.576MHz respectively, supporting standard PCM sampling rates, including 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, and 192kHz.
- External system clock inputs supporting alternative sampling rates up to 216kHz.

The PCM4204EVM requires +15V, -15V, and +5V analog power supplies. Additionally, a +5V digital power supply is required, with a +3.3V digital supply being derived onboard using a linear voltage regulator IC.

1.2 PCM4204EVM General Description and Functional Block Diagram

The PCM4204EVM provides a complete platform for evaluating the performance and features of the PCM4204 four-channel audio A/D converter. Figure 2 illustrates the functional block diagram for the evaluation module.

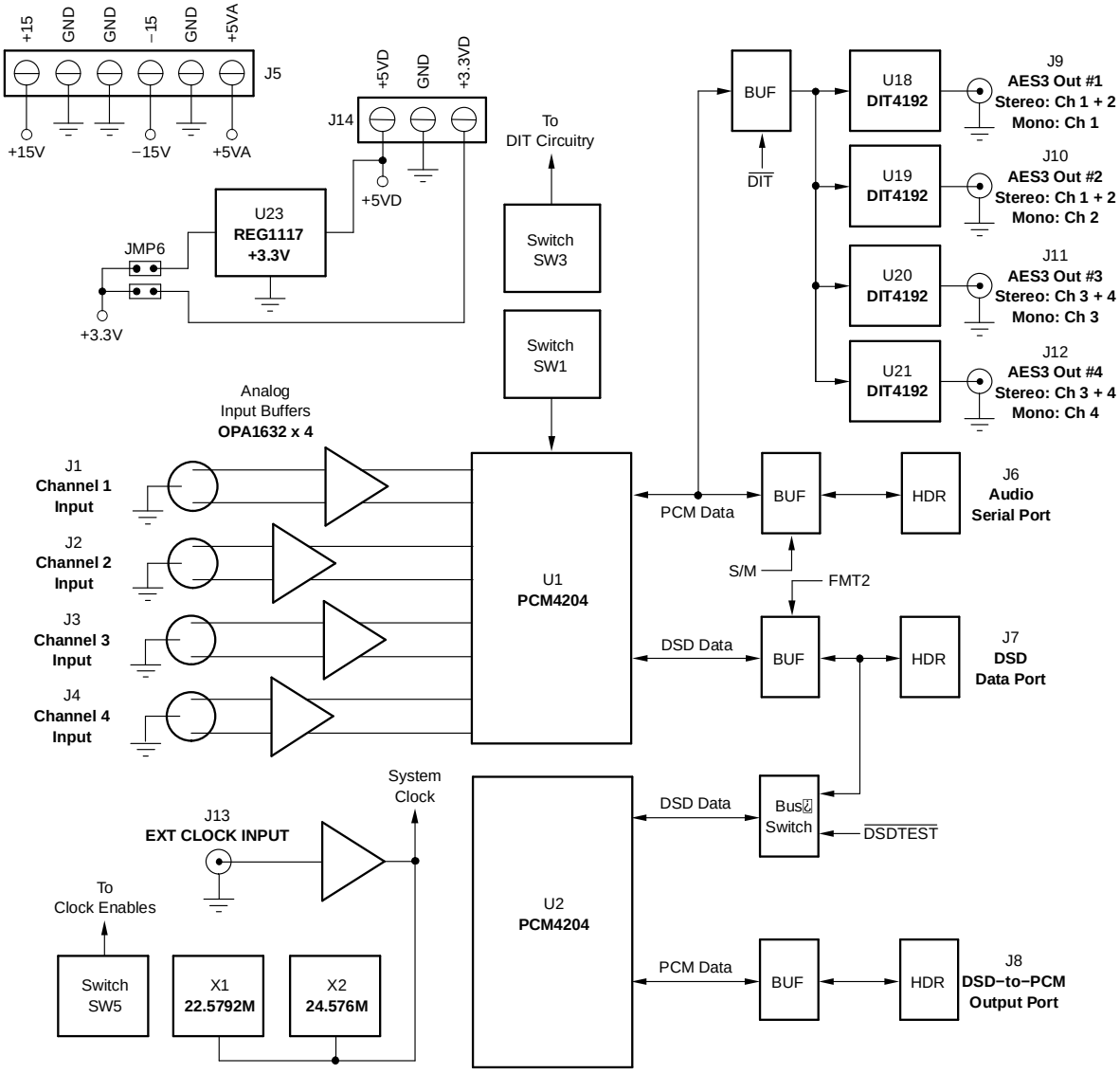

Figure 2. PCM4204EVM Functional Block Diagram

Four differential analog inputs are supported at connectors J1 through J4, corresponding to analog input channels 1 through 4, respectively. These connectors support either 3-pin male XLR or balanced TRS input plugs. Each of the analog inputs is buffered and filtered using a low noise input circuit, utilizing a Texas Instruments OPA1632 fully differential amplifier. The output of each buffer circuit is connected to a corresponding differential input of the PCM4204 (U1). The PCM4204 is then used to convert the analog signal to either a 24-bit linear PCM or 1-bit DSD representation in the digital domain.

The 24-bit PCM data output is made available at header J6, or at the AES3-encoded data outputs provided at jacks J9 through J12. The buffered header is convenient for interfacing to external development hardware or digital signal processors, while the AES3-encoded outputs may be connected to audio test systems or commercial audio equipment.

The 1-bit DSD data is available at header J7. This header is bi-directional, and may be used for either DSD output or input mode operation. A second PCM4204 (U2) is included for supporting a DSD-to-PCM format conversion test or demo mode. The resulting PCM-formatted output data is made available at header J8.

Power is connected to the board at either terminal block J5 for the analog supplies, or at terminal block J14 for the digital supplies.

Manual reset circuits are provided for both the PCM4204 (U1 and U2) and the AES3 transmitters (U18 through U21). The ADC RESET switch (SW2) is utilized for resetting the A/D converters (U1 and U2), while the DIT RESET switch (SW4) is utilized for resetting the AES3 transmitters (U18 through U21).

The system or master clock for the evaluation module may be generated onboard or by an external clock source. Oscillators X1 and X2 operate at fixed clock frequencies of 22.5792MHz and 24.576MHz, respectively. The oscillators provide low jitter clock sources for measuring the performance of the PCM4204 in Master mode operation. Alternatively, an external clock source may be connected at J13 for Master mode operation, supporting alternate system clock and sampling frequencies. For Slave mode operation, the system clock is provided from an external source through header J6 and buffer U12. Switch SW5 provides clock configuration control for the oscillators and the external clock input at connector J13.

1.3 Related Documentation from Texas Instruments

The following documents provide information regarding Texas Instrument integrated circuits used in the assembly of the PCM4204EVM. The latest revisions of these documents are available from the TI web site at http://www.ti.com .

Data Sheet	Literature Number
PCM4204 Datasheet	SBAS327
DIT4192 Datasheet	SBOS229
OPA227 Datasheet	SBOS110
OPA1632 Datasheet	SBOS286
REG1117 Datasheet	SBVS001
SN74AHC08 Datasheet	SCLS236
SN74AHC14 Datasheet	SCLS238
SN74ALVC245 Datasheet	SCES271
SN74CBTLV3245A Datasheet	SCDS034
SN74LVC1G125 Datasheet	SCES223

1.4 Additional Documentation

The following documents or references provide information regarding selected non-TI components used in the assembly of the PCM4204EVM. These documents are available from the corresponding manufacturer.

Document/Reference	Manufacturer
SM7745H Series CMOS Oscillators	Pletronics (http://www.pletronics.com)

2 Getting Started

This section provides information regarding handling and unpacking the PCM4204EVM, as well as absolute operating conditions for the unit.

2.1 Electrostatic Discharge Warning

CAUTION
Failure to observe proper ESD handling precautions may result in damage to EVM components.

Many of the components on the PCM4204EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling procedure when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation. Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 EVM Package Contents

Upon opening the PCM4204EVM package, please check to make sure that the following items are included:

- One PCM4204EVM
- One printed copy of the PCM4204 product datasheet
- One printed copy of this PCM4204EVM User's Guide

If any of these items are missing, please contact the Texas Instruments Product Information Center nearest you to inquire about replacements.

2.3 Absolute Operating Conditions

CAUTION
Exceeding the absolute operating conditions may result in damage to the evaluation module and/or the equipment connected to it.

The user should be aware of the absolute operating conditions for the PCM4204EVM. Table 1 summarizes the critical data points.

Table 1. Absolute Operating Conditions

	Min	Max	Units
Power Supplies			
+15V	+5.0	+16.0	V
-15V	-5.0	-16.0	V
+5VA	+4.5	+5.5	V
+5VD	+4.5	+5.5	V
EXT +3.3V	+3.0	+3.6	V
Audio Serial Port (J6), DSD Data Port (J7)			
V_{IH}, Input High Voltage (V_{DD} = +3.0V to +3.6V)	0.7 x V_{DD}	V_{DD} + 0.3	V
V_{IL}, Input Low Voltage (V_{DD} = +3.0V to +3.6V)	-0.3	0.3 x V_{DD}	V
Analog Inputs (connectors J1 and J2)			
Differential Input Voltage, RMS		7.9	V_{RMS}
Differential Input Voltage, Peak-to-Peak		22.3	V_{PP}

3 Hardware Description and Configuration

This section provides hardware description and configuration information for the PCM4204EVM.

3.1 Power Supply Configuration

The PCM4204EVM requires three analog power supplies and one digital power supply for operation. The analog supplies are connected at terminal block J5, while the digital supply is connected at terminal block J14.

Analog supplies include +15V and -15V DC for powering the input buffer circuits, as well as +5.0V DC for powering the analog section of the PCM4204. All supplies should be rated for at least 500mA of output current.

The digital supply requires +5.0V DC and should be rated for at least 500mA of output current. The +5.0V supply is regulated to +3.3V DC by an onboard Texas Instruments REG1117 linear voltage regulator (U23), which is used to power the digital section of the PCM4204 and the majority of the support logic circuitry. The core logic and line driver sections of the AES3 transmitters (U18 through U21) utilize the +5.0V digital supply directly.

An optional external +3.3V DC digital power supply is supported at terminal block J14. Jumper JMP6 is utilized to select either the onboard voltage regulator (U23) or an external +3.3V power source. Shorting pins 1 and 2 together using the supplied jumper block selects the onboard +3.3V voltage regulator. Shorting pins 3 and 4 together will select the external +3.3V supply terminal (EXT +3.3VD) on terminal block J14. Only one source may be selected at any time.

3.2 Analog Inputs

The PCM4204EVM includes four Neutrik combo XLR connectors, which accept either 3-pin male XLR or ¼-inch TRS phono plugs. The connectors are numbered J1 through J4, corresponding to Channels 1 through 4, respectively.

The analog inputs can accept up to a $7.9V_{RMS}$ (or $22.3V_{PP}$) differential input signal. This signal is then attenuated by a factor of 3.7 by the input buffer circuit, which corresponds to the $6.0V_{PP}$ full-scale differential input voltage for the PCM4204 analog inputs.

The input buffer circuits are each comprised of a single OPA1632 fully differential audio amplifier and associated passive components. The input buffer provides active attenuation and low pass filtering for the analog input signal. The OPA1632 outputs are DC level-shifted by approximately +2.5V using the amplifiers V_{COM}IN input (pin 2), which are connected to a buffered version of either the PCM4204 V_{COM}12 (pin 61) or V_{COM}34 outputs (pin 52).

3.3 Audio Data Format Selection

Switch SW1 is used to select the audio data format for the PCM4204 (U1). Table 2 and Table 3 summarize the available audio data formats for both Slave and Master mode operation and the corresponding SW1 switch settings.

Table 2. Audio Data Format Selection: Slave Mode Operation

S/M	FMT2	FMT1	FMT0	Audio Data Format
HI	LO	LO	LO	24-Bit Left Justified
HI	LO	LO	HI	24-Bit I^2S
HI	LO	HI	LO	24-Bit Right Justified
HI	LO	HI	HI	TDM with No BCK Delay for Start of Frame
HI	HI	LO	LO	TDM with One BCK Delay for Start of Frame
HI	HI	LO	HI	Reserved
HI	HI	HI	LO	Reserved
HI	HI	HI	HI	Reserved

Table 3. Audio Data Format Selection: Master Mode Operation

S/M	FMT2	FMT1	FMT0	Audio Data Format
LO	LO	LO	LO	24-Bit Left Justified
LO	LO	LO	HI	24-Bit I^2S
LO	LO	HI	LO	24-Bit Right Justified
LO	LO	HI	HI	DSD Output with PCM Output Disabled
LO	HI	LO	LO	DSD Input with 24-Bit Right Justified PCM Output
LO	HI	LO	HI	Reserved
LO	HI	HI	LO	Reserved
LO	HI	HI	HI	Reserved

For Slave mode operation, the Audio Serial Port header (connector J6) is utilized to interface to a Master device, such as a digital signal processor, FPGA, or an audio test system with a synchronous serial port interface. The system clock (SCKI), bit clock (BCK), and left/right word clock (LRCK) are generated by the Master device and are used to drive the SCKI (pin 15), BCK (pin 29), and LRCK (pin 30) inputs of the PCM4204. Serial audio data is output at SDOUT1 (pin 31) and SDOUT2 (pin 32). Slave mode supports PCM-formatted output data only. DSD output data is available only in Master mode.

For TDM data formats, the SUB switch on SW1 allows the user to select the sub-frame assignment for the PCM4204. Table 4 summarizes the operation of the SUB switch. Refer to the PCM4204 product datasheet for more details concerning the TDM data formats and operation.

Table 4. Sub-Frame Selection for TDM Data Formats

SUB	TDM Sub-Frame Selection
LO	Sub-frame 0 (time slots 1 through 4)
HI	Sub-frame 1 (time slots 5 through 8)

For Master mode, the system clock is provided by one of the sources described in Section 3.4 of this document. The PCM4204 internally generates the BCK and LRCK clocks, which are then output to the Audio Serial Port header (connector J6) and the AES3 digital interface transmitters, which then drive output connectors J9 through J12.

Master mode may also be configured to support 1-bit DSD-formatted audio output data. For the DSD mode formats, header J7 provides the direct input/output interface for the PCM 4204 (U1) DSD data port. In addition, there is a second PCM4204 (U2), configured to perform 1-bit DSD to 24-bit PCM format conversion with the PCM output provided at header J8. The DSD output from U1 may be routed to the DSD input of U2, providing a DSD-to-PCM test or demonstration mode.

The $\overline{\text{DSDTEST}}$ switch on SW1 is used to enable or disable the DSD test mode, as shown in Table 5. The data format for U1 must be set up for DSD Output mode, as shown in Table 3. Then the DSD test mode is enabled, routing the DSD data output from U1, through bus switch U16, and then to the DSD port of U2, which is configured for DSD Input mode. The DSD-to-PCM format conversion is then performed and 24-bit PCM data is output at header J8.

Table 5. DSD-to-PCM Conversion Test Mode Selection

$\overline{\text{DSDTEST}}$	DSD-to-PCM Test Mode
LO	Enabled
HI	Disabled

3.4 System Clock Configuration

Switch SW5 is used to select the system clock source for the PCM4204EVM. Table 6 summarizes the available clock source options. The onboard oscillators support standard PCM sampling rates in Master mode, including 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, and 192kHz. The external clock input (connector J13) may be used to supply alternate system clock frequencies that support additional sample rates.

For Slave mode operation, the system clock is input at the SCKI pin of header J6.

Table 6. System Clock Source Selection

Switch SW5			System Clock Source	Used for Master or Slave Mode Operation?
$\overline{\text{EXT}}$	OSC1	OSC0		
LO	LO	LO	External clock input at J13	Master
HI	LO	LO	External clock input at the SCKI pin of header J6	Slave
HI	LO	HI	Oscillator X1, 22.5792MHz	Master
HI	HI	LO	Oscillator X2, 22.576MHz	Master

3.5 Sampling Mode Selection

The sampling mode of the PCM4204 (U1 and U2) is selected using switch SW1. Table 7 through Table 10 summarize the available sampling modes for both PCM and DSD output modes.

Single Rate sampling mode is designed for output sampling rates up to 54kHz. The modulator oversampling rate is set to 128x.

Dual Rate sampling mode is designed for output sampling rates greater than 54kHz and up to 108kHz. The modulator oversampling rate is set to 64x.

Quad Rate sampling mode is designed for output sampling rates greater than 108kHz and up to 216kHz. The modulator oversampling rate is set to 32x.

Table 7. Sampling Mode Selection: PCM Slave Mode Audio Formats

FS2	FS1	FS0	Sampling Mode
LO	LO	LO	Single Rate with Clock Auto-Detection
LO	LO	HI	Dual Rate with Clock Auto-Detection
LO	HI	LO	Quad Rate with Clock Auto-Detection
LO	HI	HI	Reserved
HI	LO	LO	Reserved
HI	LO	HI	Reserved
HI	HI	LO	Reserved
HI	HI	HI	Reserved

Table 8. Sampling Mode Selection: PCM Master Mode Audio Formats

FS2	FS1	FS0	Sampling Mode
LO	LO	LO	Single Rate with $f_{SCKI} = 768f_S$
LO	LO	HI	Single Rate with $f_{SCKI} = 512f_S$
LO	HI	LO	Single Rate with $f_{SCKI} = 384f_S$

Table 8. Sampling Mode Selection: PCM Master Mode Audio Formats (continued)

FS2	FS1	FS0	Sampling Mode
LO	HI	HI	Single Rate with $f_{SCKI} = 256f_S$
HI	LO	LO	Dual Rate with $f_{SCKI} = 384f_S$
HI	LO	HI	Dual Rate with $f_{SCKI} = 256f_S$
HI	HI	LO	Quad Rate with $f_{SCKI} = 192f_S$
HI	HI	HI	Quad Rate with $f_{SCKI} = 128f_S$

Table 9. Sampling Mode Selection: DSD Output Mode

FS2	FS1	FS0	Sampling Mode
LO	LO	LO	$128f_S$ DSD Output Rate with $f_{SCKI} = 768f_S$
LO	LO	HI	$128f_S$ DSD Output Rate with $f_{SCKI} = 512f_S$
LO	HI	LO	$128f_S$ DSD Output Rate with $f_{SCKI} = 384f_S$
LO	HI	HI	$128f_S$ DSD Output Rate with $f_{SCKI} = 256f_S$
HI	LO	LO	$64f_S$ DSD Output Rate with $f_{SCKI} = 384f_S$
HI	LO	HI	$64f_S$ DSD Output Rate with $f_{SCKI} = 256f_S$
HI	HI	LO	Reserved
HI	HI	HI	Reserved

Table 10. Sampling Mode Selection: DSD Input Mode

FS2	FS1	FS0	Sampling Mode
LO	LO	LO	Reserved
LO	LO	HI	$128f_S$ DSD Input Rate with $f_{SCKI} = 512f_S$
LO	HI	LO	$128f_S$ DSD Input Rate with $f_{SCKI} = 384f_S$
LO	HI	HI	$128f_S$ DSD Input Rate with $f_{SCKI} = 256f_S$
HI	LO	LO	$64f_S$ DSD Input Rate with $f_{SCKI} = 384f_S$
HI	LO	HI	$64f_S$ DSD Input Rate with $f_{SCKI} = 256f_S$
HI	HI	LO	Reserved
HI	HI	HI	Reserved

3.6 Digital High-Pass Filter

The PCM4204 includes a digital high-pass filter function for all four channels, designed for removing the DC component from the digitized signal. The high-pass filter is not available when using the DSD output mode. The high-pass filter function may be enabled or disabled using the HPFD switch on SW1. Table 11 summarizes the operation of the HPFD switch.

Table 11. Digital High-Pass Filter Configuration

HPFD	Digital High-Pass Filter Function
LO	Enabled
HI	Disabled

3.7 Digital Interface Transmitter Configuration

Four Texas Instruments DIT4192 digital interface transmitters provide AES3-encoded outputs for the PCM4204EVM. Switch SW3 is utilized to configure the transmitters. The outputs of the transmitters are available at connectors J9 through J12, which are RCA phono jacks. These outputs are designed for use with 75Ω coaxial cable connections.

The transmitters are enabled using the $\overline{DIT}$ switch of SW3. The $\overline{DIT}$ switch operation is summarized in Table 12.

Table 12. Digital Interface Transmitter Configuration

$\overline{DIT}$	Digital Interface Filter Function
LO	Enabled
HI	Disabled

Like the PCM4204, the DIT4192 transmitters must be configured for the proper master (or system) clock frequency. The transmitter master clock is driven by the same source as the PCM4204 system clock, as described in Section 3.4 of this document. Table 13 summarizes the master clock options for the DIT4192 transmitters using switch SW3.

Table 13. Transmitter Master Clock Configuration

CLK1	CLK0	Transmitter MCLK Frequency
LO	LO	$128f_S$
LO	HI	$256f_S$
HI	LO	$384f_S$
HI	HI	$512f_S$

The audio data input format for the transmitters must also be set to match the PCM output data format for the PCM4204. Table 14 shows the transmitter data format settings, configured using switch SW3. The transmitters do not support TDM or DSD data formats.

Table 14. Transmitter Audio Data Format Selection

FMT1	FMT0	Transmitter Audio Data Format (PCM Only)
LO	LO	24-Bit Left Justified
LO	HI	24-Bit I^2S
HI	LO	24-Bit Right Justified
HI	HI	16-Bit Right Justified (not used)

The DIT4192 transmitters may be operated in either Stereo or Mono mode. In Stereo mode, two channels of audio data are transmitted at the input sampling frequency. In Mono mode, two consecutive samples of only one channel are transmitted at one-half the input sampling rate. The Mono mode is useful for performance testing with f_S = 176.4kHz or f_S = 192kHz with a system that can only accept only half these rates. This is the case with the Audio Precision System Two Cascade or Cascade Plus test system, which was used for factory performance testing of the PCM4204. Mono mode can be used in conjunction with the Audio Precision Dual BNC digital input mode to test at sampling rates up to 216kHz.

The MONO12 and MONO34 switches on SW3 are used to enable or disable Mono mode operation. Table 15 summarizes the operation of these switches.

Table 15. Mono Mode Configuration

MONO12	**Transmitter U18 and U19 Operation**
LO	Stereo Mode Connectors J9 and J10 will both output AES3-encoded data for Channels 1 and 2
HI	Mono Mode Connector J9 will output AES3-encoded data for Channel 1 Connector J10 will output AES3-encoded data for Channel 2
MONO34	**Transmitter U20 and U21 Operation**
LO	Stereo Mode Connectors J11 and J12 will both output AES3-encoded data for Channels 3 and 4
HI	Mono Mode Connector J11 will output AES3-encoded data for Channel 3 Connector J12 will output AES3-encoded data for Channel 4

3.8 Reset Operations

The PCM4204EVM includes two reset switches, SW2 and SW4. Both are momentary contact pushbutton switches that are normally open. SW2 provides the manual reset for the PCM4204 devices (U1 and U2), while switch SW4 provides the manual reset for the four DIT4192 transmitters (U18 through U21). Figure 3 and Figure 4 illustrate the onboard reset circuitry.

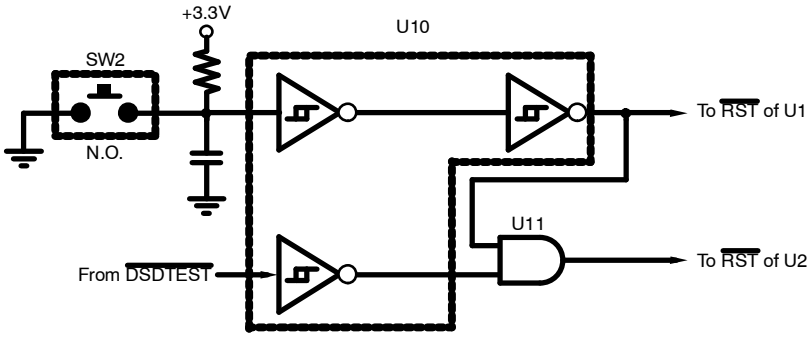

Figure 3. ADC Reset Circuitry

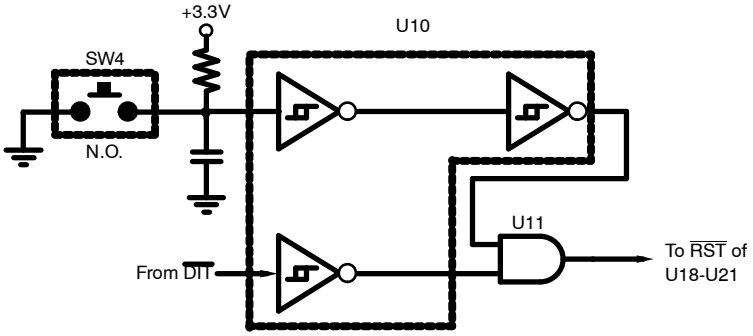

Figure 4. DIT (Transmitter) Reset Circuitry

For the ADC reset function, there are two outputs from the reset circuit, one for U1 and the other for U2. U1 may be reset at any time by momentarily pressing and then releasing switch SW1. U2 may be reset by SW2 only when the DSDTEST switch of SW1 is set to LO. If DSDTEST is set HI, the AND gate output of the reset circuit is forced low, which will force U2 into power-down mode.

For the DIT reset function, the output of the reset circuit is connected to the RST pins of DIT4192 transmitters (U18 through U21). The transmitters may be reset only when the DIT switch of SW3 is set LO by momentarily pressing and then releasing switch SW4. If the DIT switch is set HI, the AND gate output of the reset circuit is forced low, which will force U18 through U21 into power-down mode.

4 Schematic, PCB Layout, and Bill of Materials

This section provides the electrical schematic and physical layout information for the PCM4204EVM. The bill of materials is included as a component reference.

NOTE

Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing PCM4204EVM PCBs.

4.1 Schematic

The electrical schematics for the PCM4204EVM are shown in Figure 5 and Figure 6. The components shown in the schematics are listed in Table 16 for reference.

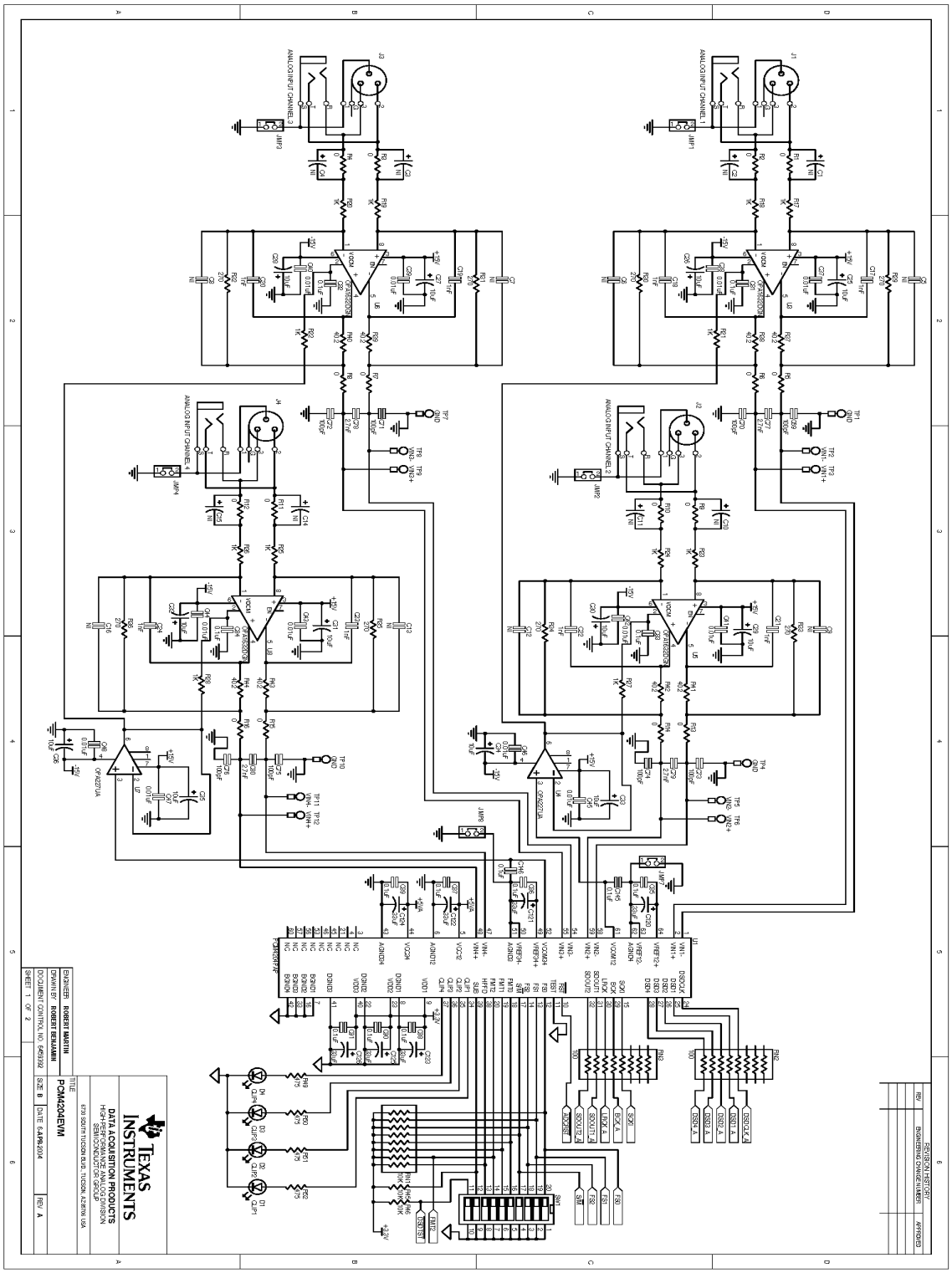

Figure 5. PCM4204EVM Schematic-Analog Section

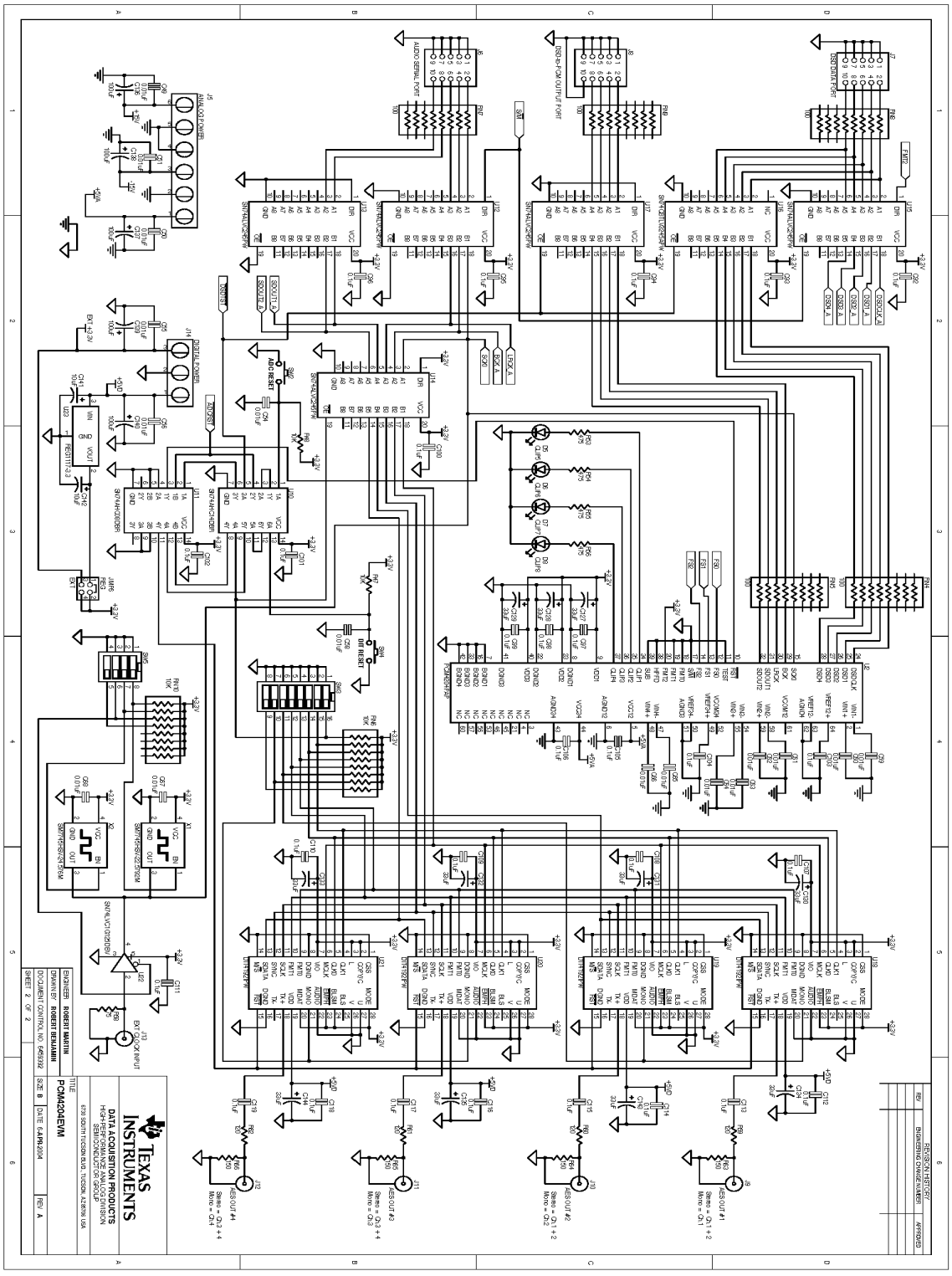

Figure 6. PCM4204EVM Schematic-Digital Section

4.2 PCB Layout

The PCM4204EVM is a 4-layer printed circuit board with the following layer structure:

- Layer 1: Top (Component Side)
- Layer 2: Ground Plane
- Layer 3: Power
- Layer 4: Bottom (Solder Side)

The ground plane doubles as a heat sink for the PCM4204 PowerPAD package. Refer to the product data sheet for more information on the purpose and application of the PowerPAD connection.

Figure 7 through Figure 12 show the top and bottom side silkscreen images, along with the top, ground plane, power, and bottom layers of the PCB.

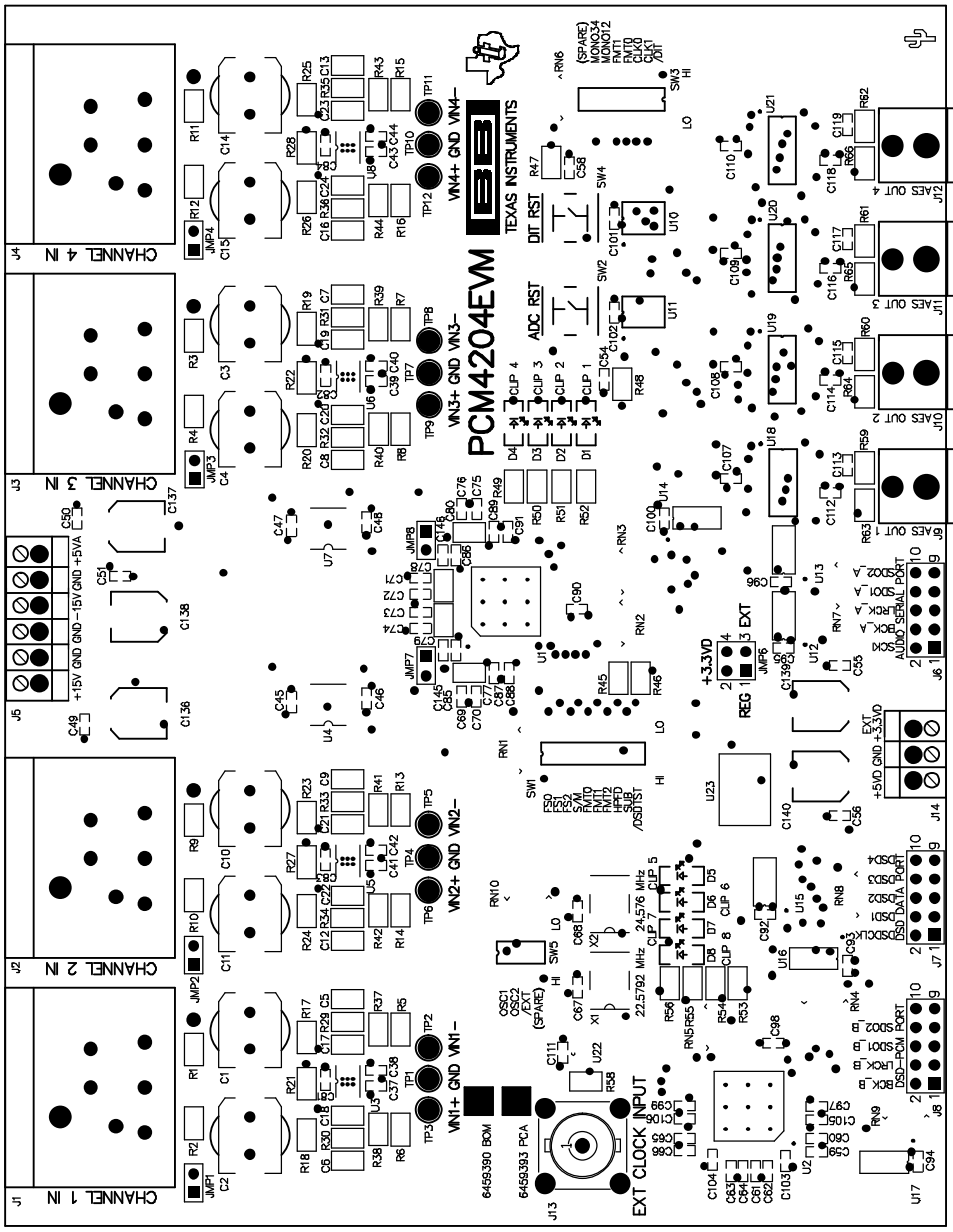

Figure 7. Top Side Silkscreen

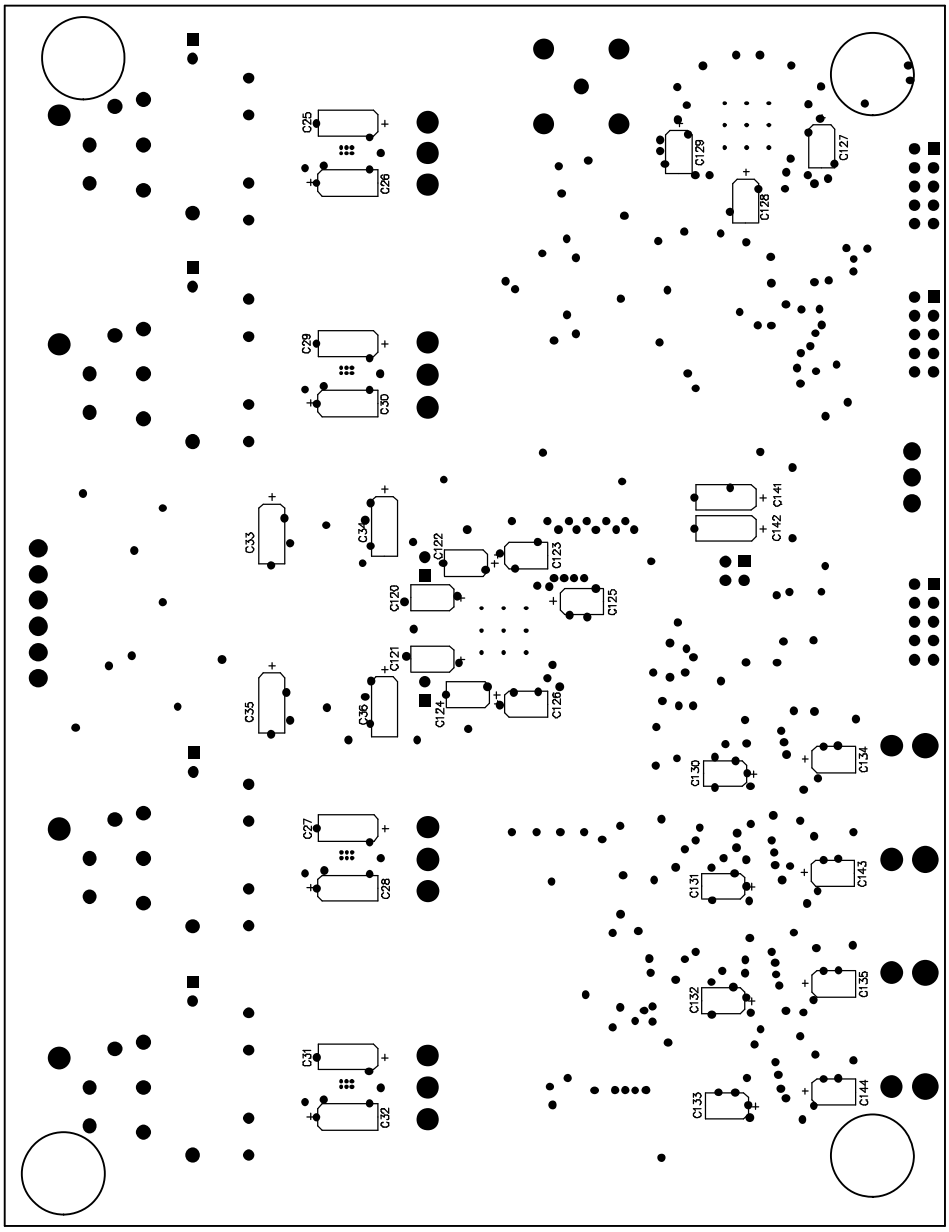

Figure 8. Bottom Side Silkscreen

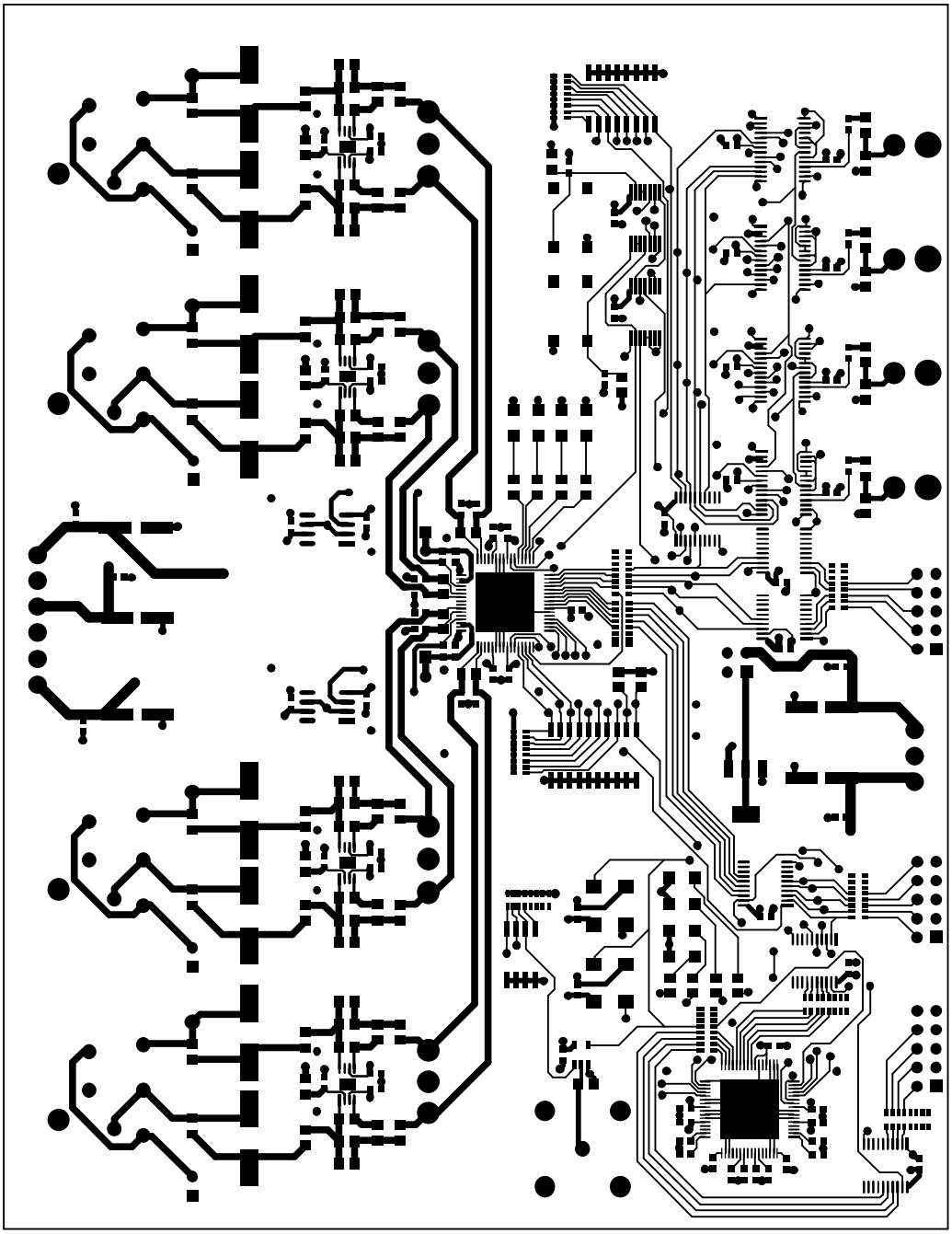

Figure 9. Top Layer (Component Side)

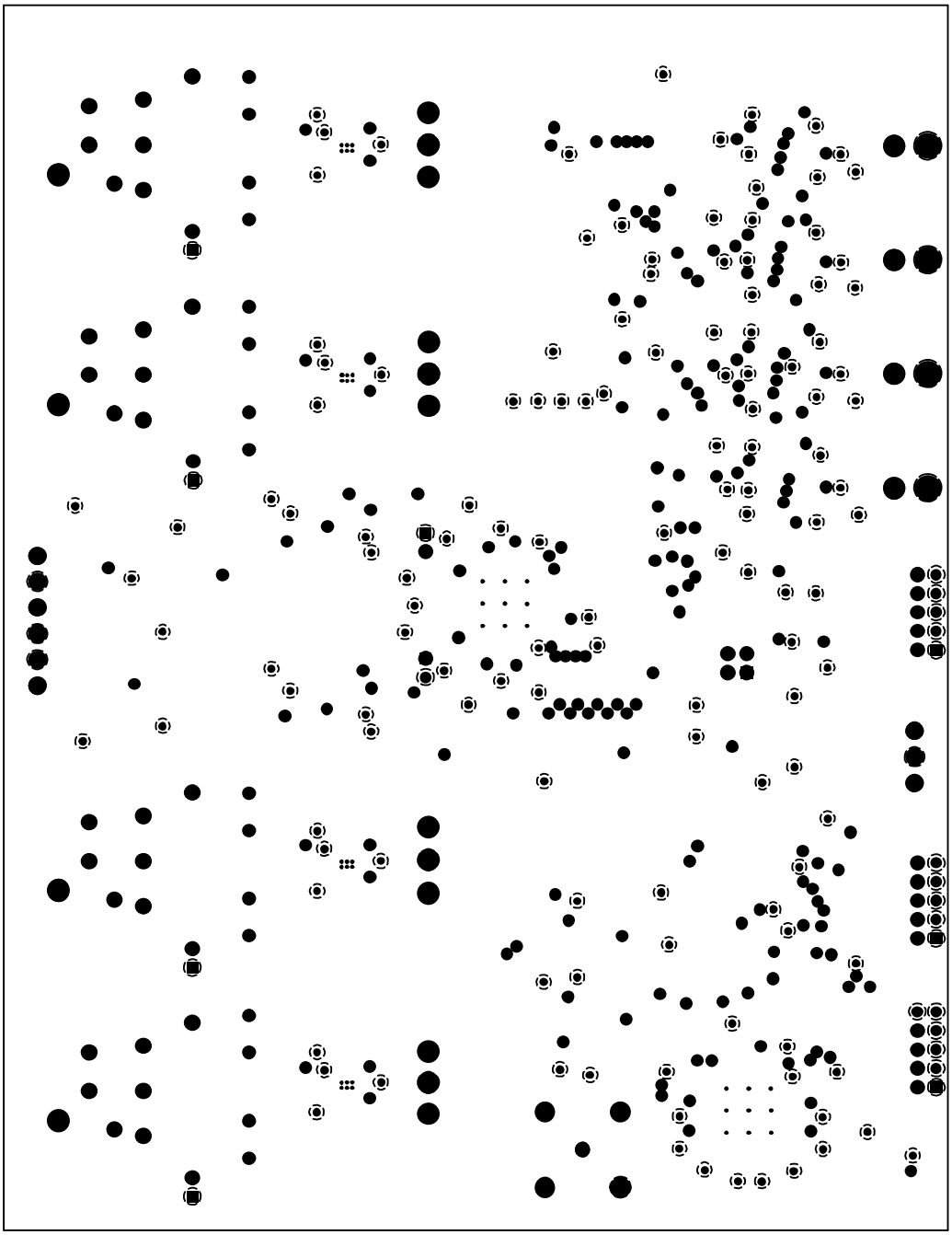

Figure 10. Ground Plane Layer

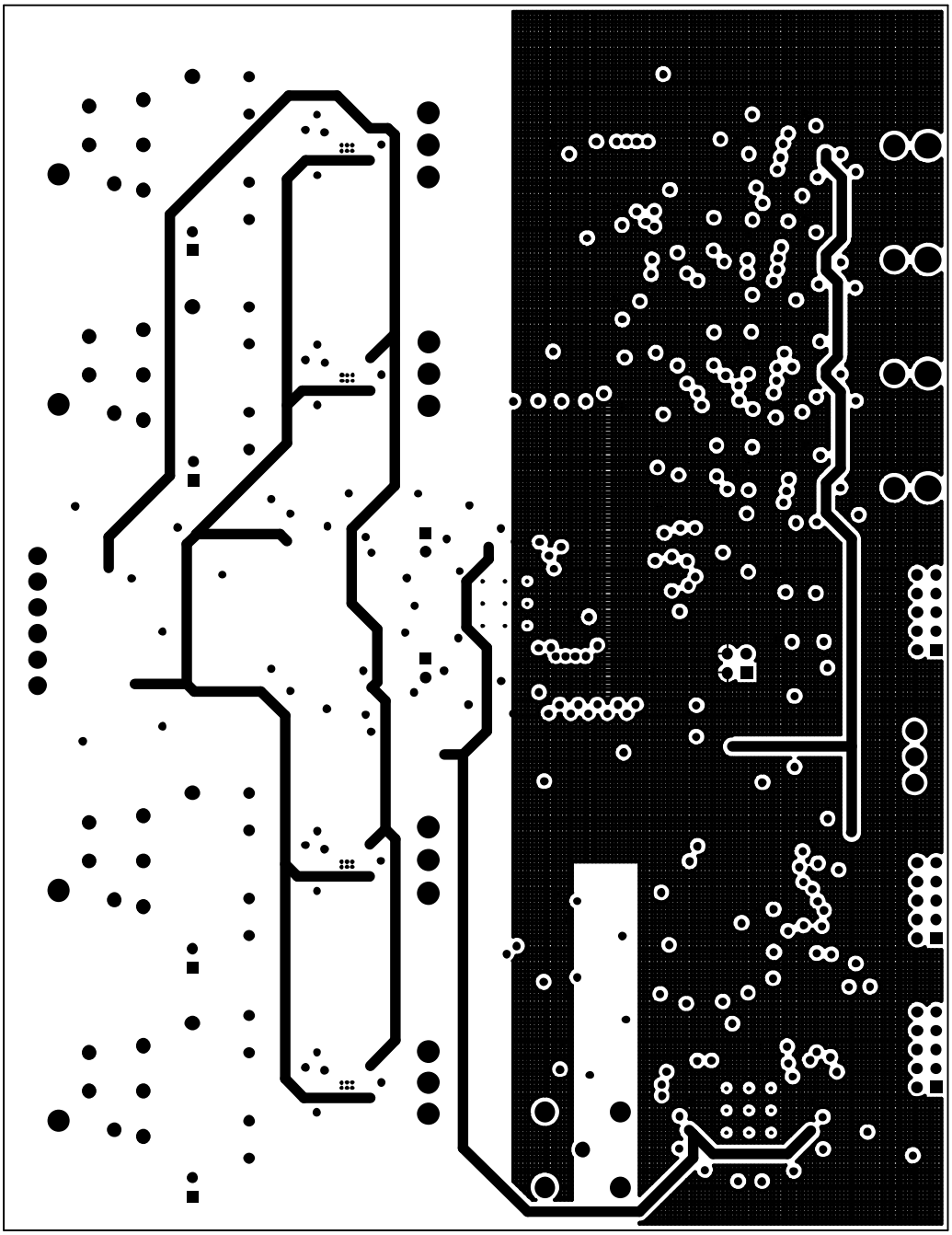

Figure 11. Power Plane Layer

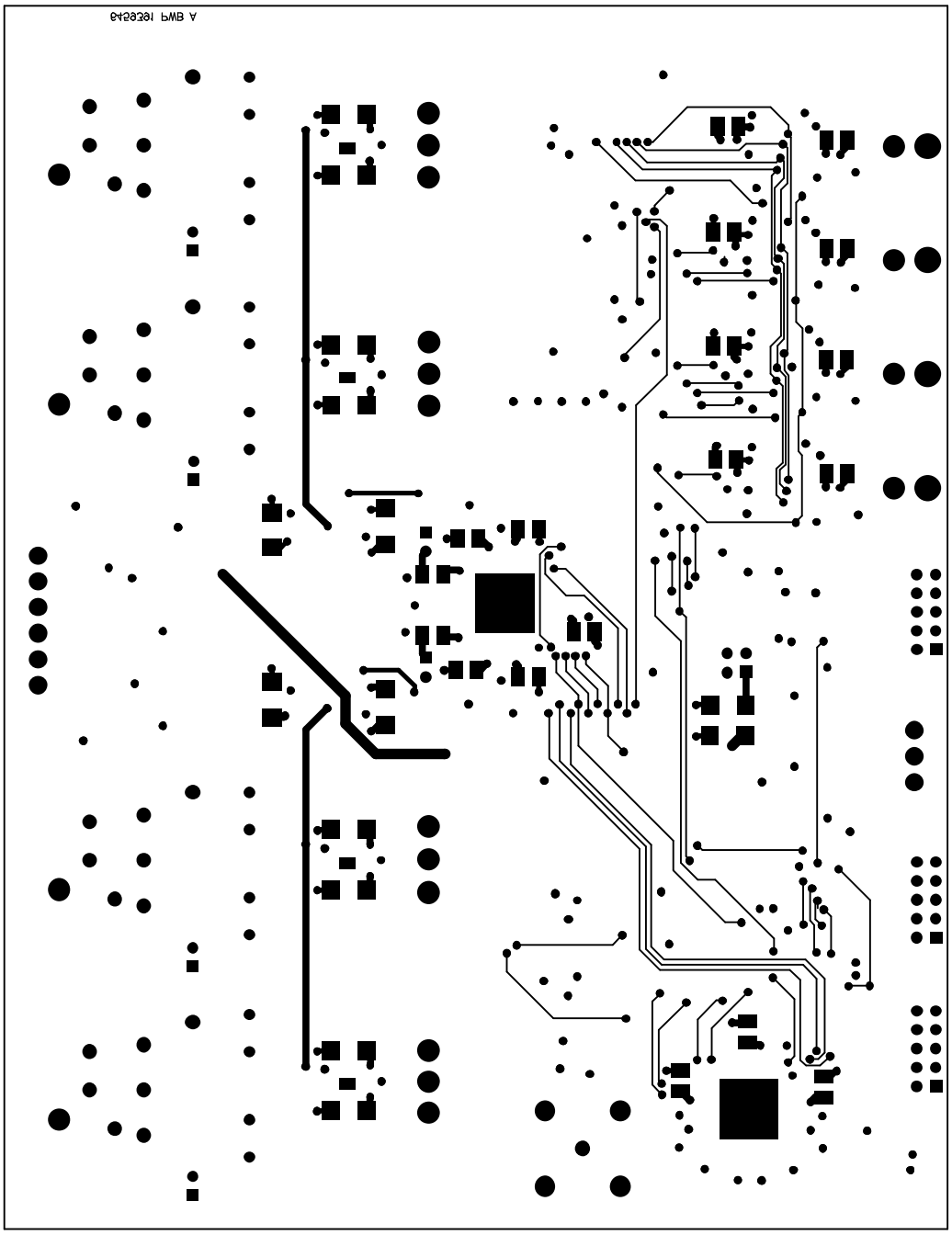

Figure 12. Bottom Layer (Solder Side)

4.3 Bill of Materials

The Bill of Materials, listing the components used in the assembly of the PCM4204EVM, is shown in Table 16.

Table 16. PCM4204EVM Bill of Materials

ITEM	VALUE	Ref Des	QTY PER BOARD	MFR	MFR PART NUMBER	DESCRIPTION
1	100pF	C69-C76	8	Kemet	C0603C101J5GACTU	Chip Capacitor, C0G Ceramic, 100pF ±5%, 50WV, Size = 0603
2	1nF	C17-C24	8	Kemet	C0805C102J3GAC	Chip Capacitor, C0G Ceramic, 1nF ±5%, 25WV, Size = 0805
3	2.7nF	C77-C80	4	Kemet	C0805C272J3GAC	Chip Capacitor, C0G Ceramic, 2.7nF ±5%, 25WV, Size = 0805
4	0.01μF	C37-C51, C54-C68	30	Kemet	C0603C103J5RACTU	Chip Capacitor, X7R Ceramic, 0.01μF ±5%, 50WV, Size = 0603
5	0.1μF	C85-C119	35	Kemet	C0603C104J4RACTU	Chip Capacitor, X7R Ceramic, 0.1μF ±5%, 16WV, Size = 0603
6	10μF	C25-C36, C141, C142	14	Kemet	T494C106K025AS	Chip Capacitor, Low ESR Tantalum, 10μF ±10%, 25WV, Size = C
7	33μF	C120-C135, C143, C144	18	Kemet	T494B336K010AS	Chip Capacitor, Low ESR Tantalum, 33μF ±10%, 10WV, Size = B
8	100μF	C136-C140	5	Panasonic	EEV-FK1E101XP	Capacitor, SMT Aluminum Electrolytic, 100μF ±20%, 25WV
9		D1-D8	8	Lumex	SML-LX1206IC-TR	Red LED, Surface Mount, Size = 1206
10		J1-J4	4	Neutrik	NCJ6FI	Combo Connector, Female XLR and TRS, Vertical PC Mount
11		J5	1	Weidmuller	9967720000	3.5mm PCB Terminal Block, 6 poles
12		J6-J8	3	Samtec	TSW-105-07-G-D	Terminal Strip, 10-pin (5x2)
13		J9-J12	4	CUI Stack	RJC-041	RCA Phono Jack, Black Shell
14		J13	1	Kings Electronics	KC-79-274-M06	BNC Connector, Female, PC Mount
15		J14	1	Weidmuller	169968000	3.5mm PCB Terminal Block, 3 poles
16		JMP1-JMP4	4	Samtec	TSW-102-07-G-S	Terminal Strip, 2-pin (2x1)
17		JMP6	1	Samtec	TSW-102-07-G-D	Terminal Strip, 4-pin (2x2)
18	0	R1-R16	16	Panasonic	ERJ-6EY0R00V	Chip Resistor, 0Ω, Shunt, Size = 0805
19	40.2	R37-R44	8	Panasonic	ERJ-6EN-F40R2V	Chip Resistor, Thick Film, 1% Tolerance, 40.2Ω, 1/10W, Size = 0805
20	75	R58	1	Panasonic	ERJ-6ENF75R0V	Chip Resistor, Thick Film, 1% Tolerance, 75Ω, 1/10W, Size = 0805
21	120	R59-R62	4	Panasonic	ERJ-6ENF1200V	Chip Resistor, Thick Film, 1% Tolerance, 120Ω, 1/10W, Size = 0805
22	150	R63-R66	4	Panasonic	ERJ-6ENF1500V	Chip Resistor, Thick Film, 1% Tolerance, 150Ω, 1/10W, Size = 0805
23	270	R29-R36	8	Panasonic	ERA-6YEB271V	Chip Resistor, Metal Film, 0.1% Tolerance, 270Ω, 1/10W, Size = 0805
24	475	R49-R56	8	Panasonic	ERJ-6ENF4750V	Chip Resistor, Thick Film, 1% Tolerance, 475Ω, 1/10W, Size = 0805
25	1K	R17-R26	10	Panasonic	ERA-6YEB102V	Chip Resistor, Metal Film, 0.1% Tolerance, 1kΩ, 1/10W, Size = 0805
26	10K	R45-R48	4	Panasonic	ERJ-6ENF1002V	Chip Resistor, Thick Film, 1% Tolerance, 10kΩ, 1/10W, Size = 0805
27	100	RN2-RN5, RN7-RN9	7	CTS	742C163101J	Thick Film Chip Resistor Array, 100Ω, 16-Terminal, 8 Resistors, Isolated

Table 16. PCM4204EVM Bill of Materials (continued)

28	10K	RN1, RN6, RN10	3	CTS	742C163103J	Thick Film Chip Resistor Array, 10kΩ, 16-Terminal, 8 Resistors, Isolated
29		SW1	1	ITT Industries/ C&K	TDA08H0SK1	DIP Switch, 8 Element, Half-Pitch, Surface-Mount, Tape Sealed
30		SW2, SW4	2	Omron	B3S-1000	Momentary Tact Switch, SMT without Ground Terminal
31		SW3	1	ITT Industries/ C&K	TDA08H0SK1	DIP Switch, 8 Element, Half-Pitch, Surface-Mount, Tape Sealed
32		SW5	1	ITT Industries/ C&K	TDA04H0SK1	DIP Switch, 4 Element, Half-Pitch, Surface-Mount, Tape Sealed
33		U1, U2	2	Texas Instruments	PCM4204PAP	Four-Channel Audio A/D Converter
34		U3, U5, U6, U8	4	Texas Instruments	OPA1632DGN	Fully-Differential Audio Amplifier
35		U4, U7	2	Texas Instruments	OPA227UA	Precision Operational Amplifier
36		U10	1	Texas Instruments	SN74AHC14DBR	Hex Schmitt-Trigger Inverters
37		U11	2	Texas Instruments	SN74AHC08DBR	Quad 2-Input Positive AND Gates
38		U12-U14, U15, U17	5	Texas Instruments	SN74ALVC245PW	Octal Bus Transceiver with Tri-State Outputs
39		U16	1	Texas Instruments	SN74CBTLV3245APW	Octal FET Bus Switch
40		U18-U21	4	Texas Instruments	DIT4192IPW	192kHz Digital Audio Transmitter
41		U22	1	Texas Instruments	SN74LVC1G125DBV	Single Non-Inverting Buffer with Tri-State Output
42		U23	1	Texas Instruments	REG1117-3.3	Linear Voltage Regulator, +3.3V
43		TP1-TP12	12	Keystone Electronics	5006	PCB Test Point, Compact, Through-hole
44		X1	1	Pletronics	SM7745HSW-22.5792M	+3.3V Surface-Mount Clock Oscillator, CMOS Output with Active High Enable, 22.5792MHz±50ppm
45		X2	1	Pletronics	SM7745HSW-24.576M	+3.3V Surface-Mount Clock Oscillator, CMOS Output with Active High Enable, 24.576MHz±50ppm
46			5	Samtec	SNT-100-BK-G-H	Shorting Blocks
47			4	3M Bumpon	SJ-5003	Self-Adhesive Rubber Feet

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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During normal operation, some circuit components may have case temperatures greater than 37°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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