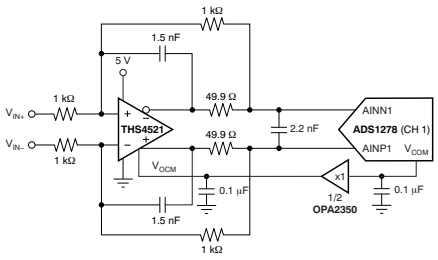
VERY LOW POWER, NEGATIVE RAIL INPUT, RAIL-TO-RAIL OUTPUT, FULLY DIFFERENTIAL AMPLIFIER

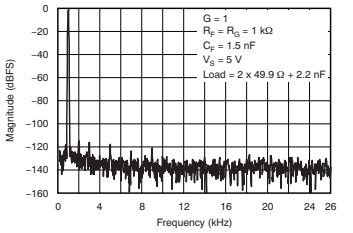
Check for Samples: THS4521, THS4522, THS4524

FEATURES

- **Fully Differential Architecture**
- **Bandwidth: 145 MHz**
- **Slew Rate: 490 V/μs**
- **HD_2: –133 dBc at 10 kHz (1 V_{RMS}, R_L = 1 kΩ)**
- **HD_3: –140 dBc at 10 kHz (1 V_{RMS}, R_L = 1 kΩ)**
- **Input Voltage Noise: 4.6 nV/√Hz (f = 100 kHz)**
- **THD+N: –112dBc (0.00025%) at 1 kHz (22-kHz BW, G = 1, 5 V_{PP})**
- **Open-Loop Gain: 119 dB**
- **NRI—Negative Rail Input**
- **RRO—Rail-to-Rail Output**
- **Output Common-Mode Control (with Low Offset and Drift)**
- **Power Supply:**
  - **Voltage: +2.5 V (±1.25 V) to +5.5 V (±2.75 V)**
  - **Current: 1.14 mA/ch**
- **Power-Down Capability: 20 μA (typ)**

THS4521 and ADS1278 Combined Performance





Tone (Hz)	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
1 k	–0.50	109.1	–107.9	105.5	113.7

APPLICATIONS

- **Low-Power SAR and ΔΣ ADC Drivers**
- **Low-Power Differential Driver**
- **Low-Power Differential Signal Conditioning**
- **Low-Power, High-Performance Differential Audio Amplifier**

DESCRIPTION

The THS4521, THS4522, and THS4524 family of devices are very low-power, fully differential op amps with rail-to-rail output and an input common-mode range that includes the negative rail. These amplifiers are designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter, and provide exceptional performance in audio applications.

The family includes single (THS4521), dual (THS4522), and quad (THS4524) versions.

These fully differential op amps feature accurate output common-mode control that allows for dc-coupling when driving analog-to-digital converters (ADCs). This control, coupled with an input common-mode range below the negative rail as well as rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, these devices are ideally suited for driving both successive-approximation register (SAR) and delta-sigma (ΔΣ) ADCs using only a single +2.5V to +5V and ground power supply.

The THS4521, THS4522, and THS4524 family of fully differential op amps is characterized for operation over the full industrial temperature range from –40°C to +85°C.

RELATED PRODUCTS

DEVICE	BW (MHz)	I_Q (mA)	THD (dBc) at 100 kHz	V_N (nV/√Hz)	RAIL-TO-RAIL
THS4520	570	15.3	–114	2	Out
THS4121	100	16	–79	5.4	In/Out
THS4130	150	16	–107	1.3	No

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS4521	SOIC-8	D	–40°C to +85°C	TH4521	THS4521ID	Rails, 75
					THS4521IDR	Tape and reel, 2500
	MSOP-8	DGK		4521	THS4521IDGKT	Tape and reel, 250
					THS4521IDGKR	Tape and reel, 2500
THS4522	TSSOP-16	PW	–40°C to +85°C	THS4522	THS4522IPW	Rails, 90
					THS4522IPWR	Tape and reel, 2000
THS4524	TSSOP-38	DBT	–40°C to +85°C	THS4524	THS4524IDBT	Rails, 50
					THS4524IDBTR	Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the relevant product folders at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		THS4521, THS4522. THS4524	UNIT
Supply Voltage, $V_{S–}$ to V_{S+}		5.5	V
Input/Output Voltage, V_I ($V_{IN±}$, $V_{OUT±}$, V_{OCM} pins)		($V_{S–}$) – 0.7 to (V_{S+}) + 0.7V	V
Differential Input Voltage, V_{ID}		1	V
Output Current, I_O		100	mA
Input Current, I_I ($V_{IN±}$, V_{OCM} pins)		10	mA
Continuous Power Dissipation		See Thermal Characteristic Specifications	
Maximum Junction Temperature, T_J		+150	°C
Maximum Junction Temperature, T_J (continuous operation, long-term reliability)		+125	°C
Operating Free-air Temperature Range, T_A		–40 to +85	°C
Storage Temperature Range, T_{STG}		–65 to +150	°C
ESD Rating:	Human Body Model (HBM)	1300	V
	Charge Device Model (CDM)	1000	V
	Machine Model (MM)	50	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL[1]
		MIN	TYP	MAX		
AC PERFORMANCE						
Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		135		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		49		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 5		18.6		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 10		9.3		MHz	C
Gain Bandwidth Product	V_{OUT} = 100 mV_{PP}, G = 10		93		MHz	C
Large-Signal Bandwidth	V_{OUT} = 2 V_{PP}, G = 1		95		MHz	C
Bandwidth for 0.1-dB Flatness	V_{OUT} = 2 V_{PP}, G = 1		20		MHz	C
Rising Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		420		V/µs	C
Falling Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		460		V/µs	C
Overshoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		1.2		%	C
Undershoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		2.1		%	C
Rise Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		4		ns	C
Fall Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		3.5		ns	C
Settling Time to 1%	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		13		ns	C
Harmonic Distortion						
2nd harmonic	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1[2], differential input		–122		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1		–85		dBc	C
3rd harmonic	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1[2], differential input		–141		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1		–90		dBc	C
Second-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–83		dBc	C
Third-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–90		dBc	C
Input Voltage Noise	f > 10 kHz		4.6		nV/√Hz	C
Input Current Noise	f > 100 kHz		0.6		pA/√Hz	C
Overdrive Recovery Time	Overdrive = ±0.5 V		80		ns	C
Output Balance Error	V_{OUT} = 100 mV, f ≤ 2 MHz (differential input)		–57		dB	C
Closed-Loop Output Impedance	f = 1 MHz (differential)		0.3		Ω	C
Channel-to-Channel Crosstalk (THS4522, THS4524)	f = 10 kHz, measured differentially		–125		dB	C
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})		100	116		dB	A
Input-Referred Offset Voltage	T_A = +25°C		±0.2	±2	mV	A
	T_A = –40°C to +85°C		±0.5	±3.5	mV	B
Input offset voltage drift[3]	T_A = –40°C to +85°C		±2		µV/°C	C
Input Bias Current	T_A = +25°C		0.65	0.85	µA	B
	T_A = –40°C to +85°C		0.75	0.95	µA	B
Input bias current drift[3]	T_A = –40°C to +85°C		±1.75	±2	nA/°C	B
Input Offset Current	T_A = +25°C		±50	±60	pA	B
	T_A = –40°C to +85°C		±60	±70	pA	B
Input offset current drift[3]	T_A = –40°C to +85°C		±0.16	±0.25	pA/°C	B

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Not directly measureable; calculated using noise gain of 101 as described in the Applications section, *Audio Performance*.
(3) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at –40°C and +85°C, computing the difference, and dividing by 125.

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER			CONDITIONS	THS4521, THS4522, THS4524 MIN	TYP	MAX	UNIT	TEST LEVEL (1)
INPUT								
Common-Mode Input Voltage Low			T_A = +25°C		–0.2	–0.1	V	A
			T_A = –40°C to +85°C		–0.1	0	V	B
Common-Mode Input Voltage High			T_A = +25°C	1.9	2		V	A
			T_A = –40°C to +85°C	1.8	1.9		V	B
Common-Mode Rejection Ratio (CMRR)				80	100		dB	A
Input Resistance					110‖1.5		kΩ‖pF	C
OUTPUT								
Output Voltage Low			T_A = +25°C		0.08	0.15	V	A
			T_A = –40°C to +85°C		0.09	0.2	V	B
Output Voltage High			T_A = +25°C	3.0	3.1		V	A
			T_A = –40°C to +85°C	2.95	3.05		V	B
Output Current Drive (for linear operation)			R_L = 50 Ω		±35		mA	C
POWER SUPPLY								
Specified Operating Voltage				2.5		5.5	V	B
Quiescent Operating Current, per channel			T_A = +25°C	0.9	1.0	1.2	mA	A
			T_A = –40°C to +85°C	0.85	1.0	1.25	mA	B
Power-Supply Rejection Ratio (±PSRR)				80	100		dB	A
POWER DOWN								
Enable Voltage Threshold			Assured *on* above 2.1 V		1.6	2.1	V	A
Disable Voltage Threshold			Assured *off* below 0.7 V	0.7	1.6		V	A
Disable Pin Bias Current					1		µA	C
Power Down Quiescent Current					10		µA	C
Turn-On Time Delay			Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω		108		ns	B
Turn-Off Time Delay			Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω		88		ns	B
V_{OCM} VOLTAGE CONTROL								
Small-Signal Bandwidth					23		MHz	C
Slew Rate					55		V/µs	C
Gain				0.98	0.99	1.02	V/V	A
Common-Mode Offset Voltage from V_{OCM} Input			Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 1.65 V ±0.5 V		±2.5	±4	mV	B
Input Bias Current			V_{OCM} = 1.65 V ±0.5 V		±5	±8	µA	B
V_{OCM} Voltage Range				1	0.8 to 2.5	2.3	V	A
Input Impedance					72‖1.5		kΩ‖pF	C
Default Output Common-Mode Voltage Offset from (V_{S+} – V_{S-})/2			Measured at V_{OUT} with V_{OCM} input open		±1.5	±5	mV	A
THERMAL CHARACTERISTICS								
Specified Operating Range All Packages					–40 to +85		°C	C
Thermal Resistance, θ_{JA}			Junction-to-ambient					
THS4521	D	SO-8			194		°C/W	C
	DGK	MSOP-8			269		°C/W	C
THS4522	PW	TSSOP-16			116		°C/W	C
THS4524	DBT	TSSOP-38			81		°C/W	C

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
AC PERFORMANCE						
Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		145		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		50		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 5		20		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 10		9.5		MHz	C
Gain Bandwidth Product	V_{OUT} = 100 mV_{PP}, G = 10		95		MHz	C
Large-Signal Bandwidth	V_{OUT} = 2 V_{PP}, G = 1		145		MHz	C
Bandwidth for 0.1-dB Flatness	V_{OUT} = 2 V_{PP}, G = 1		30		MHz	C
Rising Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		490		V/µs	C
Falling Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		600		V/µs	C
Overshoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		1		%	C
Undershoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		2.6		%	C
Rise Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		3.4		ns	C
Fall Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		3		ns	C
Settling Time to 1%	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		10		ns	C
Harmonic Distortion						
2nd harmonic	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1(2), differential input		–122		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1		–85		dBc	C
3rd harmonic	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1(2), differential input		–141		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1		–91		dBc	C
Second-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–86		dBc	C
Third-Order Intermodulation Distortion	Two-tone, f_1 = 2 MHz, f_2 = 2.2 MHz, V_{OUT} = 2-V_{PP} envelope		–93		dBc	C
Input Voltage Noise	f > 10 kHz		4.6		nV/√Hz	C
Input Current Noise	f > 100 kHz		0.6		pA/√Hz	C
SNR	V_{OUT} = 5 V_{PP}, 20 Hz to 22 kHz BW, differential input		114		dBc	C
THD+N	f = 1 kHz , V_{OUT} = 5 V_{PP}, 20 Hz to 22 kHz BW, differential input		112		dBc	C
Overdrive Recovery Time	Overdrive = ±0.5 V		75		ns	C
Output Balance Error	V_{OUT} = 100 mV, f < 2 MHz, V_{IN} differential		–57		dB	C
Closed-Loop Output Impedance	f = 1 MHz (differential)		0.3		Ω	C
Channel-to-Channel Crosstalk (THS4522. THS4524)	f = 10 kHz, measured differentially		–125		dB	C
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})		100	119		dB	A
Input-Referred Offset Voltage	T_A = +25°C		±0.24	±2	mV	A
	T_A = –40°C to +85°C		±0.5	±3.5	mV	B
Input offset voltage drift(3)	T_A = –40°C to +85°C		±2		µV/°C	C
Input Bias Current	T_A = +25°C		0.7	0.9	µA	B
	T_A = –40°C to +85°C		0.9	1.1	µA	B
Input bias current drift(3)	T_A = –40°C to +85°C		±1.8	±2.2	nA/°C	B
Input Offset Current	T_A = +25°C		±50	±60	pA	B

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Not directly measureable; calculated using noise gain of 101 as described in the Applications section, *Audio Performance*.
(3) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at –40°C and +85°C, computing the difference, and dividing by 125.

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

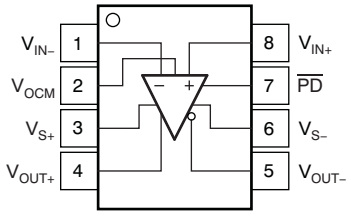
At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	THS4521, THS4522, THS4524			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
Input Offset Current, *continued*	T_A = –40°C to +85°C		±60	±75	pA	B
Input offset current drift(4)	T_A = –40°C to +85°C		±0.16	±0.25	pA/°C	B
INPUT						
Common-Mode Input Voltage Low	T_A = +25°C		–0.2	–0.1	V	A
	T_A = –40°C to +85°C		–0.1	0	V	B
Common-Mode Input Voltage High	T_A = +25°C	3.6	3.7		V	A
	T_A = –40°C to +85°C	3.5	3.6		V	B
Common-Mode Rejection Ratio (CMRR)		80	102		dB	A
Input Impedance			100‖0.7		kΩ‖pF	C
OUTPUT						
Output Voltage Low	T_A = +25°C		0.10	0.15	V	A
	T_A = –40°C to +85°C		0.115	0.2	V	B
Output Voltage High	T_A = +25°C	4.7	4.75		V	A
	T_A = –40°C to +85°C	4.65	4.7		V	B
Output Current Drive (for linear operation)	R_L = 50 Ω		±55		mA	C
POWER SUPPLY						
Specified Operating Voltage		2.5		5.5	V	B
Quiescent Operating Current, per channel	T_A = +25°C	0.95	1.14	1.25	mA	A
	T_A = –40°C to +85°C	0.9	1.15	1.3	mA	B
Power-Supply Rejection Ratio (±PSRR)		80	100		dB	A
POWER DOWN						
Enable Voltage Threshold	Ensured *on* above 2.1 V		1.6	2.1	V	A
Disable Voltage Threshold	Ensured *off* below 0.7 V	0.7	1.6		V	A
Disable Pin Bias Current			1		µA	C
Power Down Quiescent Current			20		µA	C
Turn-On Time Delay	Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω		70		ns	B
Turn-Off Time Delay	Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω		60		ns	B
V_{OCM} VOLTAGE CONTROL						
Small-Signal Bandwidth			23		MHz	C
Slew Rate			55		V/µs	C
Gain		0.98	0.99	1.02	V/V	A
Common-Mode Offset Voltage from V_{OCM} Input	Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 2.5V ±1 V		±5	±9	mV	B
Input Bias Current	V_{OCM} = 2.5V ±1 V		±20	±25	µA	B
V_{OCM} Voltage Range		1	0.8 to 4.2	4	V	A
Input Impedance			46‖1.5		kΩ‖pF	C
Default Output Common-Mode Voltage Offset from (V_{S+} – V_{S-})/2	Measured at V_{OUT} with V_{OCM} input open		±1	±5	mV	A
THERMAL CHARACTERISTICS						
Specified Operating Range All Packages		–40		+85	°C	C
Thermal Resistance, θ_{JA}	Junction-to-ambient					
THS4521 D SO-8			194		°C/W	C
DGK MSOP-8			269		°C/W	C
THS4522 PW TSSOP-16			116		°C/W	C
THS4524 DBT TSSOP-38			81		°C/W	C

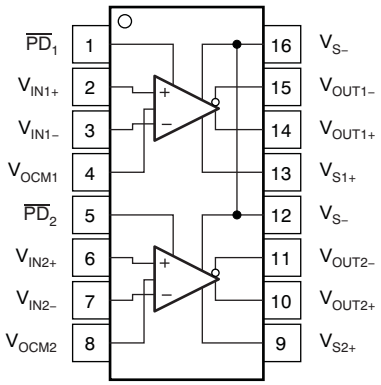
(4) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at –40°C and +85°C, computing the difference, and dividing by 125.

DEVICE INFORMATION

THS4521
SOIC-8, MSOP-8 (D, DGK PACKAGES)
(TOP VIEW)



THS4522
TSSOP-16 (PW PACKAGE)
(TOP VIEW)



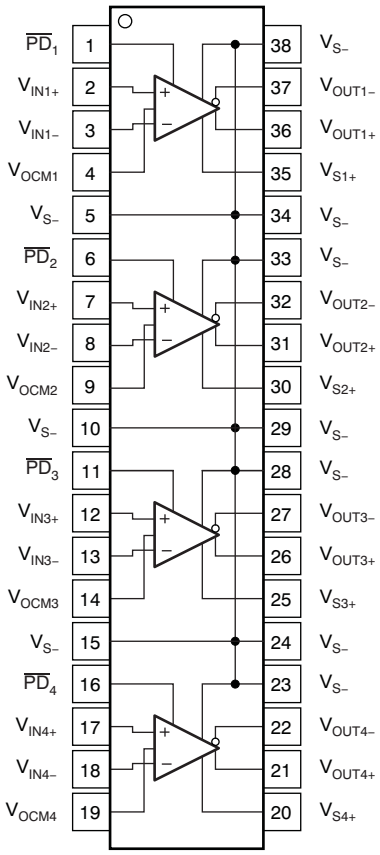
TERMINAL FUNCTIONS: THS4521

SOIC-8, MSOP-8		DESCRIPTION
PIN NO.	NAME	
1	$V_{IN–}$	Inverting amplifier input
2	V_{OCM}	Common-mode voltage input
3	V_{S+}	Amplifier positive power-supply input
4	V_{OUT+}	Noninverting amplifier output
5	$V_{OUT–}$	Inverting amplifier output
6	$V_{S–}$	Amplifier negative power-supply input. Note that $V_{S–}$ is tied together on multi-channel devices.
7	$\overline{PD}$	Power down. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
8	V_{IN+}	Noninverting amplifier input

TERMINAL FUNCTIONS: THS4522

TSSOP-16		DESCRIPTION
PIN NO.	NAME	
1	$\overline{PD}_1$	Power down 1. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
2	V_{IN1+}	Noninverting amplifier 1 input
3	$V_{IN1–}$	Inverting amplifier 1 input
4	V_{OCM1}	Common-mode voltage input 1
5	$\overline{PD}_2$	Power down 2. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
6	V_{IN2+}	Noninverting amplifier 2 input
7	$V_{IN2–}$	Inverting amplifier 2 input
8	V_{OCM2}	Common-mode voltage input 2
9	V_{S+2}	Amplifier 2 positive power-supply input
10	V_{OUT2+}	Noninverting amplifier 2 output
11	$V_{OUT2–}$	Inverting amplifier 2 output
12	$V_{S–}$	Negative power-supply input. Note that $V_{S–}$ is tied together on multi-channel devices.
13	V_{S+1}	Amplifier 1 positive power-supply input
14	V_{OUT1+}	Noninverting amplifier 1 output
15	$V_{OUT1–}$	Inverting amplifier 1 output
16	$V_{S–}$	Negative power-supply input. Note that $V_{S–}$ is tied together on multi-channel devices.

THS4524
TSSOP-38 (DBT PACKAGE)
(TOP VIEW)



TERMINAL FUNCTIONS: THS4524

TSSOP-38		DESCRIPTION
PIN NO.	NAME	
1	$\overline{PD}_1$	Power down 1. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
2	V_{IN1+}	Noninverting amplifier 1 input
3	V_{IN1-}	Inverting amplifier 1 input
4	V_{OCM1}	Common-mode voltage input 1
5	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
6	$\overline{PD}_2$	Power down 2. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
7	V_{IN2+}	Noninverting amplifier 2 input
8	V_{IN2-}	Inverting amplifier 2 input
9	V_{OCM2}	Common-mode voltage input 2
10	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
11	$\overline{PD}_3$	Power down 3. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
12	V_{IN3+}	Noninverting amplifier 3 input
13	V_{IN3-}	Inverting amplifier 3 input
14	V_{OCM3}	Common-mode voltage input 3
15	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
16	$\overline{PD}_4$	Power down 4. $\overline{PD}$ = logic low puts channel into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
17	V_{IN4+}	Noninverting amplifier 4 input
18	V_{IN4-}	Inverting amplifier 4 input
19	V_{OCM4}	Common-mode voltage input 4
20	V_{S4+}	Amplifier 4 positive power-supply input
21	V_{OUT4+}	Noninverting amplifier 4 output
22	V_{OUT4-}	Inverting amplifier 4 output
23	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
24	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
25	V_{S3+}	Amplifier 3 positive power-supply input
26	V_{OUT3+}	Noninverting amplifier3 output
27	V_{OUT3-}	Inverting amplifier3 output
28	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
29	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
30	V_{S2+}	Amplifier 2 positive power-supply input
31	V_{OUT2+}	Noninverting amplifier 2 output
32	V_{OUT2-}	Inverting amplifier 2 output
33	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
34	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
35	V_{S1+}	Amplifier 1 positive power-supply input
36	V_{OUT1+}	Noninverting amplifier 1 output
37	V_{OUT1-}	Inverting amplifier 1 output
38	V_{S-}	Negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.

TYPICAL CHARACTERISTICS

Table of Graphs: $V_{S+} - V_{S-} = 3.3$ V

TITLE	FIGURE
Small-Signal Frequency Response	Figure 1
Large-Signal Frequency Response	Figure 2
Large- and Small-Signal Pulse Response	Figure 3
Slew Rate vs V_{OUT} Step	Figure 4
Overdrive Recovery	Figure 5
10-kHz Output Spectrum on AP Analyzer	Figure 6
Harmonic Distortion vs Frequency	Figure 7
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 8
Harmonic Distortion vs Gain at 1 MHz	Figure 9
Harmonic Distortion vs Load at 1 MHz	Figure 10
Harmonic Distortion vs V_{OCM} at 1 MHz	Figure 11
Two-Tone, Second- and Third-Order Intermodulation Distortion vs Frequency	Figure 12
Single-Ended Output Voltage Swing vs Load Resistance	Figure 13
Main Amplifier Differential Output Impedance vs Frequency	Figure 14
Frequency Response vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 15
R_O vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 16
Rejection Ratio vs Frequency	Figure 17
THS4522, THS4524 Crosstalk (Measured Differentially)	Figure 18
Turn-on Time	Figure 19
Turn-off Time	Figure 20
Input-Referred Voltage Noise and Current Noise Spectral Density	Figure 21
Main Amplifier Differential Open-Loop Gain and Phase	Figure 22
Output Balance Error vs Frequency	Figure 23
V_{OCM} Small-Signal Frequency Response	Figure 24
V_{OCM} Large-Signal Frequency Response	Figure 25
V_{OCM} Input Impedance vs Frequency	Figure 26

Table of Graphs: $V_{S+} - V_{S-} = 5$ V

TITLE	FIGURE
Small-Signal Frequency Response	Figure 27
Large-Signal Frequency Response	Figure 28
Large- and Small-Signal Pulse Response	Figure 29
Slew Rate vs V_{OUT} Step	Figure 30
Overdrive Recovery	Figure 31
10-kHz Output Spectrum on AP Analyzer	Figure 32
Harmonic Distortion vs Frequency	Figure 33
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 34
Harmonic Distortion vs Gain at 1 MHz	Figure 35
Harmonic Distortion vs Load at 1 MHz	Figure 36
Harmonic Distortion vs V_{OCM} at 1 MHz	Figure 37
Two-Tone, Second- and Third-Order Intermodulation Distortion vs Frequency	Figure 38
Single-Ended Output Voltage Swing vs Load Resistance	Figure 39
Main Amplifier Differential Output Impedance vs Frequency	Figure 40
Frequency Response vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 41
R_O vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 42
Rejection Ratio vs Frequency	Figure 43
THS4522, THS4524 Crosstalk (Measured Differentially)	Figure 44
Turn-on Time	Figure 45
Turn-off Time	Figure 46
Input-Referred Voltage Noise and Current Noise Spectral Density	Figure 47
Main Amplifier Differential Open-Loop Gain and Phase	Figure 48
Output Balance Error vs Frequency	Figure 49
V_{OCM} Small-Signal Frequency Response	Figure 50
V_{OCM} Large-Signal Frequency Response	Figure 51
V_{OCM} Input Impedance vs Frequency	Figure 52

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

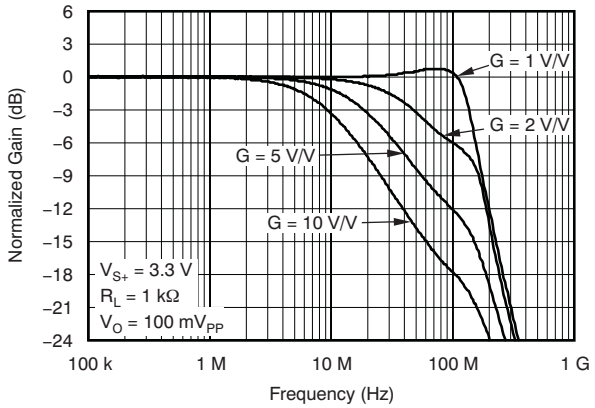


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

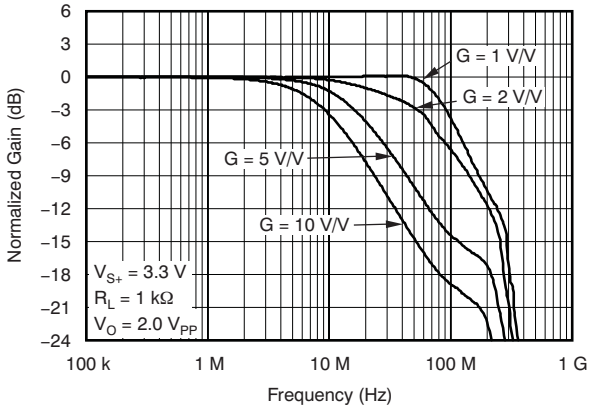


Figure 2.

LARGE- AND SMALL-SIGNAL PULSE RESPONSE

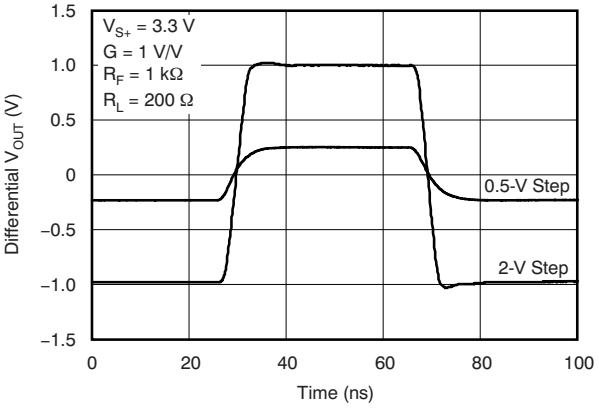


Figure 3.

SLEW RATE vs V_{OUT}

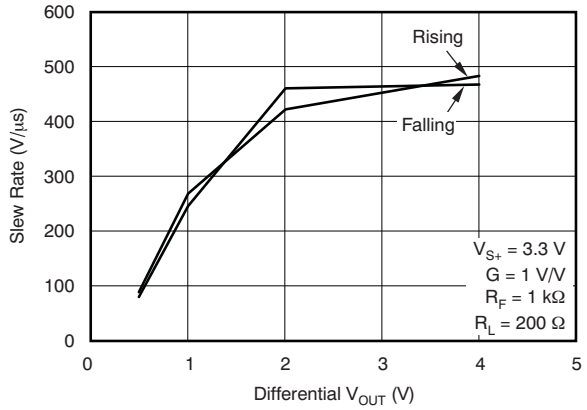


Figure 4.

OVERDRIVE RECOVERY

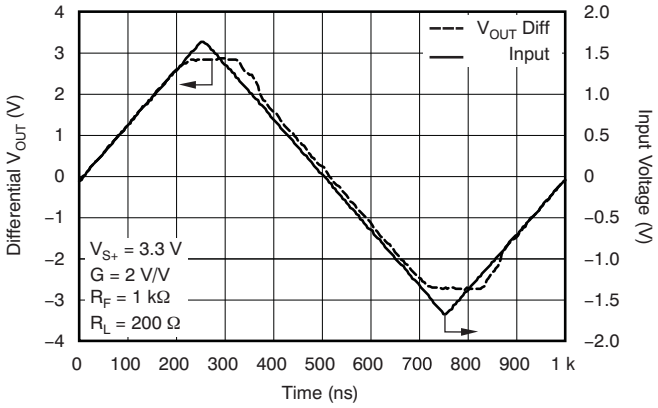


Figure 5.

10-kHz OUTPUT SPECTRUM ON AP ANALYZER

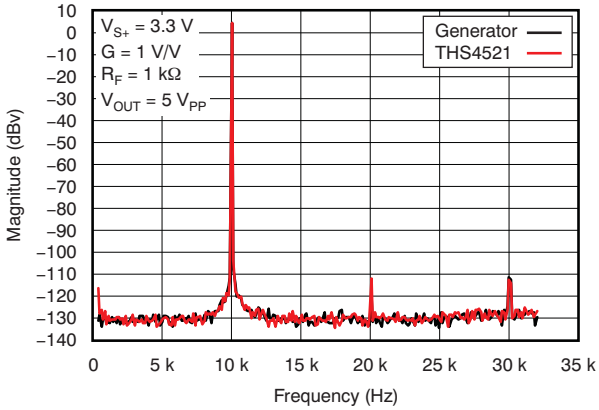


Figure 6.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

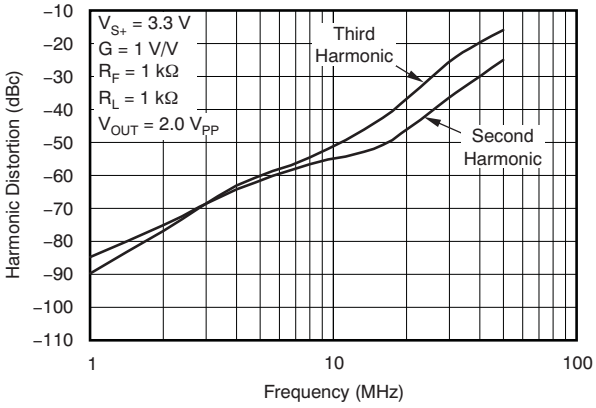


Figure 7.

HARMONIC DISTORTION vs V_{OUT} AT 1 MHZ

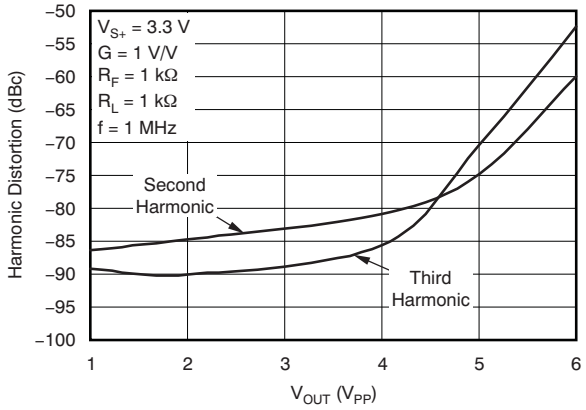


Figure 8.

HARMONIC DISTORTION vs GAIN AT 1 MHZ

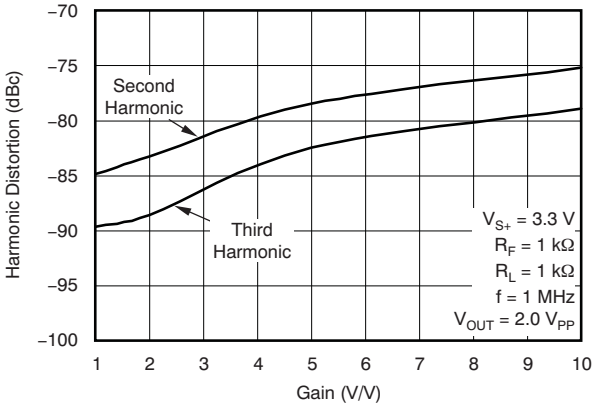


Figure 9.

HARMONIC DISTORTION vs LOAD AT 1 MHZ

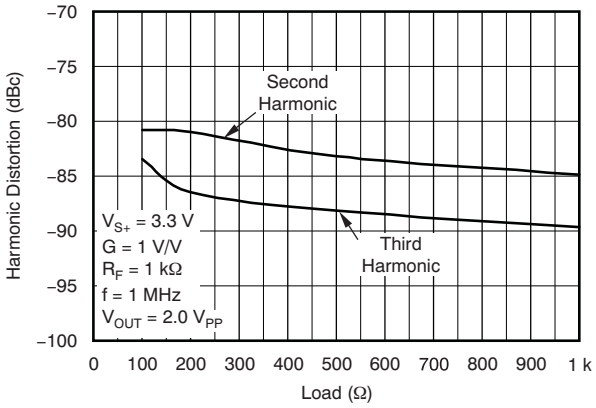


Figure 10.

HARMONIC DISTORTION vs V_{OCM} AT 1 MHZ

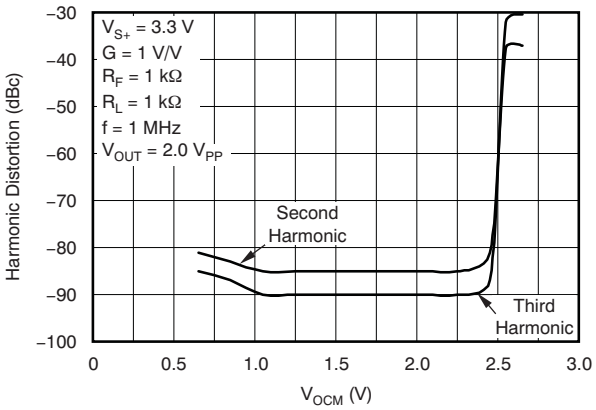


Figure 11.

TWO-TONE INTERMODULATION DISTORTION vs FREQUENCY

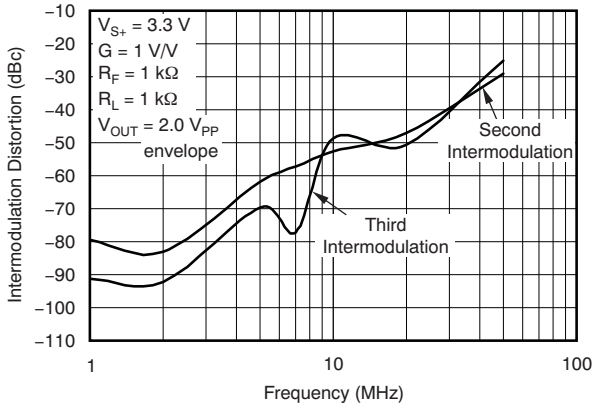


Figure 12.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SINGLE-ENDED OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

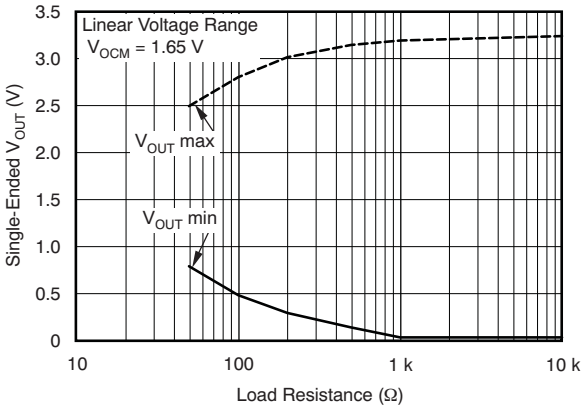


Figure 13.

MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

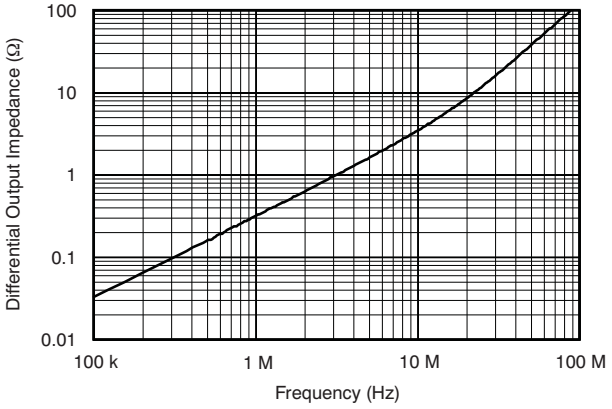


Figure 14.

FREQUENCY RESPONSE vs C_{LOAD} R_{LOAD} = 1 kΩ

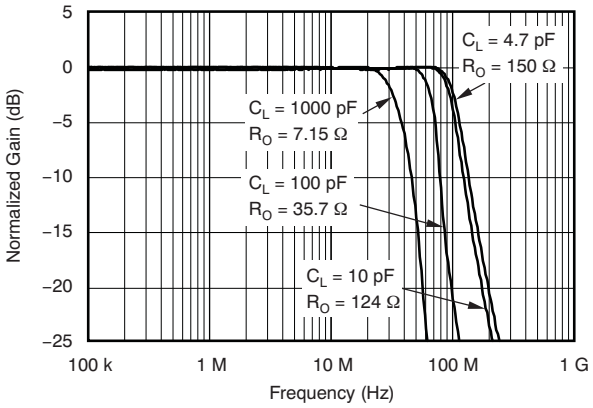


Figure 15.

R_O vs C_{LOAD} R_{LOAD} = 1 kΩ

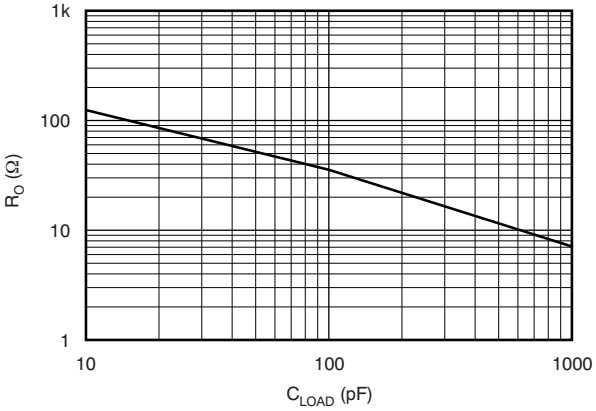


Figure 16.

REJECTION RATIO vs FREQUENCY

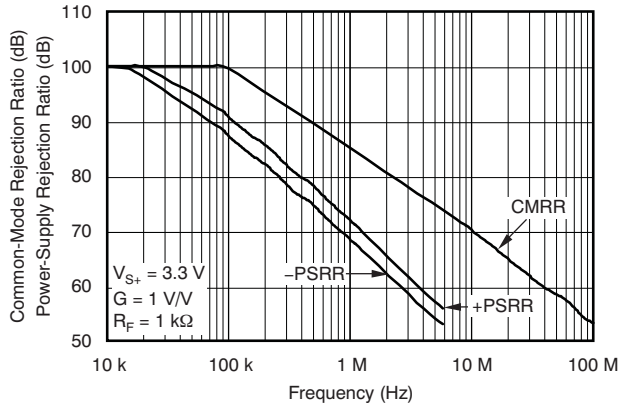


Figure 17.

THS4522, THS4524 CROSSTALK (MEASURED DIFFERENTIALLY)

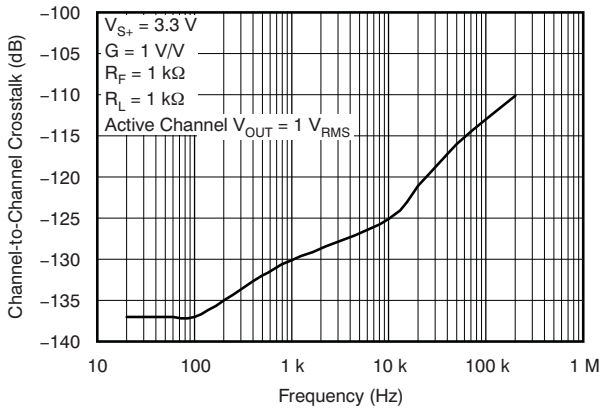


Figure 18.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

TURN-ON TIME

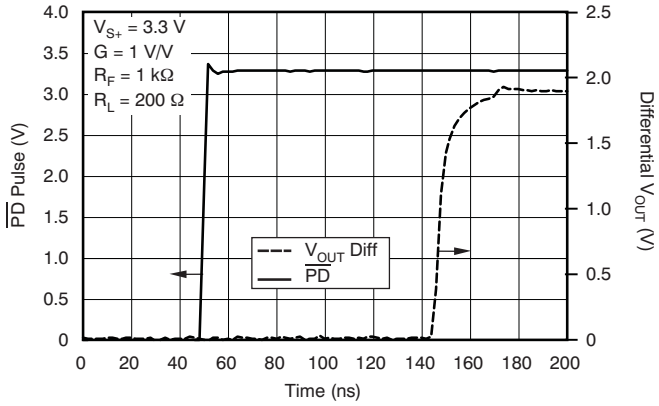


Figure 19.

TURN-OFF TIME

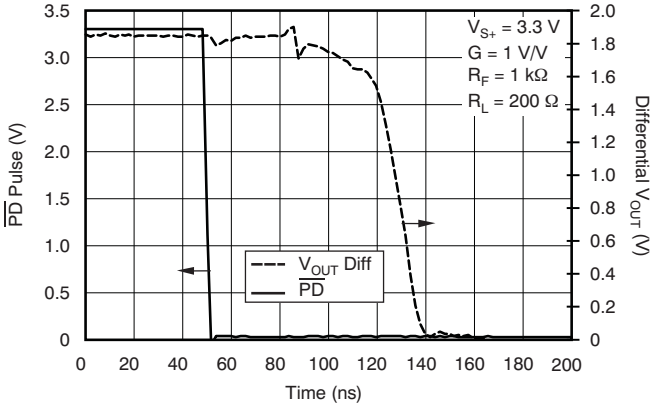


Figure 20.

INPUT-REFERRED VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY

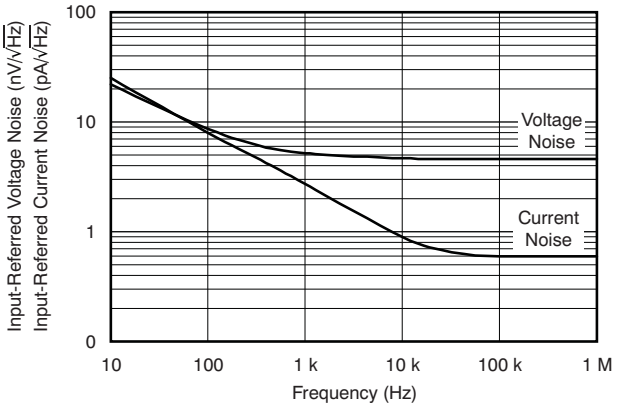


Figure 21.

MAIN AMPLIFIER DIFFERENTIAL OPEN-LOOP GAIN AND PHASE

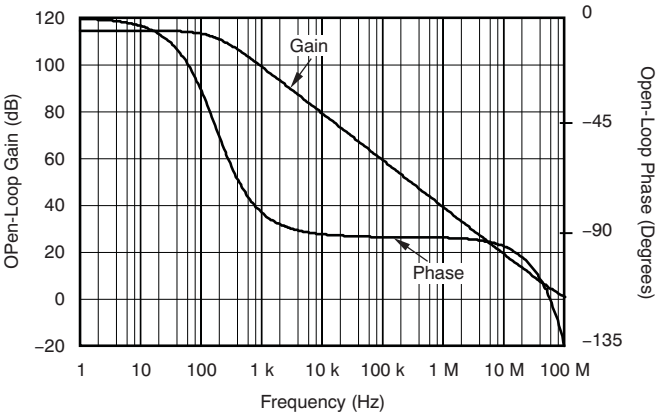


Figure 22.

OUTPUT BALANCE ERROR vs FREQUENCY

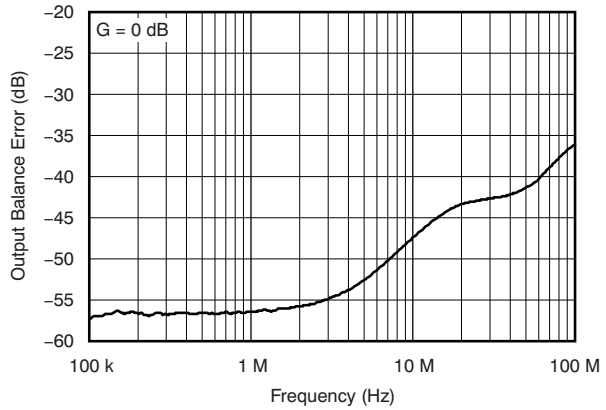


Figure 23.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

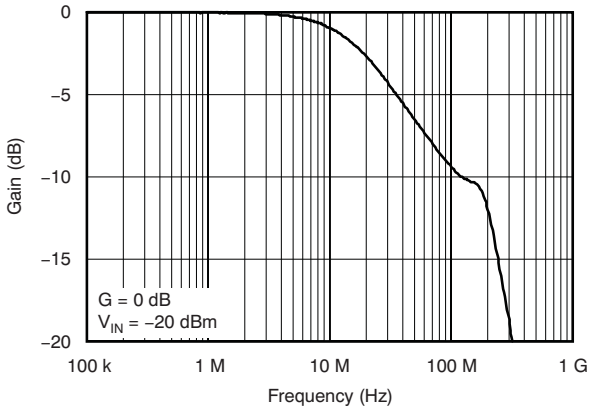


Figure 24.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

V_{OCM} LARGE-SIGNAL PULSE RESPONSE

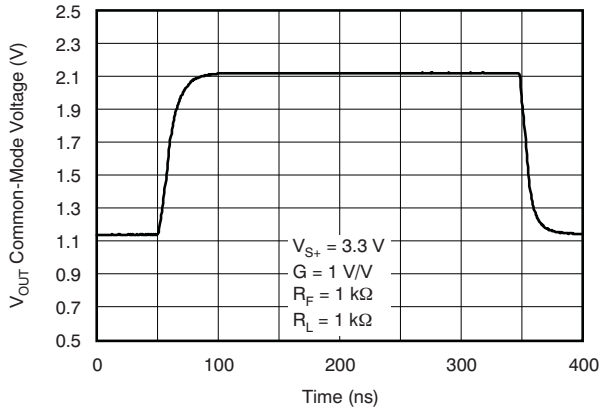


Figure 25.

V_{OCM} INPUT IMPEDANCE vs FREQUENCY

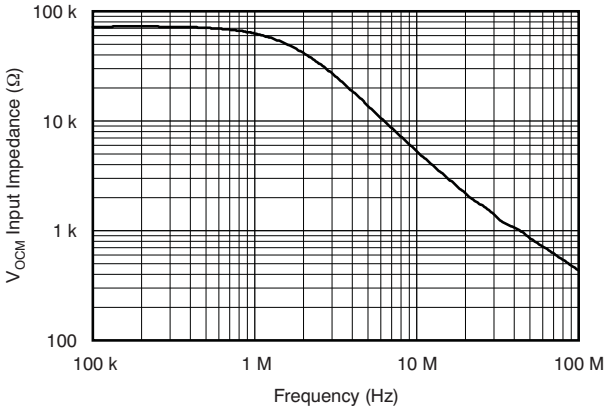


Figure 26.

TYPICAL CHARACTERISTICS: 5 V

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

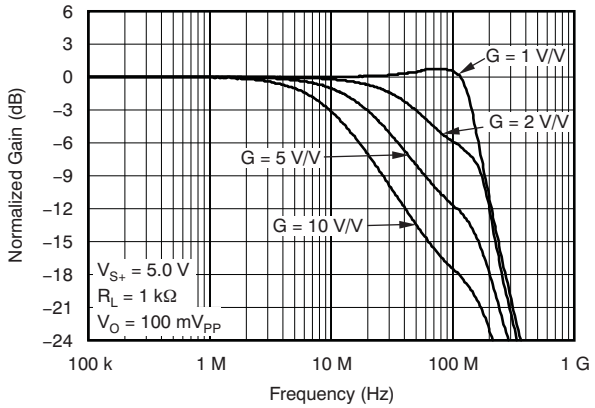


Figure 27.

LARGE-SIGNAL FREQUENCY RESPONSE

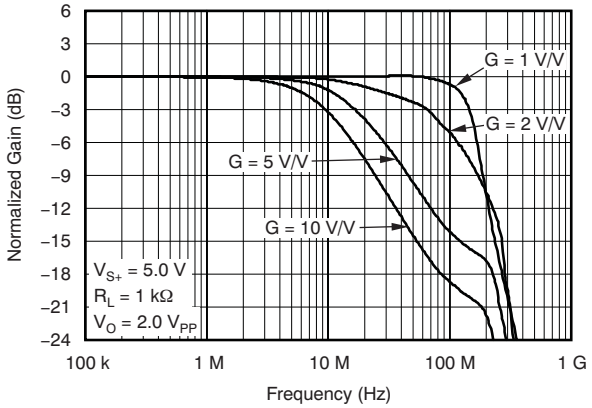


Figure 28.

LARGE- AND SMALL-SIGNAL PULSE RESPONSE

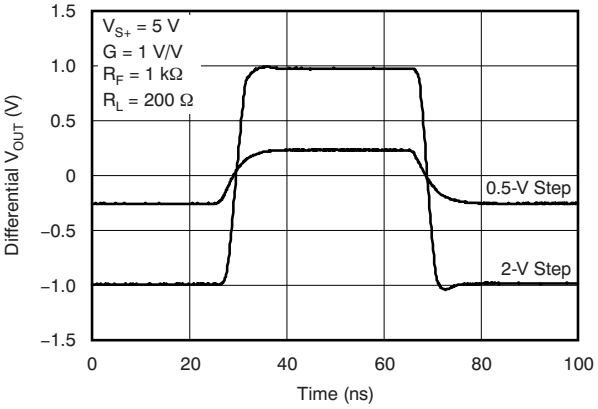


Figure 29.

SLEW RATE vs V_{OUT}

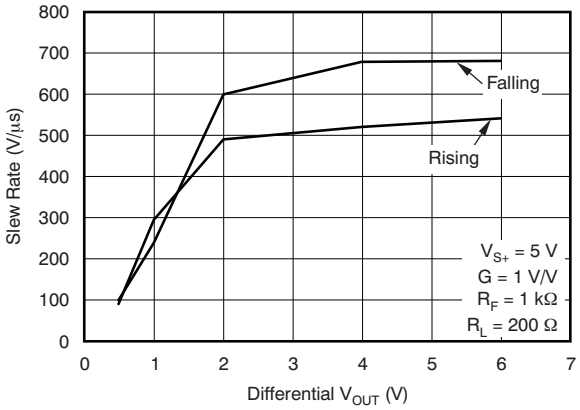


Figure 30.

OVERDRIVE RECOVERY

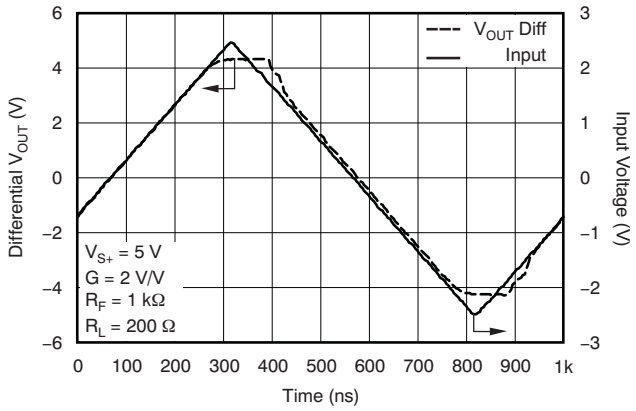


Figure 31.

10-kHz OUTPUT SPECTRUM ON AP ANALYZER AT V_{OUT} = 8 V_{PP}

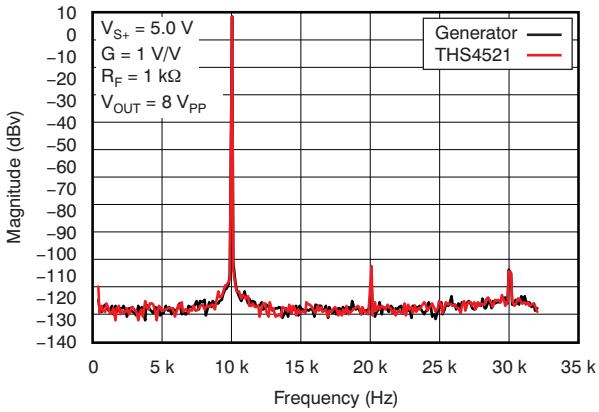


Figure 32.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

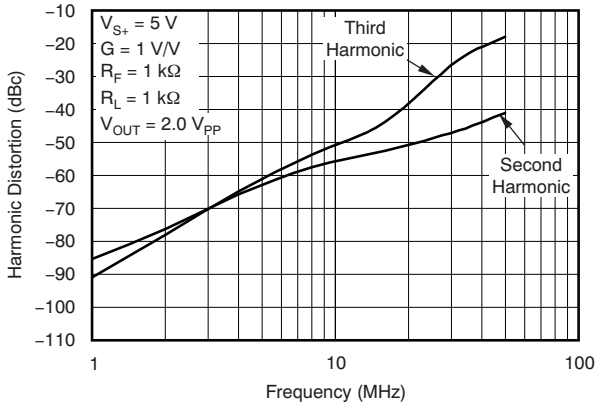


Figure 33.

HARMONIC DISTORTION vs V_{OUT} AT 1 MHZ

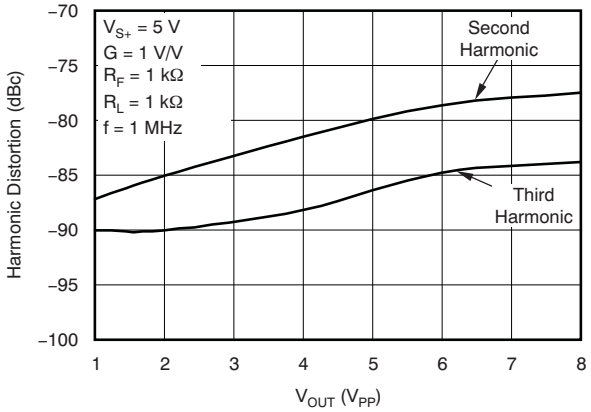


Figure 34.

HARMONIC DISTORTION vs GAIN AT 1 MHZ

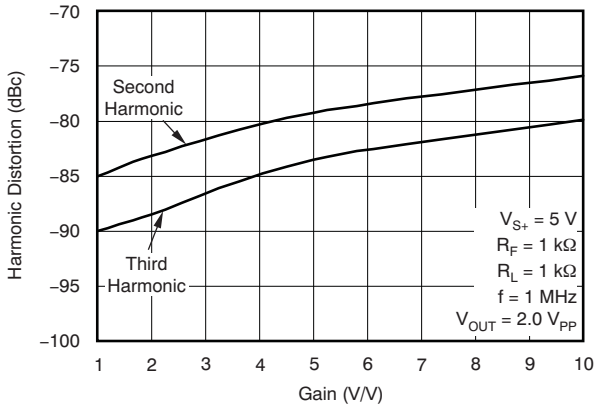


Figure 35.

HARMONIC DISTORTION vs LOAD AT 1 MHZ

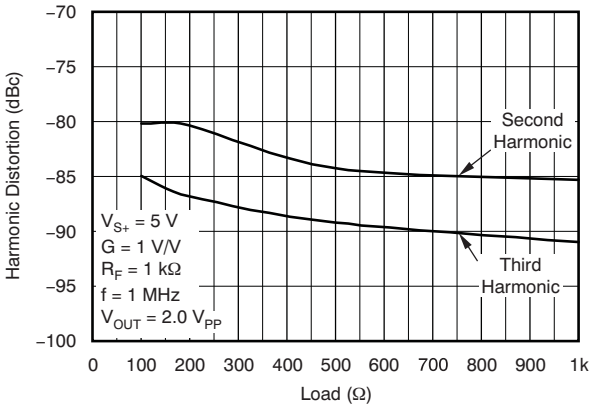


Figure 36.

HARMONIC DISTORTION vs V_{OCM} AT 1 MHZ

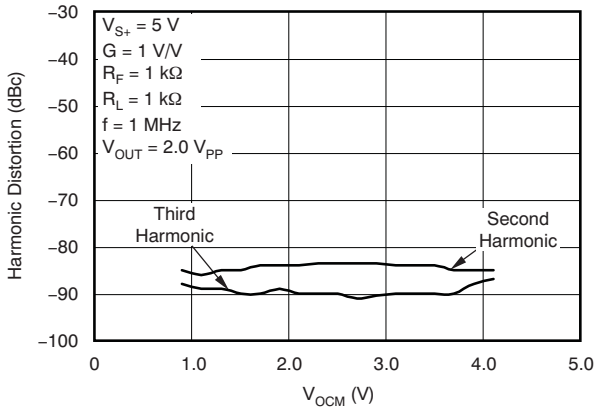


Figure 37.

TWO-TONE INTERMODULATION DISTORTION vs FREQUENCY

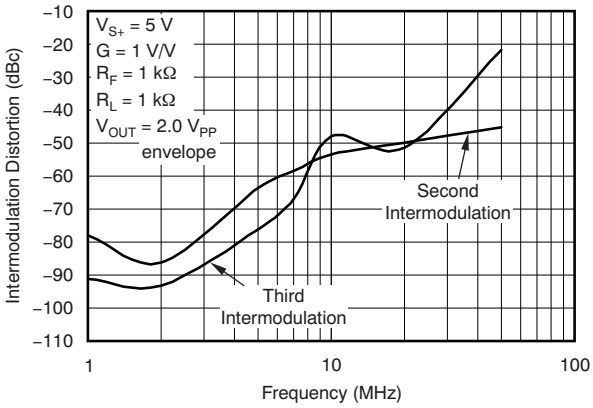


Figure 38.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

SINGLE-ENDED OUTPUT VOLTAGE SWING vs DIFFERENTIAL LOAD RESISTANCE

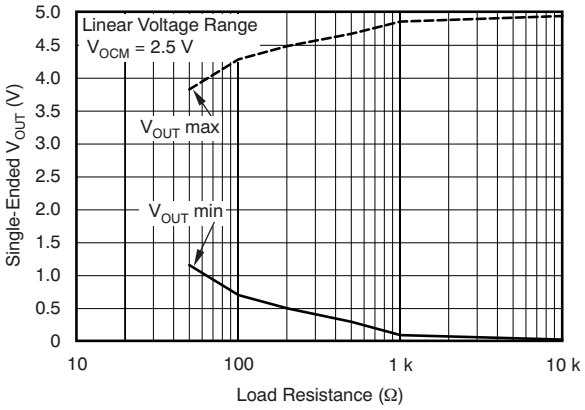


Figure 39.

MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

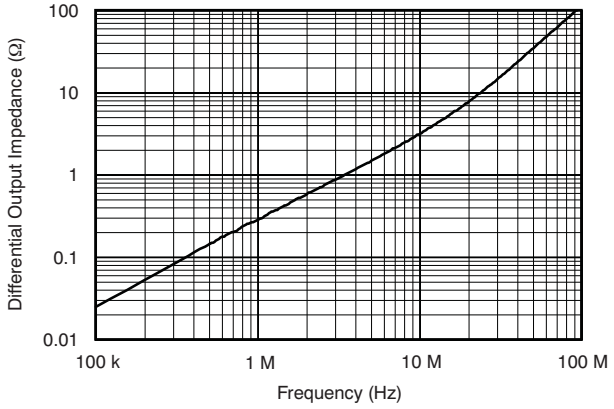


Figure 40.

FREQUENCY RESPONSE vs C_{LOAD} R_{LOAD} = 1 kΩ

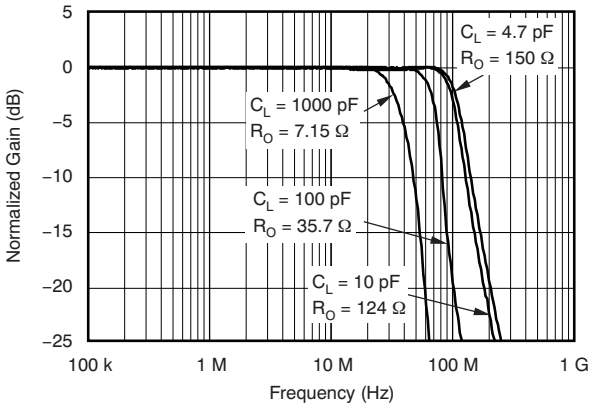


Figure 41.

R_O vs C_{LOAD} R_{LOAD} = 1 kΩ

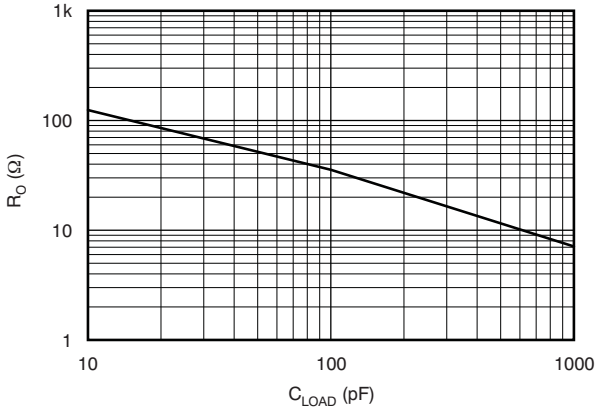


Figure 42.

REJECTION RATIO vs FREQUENCY

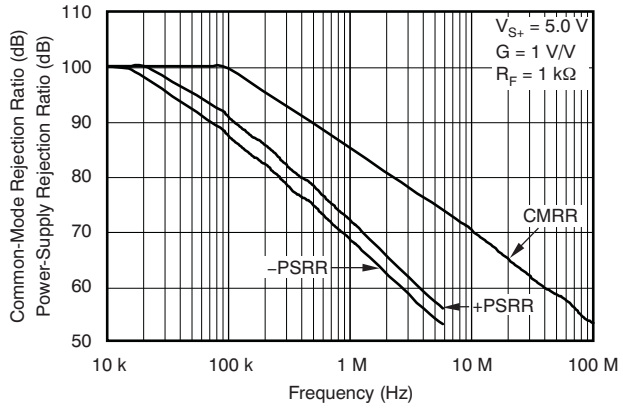


Figure 43.

THS4522, THS4524 CROSSTALK (MEASURED DIFFERENTIALLY)

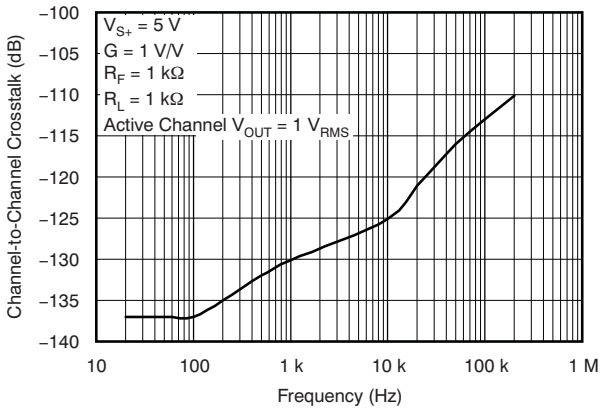


Figure 44.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

TURN-ON TIME

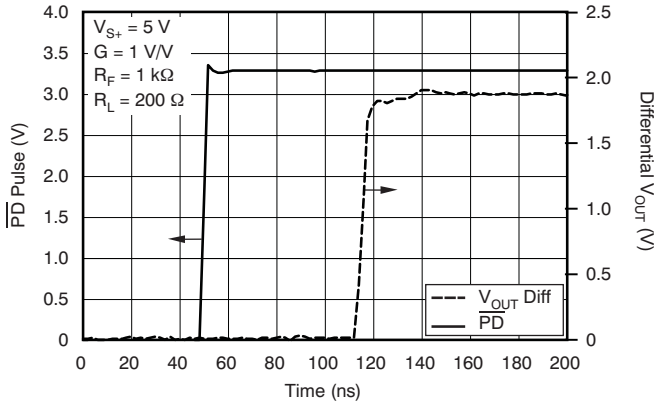


Figure 45.

TURN-OFF TIME

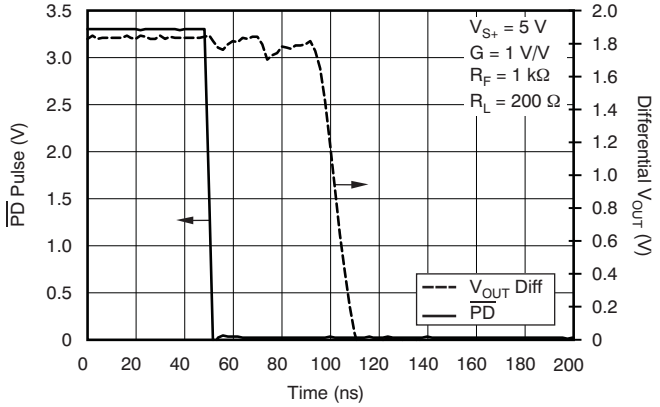


Figure 46.

INPUT-REFERRED VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY

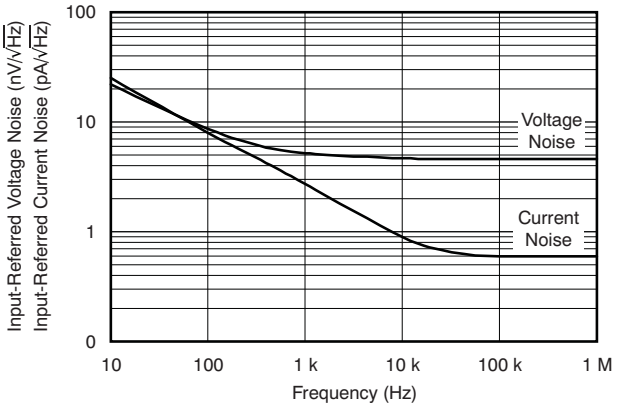


Figure 47.

MAIN AMPLIFIER DIFFERENTIAL OPEN-LOOP GAIN AND PHASE

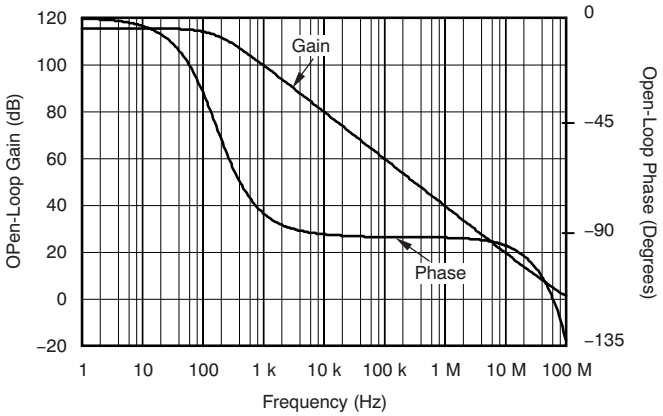


Figure 48.

OUTPUT BALANCE ERROR vs FREQUENCY

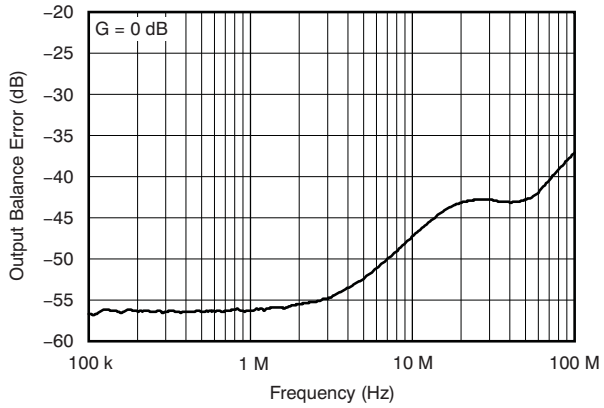


Figure 49.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

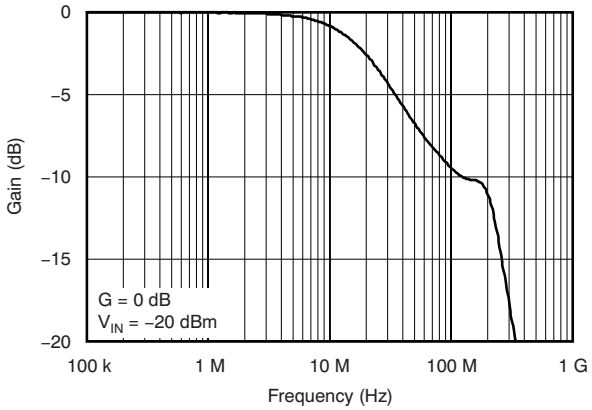


Figure 50.

TYPICAL CHARACTERISTICS: 5 V (continued)

At V_{S+} = +5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_F = 1 kΩ, R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

V_{OCM} LARGE-SIGNAL PULSE RESPONSE

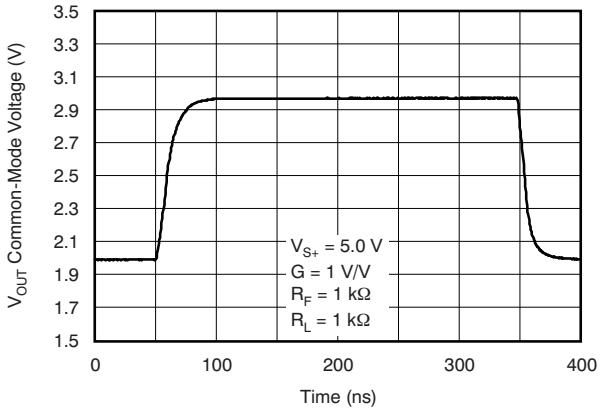


Figure 51.

V_{OCM} INPUT IMPEDANCE vs FREQUENCY

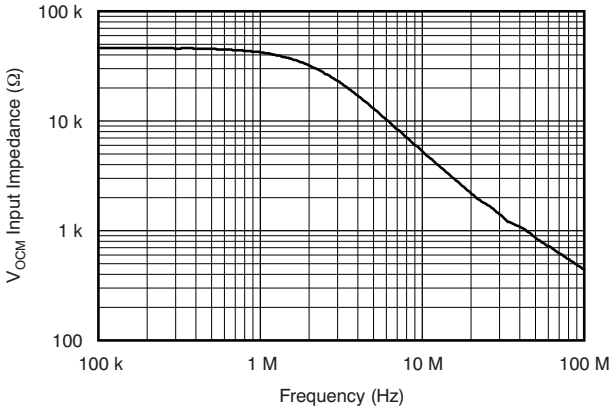


Figure 52.

TEST CIRCUITS

Overview

The THS4521, THS4522, and THS4524 family is tested with the test circuits shown in this section; all circuits are built using the available THS4521 evaluation module (EVM). For simplicity, power-supply decoupling is not shown; see the layout in the *Applications* section for recommendations. Depending on the test conditions, component values change in accordance with Table 1 and Table 2, or as otherwise noted. In some cases the signal generators used are ac-coupled and in others they dc-coupled 50-Ω sources. To balance the amplifier when ac-coupled, a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input; when dc-coupled, only the 49.9-Ω resistor to ground is added across R_{IT}. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated in a single-supply configuration as described in the *Applications* section with no impact on performance. Also, for most of the tests, except as noted, the devices are tested with single-ended inputs and a transformer on the output to convert the differential output to single-ended because common lab test equipment has single-ended inputs and outputs. Similar or better performance can be expected with differential inputs and outputs.

As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The ***Atten*** column in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output (as shown in Figure 54), the signal sees slightly more loss because of transformer and line loss; these numbers are approximate.

Table 1. Gain Component Values for Single-Ended Input(1)

Gain	R_F	R_G	R_{IT}
1 V/V	1 kΩ	1 kΩ	52.3 Ω
2 V/V	1 kΩ	487 Ω	53.6 Ω
5 V/V	1 kΩ	187 Ω	59.0 Ω
10 V/V	1 kΩ	86.6 Ω	69.8 Ω

1. Gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 2. Load Component Values For 1:1 Differential to Single-Ended Output Transformer(1)

R_L	R_O	R_{OT}	Atten
100 Ω	24.9 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB

1. Total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Frequency Response

The circuit shown in Figure 53 is used to measure the frequency response of the circuit.

An HP network analyzer is used as the signal source and the measurement device. The output impedance of the HP network analyzer is is dc-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor to ground is inserted across R_{IT} on the alternate input.

The output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB because of the voltage divider on the output.

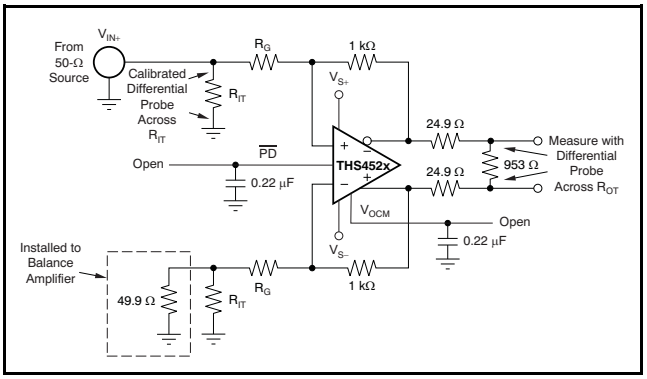


Figure 53. Frequency Response Test Circuit

Distortion

The circuit shown in Figure 54 is used to measure harmonic and intermodulation distortion of the amplifier.

An HP signal generator is used as the signal source and the output is measured with a Rhode and Schwarz spectrum analyzer. The output impedance of the HP signal generator is ac-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1–1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

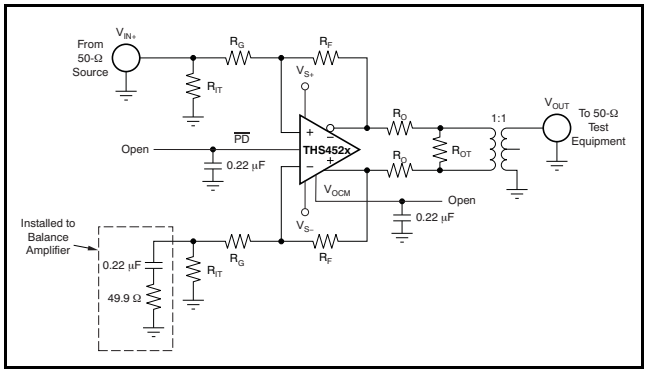


Figure 54. Distortion Test Circuit

Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Turn-Off Time

The circuit shown in Figure 55 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and ampliifer turn-on/turn-off time. Turn-on and turn-off time are measured with the same circuit modified for 50-Ω input impedance on the $\overline{PD}$ input by replacing the 0.22-μF capacitor with a 49.9-Ω resistor. For output impedance, the signal is injected at V_{OUT} with V_{IN} open; the drop across the 2x 49.9-Ω resistors is then used to calculate the impedance seen looking into the amplifier output.

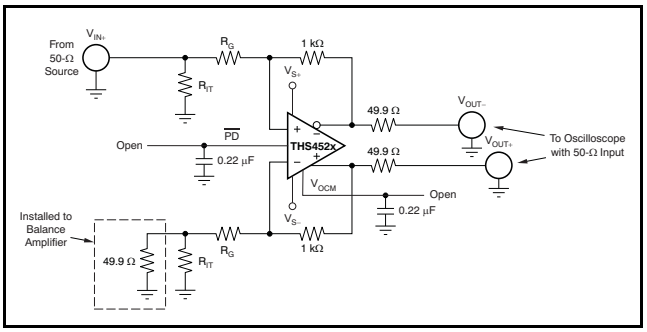


Figure 55. Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Turn-Off Test Circuit

Common-Mode and Power-Supply Rejection

The circuit shown in Figure 56 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input. Figure 57 is used to measure the PSRR of V_{S+} and V_{S-}. The power supply under test is applied to the network analyzer dc offset input. For both CMRR and PSRR, the output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB as a result of the voltage divider on the output. For these tests, the resistors are matched for best results.

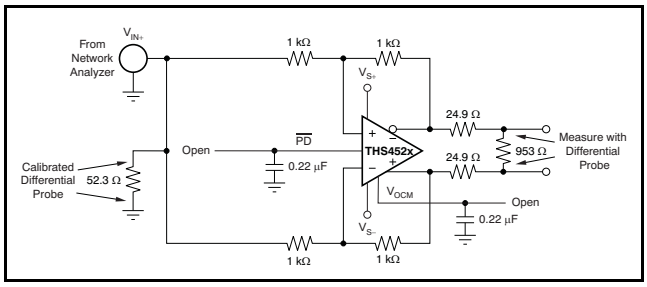


Figure 56. CMRR Test Circuit

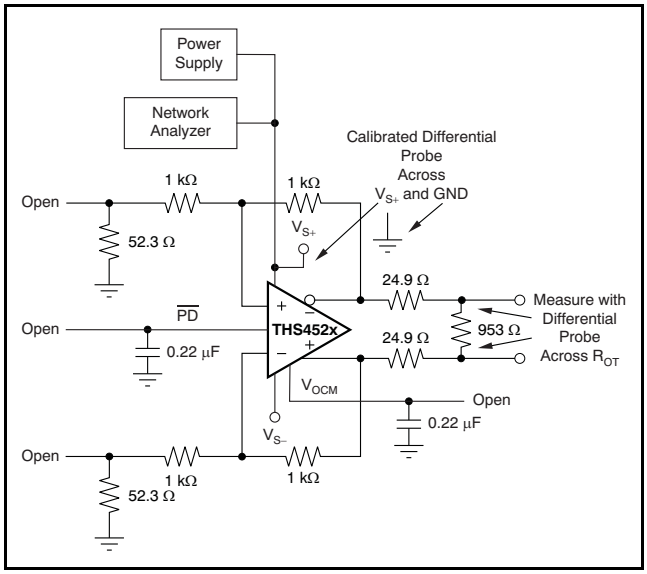


Figure 57. PSRR Test Circuit

V_{OCM} Input

The circuit illustrated in Figure 58 is used to measure the frequency response and input impedance of the V_{OCM} input. Frequency response is measured using a Tektronix high-impedance differential probe, with R_{CM} = 0 Ω at the common point of V_{OUT+} and V_{OUT-}, formed at the summing junction of the two matched 499-Ω resistors, with respect to ground. The input impedance is measured using a Tektronix high-impedance differential probe at the V_{OCM} input with R_{CM} = 10 kΩ and the drop across the 10-kΩ resistor is used to calculate the impedance seen looking into the amplifier V_{OCM} input.

The circuit shown in Figure 59 measures the transient response and slew rate of the V_{OCM} input. A 1-V step input is applied to the V_{OCM} input and the output is measured using a 50-Ω oscilloscope input referenced back to the amplifier output.

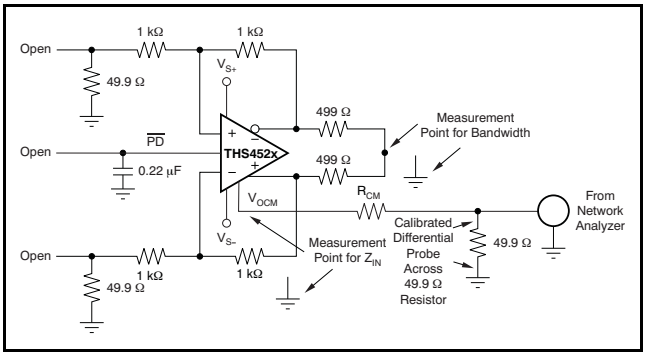


Figure 58. V_{OCM} Input Test Circuit

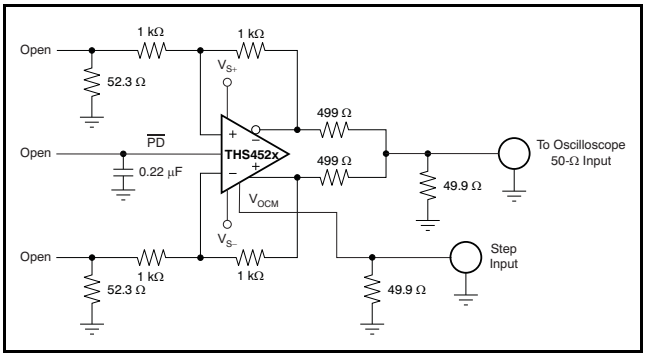


Figure 59. V_{OCM} Transient Response and Slew Rate Test Circuit

APPLICATION INFORMATION

The following circuits show application information for the THS4521, THS4522, and THS4524 family. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; see the *EVM and Layout Recommendations* section for suggested guidelines. For more details on the use and operation of fully differential op amps, refer to the Application Report *Fully-Differential Amplifiers* (SLOA054), available for download from the TI web site at www.ti.com.

Differential Input to Differential Output Amplifier

The THS4521, THS4522, and THS4524 family are fully-differential operational amplifiers that can be used to amplify differential input signals to differential output signals. Figure 60 shows a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is set by R_F divided by R_G.

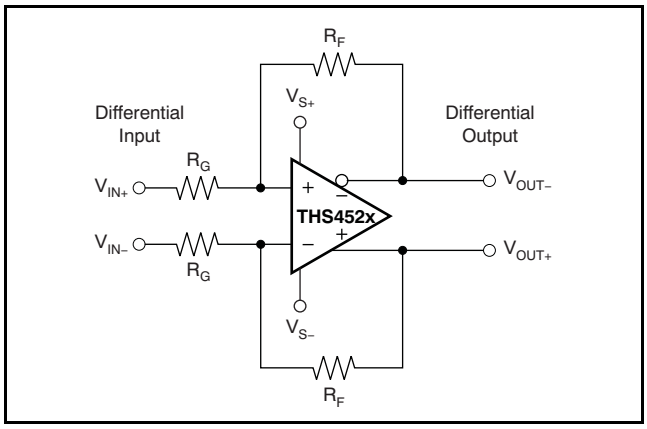


Figure 60. Differential Input to Differential Output Amplifier

Single-Ended Input to Differential Output Amplifier

The THS4521, THS4522, and THS4524 family can also amplify and convert single-ended input signals to differential output signals. Figure 61 illustrates a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is again set by R_F divided by R_G.

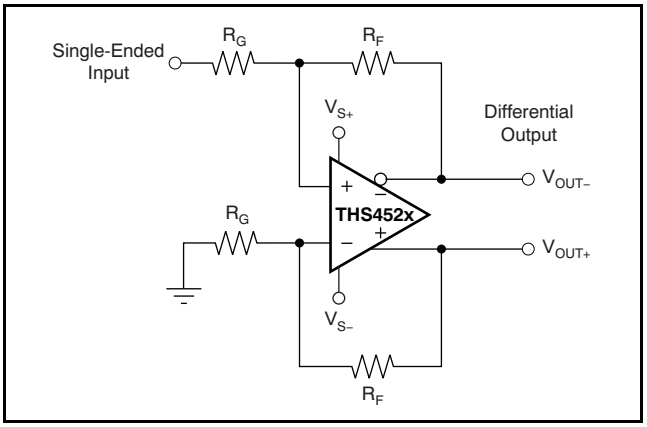


Figure 61. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential op amp is the voltage at the **+** and **–** input pins of the device.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore, finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$\left(V_{OUT+} \times \frac{R_G}{R_G + R_F}\right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F}\right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}. As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-model voltage is set by the voltage at the V_{OCM} pin. The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source.

Figure 62 represents the V_{OCM} input. The internal V_{OCM} circuit has typically 23 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. A 0.22-µF bypass capacitor is recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula in Equation 2:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where:

- V_{OCM} is the voltage applied to the V_{OCM} pin

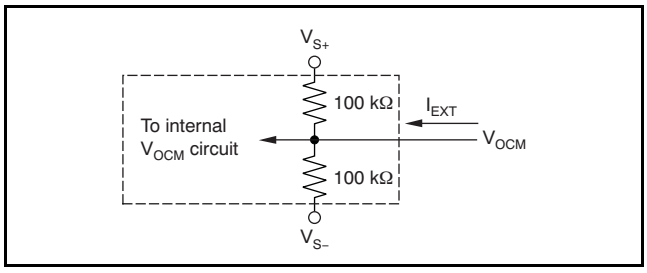


Figure 62. V_{OCM} Input Circuit

Typical Performance Variation with Supply Voltage

The THS4521, THS4522, and THS4524 family of devices provide excellent performance across the specified power-supply range of 2.5 V to 5.5 V with only minor variations. The input and output voltage compliance ranges track with the power supply in nearly a 1:1 correlation. Other changes can be observed in slew rate, output current drive, open-loop gain, bandwidth, and distortion. Table 3 shows the typical variation to be expected in these key performance parameters.

Single-Supply Operation

To facilitate testing with common lab equipment, the THS4521EVM allows for split-supply operation; most of the characterization data presented in this data sheet is measured using split-supply power inputs. The device can easily be used with a single-supply power input without degrading performance.

Figure 63 shows a dc-coupled single-supply circuit with single-ended inputs. This circuit can also be applied to differential input sources.

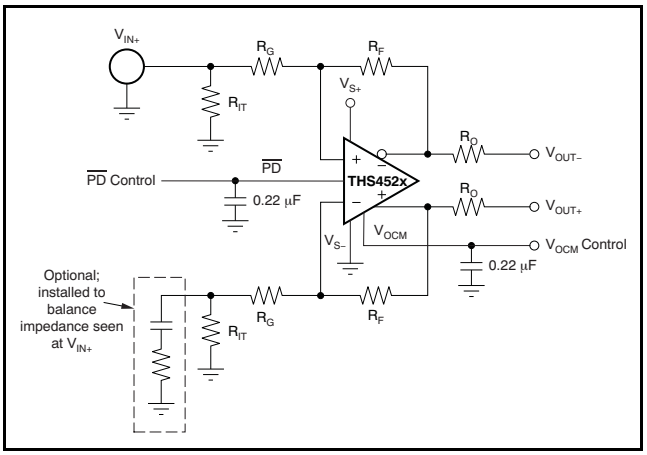


Figure 63. THS4521 DC-Coupled Single-Supply with Single-Ended Inputs

The input common-mode voltage range of the THS4521, THS4522, and THS4524 family is designed to include the negative supply voltage. in the circuit shown in Figure 63, the signal source is referenced to ground. V_{OCM} is set by an external control source or, if left unconnected, the internal circuit defaults to midsupply. Together with the input impedance of the amplifier circuit, R_{IT} provides input termination, which is also referenced to ground.

Note that R_{IT} and optional matching components are added to the alternate input to balance the impedance at signal input.

Table 3. Typical Performance Variation versus Power-Supply Voltage

PARAMETER	V_S = 5 V	V_S = 3.3 V	V_S = 2.5 V
–3-dB Small-signal bandwidth	145 MHz	135 MHz	125 MHz
Slew rate (2-V step)	490 V/µs	420 V/µs	210 V/µs
Harmonic distortion at 1 MHz, 2 V_{PP}, R_L = 1 kΩ			
harmonic	–85 dBc	–85 dBc	–84 dBc
harmonic	–91 dBc	–90 dBc	–88 dBc
Open-loop gain	119 dB	116 dB	115 dB
Linear output current drive	55 mA	35 mA	24 mA

Low-Power Applications and the Effects of Resistor Values on Bandwidth

For low-power operation, it may be necessary to increase the gain setting resistors values to limit current consumption and not load the source. Using larger value resistors lowers the bandwidth of the THS4521, THS4522, and THS4524 family as a result of the interactions between the resistors, the device parasitic capacitance, and printed circuit board (PCB) parasitic capacitance. Figure 64 shows the small-signal frequency response with 1-kΩ, 10-kΩ, and 100-kΩ resistors for R_F, R_G, and R_L (impedance is assumed to typically increase for all three resistors in low-power applications).

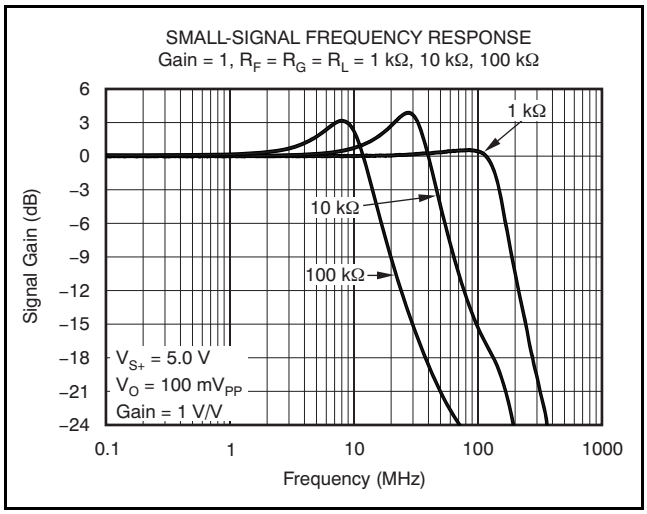


Figure 64. THS4521 Frequency Response with Various Gain Setting and Load Resistor Values

Frequency Response Variation due to Package Options

Users can see variations in the small-signal (V_{OUT} = 100 mV_{PP}) frequency response between the available package options for the THS4521, THS4522, and THS4524 family as a result of parasitic elements associated with each package and board layout changes. Figure 65 shows the variance measured in the lab; this variance is to be expected even when using a good layout.

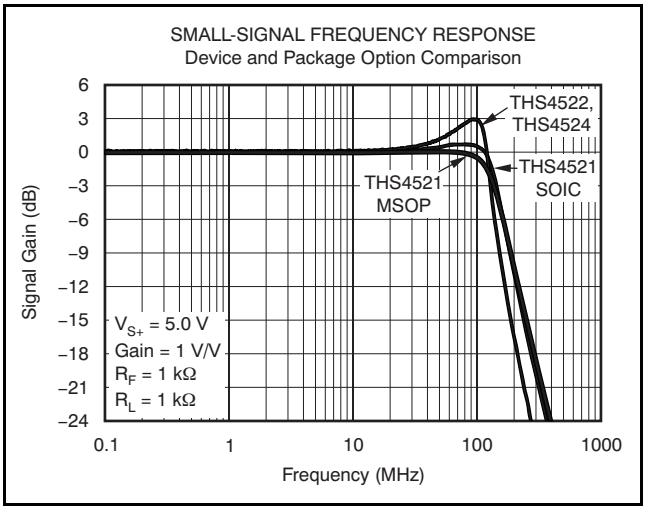


Figure 65. Small-Signal Frequency Response: Package Variations

Driving Capacitive Loads

The THS4521, THS4522, and THS4524 family is designed for a nominal capacitive load of 1 pF on each output to ground. When driving capacitive loads greater than 1 pF, it is recommended to use small resistors (R_O) in series with the output, placed as close to the device as possible. Without R_O, capacitance on the output interacts with the output impedance of the amplifier and causes phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction in phase margin results in frequency response peaking; overshoot, undershoot, and/or ringing when a step or square-wave signal is applied; and may lead to instability or oscillation. Inserting R_O isolates the phase shift from the loop gain path and restores the phase margin, but it also limits bandwidth. Figure 66 shows the recommended values of R_O versus capacitive loads (C_L), and Figure 67 shows an illustration of the frequency response with various values.

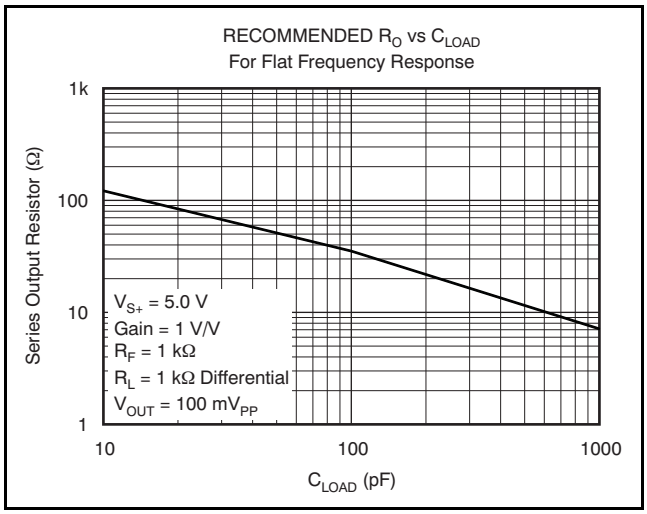


Figure 66. Recommended Series Output Resistor versus Capacitive Load for Flat Frequency Response, with R_{LOAD} = 1 kΩ

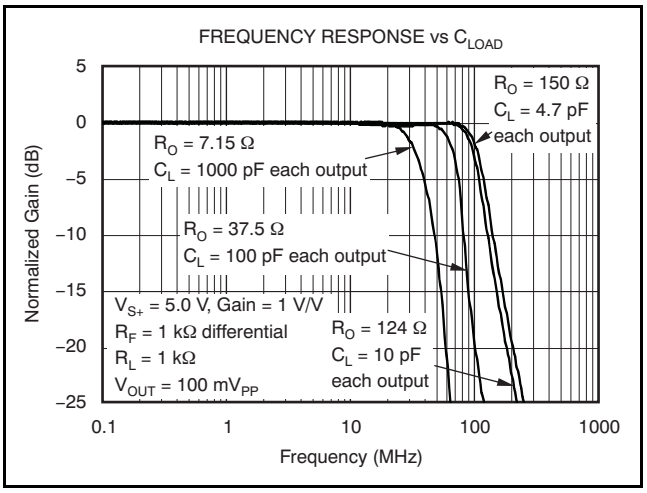


Figure 67. Frequency Response for Various R_O and C_L Values, with R_{LOAD} = 1 kΩ

Audio Performance

The THS4521, THS4522, and THS4524 family provide excellent audio performance with very low quiescent power. To show performance in the audio band, the device was tested with a SYS-2722 audio analyzer from Audio Precision. THD+N and FFT tests were performed at 1-V_{RMS} output voltage. Performance is the same on both 3.3-V and 5-V supplies. Figure 68 shows the test circuit used; see Figure 69 and Figure 70 for the performance of the analyzer using internal loopback mode (generator) together with the THS4521.

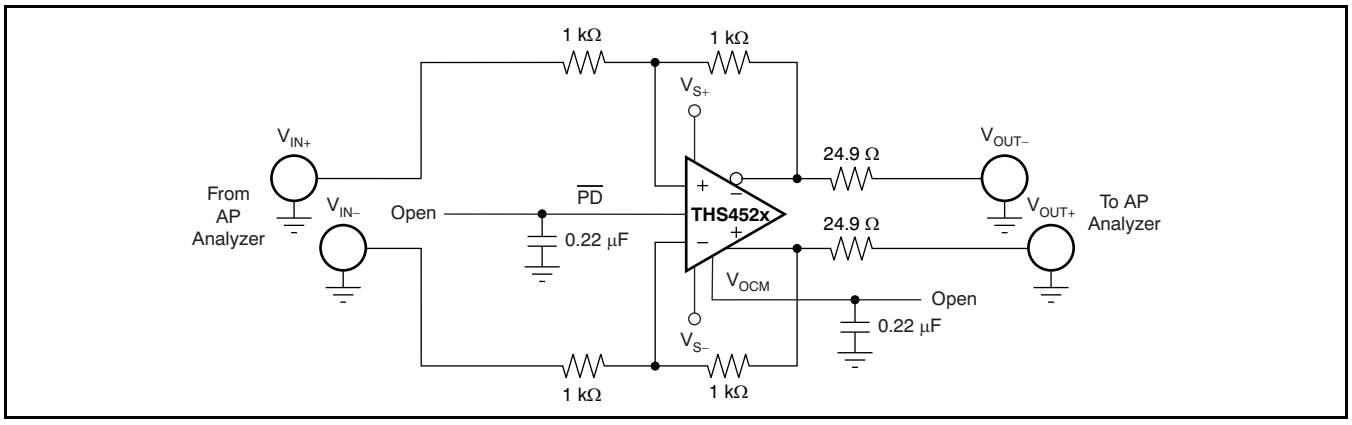


Figure 68. THS4521 AP Analyzer Test Circuit

Note that the harmonic distortion performance is very close to the same with and without the device meaning the THS4521 performance is actually much better than can be directly measured by this meathod. The actual device performance can be estimated by placing the device in a large noise gain and using the reduction in loop gain correction. The THS4521 is placed in a noise gain of 101 by adding a 10-Ω resistor directly across the input terminals of the circuit shown in Figure 68. This test was performed using the AP instrument as both the signal source and the analyzer. The second-order harmonic distortion at 1 kHz is estimated to be –122 dBc with V_O = 1V_{RMS}; third-order harmonic distortion is estimated to be –141 dBc. The third-order harmonic distortion result matches exactly with design simulations, but the second-order harmonic distortion is about 10 dB worse. This result is not unexpected because second-order harmonic distortion performance with a differential signal depends heavily on cancellation as a result of the differential nature of the signal, which depends on board layout, bypass capacitors, external cabling, and so forth. Note that the circuit of Figure 68 is also used to measure crosstalk between channels.

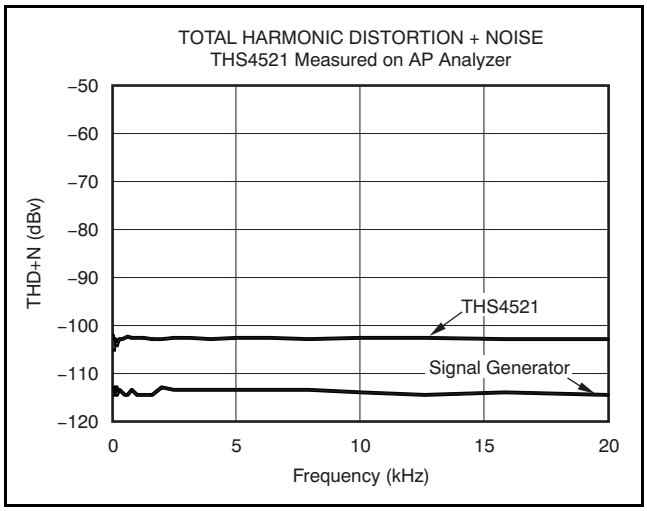


Figure 69. THS4521 1-V_{RMS} 20-Hz to 20-kHz THD+N

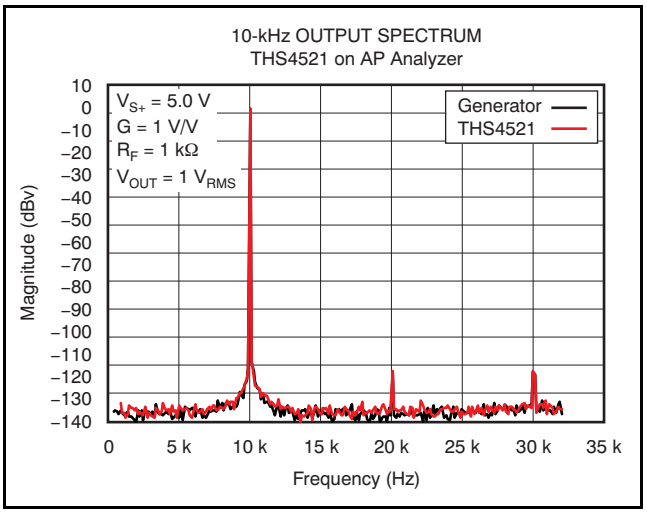


Figure 70. THS4521 1-V_{RMS} 10-kHz FFT Plot

The THS4521 shows even better THD+N performance when driving higher amplitude output, such as 5 V_{PP} that is more typical when driving an ADC. To show performance with an extended frequency range, higher gain, and higher amplitude, the device was tested with 5 V_{PP} up to 80 kHz with the AP. Figure 71 shows the resulting THD+N graph with no weighting.

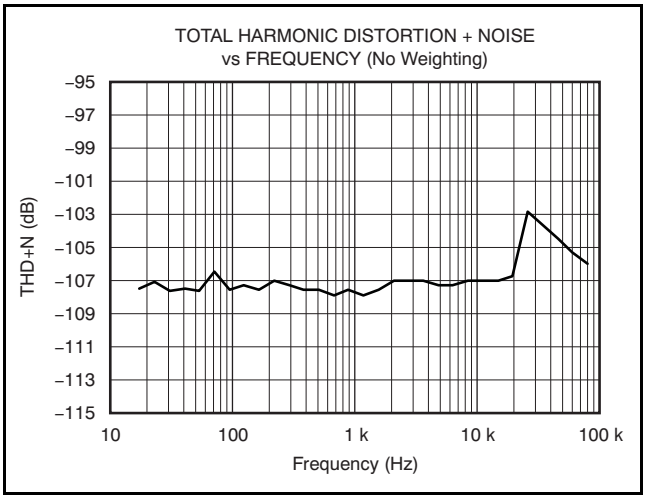


Figure 71. THD+N (No Weighting) on AP, 80-kHz Bandwidth at G = 1 with 5-V_{PP} Output

Audio On/Off Pop Performance

The THS4521 was tested to show on and off pop performance by connecting a speaker between the differential outputs and switching the power supply on and off, and also by using the $\overline{PD}$ function of the THS4521. Testing was done with and without tones. During these tests, no audible pop could be heard.

With no tone input, Figure 72 shows the pop performance when switching power on to the THS4521 and Figure 73 shows the device performance when turning the power off. The transients during power on and off illustrate that no audible pop should be heard

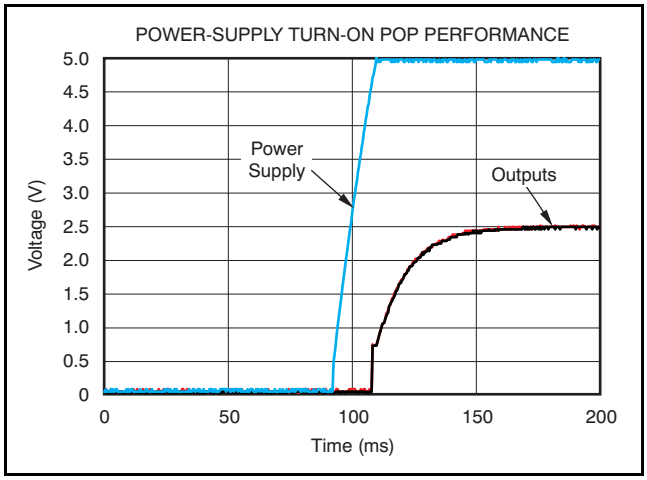


Figure 72. THS4521 Power-Supply Turn-On Pop Performance

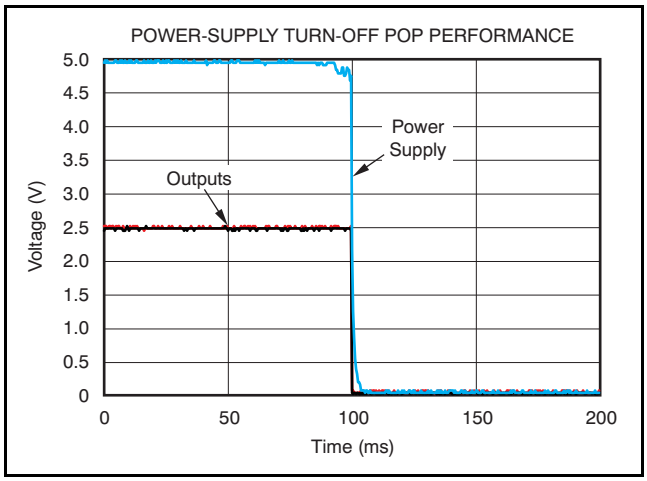


Figure 73. THS4521 Power-Supply Turn-Off Pop Performance

With no tone input, Figure 74 shows the pop performance using the $\overline{PD}$ pin to enable the THS4521, and Figure 75 shows performance using the $\overline{PD}$ pin to disable the device. Again, the transients during power on and off show that no audible pop should be heard. It should also be noted that the turn on/off times are faster using the $\overline{PD}$ pin technique.

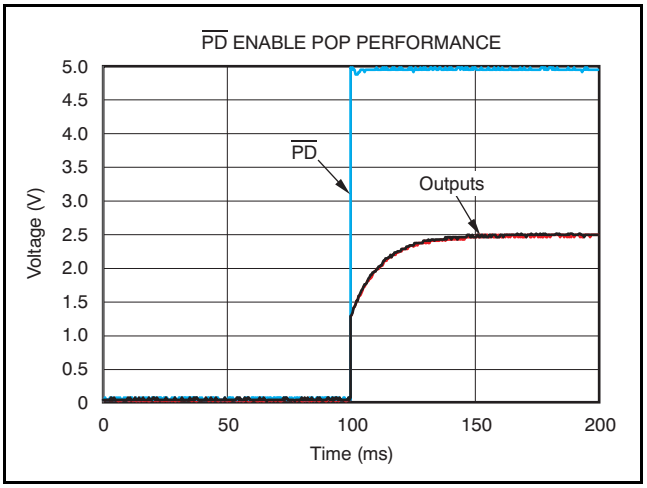


Figure 74. THS4521 $\overline{PD}$ Pin Enable Pop Performance

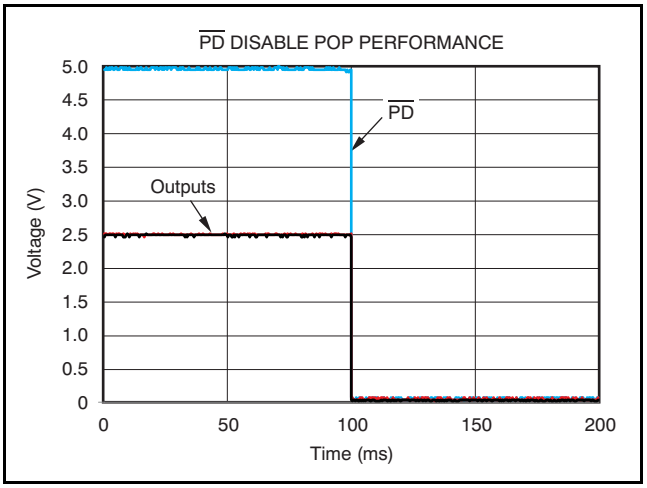


Figure 75. THS4521 $\overline{PD}$ Pin Disable Pop Performance

The power on/off pop performance of the THS4521, whether by switching the power supply or when using the power-down function built into the chip, shows that no special design should be required to prevent an audible pop.

Audio ADC Driver Performance: THS4521 and PCM4204 Combined Performance

To show achievable performance with a high-performance audio ADC, the THS4521 is tested as the drive amplifier for the PCM4204. The PCM4204 is a high-performance, four-channel ADC designed for professional and broadcast audio applications. The PCM4204 architecture uses a 1-bit delta-sigma (ΔΣ) modulator per channel that incorporates an advanced dither scheme for improved dynamic performance, and supports PCM output data. The PCM4204 provides a flexible serial port interface and many other advanced features. Refer to the PCM4204 product data sheet for more information.

The PCM4204EVM can test the audio performance of the THS4521 as a drive amplifier. The standard PCM4204EVM is provided with four OPA1632 fully-differential amplifiers, which use the same device pinout as the THS4521. For testing, one of these amplifiers is replaced with a THS4521 device in same package (MSOP), and the power supply changes to a single-supply +5V. Figure 78 shows the modifications made to the circuit. Note the resistor connecting the V_{OCM} input of the THS4521 to the input common-mode drive from the PCM4204 is shown removed and is optional; no performance change was noted with it connected or removed. The THS4521 is operated with a +5-V single-supply so the output common-mode defaults to +2.5 V as required at the input of the PCM4204. The EVM power connections were modified by connecting positive supply inputs, +15 V, +5 VA and +5 VD, to a +5-V external power supply (EXT +3.3 was not used) and connecting –15 V and all ground inputs to ground on the external power supply. Note only one external +5-V supply was needed to power all devices on the EVM.

A SYS-2722 Audio Analyzer from Audio Precision (AP) provides an analog audio input to the EVM; the PCM-formatted digital output is read by the digital input on the AP.

Data were taken using a 256-f_S system clock to achieve f_S = 48-kHz measurements, and audio output uses PCM format. Other data rates and formats are expected to show similar performance in line with that shown in the product data sheet.

Figure 76 shows the THD+N vs Frequency response with no weighting; Figure 77 shows an FFT of the output with 1-kHz input tone. Input signals to the PCM4204 for these tests is 0.5 dBFS. Dynamic range is also tested at –60 dBFS, f_{IN} = 1 kHz, and A-weighted. Table 4 summarizes testing results using the THS4521 together with the PCM4204 versus typical data sheet performance measurements, and show that it make an excellent drive amplifier for this ADC.

The test circuit shown in Figure 78 has a gain = 0.27 and attenuates the input signal. For applications that require higher gain, the circuit was modified to gains of G = 1, G = 2, and G = 5 by replacing the feedback resistors (R33 and R34) and re-tested to show performance.

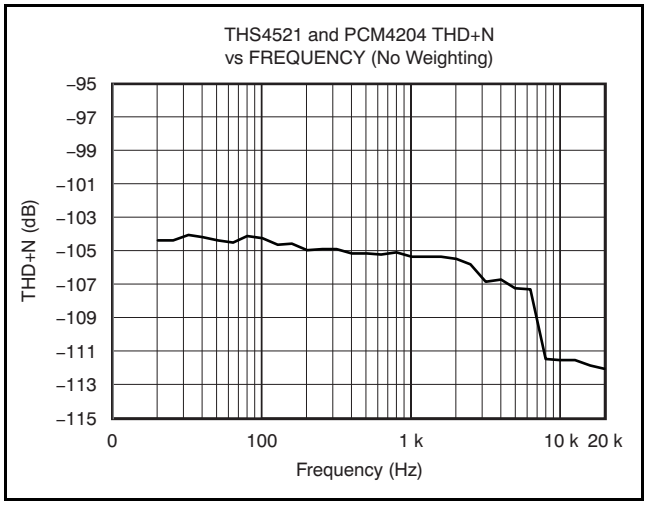


Figure 76. THS4521 and PCM4204: THD+N versus Frequency with No Weighting

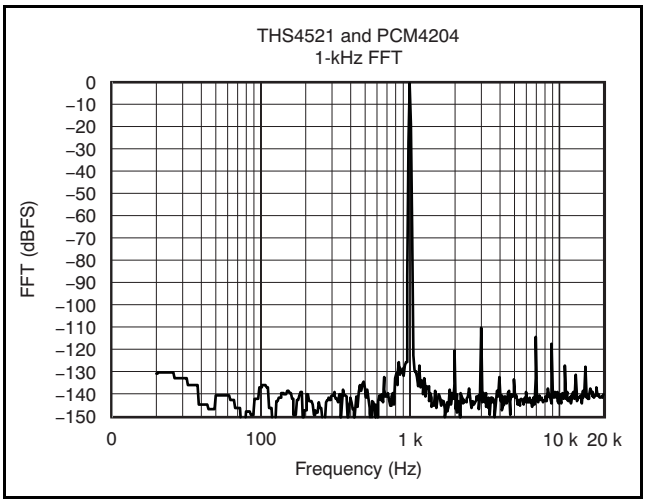


Figure 77. THS4521 and PCM4204 1-kHz FFT

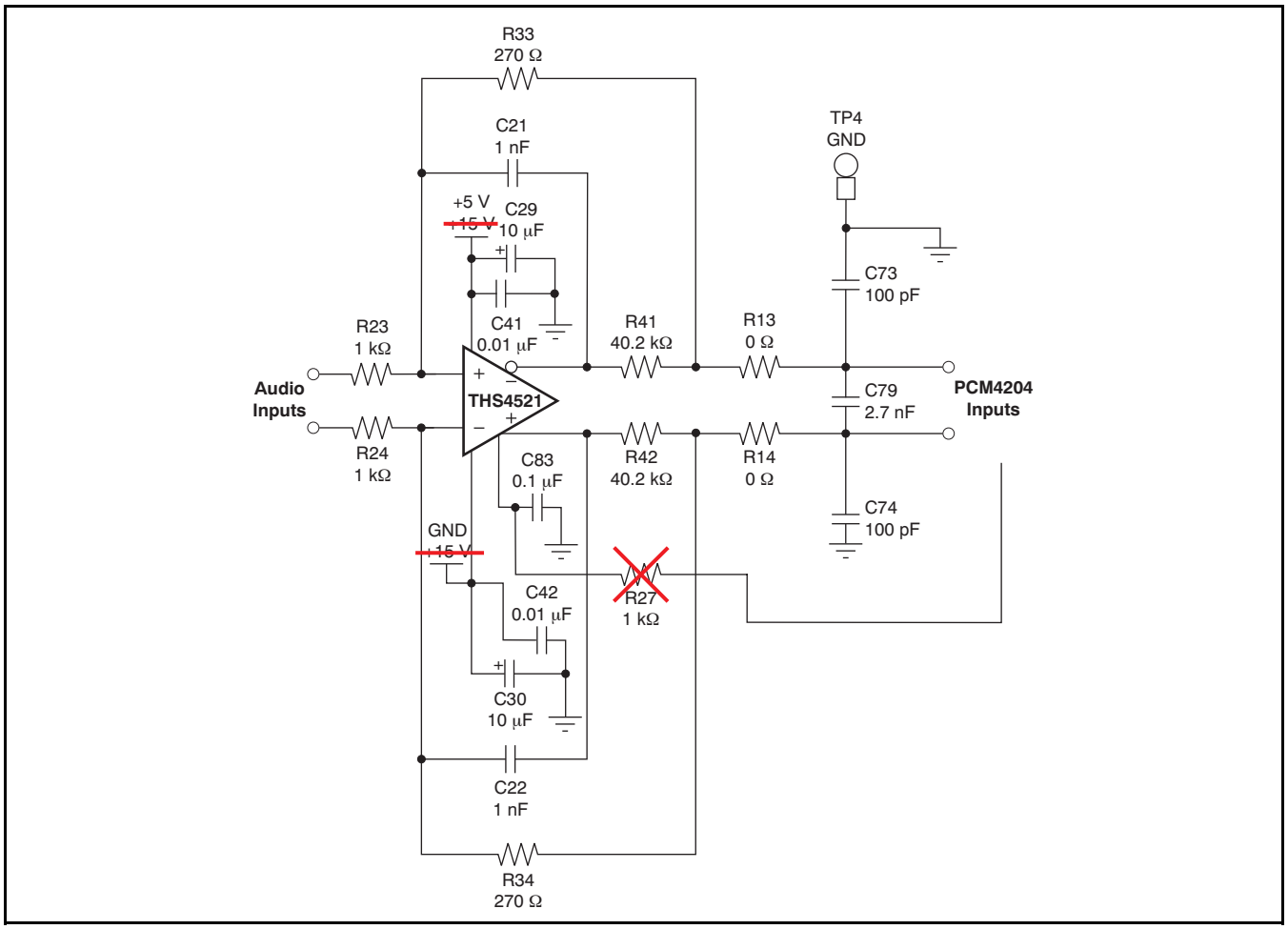


Figure 78. THS4521 and PCM4204 Test Circuit

Table 4. 1-kHz AC Analysis: Test Circuit versus PCM4204 Data Sheet Typical Specifications (f_S = 48 kSPS)

Configuration	Tone	THD+N	Dynamic Range
THS4521 and PCM4204	1 kHz	–106 dBc	117 dB
PCM4204 Data sheet (typ)	1 kHz	–105 dBc	118 dB

Figure 79 shows the THS4521 and PCM4204 THD+N versus frequency with no weighting at higher gains.

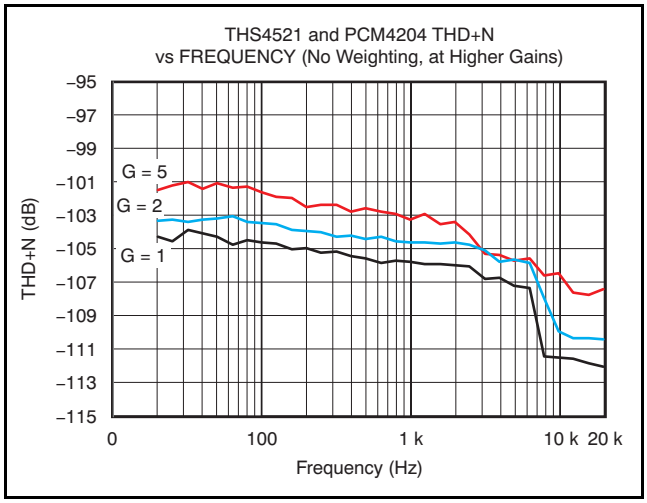


Figure 79. THS4521 and PCM4204: THD+N versus Frequency with No Weighting at Higher Gains

Audio ADC Driver Performance: THS4521 and PCM3168 Combined Performance

The THS4521 is also tested as the drive amplifier for the PCM3168A ADC input. The PCM3168A is a high-performance, single-chip, 24-bit, 6-in/8-out, audio coder/decoder (codec) with single-ended and differential selectable analog inputs and differential outputs. The six-channel, 24-bit ADC employs a ΔΣ modulator and supports 8-kHz to 96-kHz sampling rates and a 16-bit/24-bit width digital audio output word on the audio interface. The eight-channel, 24-bit digital-to-analog converter (DAC) employs a ΔΣ modulator and supports 8-kHz to 192-kHz sampling rates and a 16-bit/24-bit width digital audio input word on the audio interface. Each audio interface supports I^2S™, left-/right-justified, and DSP formats with 16-bit/24-bit word width. In addition, the PCM3168A supports the time-division-multiplexed (TDM) format.. The PCM3168A provides flexible serial port interface and many other advanced features. Refer to the PCM3168A product data sheet for more information.

The PCM3168A EVM is used to test the audio performance of the THS4521 as a drive amplifier. The standard PCM3168A EVM is provided with OPA2134 op amps that are used to convert single-ended inputs to differential to drive the ADC. For testing, the op amp output series resistors are removed from one of the channels and a THS4521, mounted on its standard EVM, is connected to the ADC inputs via short coaxial cables. The THS4521 EVM is configured for both differential inputs as shown in Figure 60 and for single-ended input as shown in Figure 61 with 1-kΩ resistors for R_F and R_G, and 24.9-Ω resistors in series with each output to isolate the outputs from the reactive load of the coaxial cables. To limit the noise from the external EVM and cables, a 2.7-nF capacitor is placed differentially across the PCM3168A inputs. The THS4521 is operated with a single-supply +5-V supply so the output common-mode of the THS4521 defaults to +2.5 V as required at the input of the PCM3168A. The PCM3168A EVM is configured and operated as described in the PCM3168AEVM User Guide. The ADC was tested with an external THS4521 EVM with both single-ended input and differential inputs. In both configurations, the results are the same. Figure 80 shows the THD+N versus frequency and Table 5 compares the result to the PCM3168 data sheet typical specification at 1 kHz. Both graphs show that it makes an excellent drive amplifier for this ADC. **Note:** a 2700 series Audio Analyzer from Audio Precision is used to generate the input signals to the THS4521 and to analyze the digital data from the PCM3168.

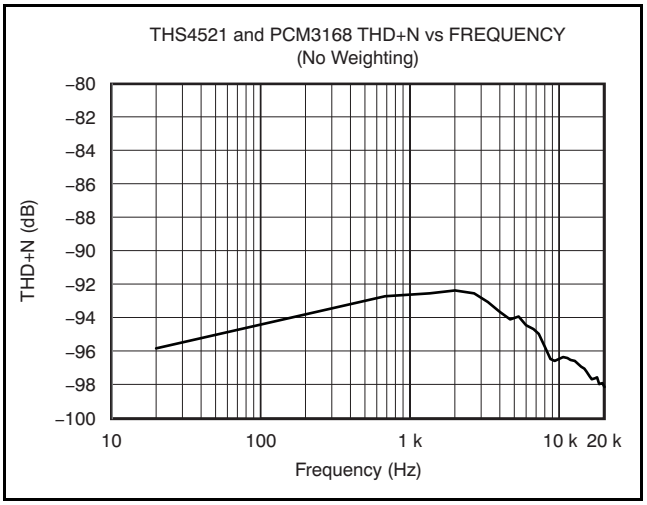


Figure 80. THS4521 and PCM3168: THD+N versus Frequency with No Weighting

Table 5. 1-kHz AC Analysis: Test Circuit vs PCM3168 Data Sheet Typical Specifications (f_S = 48 kSPS)

Configuration	Tone	THD+N
THS4521 and PCM3168	1 kHz	–92.6 dBc
PCM3168 Data sheet (typ)	1 kHz	–93 dBc

ADC Driver Performance: THS4521 and ADS1278 Combined Performance

The THS4521 provides excellent performance when driving high-performance ΔΣ and successive approximation register (SAR) ADCs in audio and industrial applications using a single 3-V to 5-V power supply. To show achievable performance, the THS4521 is tested as the drive amplifier for the ADS1278 24-bit ADC. The ADS1278 offers excellent ac and dc performance, with four selectable operating modes from 10 kSPS to 128 kSPS to enable the user to fine-tune performance and power for specific application needs. The circuit shown in Figure 81 was used to test the performance. Data were taken using the High-Resolution mode (52 kSPS) of the ADS1278 with input frequencies at 1 kHz and 10 kHz and signal levels 1/2 dB below full-scale (–0.5 dBFS). FFT plots showing the spectral performance are given in Figure 82 and Figure 83; tabulated ac analysis results are shown in Table 6 and compared to the ADS1278 data sheet typical performance specifications.

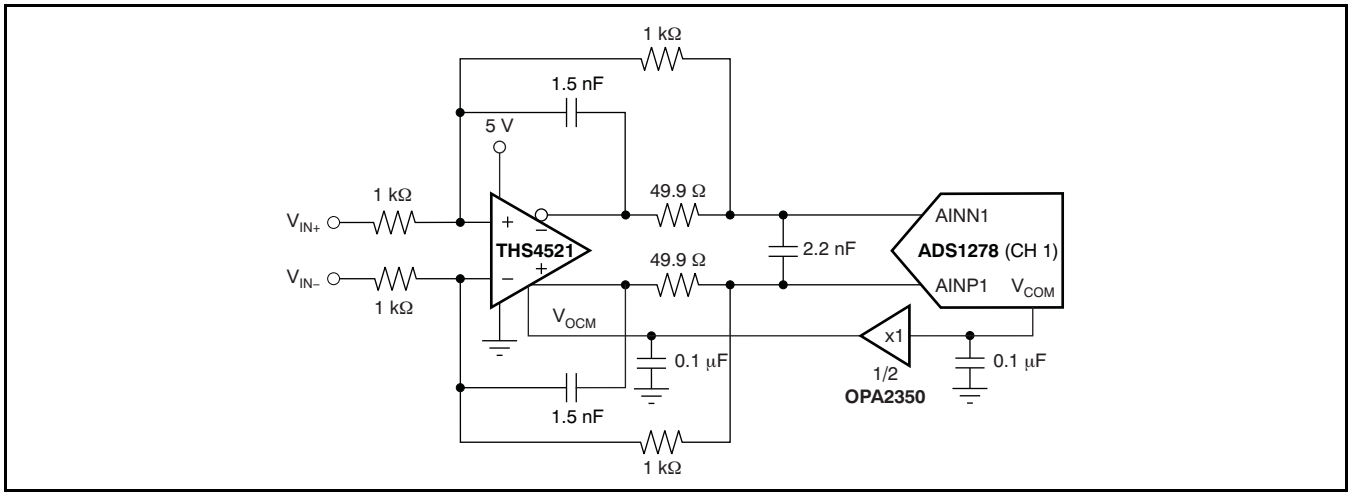


Figure 81. THS4521 and ADS1278 (Ch 1) Test Circuit

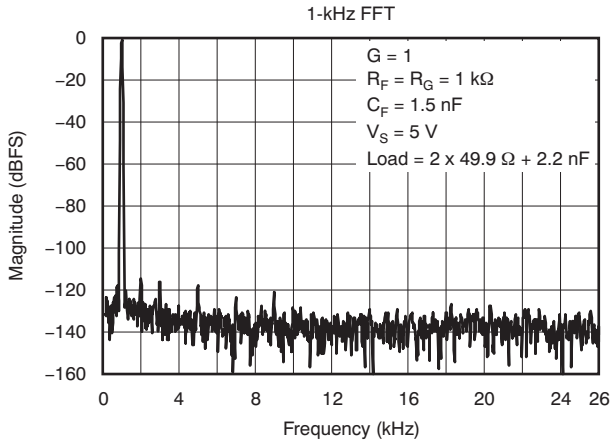


Figure 82. 1-kHz FFT

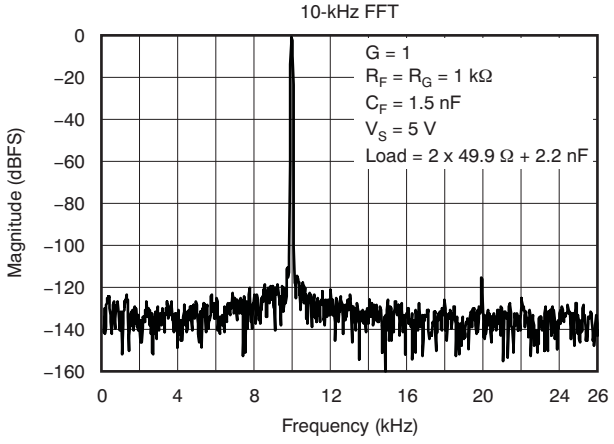


Figure 83. 10-kHz FFT

Table 6. AC Analysis

Configuration	Tone	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
THS4521and ADS1278	1 kHz	–0.5	109	–108	105	114
	10 kHz	–0.5	102	–110	101	110
ADS1278 Data sheet (typ)	1 kHz	–0.5	110	–108	—	109

ADC Driver Performance: THS4521 and ADS8321 Combined Performance

To demonstrate achievable performance, the THS4521 is tested as the drive amplifier for the ADS8321 16-bit SAR ADC. The ADS8321 offers excellent ac and dc performance, with ultra-low power and small size. The circuit shown in Figure 84 was used to test the performance.

Data were taken using the ADS8321 at 100 kSPS with input frequencies of 2 kHz and 10 kHz and signal levels that were -0.5 dBFS. FFT plots that illustrate the spectral performance are given in Figure 85 and Figure 86. Tabulated ac analysis results are listed in Table 7 and compared to the ADS8321 data sheet typical performance.

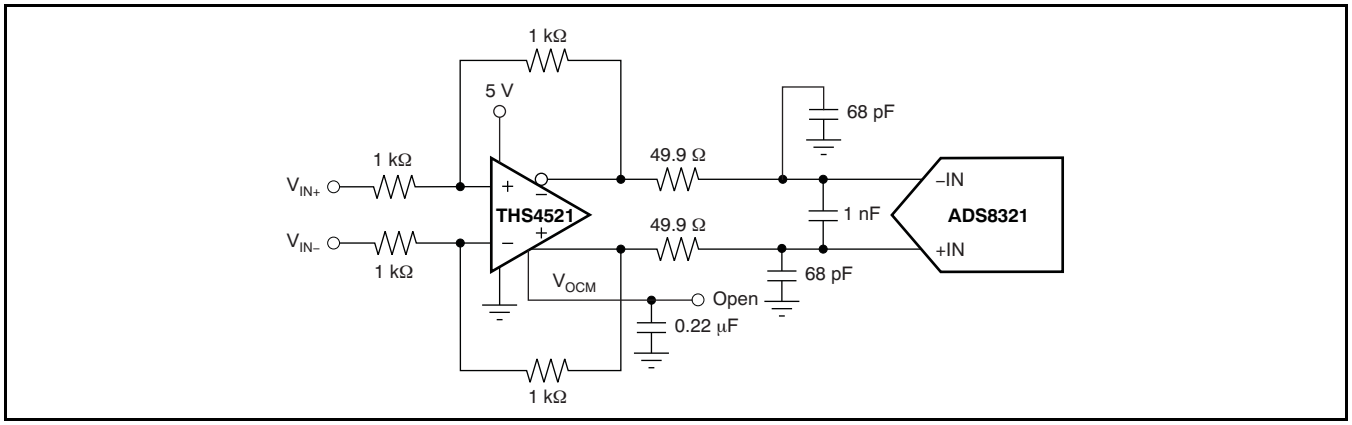


Figure 84. THS4521 and ADS8321 Test Circuit

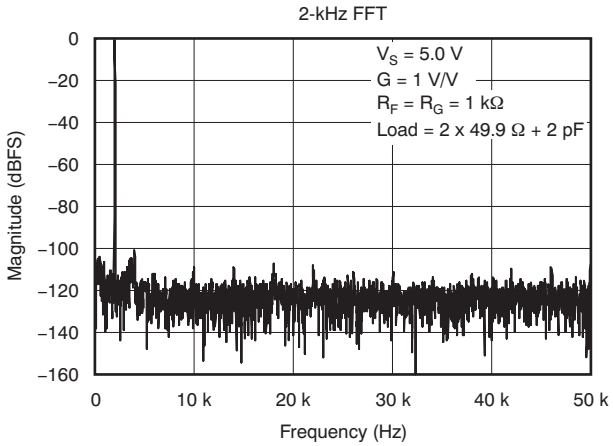


Figure 85. 2-kHZ FFT

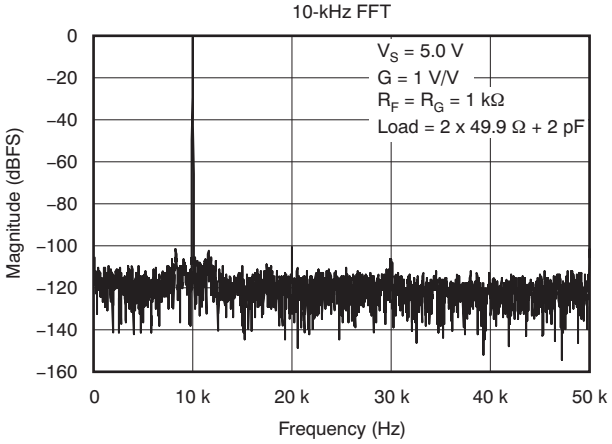


Figure 86. 10-kHz FFT

Table 7. AC Analysis

Configuration	Tone	Signal (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
THS4521 and ADS8321	2 kHz	–0.5	86.7	–97.8	86.4	100.7
	10 kHz	–0.5	85.2	–98.1	85.2	102.2
ADS8321 Data sheet (typ)	10 kHz	–0.5	87	–86	84	86

EVM AND LAYOUT RECOMMENDATIONS

Figure 87 shows the THS4521EVM schematic. PCB layers 1 through 4 are shown in Figure 88; Table 8 lists the bill of materials for the THS4521EVM as supplied from TI. It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended in each output lead, placed as near to the output pins as possible.
5. Two 0.1-μF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 10-μF power-supply decoupling capacitors should be placed within 1 inch of the device and can be shared among multple analog devices.
7. A 0.22-μF capacitor should be placed between the V_{OCM} input pin and ground near to the pin. This capacitor limits noise coupled into the pin.
8. The $\overline{PD}$ pin uses TTL logic levels; a bypass capacitor is not necessary if actively driven, but can be used for robustness in noisy environments whether driven or not.
9. If input termination resistors R_{10} and R_{11} are used, a single point connection to ground on L2 is recommended.

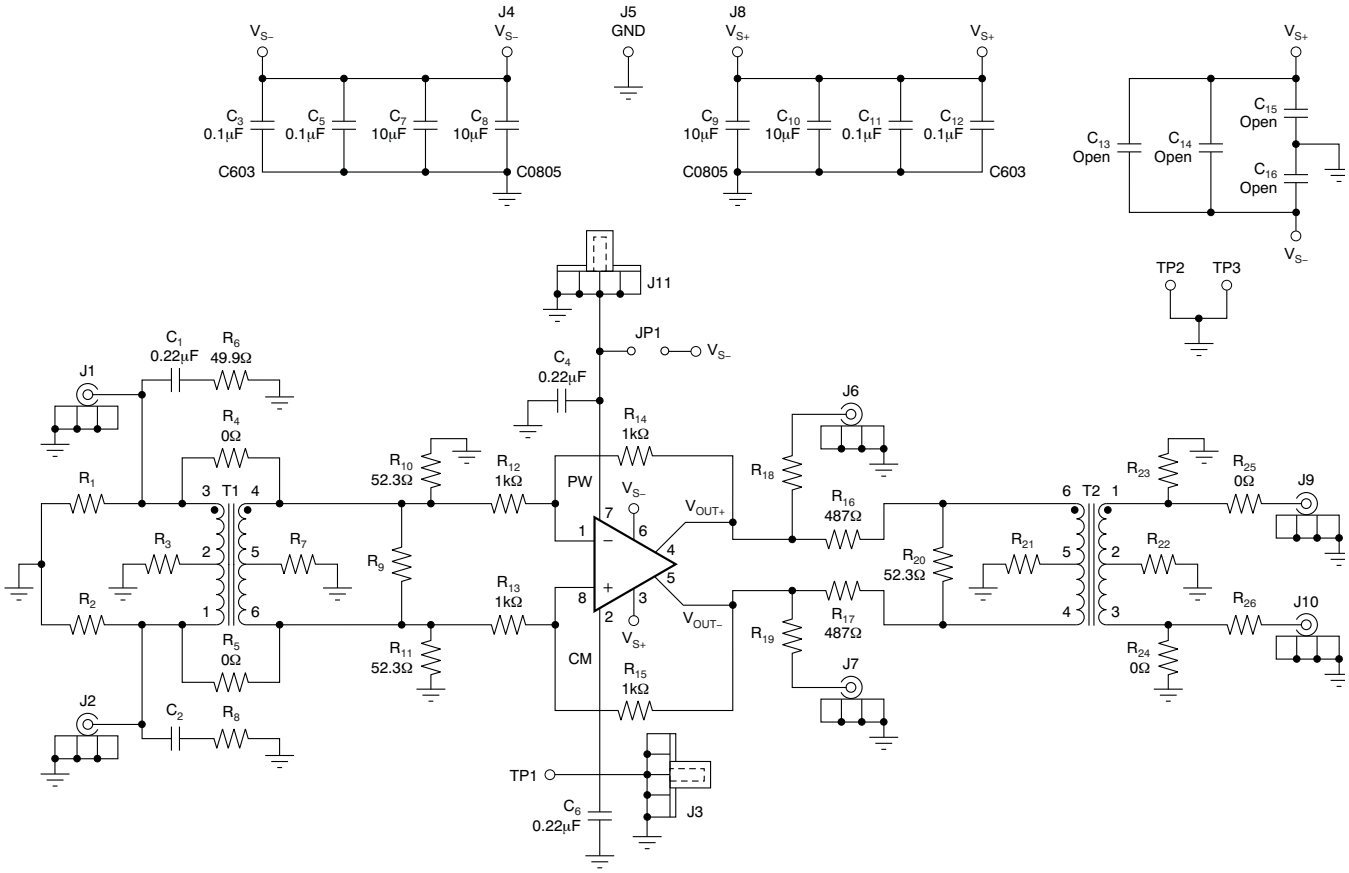


Figure 87. THS4521EVM: Schematic

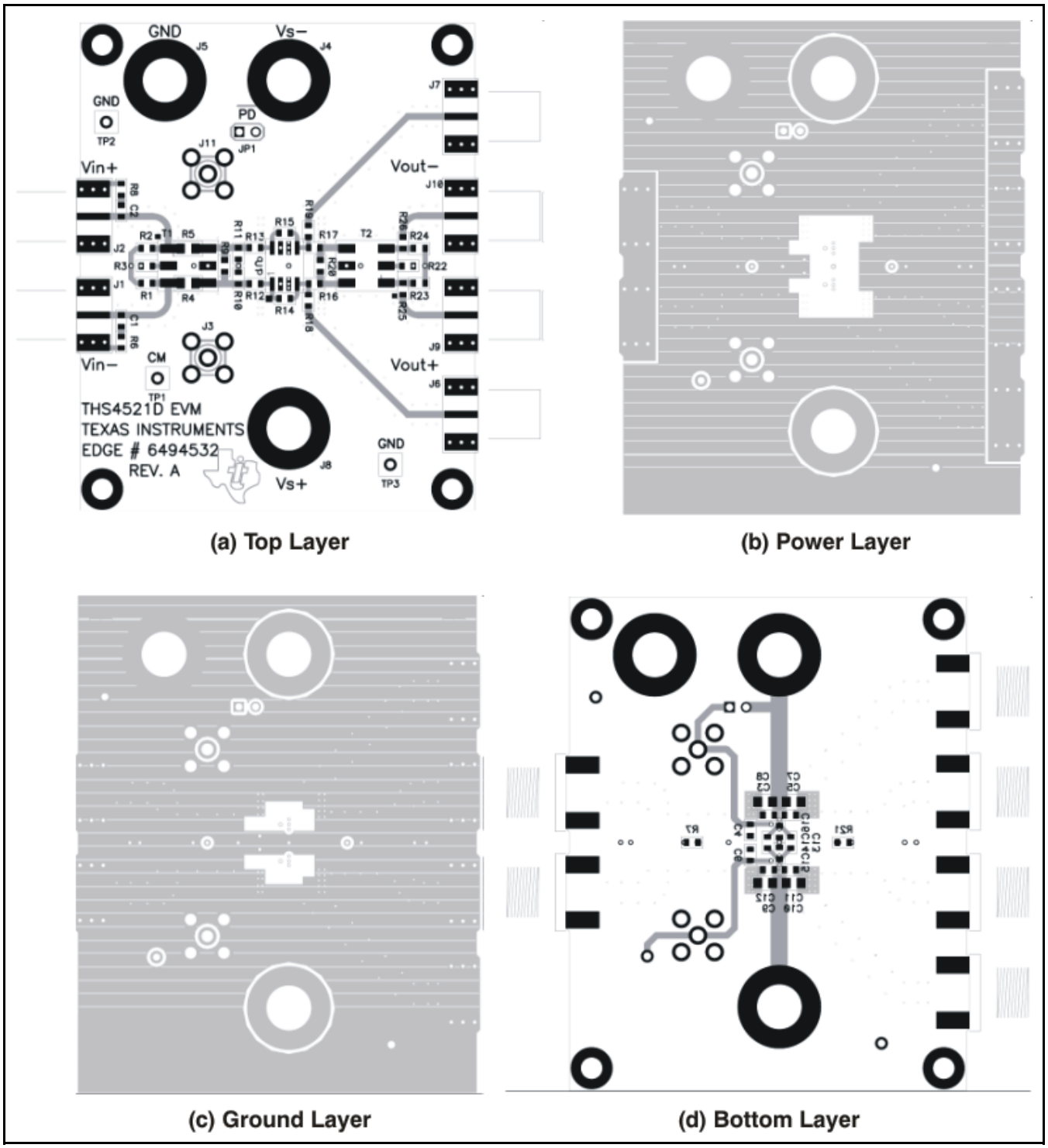


Figure 88. THS4521EVM: Layer 1 to Layer 4 Images

Table 8. THS4521EVM Parts List

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QTY	MANUFACTURER PART NUMBER
1	Capacitor, 10.0 μF, ceramic, X5R, 6.3 V	0805	C7, C8, C9, C10	4	(AVX) 08056D106KAT2A
2	Capacitor, 0.1 μF, ceramic, X7R, 16 V	0603	C3, C5, C11, C12	4	(AVX) 0603YC104KAT2A
3	Capacitor, 0.22 μF, ceramic, X7R, 10 V	0603	C1, C4, C6	3	(AVX) 0603ZC224KAT2A
4	Open	0603	C2, C13, C14, C15, C16	5	
5	Open	0603	R1, R2, R3, R7, R8, R9, R18, R19, R21, R22, R23, R26	12	
6	Resistor, 0 Ω	0603	R24, R25	2	(ROHM) MCR03EZPJ000
7	Resistor, 49.9 Ω, 1/10W, 1%	0603	R6	1	(ROHM) MCR03EZPFX49R9
8	Resistor, 52.3 Ω, 1/10W, 1%	0603	R10, R11, R20	3	(ROHM) MCR03EZPFX52R3
9	Resistor, 487 Ω, 1/10W, 1%	0603	R16, R17	2	(ROHM) MCR03EZPFX4870
10	Resistor, 1k Ω, 1/10W, 1%	0603	R12, R13, R14, R15	4	(ROHM) MCR03EZPFX1001
11	Resistor, 0 Ω	0805	R4, R5	2	(ROHM) MCR10EZPJ000
12	Open		T1	1	
13	Transformer, RF		T2	1	(MINI-CIRCUITS) ADT1-1WT
14	Jack, Banana receptance, 0.25-in dia. hole		J4, J5, J8	3	(SPC) 813
15	Open		J1, J3, J6, J7, J10, J11	6	
16	Connector, edge, SMA PCB jack		J2, J9	2	(JOHNSON) 142-0701-801
17	Header, 0.1 in CTRS, 0.025-in sq. pins	2 POS.	JP1	1	(SULLINS) PBC36SAAN
18	Shunts		JP1	1	(SULLINS) SSC02SYAN
19	Test point, Red		TP1	1	(KEYSTONE) 5000
20	Test point, Black		TP2, TP3	2	(KEYSTONE) 5001
21	IC, THS4521		U1	1	(TI) THS4521D
22	Standoff, 4-40 hex, 0.625 in length			4	(KEYSTONE) 1808
23	Screw, Phillips, 4-40, .250 in			4	SHR-0440-016-SN
24	Board, printed circuit			1	(TI) EDGE# 6494532

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3 V to 5.5 V and the output voltage range of 3 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August, 2010) to Revision E **Page**

- Changed test level indication for 5-V input offset voltage drift from B to C 5

Changes from Revision C (June, 2010) to Revision D **Page**

- Updated format of *Input/output voltage* parameter in Absolute Maximum Ratings table 2
- Added *Input current* parameter to Absolute Maximum Ratings table 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4521ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521	Samples
THS4521IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	4521	Samples
THS4521IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	4521	Samples
THS4521IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TH4521	Samples
THS4522IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4522	Samples
THS4522IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4522	Samples
THS4524IDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4524	Samples
THS4524IDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS4524	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF THS4521, THS4524 :

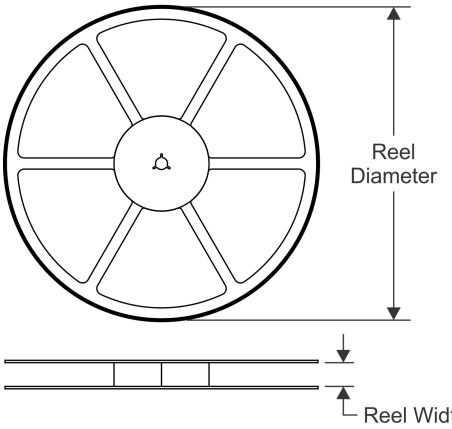
- Enhanced Product: THS4524-EP

NOTE: Qualified Version Definitions:

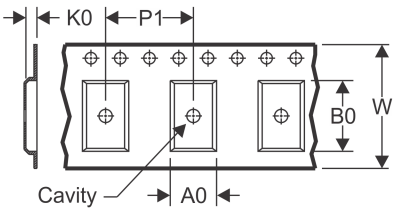
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

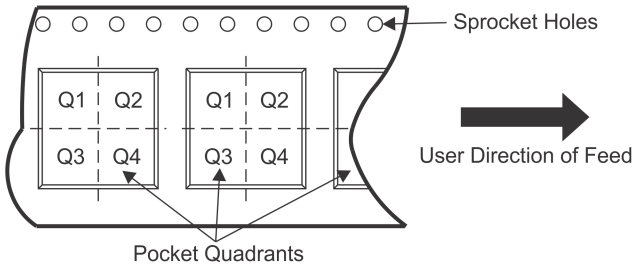


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

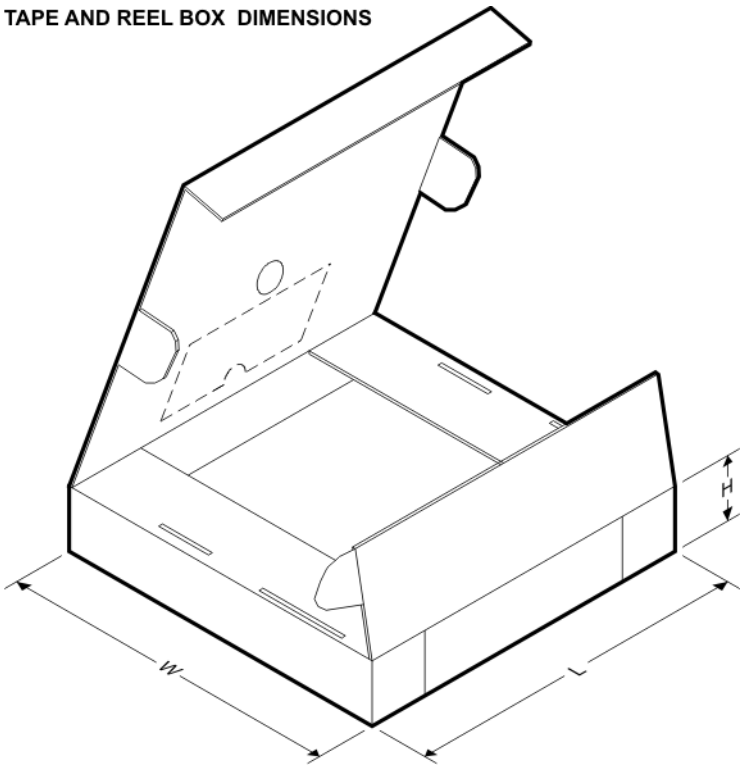
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4521IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4521IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4521IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4522IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

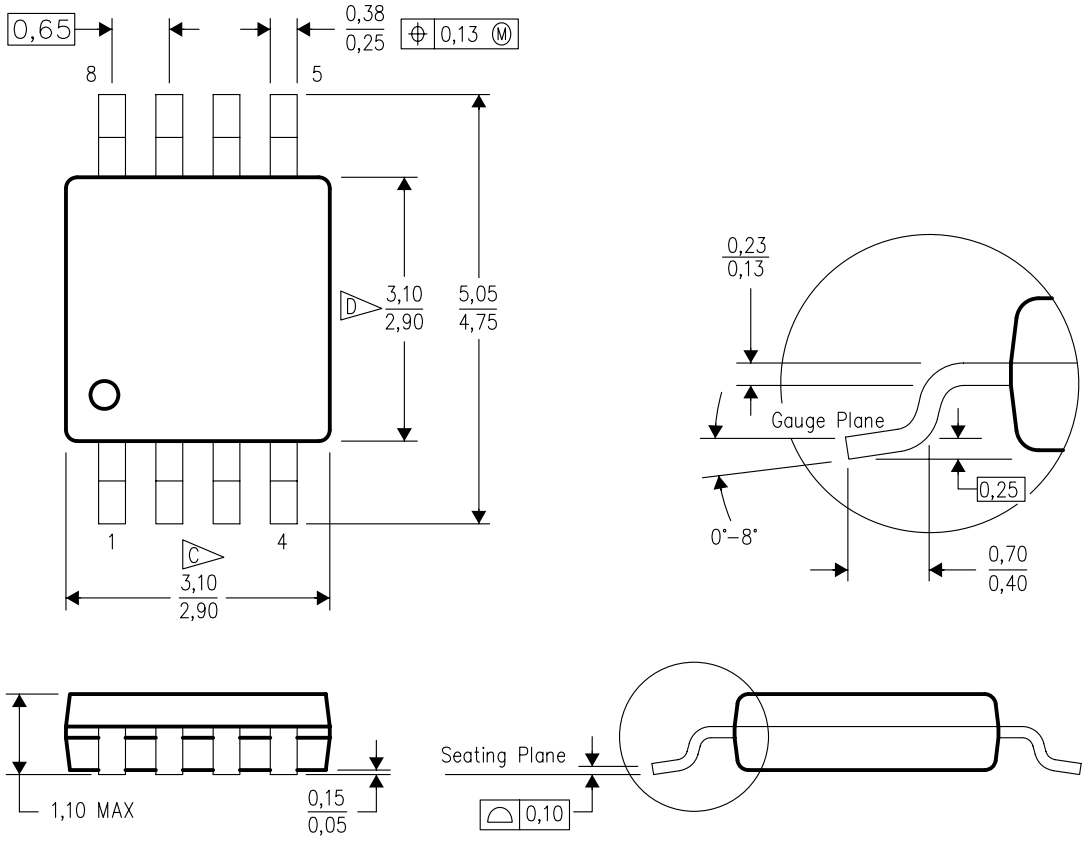
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4521IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
THS4521IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
THS4521IDR	SOIC	D	8	2500	367.0	367.0	35.0
THS4522IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

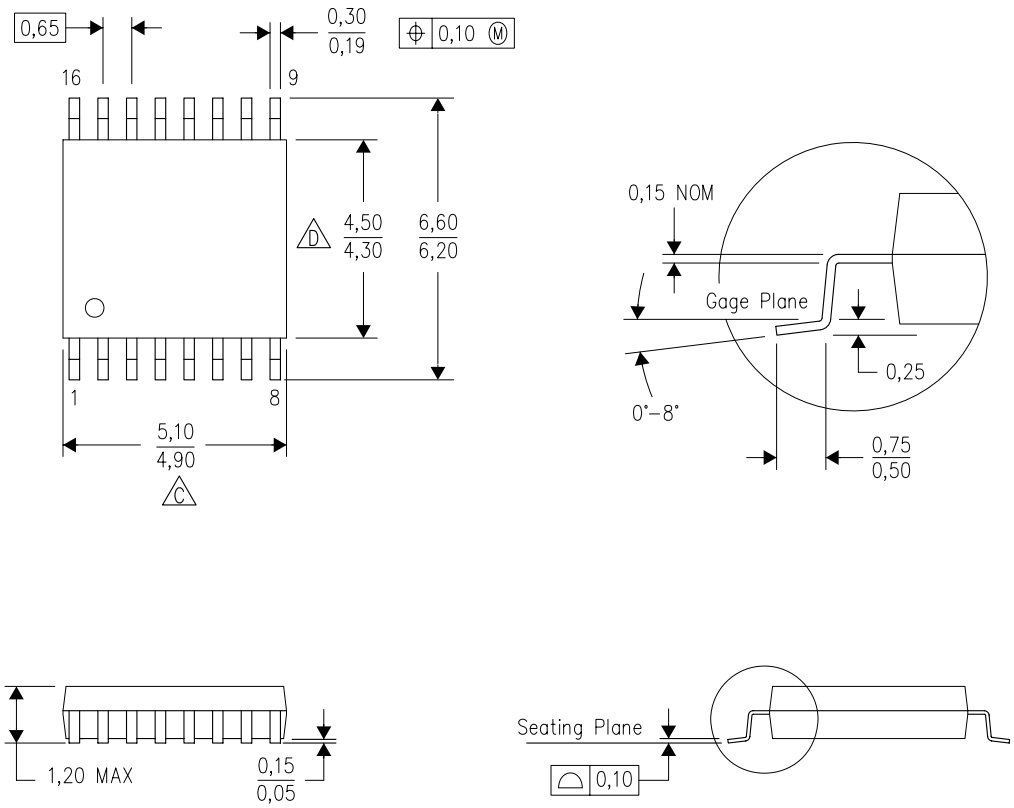
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

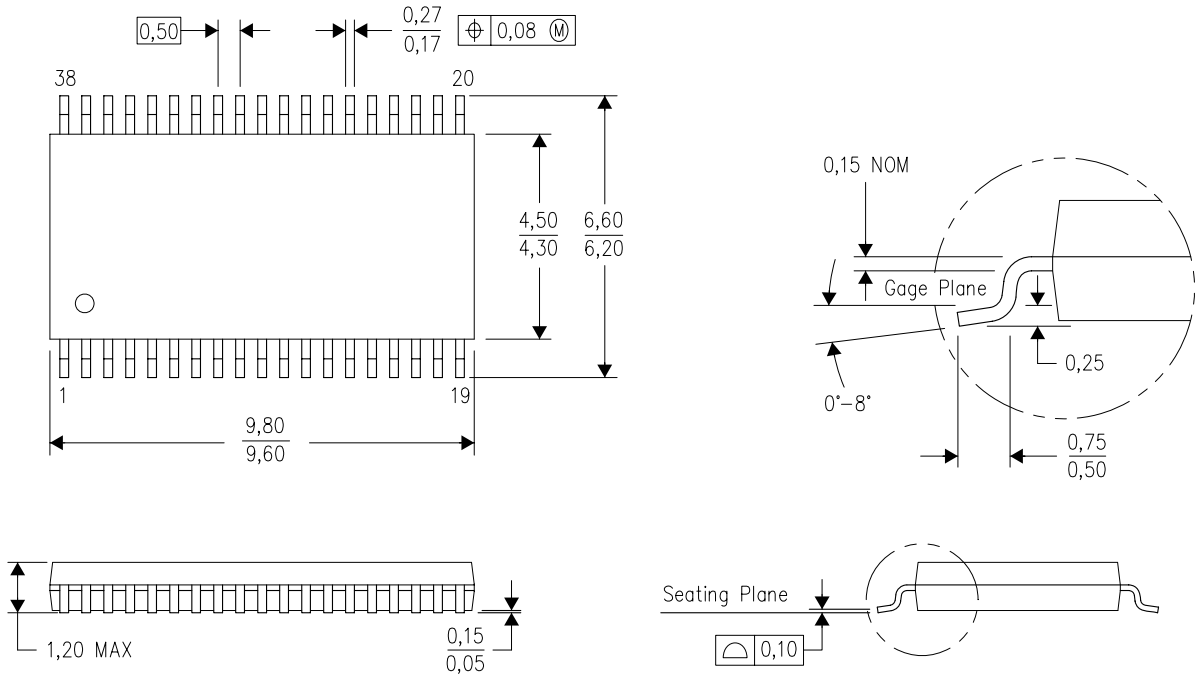
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

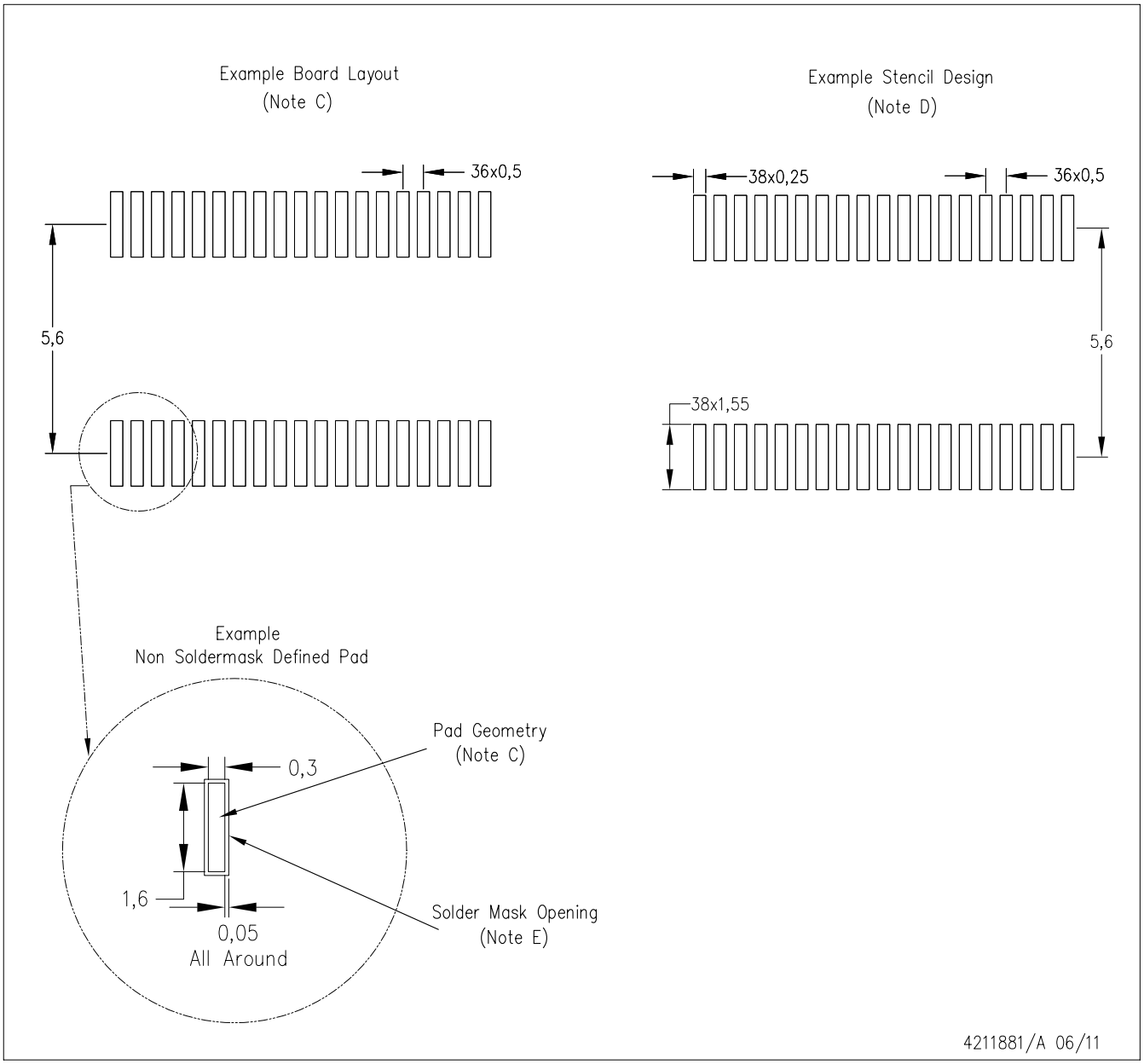
DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



4073252-6/I 03/11

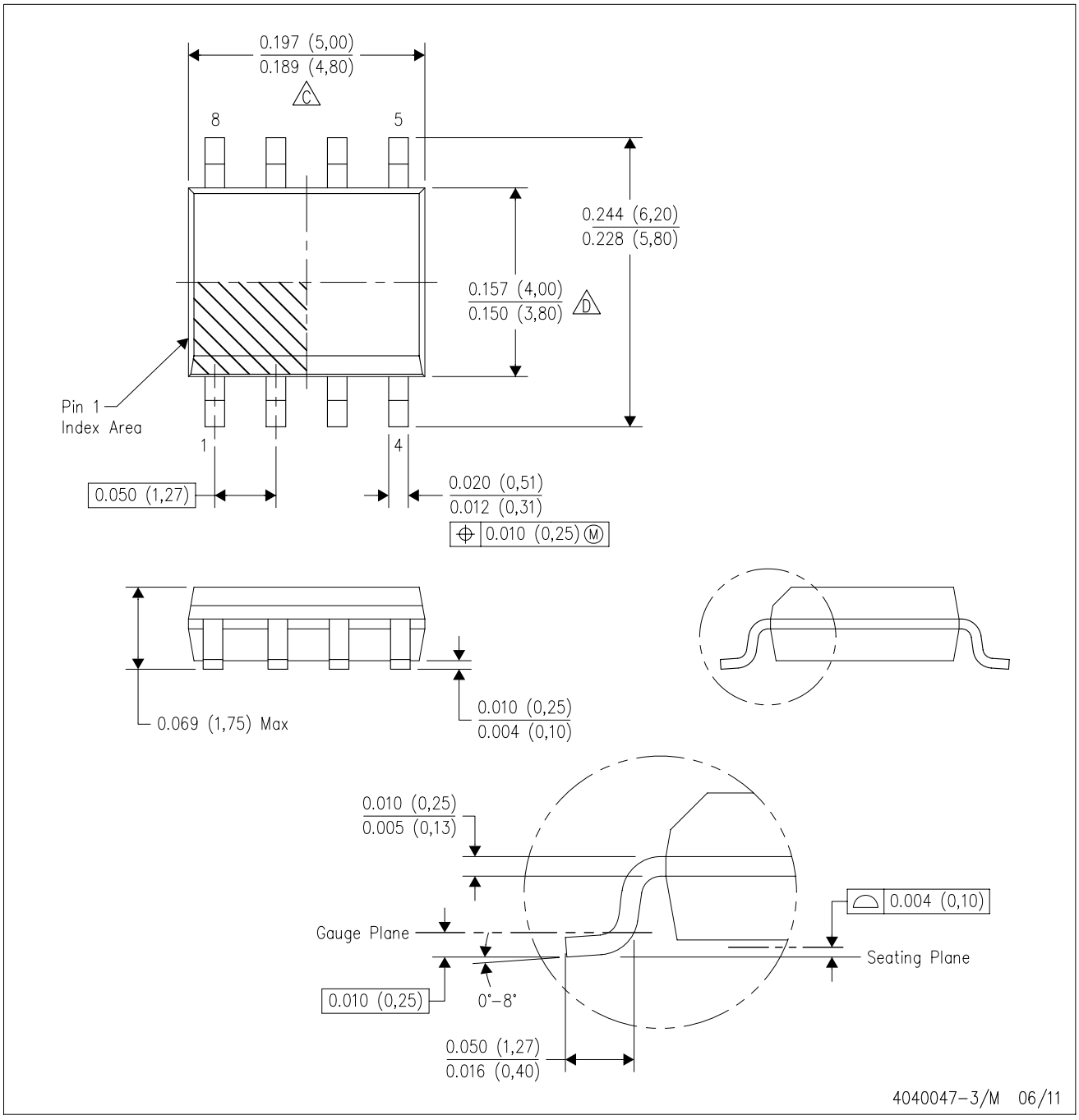
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



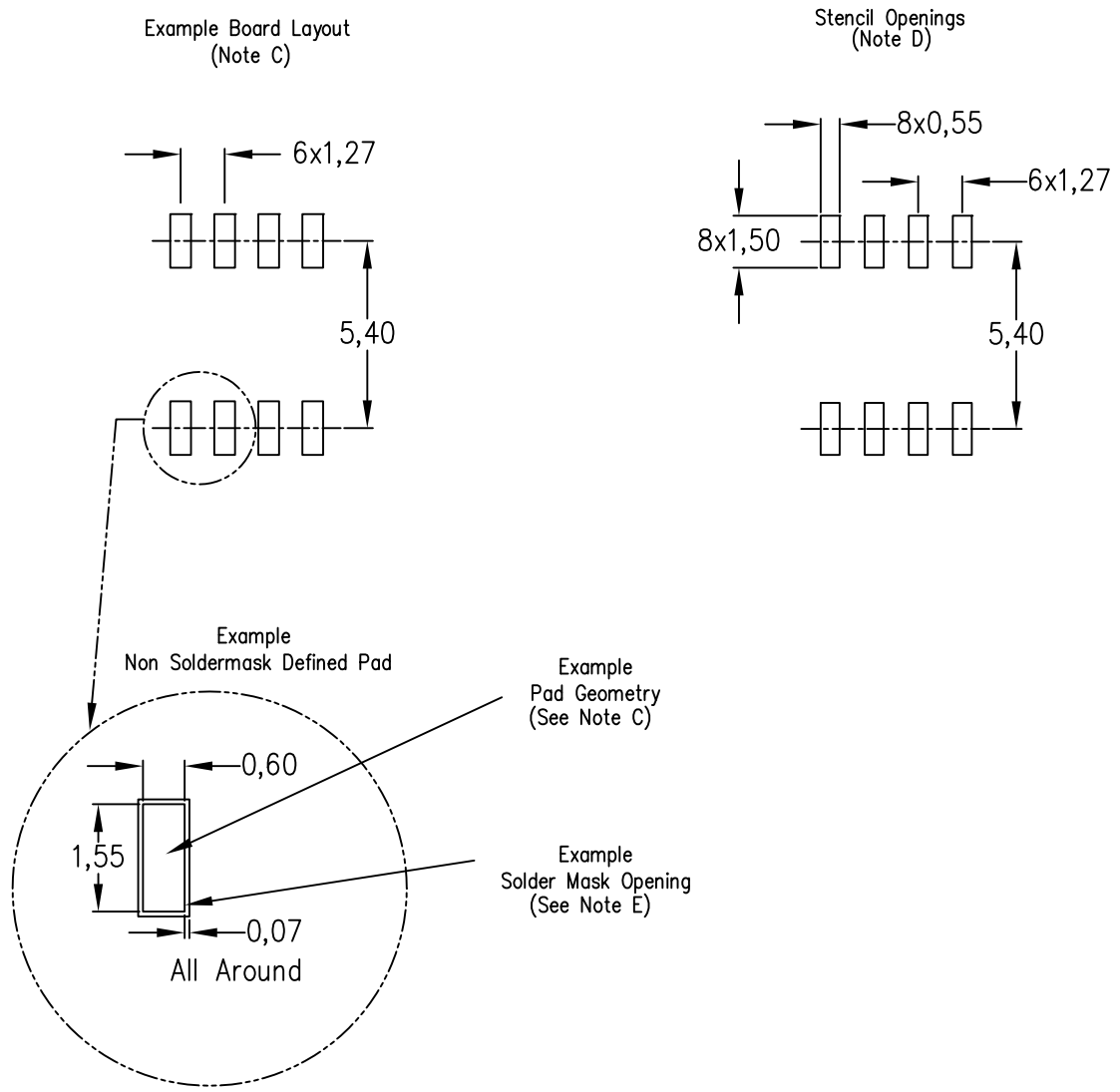
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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