TPS713xxEVM User's Guide

This user's guide describes the characteristics, operation, and use of the TPS713xxEVM-050 dual RF LDO evaluation module (EVM). This EVM features the TPS71319DRC and the TPS71334DRC devices. Each device can deliver up to 250mA at each output. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and printed circuit board (PCB) layout drawings for the evaluation module.

Contents

List of Figures

List of Tables

1   Related Documentation From Texas Instruments

TPS713xx data sheet ([SBVS055](#)).

2   Introduction

The Texas Instruments TPS713xxEVM helps designers evaluate the operation and performance of the TPS713xx family of devices. These devices are tailored to applications that need both high PSRR and low output noise.

This EVM is designed to operate with an input voltage up to +5.5V. The default output voltage of this EVM is +1.8V (VOUT1) and +2.5V (VOUT2) for U1 and +3.3V (VOUT1) and +1.5V (VOUT2) for U2. If desired, this EVM can easily be modified to supply higher or lower output voltages by adjusting the appropriate feedback resistor dividers. Also, other fixed output voltage versions of the devices can be easily evaluated using this EVM. Refer to the product data sheet ([SBVS055](#)) for the various fixed output voltage options available in the TPS713xx device family, as well as for more information on adjusting the output voltage.

3   Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS713xxEVM-050.

3.1   Input/Output Connector Descriptions

J1, J8 – VIN — This is the positive connection to the input power supply. The leads to the input supply should be as short as possible for best transient performance.

J2, J9 – GND — This is the return connection for the input power supply.

J3, J10 – VOUT1 — This is the first output supply from the dual LDO. Connect this pin to the positive input of the load.

J5, J12 – VOUT2 — This is the second output supply from the dual LDO. Connect this pin to the positive input of the load.

J4, J6, J11, J13 – GND — This is the negative connection from the output of the power supply. Connect this pin to the negative input of the load.

J7, J14 – GND, $\overline{RESET}$ — This connection is the $\overline{RESET}$ output for the TPS713xxEVM-50..

JP1, JP3 – EN1 — This jumper enables and disables VOUT1.

JP2, JP4 – EN2 — This jumper enables and disables VOUT2.

3.2   Setup and Operation

Connect an input supply between J1 and J2 or J8 and J9, depending on which device you intend to evaluate. The voltage range on this supply should not exceed +5.5V. Loads should be connected between J3 and J4, J5, and J6, or J11 and J10, J12, and J13, depending on the circuit being evaluated. Enable the output by positioning JP1, JP2, JP3, and JP4 to connect the EN and ON pins. The TPS71319 (U1) device is set to provide output voltages of +1.8V and +2.5V. The TPS71334 (U2) is also available for evaluation, and provides output voltages of +3.3V and +1.5V.

4   Board Layout

This section provides the TPS713xxEVM-050 board layout and illustrations.

> **Note:**
> Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS713xxEVM PCBs.

4.1   Layout

Board layout is critical for best PSRR and output accuracy. Figure 1, Figure 2, and Figure 3 show the board layout for the TPS713xxEVM-050 PCB. Careful attention has been given to the placement of input, output, and noise reduction capacitors. For best accuracy with adjustable devices, the feedback point should be connected at the load.
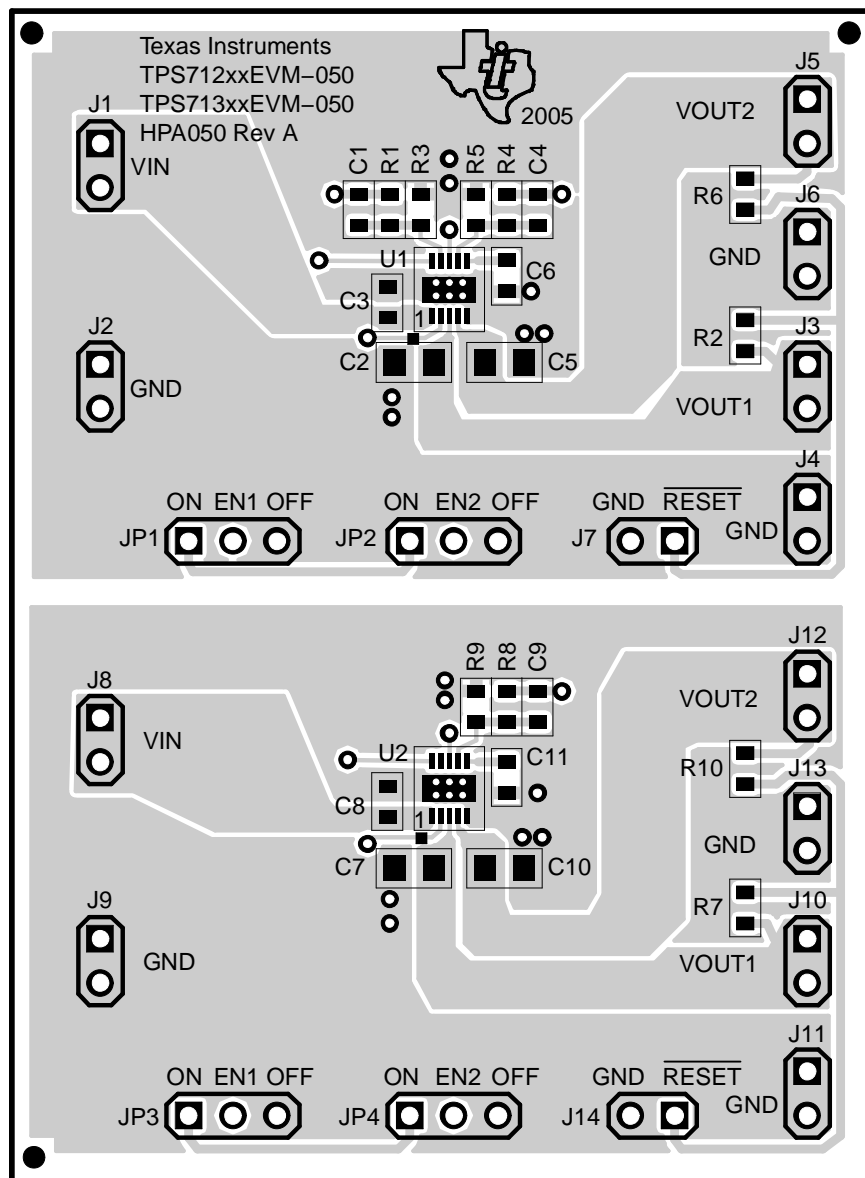
Figure 1. Assembly Layer
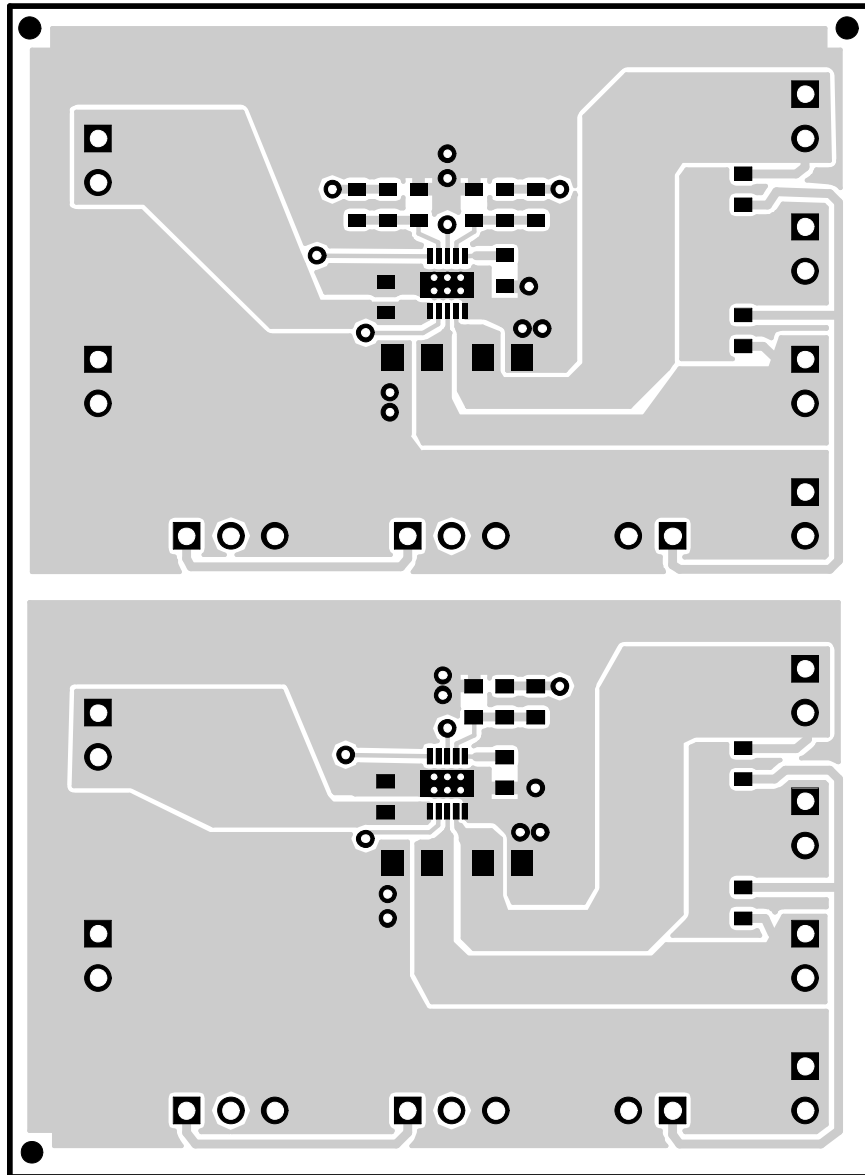
Figure 2. Top Layer Routing
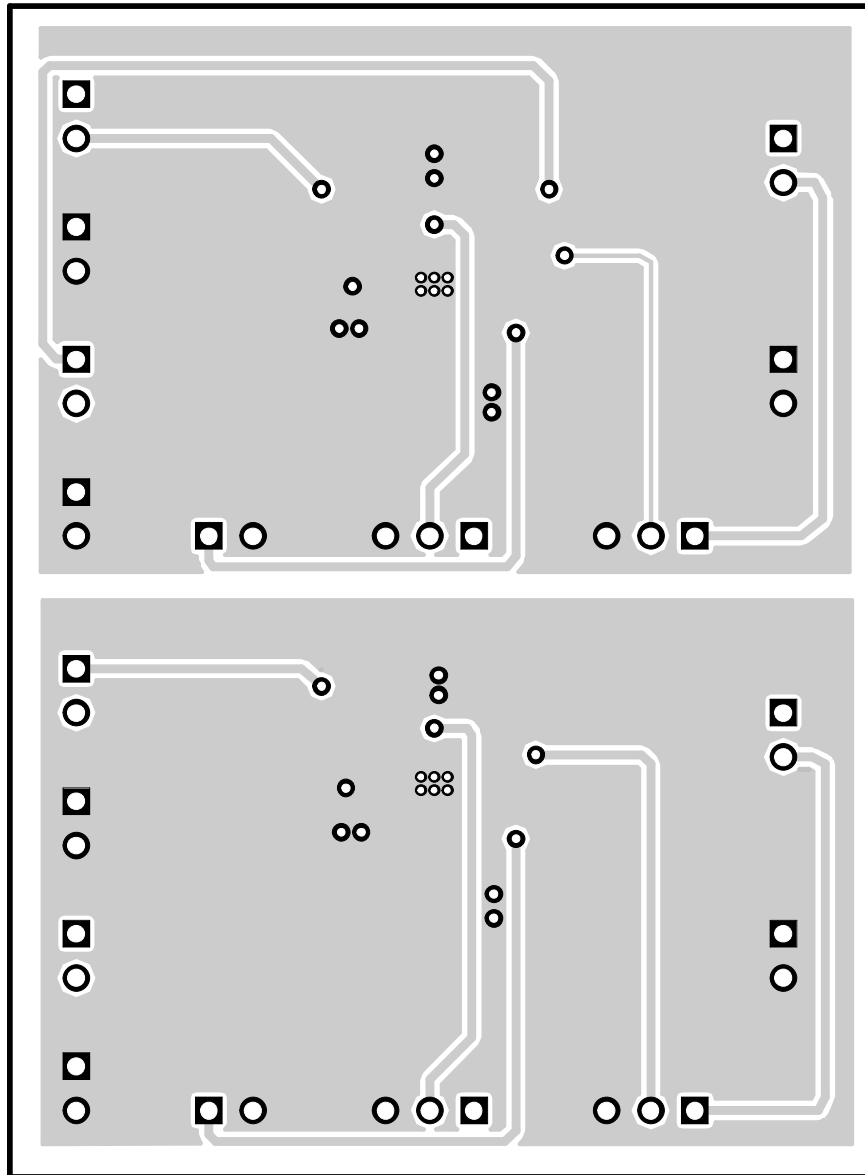
Figure 3. Bottom Layer Routing

5   Schematic and Bill of Materials

This section provides the TPS713xxEVM-050 schematic and bill of materials.

5.1   Schematic

Figure 4. TPS713xxEVM-050 Schematic

5.2 Bill of Materials

Table 1. TPS713xxEVM Bill of Materials

Count	Ref Des	Description	Size	Part Number	MFR
0	C1	Not populated	0603	—	
4	C2, C5, C7, C10	Capacitor, ceramic, 10-µF, 6.3-V, X5R, 10%	0805	C2012X5R0J106KT	TDK
2	C3, C8	Capacitor, ceramic, 1.0-µF, 6.3-V, X5R, 10%	0603	C1608X5R0J105KT	TDK
1	C4	Capacitor, ceramic, 22-pF, 50-V, C0G, 5%	0603	C1608C0G1H220J	TDK
2	C6, C11	Capacitor, ceramic, 0.01-µF, 25-V, X7R, 10%	0603	C1608X7R1E103KT	TDK
1	C9	Capacitor, ceramic, 100-pF, 50-V, C0G, 5%	0603	C1608C0G1H101J	TDK
14	J1 – J14	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 $\times$ 2	PTC36SAAN	Sullins
4	JP1 – JP4	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 $\times$ 3	PTC36SAAN	Sullins
0	R1	Not populated	0603	—	—
2	R2, R7	Resistor, chip, 100 kΩ, 1/16-W, 1%	0603	Std	Std
0	R3	Not populated	0603	—	—
1	R4	Resistor, chip, 31.6 kΩ, 1/16-W, 1%	0603	Std	Std
1	R5	Resistor, chip, 30.1 kΩ, 1/16-W, 1%	0603	Std	Std
0	R6, R10	Not populated	0603	—	—
1	R8	Resistor, chip, 7.15 kΩ, 1/16-W, 1%	0603	Std	Std
1	R9	Resistor, chip, 30.1 kΩ, 1/16-W, 1%	0603	Std	Std
1	U1	IC, dual 250 mA output, RF LDO regulator	QFN-10	TPS71319DRC	TI
1	U2	IC, dual 250 mA output, RF LDO regulator	QFN-10	TPS71334DRC	TI
1	—	PCB, 2.65 in $\times$ 1.95 in $\times$ 0.062 in	—	HPA050	Any
4	—	Shunt, 100 mil, black	0.100	929950-00	3M

FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE Liable to the other FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0V to 5.5V and the output voltage range of 1.225V to 5.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +125°C. The EVM is designed to operate properly with certain components up to +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

IMPORTANT NOTICE