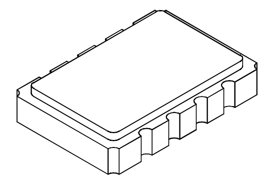
SC3040B

400.0 MHz Differential Sine-Wave Clock

- ***Quartz SAW Frequency Stability***
- ***Fundamental Fixed Frequency***
- ***Excellent Jitter and Symmetry***
- ***Rugged, Miniature, Surface-Mount Case***
- ***Low-Voltage Power Supply (3.3 VDC)***
- ***Directive 2002/95/EC (ROHS) Compliant by June, 2006***

This digital clock is designed for use in telecom applications; such as Timing for Terabit Router applications. Fundamental-mode oscillation is made possible by surface-acoustic-wave (SAW) technology. The design results in low jitter, compact size, and low power consumption. Differential outputs provide a sine wave that is made to drive 50 Ω loads.



SMC-8 Case

Absolute Maximum Ratings

Rating	Value	Units
Power Supply Voltage (V_{CC} at Terminal 1)	0 to +4.0	VDC
Input Voltage (ENABLE at Terminal 8)	0 to +4.0	VDC
Case Temperature (Powered or Storage)	-40 to +85	°C

Electrical Characteristics

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Output Frequency	Absolute Frequency	f_O	1, 2	399.920		400.080	MHz
	Tolerance from 400.000 MHz	Δf_O				±200	ppm
Q and $\overline{Q}$ Output	Power 50Ω (VSWR ≤ 1.2)	P_O	1, 3	0.5		5.5	dBm
	Operating Load VSWR					2:1	
	Symmetry		3, 4, 5	49		51	%
	Harmonic Spurious		3, 4, 6		-25	-20	dBc
	Nonharmonic Spurious					-60	dBc
Q and $\overline{Q}$ Period Jitter	No Noise on V_{CC}		3, 4, 6, 7		15	30	ps_{P-P}
	200 mV_{P-P} from 1 MHz to ½ f_O on		3, 4, 7, 8			35	ps_{P-P}
Output (Disabled)	Amplitude into 50 Ω		3, 9			75	mV_{P-P}
Output DC Resistance (between Q & $\overline{Q}$)			3	100			KΩ
ENABLE (Terminal 14)	Input HIGH Voltage	V_{IH}	3, 9	V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
	Input LOW Voltage	V_{IL}		0.0		0.20	V
	Input HIGH Current	I_{IH}			3	5	mA
	Input LOW Current	I_{IL}				-1	mA
	Propagation Delay	t_{PD}				1	ms
DC Power Supply	Operating Voltage	V_{CC}	1, 3	+3.13	+3.30	+3.47	VDC
	Operating Current	I_{CC}			18	40	mA
Operating Ambient Temperature		T_A	1, 3	0		+70	°C
Lid Symbolization (YY = Year, WW = Week)		RFM SC3040B 400.00 MHz YYWW					

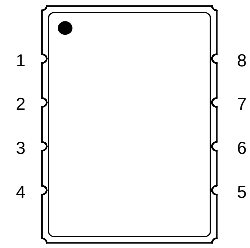
CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.

NOTES:

1. Unless otherwise noted, all specifications include any combination of load VSWR, VCC, and TA. In addition, Q and $\overline{Q}$ are terminated into 50 Ω loads to ground. (See: Typical Test Circuit.)
2. One or more of the following United States patents apply: 4,616,197; 4,670,681; 4,760,352.
3. The design, manufacturing process, and specifications of this device are subject to change without notice.
4. Only under the nominal conditions of 50 Ω load impedance with VSWR ≤ 1.2 and nominal power supply voltage.
5. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of Q or $\overline{Q}$. (See: Timing Definitions.)
6. Jitter and other spurious outputs induced by externally generated electrical noise on V_{CC} or mechanical vibration are not included. Dedicated external voltage regulation and careful PCB layout are recommended for optimum performance.
7. Applies to period jitter of Q and $\overline{Q}$. Measurements are made with the Tektronix CSA803 signal analyzer with at least 1000 samples.
8. Period jitter measured with a 200 mV_{P-P} sine wave swept from 1 MHz to one-half of f_O at the V_{CC} power supply terminal.
9. The outputs are enabled when Terminal 8 is at logic HIGH. Propagation delay is defined as the time from the 50% point on the rising edge of ENABLE to the 90% point on the rising edge of the output amplitude or as the fall time from the 50% point to the 10% point. (SEE: Timing Definitions.)

Electrical Connections

Terminal Number	Connection
1	V_{CC}
2	Ground
3	NC or Ground
4	Q Output
5	$\overline{Q}$ Output
6	Ground
7	Ground
8	ENABLE
LID	Ground

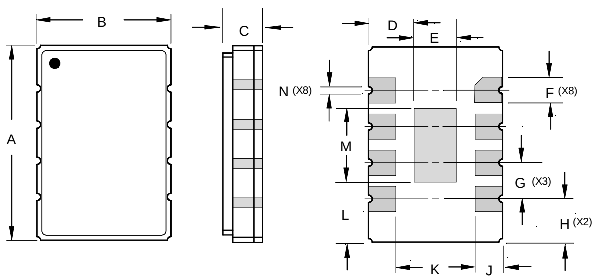


TOP VIEW

Case Design

All pads consist of 30 microinches (min) electroless gold on 50 microinches (min) electroless nickel over base metal. The metallic center pad was designed for mechanical support. Grounding of this pad is optional.

Lid symbolization, including terminal 1 locator dot, are in contrasting ink. Symbolization varies by model number. For purposes of illustration, only terminal 1 dot is shown.

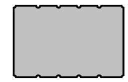


Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	13.46	13.97	0.530	0.550
B	9.14	9.66	0.360	0.380
C	2.05 Nominal		0.081 Nominal	
D	3.56 Nominal		0.141 Nominal	
E	2.24 Nominal		0.088 Nominal	
F	1.27 Nominal		0.050 Nominal	
G	2.54 Nominal		0.100 Nominal	
H	3.05 Nominal		0.120 Nominal	
J	1.93 Nominal		0.076 Nominal	
K	5.54 Nominal		0.218 Nominal	
L	4.32 Nominal		0.170 Nominal	
M	4.83 Nominal		0.190 Nominal	
N	0.50 Nominal		0.020 Nominal	

Materials	
Solder Pad Termination	Au plating 30 - 60 µinches (76.2-152 µm) over 80-200 µinches (203-508 µm) Ni.
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 µinches Thick
Body	Al_2O_3 Ceramic

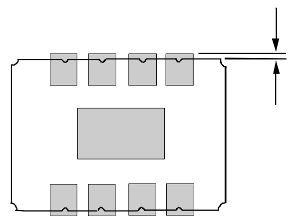
Footprint

Actual size footprint:



Typical Printed Circuit Board Land Pattern

A typical land pattern for a circuit board is shown below. Grounding of the metallic center pad is optional.



Typically 0.01" to 0.05" or 0.25 mm to 1.25 mm (8 Places)

(The optimum value of this dimension is dependent on the PCB assembly process employed.)

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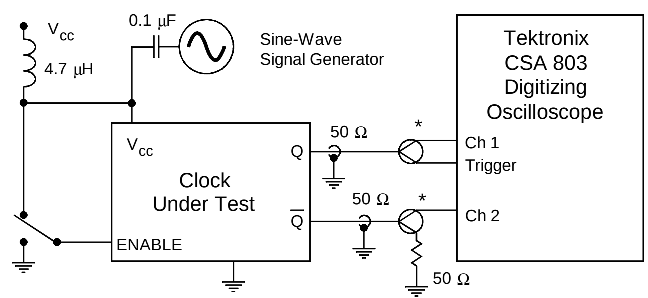
Typical Test Circuit



*Power Splitter, Mini-Circuits ZFSC2-4

Timing Definitions