# SCAN92LV090 9 Channel Bus LVDS Transceiver w/ Boundary SCAN

**Check for Samples: SCAN92LV090**

## FEATURES

- **IEEE 1149.1 (JTAG) Compliant**
- **Bus LVDS Signaling**
- **Low Power CMOS Design**
- **High Signaling Rate Capability (Above 100 Mbps)**
- **0.1V to 2.3V Common Mode Range for $V_{ID}$ = 200mV**
- **±100 mV Receiver Sensitivity**
- **Supports Open and Terminated Failsafe on Port Pins**
- **3.3V Operation**
- **Glitch Free Power Up/Down (Driver & Receiver Disabled)**
- **Light Bus Loading (5 pF Typical) per Bus LVDS Load**
- **Designed for Double Termination Applications**
- **Balanced Output Impedance**
- **Product Offered in 64 Pin LQFP Package and NFBGA Package**
- **High Impedance Bus Pins on Power Off ($V_{CC}$ = 0V)**

## DESCRIPTION

The SCAN92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is less than ±100 mV over a ±1V common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels.

This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCK), and the optional Test Reset (TRST).
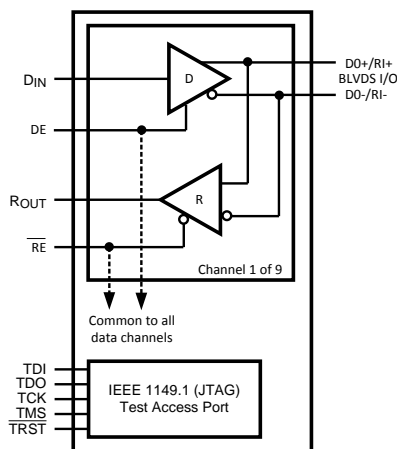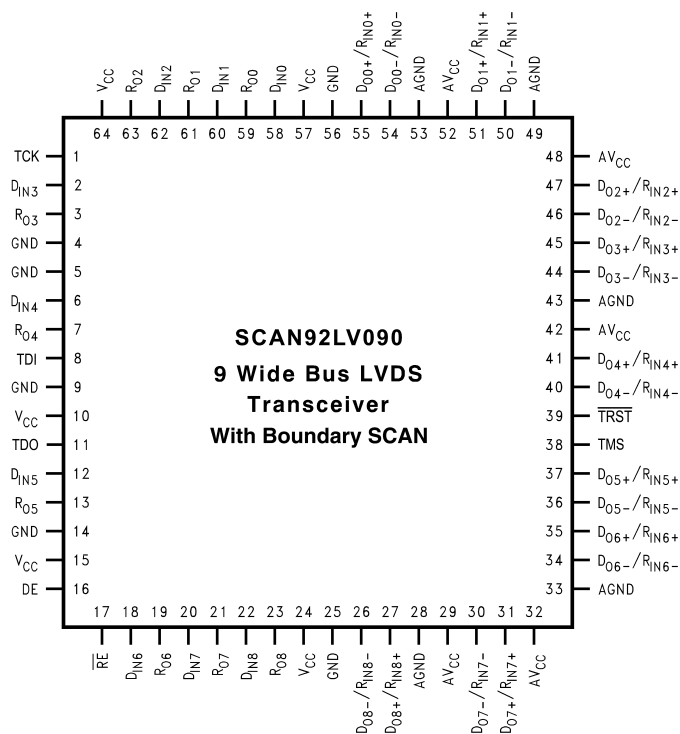
## SIMPLIFIED FUNCTIONAL DIAGRAM



**Figure 1.**

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## CONNECTION DIAGRAM



**Figure 2. Top View**
**Package Number PM0064**
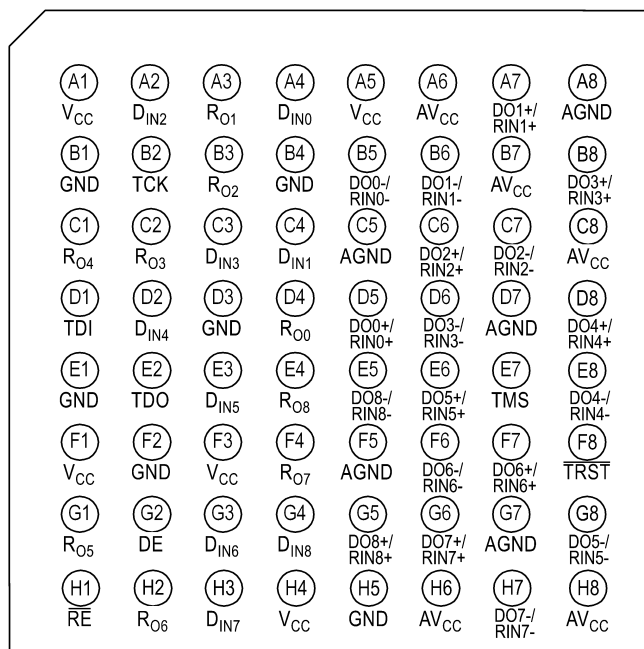


**Figure 3. Top View**
**Package Number NZC0064A**

## PINOUT DESCRIPTION

| Pin Name | LQFP Pin # | NFBGA Pin # | Input/Output | Descriptions |
|---|---|---|---|---|
| DO+/RI+ | 27, 31, 35, 37, 41, 45, 47, 51, 55 | A7, B8, C6, D5, D8, E6, F7, G5, G6 | I/O | True Bus LVDS Driver Outputs and Receiver Inputs. |
| DO−/RI− | 26, 30, 34, 36, 40, 44, 46, 50, 54 | B5, B6, C7, D6, E5, E8, F6, G8, H7 | I/O | Complimentary Bus LVDS Driver Outputs and Receiver Inputs. |
| $D_{IN}$ | 2, 6, 12, 18, 20, 22, 58, 60, 62 | A2, A4, C3, C4, D2, E3, G3, G4, H3 | I | TTL Driver Input. |
| RO | 3, 7, 13, 19, 21, 23, 59, 61, 63 | A3, B3, C1, C2, D4, E4, F4, G1, H2 | O | TTL Receiver Output. |
| $\overline{RE}$ | 17 | H1 | I | Receiver Enable TTL Input (Active Low). |
| DE | 16 | G2 | I | Driver Enable TTL Input (Active High). |
| GND | 4, 5, 9, 14, 25, 56 | B1, B4, D3, E1, F2, H5 | Power | Ground for digital circuitry (must connect to GND on PC board). These pins connected internally. |
| $V_{CC}$ | 10, 15, 24, 57, 64 | A1, A5, F1, F3, H4 | Power | $V_{CC}$ for digital circuitry (must connect to $V_{CC}$ on PC board). These pins connected internally. |
| AGND | 28, 33, 43, 49, 53 | A8, C5, D7, F5, G7 | Power | Ground for analog circuitry (must connect to GND on PC board). These pins connected internally. |
| $AV_{CC}$ | 29, 32, 42, 48, 52 | A6, B7, C8, H6, H8 | Power | Analog $V_{CC}$ (must connect to $V_{CC}$ on PC board). These pins connected internally. |
| $\overline{TRST}$ | 39 | F8 | I | Test Reset Input to support IEEE 1149.1 (Active Low) |
| TMS | 38 | E7 | I | Test Mode Select Input to support IEEE 1149.1 |
| TCK | 1 | B2 | I | Test Clock Input to support IEEE 1149.1 |
| TDI | 8 | D1 | I | Test Data Input to support IEEE 1149.1 |
| TDO | 11 | E2 | O | Test Data Output to support IEEE 1149.1 |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS [1][2][3]

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.0V |
| Enable Input Voltage (DE, $\overline{RE}$) | −0.3V to ($V_{CC}$ +0.3V) |
| Driver Input Voltage ($D_{IN}$) | −0.3V to ($V_{CC}$ +0.3V) |
| Receiver Output Voltage ($R_{OUT}$) | −0.3V to ($V_{CC}$ +0.3V) |
| Bus Pin Voltage (DO/RI±) | −0.3V to +3.9V |
| ESD (HBM 1.5 kΩ, 100 pF) | >4.5 kV |
| Driver Short Circuit Duration | momentary |
| Receiver Short Circuit Duration | momentary |
| Maximum Package Power Dissipation at 25°C | LQFP | 1.74 W |
| | Derate LQFP Package | 13.9 mW/°C |
| | $\theta_{ja}$ | 71.7°C/W |
| | $\theta_{jc}$ | 10.9°C/W |
| Junction Temperature | +150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | 260°C |

(1)   Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(2)   All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except $V_{OD}$, $\Delta V_{OD}$ and $V_{ID}$.
(3)   If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

## RECOMMENDED OPERATING CONDITIONS

|  |  | Min | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) |  | 3.0 | 3.6 | V |
| Receiver Input Voltage |  | 0.0 | 2.4 | V |
| Operating Free Air Temperature |  | −40 | +85 | °C |
| Maximum Input Edge Rate | (20% to 80%) [1] |  |  | Δt/ΔV |
|  | Data |  | 1.0 | ns/V |
|  | Control |  | 3.0 | ns/V |

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, $Z_O$ = 50Ω, $t_r$, $t_f$ = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating supply voltage and temperature ranges unless otherwise specified [1][2]

| Symbol | Parameter | Conditions | | Pin | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Output Differential Voltage | $R_L$ = 27Ω, See Figure 4 | | DO+/RI+, DO−/RI− | 240 | 300 | 460 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | | | 27 | mV |
| $V_{OS}$ | Offset Voltage | | | | 1.1 | 1.3 | 1.5 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change | | | | | 5 | 10 | mV |
| $V_{OH}$ | Driver Output High Voltage[3] | $R_L$ = 27Ω | | | | 1.4 | 1.65 | V |
| $V_{OL}$ | Driver Output Low Voltage[3] | $R_L$ = 27Ω | | | 0.95 | 1.1 | | V |
| $I_{OSD}$ | Output Short Circuit Current [4] | $V_{OD}$ = 0V, DE = $V_{CC}$, Driver outputs shorted together | | | | \|36\| | \|65\| | mA |
| $V_{OH}$ | Voltage Output High [5] | $V_{ID}$ = +300 mV | $I_{OH}$ = −400 µA | $R_{OUT}$ | $V_{CC}$−0.2 | | | V |
| | | Inputs Open | | | $V_{CC}$−0.2 | | | V |
| | | Inputs Terminated, $R_L$ = 27Ω | | | $V_{CC}$−0.2 | | | V |
| $V_{OL}$ | Voltage Output Low | $I_{OL}$ = 2.0 mA, $V_{ID}$ = −300 mV | | | | 0.05 | 0.075 | V |
| $I_{OD}$ | Receiver Output Dynamic Current [4] | $V_{ID}$ = 300mV, $V_{OUT}$ = $V_{CC}$−1.0V | | | −110 | \|75\| | | mA |
| | | $V_{ID}$ = −300mV, $V_{OUT}$ = 1.0V | | | | \|75\| | 110 | mA |
| $V_{TH}$ | Input Threshold High | DE = 0V, $V_{CM}$ = 1.5V | | DO+/RI+, DO−/RI− | | | +100 | mV |
| $V_{TL}$ | Input Threshold Low | | | | −100 | | | mV |
| $V_{CMR}$ | Receiver Common Mode Range | | | | \|$V_{ID}$\|/2 | | 2.4 − \|$V_{ID}$\|/2 | V |
| $I_{IN}$ | Input Current | DE = 0V, $\overline{RE}$ = 2.4V, $V_{IN}$ = +2.4V or 0V | | | −25 | ±1 | +25 | µA |
| | | $V_{CC}$ = 0V, $V_{IN}$ = +2.4V or 0V | | | −20 | ±1 | +20 | µA |
| $V_{IH}$ | Minimum Input High Voltage | | | $D_{IN}$, DE, $\overline{RE}$, TCK, $\overline{TRST}$, TMS, TDI | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Maximum Input Low Voltage | | | | GND | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{CC}$ or 2.4V | | $D_{IN}$, DE, $\overline{RE}$ | −20 | ±10 | +20 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = GND or 0.4V | | | −20 | ±10 | +20 | µA |
| $V_{CL}$ | Input Diode Clamp Voltage | $I_{CLAMP}$ = −18 mA | | | −1.5 | −0.8 | | V |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{CC}$ | | TDI, TMS, TCK, $\overline{TRST}$ | -20 | | +20 | µA |
| $I_{ILR}$ | Input Low Current | $V_{IN}$ = GND, $V_{CC}$ = 3.6v | | TDI, TMS, $\overline{TRST}$ | -25 | | -115 | µA |

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except $V_{OD}$, $\Delta V_{OD}$ and $V_{ID}$.
(2) All typicals are given for $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise stated.
(3) The SCAN92LV090 functions within datasheet specification when a resistive load is applied to the driver outputs.
(4) Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.
(5) $V_{OH}$ failsafe terminated test performed with 27Ω connected between RI+ and RI− inputs. No external voltage is applied.

Product Folder Links: *SCAN92LV090*

## DC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified [1][2]

| Symbol | Parameter | Conditions | Pin | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-----|-------|
| $I_{IL}$ | Input Low Current | VIN = GND | TCK | -20 | | +20 | µA |
| $I_{CCD}$ | Power Supply Current Drivers Enabled, Receivers Disabled | No Load, DE = $\overline{RE}$ = $V_{CC}$, DIN = $V_{CC}$ or GND | $V_{CC}$ | | 50 | 80 | mA |
| $I_{CCR}$ | Power Supply Current Drivers Disabled, Receivers Enabled | DE = $\overline{RE}$ = 0V, $V_{ID}$ = ±300mV | | | 50 | 80 | mA |
| $I_{CCZ}$ | Power Supply Current, Drivers and Receivers tri-state | DE = 0V; $\overline{RE}$ = $V_{CC}$, DIN = $V_{CC}$ or GND | | | 50 | 80 | mA |
| $I_{CC}$ | Power Supply Current, Drivers and Receivers Enabled | DE = $V_{CC}$; $\overline{RE}$ = 0V, DIN = $V_{CC}$ or GND, $R_L$ = 27Ω | | | 160 | 210 | mA |
| $I_{CCS}$ | Power Supply Current (SCAN Test Mode), Drivers and Receivers Enabled | DE = $V_{CC}$; $\overline{RE}$ = 0V, DIN = $V_{CC}$ or GND, $R_L$ = 27Ω, TAP in any state other than Test-Logic-Reset | | | 180 | 230 | mA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{CC}$ = 0V or OPEN, $D_{IN}$, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED}$ = 3.6V (Port Pins) | DO+/RI+, DO−/RI− | −20 | | +20 | µA |
| $C_{OUTPUT}$ | Capacitance @ Bus Pins | | DO+/RI+, DO−/RI− | | 5 | | pF |
| $C_{OUTPUT}$ | Capacitance @ $R_{OUT}$ | | $R_{OUT}$ | | 7 | | pF |

## AC ELECTRICAL CHARACTERISTICS

Over recommended operating supply voltage and temperature ranges unless otherwise specified [1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-------|
| **DIFFERENTIAL DRIVER TIMING REQUIREMENTS** | | | | | | |
| $t_{PHLD}$ | Differential Prop. Delay High to Low [2] | $R_L$ = 27Ω, See Figure 5 and Figure 6 $C_L$ = 10 pF | 1.0 | 1.8 | 2.6 | ns |
| $t_{PLHD}$ | Differential Prop. Delay Low to High [2] | | 1.0 | 1.8 | 2.6 | ns |
| $t_{SKD1}$ | Differential Skew $|t_{PHLD}−t_{PLHD}|$ [3] | | | 120 | | ps |
| $t_{SKD2}$ | Chip to Chip Skew [4] | | | | 1.6 | ns |
| $t_{SKD3}$ | Channel to Channel Skew [5] | | | 0.25 | 0.55 | ns |
| $t_{TLH}$ | Transition Time Low to High | | | 0.5 | 1.2 | ns |
| $t_{THL}$ | Transition Time High to Low | | | 0.5 | 1.2 | ns |
| $t_{PHZ}$ | Disable Time High to Z | $R_L$ = 27Ω, See Figure 7 and Figure 8 $C_L$ = 10 pF | | 3 | 8 | ns |
| $t_{PLZ}$ | Disable Time Low to Z | | | 3 | 8 | ns |
| $t_{PZH}$ | Enable Time Z to High | | | 3 | 8 | ns |
| $t_{PZL}$ | Enable Time Z to Low | | | 3 | 8 | ns |
| **DIFFERENTIAL RECEIVER TIMING REQUIREMENTS** | | | | | | |
| $t_{PHLD}$ | Differential Prop. Delay High to Low [2] | See Figure 9 and Figure 10 $C_L$ = 35 pF | 2.0 | 2.4 | 3.9 | ns |
| $t_{PLHD}$ | Differential Prop Delay Low to High [2] | | 2.0 | 2.4 | 3.9 | ns |
| $t_{SDK1}$ | Differential Skew $|t_{PHLD}−t_{PLHD}|$ [3] | | | 210 | | ps |
| $t_{SDK2}$ | Chip to Chip Skew [4] | | | | 1.9 | ns |
| $t_{SDK3}$ | Channel to Channel skew [5] | | | 0.35 | 0.7 | ns |
| $t_{TLH}$ | Transition Time Low to High | | | 1.5 | 2.5 | ns |
| $t_{THL}$ | Transition Time High to Low | | | 1.5 | 2.5 | ns |

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, $Z_O$ = 50Ω, $t_r$, $t_f$ = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.
(2) Propagation delays are specified by design and characterization.
(3) $t_{SKD1}$ $|t_{PHLD}−t_{PLHD}|$ is the worse case skew between any channel and any device over recommended operation conditions.
(4) Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.
(5) Channel to Channel skew is the difference in driver output or receiver output propagation delay between any channels within a device, common edge.

## AC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified [1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-----------|------------|-----|-----|-----|-------|
| $t_{PHZ}$ | Disable Time High to Z | $R_L = 500\Omega$, See Figure 11 and Figure 12 $C_L = 35$ pF | | 4.5 | 10 | ns |
| $t_{PLZ}$ | Disable Time Low to Z | | | 3.5 | 8 | ns |
| $t_{PZH}$ | Enable Time Z to High | | | 3.5 | 8 | ns |
| $t_{PZL}$ | Enable Time Z to Low | | | 3.5 | 8 | ns |
| **SCAN CIRCUITRY TIMING REQUIREMENTS** | | | | | | |
| $f_{MAX}$ | Maximum TCK Clock Frequency | $R_L = 500\Omega$, $C_L = 35$ pF | 25.0 | 75.0 | | MHz |
| $t_S$ | TDI to TCK, H or L | | 1.5 | | | ns |
| $t_H$ | TDI to TCK, H or L | | 1.5 | | | ns |
| $t_S$ | TMS to TCK, H or L | | 2.5 | | | ns |
| $t_H$ | TMS to TCK, H or L | | 1.5 | | | ns |
| $t_W$ | TCK Pulse Width, H or L | | 10.0 | | | ns |
| $t_W$ | $\overline{TRST}$ Pulse Width, L | | 2.5 | | | ns |
| $t_{REC}$ | Recovery Time, $\overline{TRST}$ to TCK | | 2.0 | | | ns |

Product Folder Links: *SCAN92LV090*

## APPLICATIONS INFORMATION

General application guidelines and hints may be found in the following application notes: AN-808 (SNLA028), AN-1108 (SNLA008), AN-977 (SNLA166), AN-971 (SNLA165), and AN-903 (SNLA034).

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Two or three high frequency, multi-layer ceramic (MLC) surface mount (0.1 µF, 0.01 µF, 0.001 µF) in parallel should be used between each $V_{CC}$ and ground. The capacitors should be as close as possible to the $V_{CC}$ pin.
    - Multiple vias should be used to connect $V_{CC}$ and Ground planes to the pads of the by-pass capacitors.
    - In addition, randomly distributed by-pass capacitors should be used.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.
- Isolate TTL signals from Bus LVDS signals

MEDIA (CONNECTOR or BACKPLANE) SELECTION:

- Use controlled impedance media. The backplane and connectors should have a matched differential impedance.

### Table 1. Functional Table

| MODE SELECTED | DE | $\overline{RE}$ |
|---|---|---|
| DRIVER MODE | H | H |
| RECEIVER MODE | L | L |
| tri-state MODE | L | H |
| LOOP BACK MODE | H | L |

### Table 2. Transmitter Mode

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| DE | $D_{IN}$ | DO+ | DO− |
| H | L | L | H |
| H | H | H | L |
| H | $0.8V< D_{IN} <2.0V$ | X | X |
| L | X | Z | Z |

### Table 3. Receiver Mode[1]

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{RE}$ | (RI+) − (RI−) | |
| L | L (< −100 mV) | L |
| L | H (> +100 mV) | H |
| L | −100 mV < $V_{ID}$ < +100 mV | X |
| H | X | Z |

(1)  X = High or Low logic state
    L = Low state
    Z = High impedance state
    H = High state

## TEST CIRCUITS AND TIMING WAVEFORMS
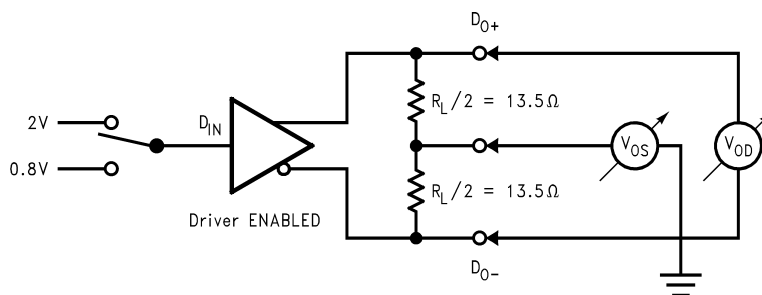


**Figure 4. Differential Driver DC Test Circuit**
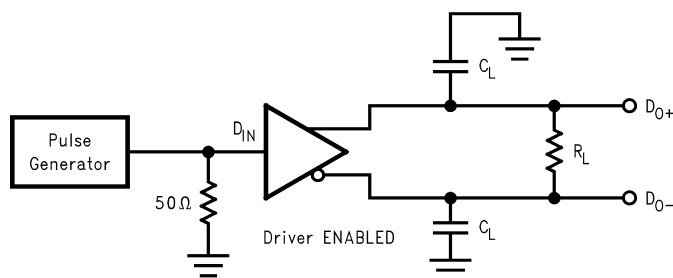


**Figure 5. Differential Driver Propagation Delay and Transition Time Test Circuit**
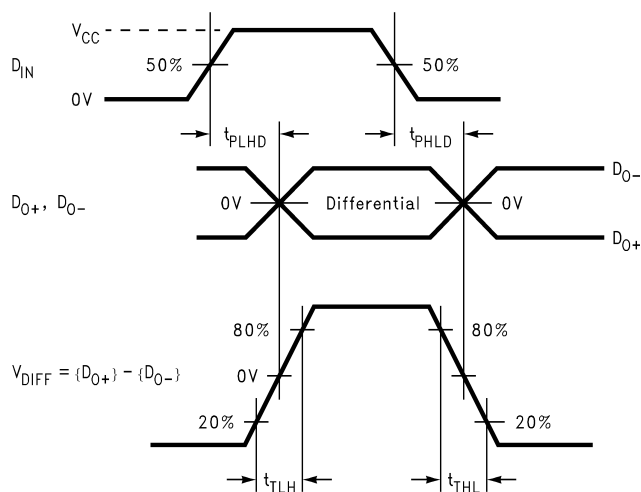


**Figure 6. Differential Driver Propagation Delay and Transition Time Waveforms**

Product Folder Links: *SCAN92LV090*
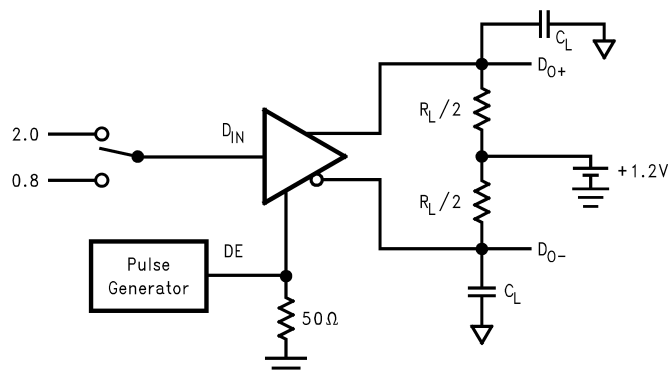
**Figure 7. Driver Tri-State Delay Test Circuit**
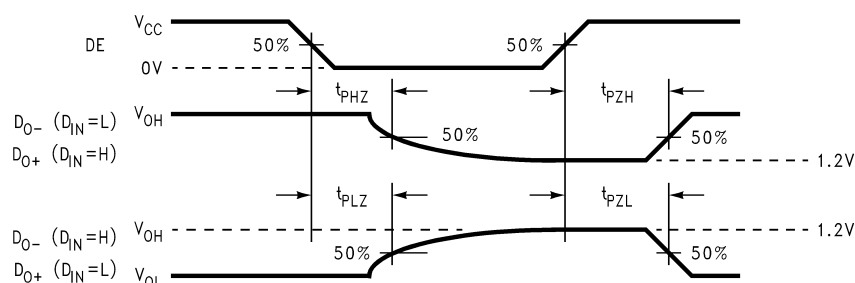


**Figure 8. Driver Tri-State Delay Waveforms**
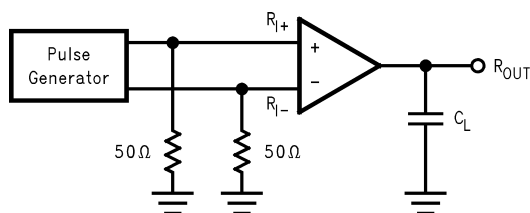


**Figure 9. Receiver Propagation Delay and Transition Time Test Circuit**
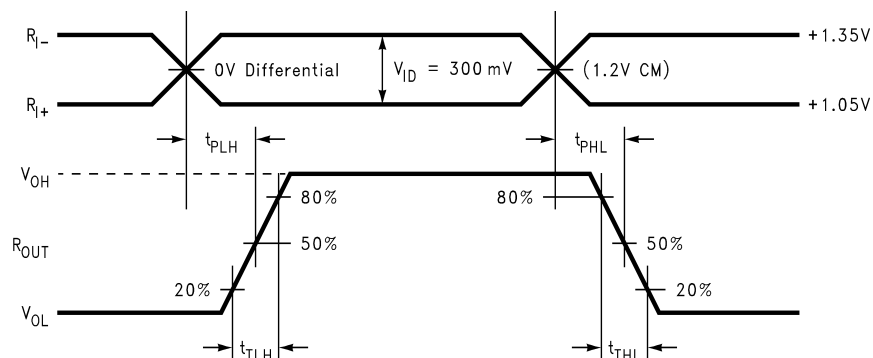


**Figure 10. Receiver Propagation Delay and Transition Time Waveforms**
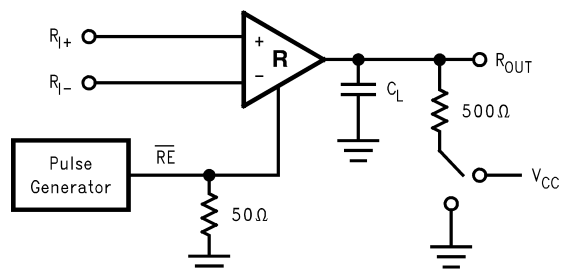
**Figure 11. Receiver Tri-State Delay Test Circuit**
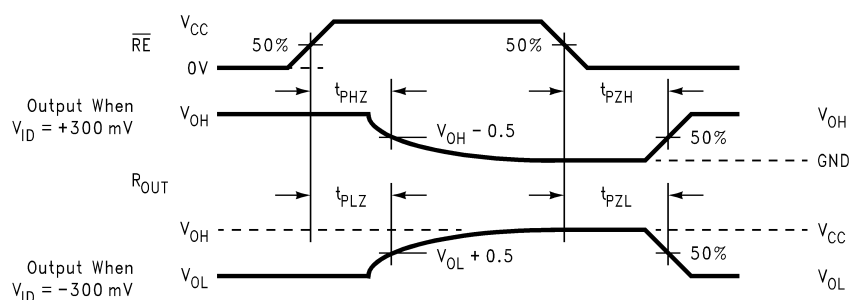


**Figure 12. Receiver Tri-State Delay Waveforms**

## TYPICAL BUS APPLICATION CONFIGURATIONS
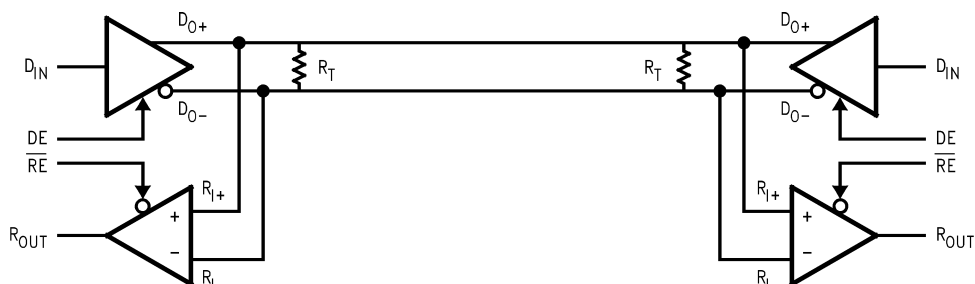


**Figure 13. Bi-Directional Half-Duplex Point-to-Point Applications**
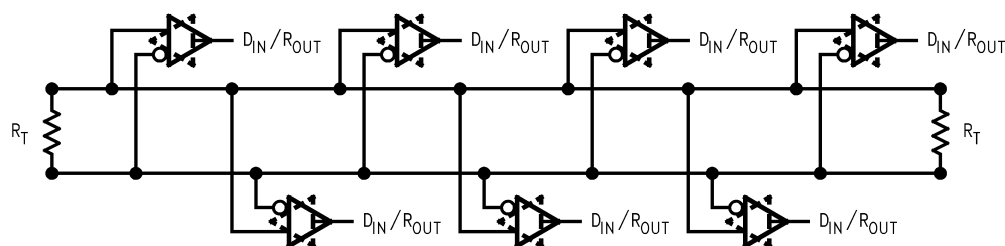


**Figure 14. Multi-Point Bus Applications**

Product Folder Links: *SCAN92LV090*

## DESCRIPTION OF BOUNDARY-SCAN CIRCUITRY

The SCAN92LV090 features two unique Scan test modes, each which requires a unique BSDL model depending on the level of test access and fault coverage goals. In the first mode (Mode0), only the TTL Inputs and Outputs of each transceiver are accessible via a 1149.1 compliant protocol. In the second mode (Mode1), both the TTL Inputs and Outputs and the differential LVDS I/Os are included in the Scan chain.

All test modes are handled by the ATPG software, and BSDL selection should be invisible to the user.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.
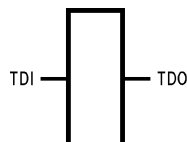


**Figure 15. Bypass Register Scan Chain Definition
Logic 0**

The INSTRUCTION register is an eight-bit register which captures the value 00111101.
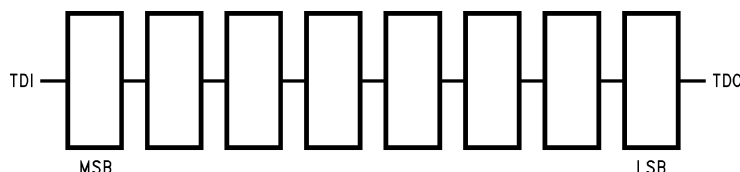


**Figure 16. Instruction Register Scan Chain Definition**

### Table 4. MSB → LSB (Mode0)

| Instruction Code | Instruction |
| --- | --- |
| 00000000 | EXTEST |
| 10000010 | SAMPLE/PRELOAD |
| 10000111 | CLAMP |
| 00000110 | HIGHZ |
| All Others | BYPASS |

### Table 5. MSB → LSB (Mode1)

| Instruction Code | Instruction |
| --- | --- |
| 10011001 | EXTEST |
| 10010010 | SAMPLE/PRELOAD |
| 10001111 | CLAMP |
| 00000110 | HIGHZ |
| All Others | BYPASS |
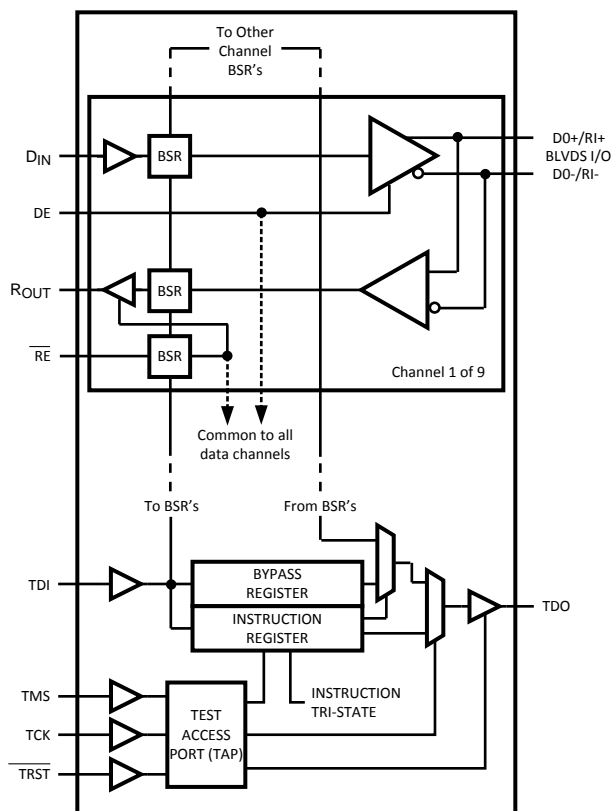
**Figure 17. Mode 0 Boundary Scan Register Configuration**
**(Refer to the BSDL for exact register order)**
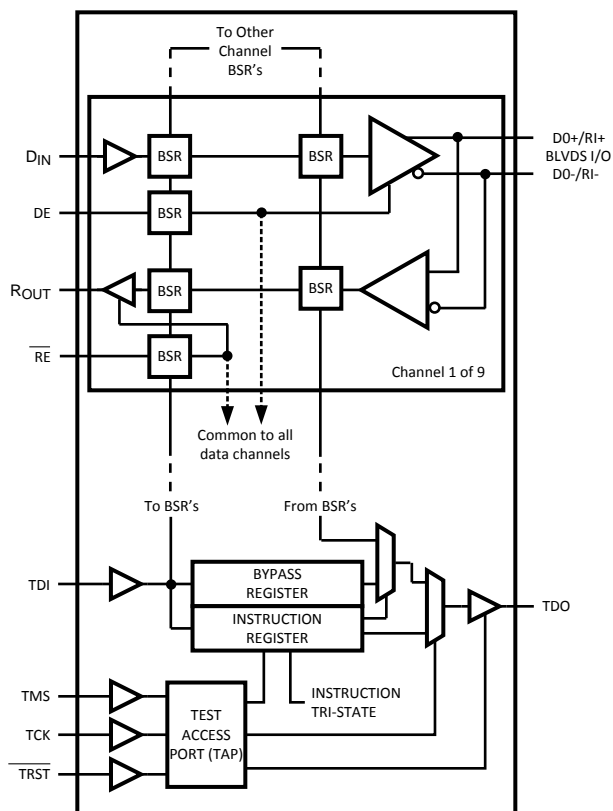
**Figure 18. Mode 1 Boundary Scan Register Configuration
(Refer to the BSDL for exact register order)**

# REVISION HISTORY

**Changes from Revision H (April 2013) to Revision I**                                                                                                          **Page**

![Texas Instruments logo]

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SCAN92LV090SLC | NRND | NFBGA | NZC | 64 | 360 | TBD | Call TI | Call TI | -40 to 85 | SCAN92LV090 SLC | |
| SCAN92LV090SLC/NOPB | ACTIVE | NFBGA | NZC | 64 | 360 | Green (RoHS & no Sb/Br) | SNAGCU | Level-4-260C-72 HR | -40 to 85 | SCAN92LV090 SLC | Samples |
| SCAN92LV090VEH/NOPB | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | SN \| CU SN | Level-3-260C-168 HR | -40 to 85 | SCAN92LV090 VEH | Samples |
| SCAN92LV090VEHX/NOPB | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | SCAN92LV090 VEH | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
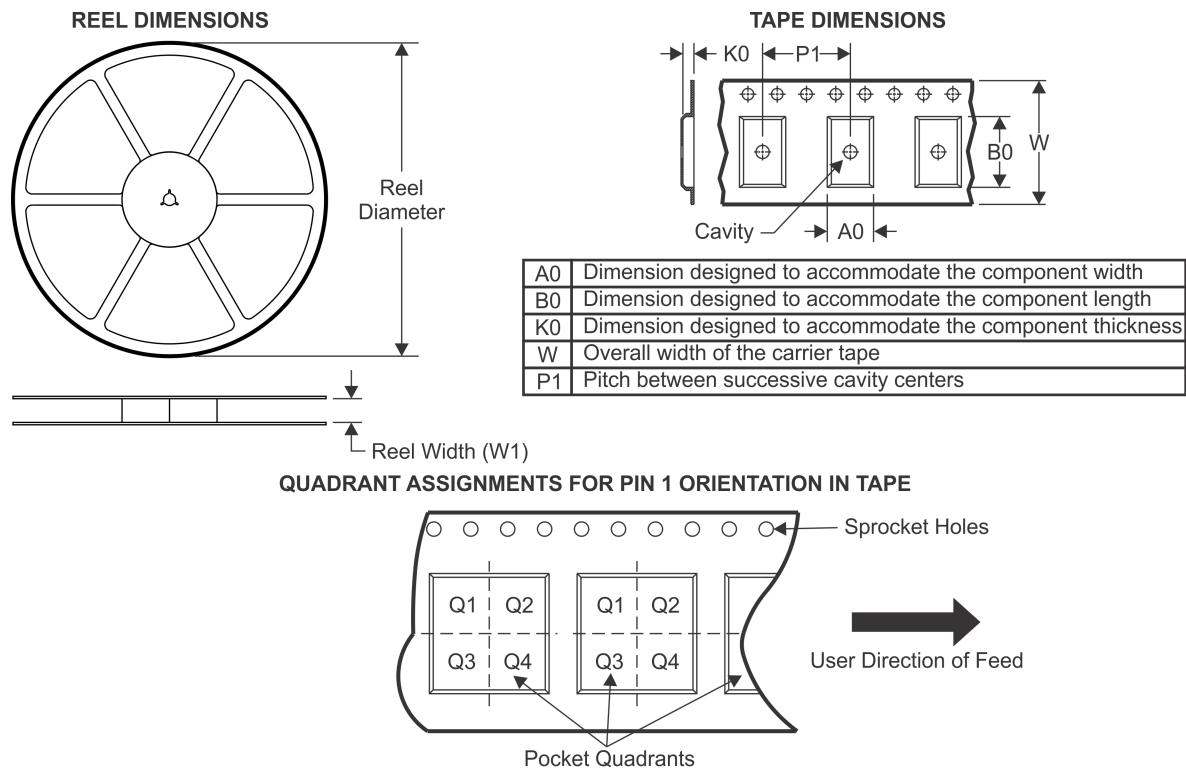
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SCAN92LV090VEHX/NOPB | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 12.35 | 12.35 | 2.2 | 16.0 | 24.0 | Q2 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SCAN92LV090VEHX/NOPB | LQFP | PM | 64 | 1000 | 367.0 | 367.0 | 45.0 |

# NZC0064A



DIMENSIONS ARE IN MILLIMETERS

SLC64A (Rev C)
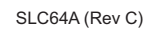
**PM (S-PQFP-G64)**                                        **PLASTIC QUAD FLATPACK**



4040152/C 11/96
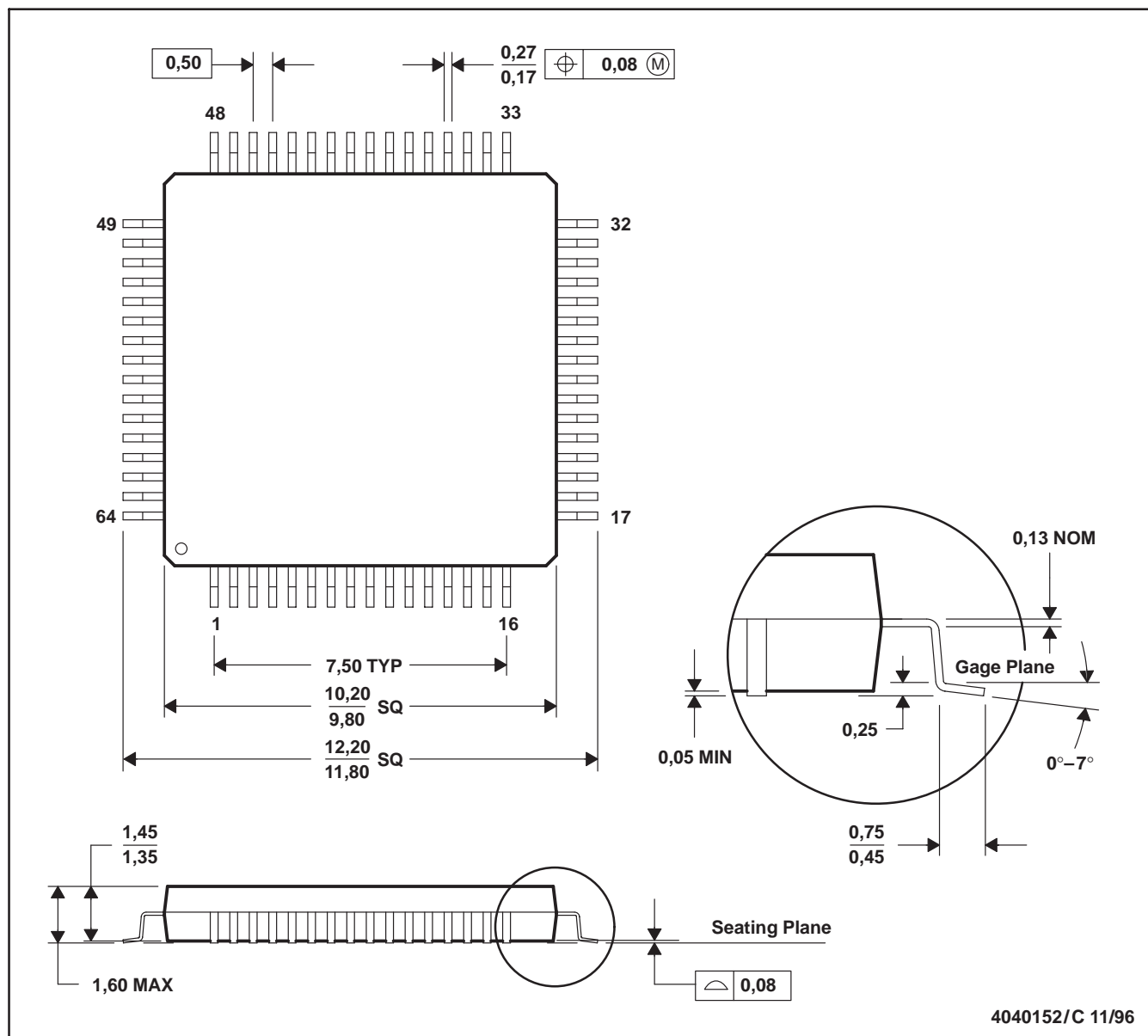
NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Falls within JEDEC MS-026
            D. May also be thermally enhanced plastic with leads connected to the die pads.

1

# IMPORTANT NOTICE

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
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