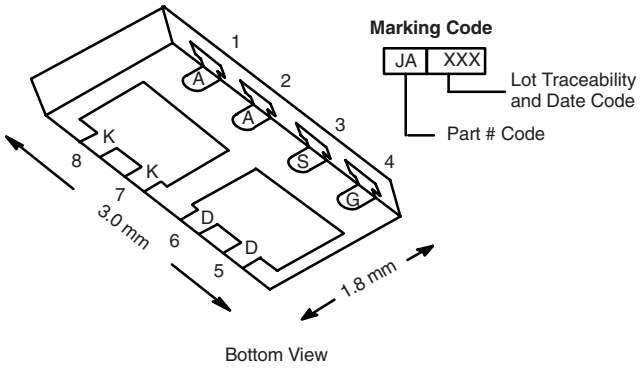
P-Channel 20-V (D-S) MOSFET with Schottky Diode

MOSFET PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
- 20	0.058 at V_{GS} = - 4.5 V	6	5.5 nC
	0.100 at V_{GS} = - 2.5 V	6	

SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_F (V) Diode Forward Voltage	I_F (A)[a]
20	0.375 at 1 A	2

PowerPAK® ChipFET® Dual



Bottom View

Ordering Information: Si5857DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

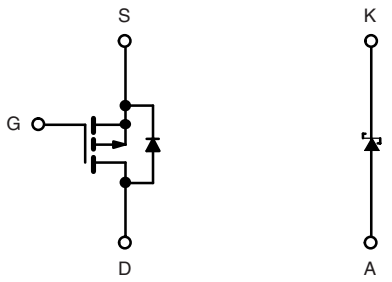
FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- LITTLE FOOT® *Plus* Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.8 mm Profile
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Charging Switch for Portable Devices
  - With Integrated Low V_F Trench Schottky Diode



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage (MOSFET)		V_{DS}	- 20	V
Reverse Voltage (Schottky)		V_{KA}	20	
Gate-Source Voltage (MOSFET)		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C) (MOSFET)	T_C = 25 °C	I_D	6[a]	A
	T_C = 70 °C		6[a]	
	T_A = 25 °C		- 5[b, c]	
	T_A = 70 °C		- 4[b, c]	
Pulsed Drain Current (MOSFET)		I_{DM}	- 20	
Continuous Source Current (MOSFET Diode Conduction)	T_C = 25 °C	I_S	- 6[a]	
	T_A = 25 °C		1.9[b, c]	
Average Forward Current (Schottky)		I_F	2	
Pulsed Forward Current (Schottky)		I_{FM}	7	
Maximum Power Dissipation (MOSFET)	T_C = 25 °C	P_D	10.4	W
	T_C = 70 °C		6.7	
	T_A = 25 °C		2.3[b, c]	
	T_A = 70 °C		1.5[b, c]	
Maximum Power Dissipation (Schottky)	T_C = 25 °C	P_D	7.8	W
	T_C = 70 °C		5	
	T_A = 25 °C		2.1[b, c]	
	T_A = 70 °C		1.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendation (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[b, f]	t ≤ 5 s	R_{thJA}	43	55	°C/W
Maximum Junction-to-Case (Drain) (MOSFET)		R_{thJC}	9.5	12	
Maximum Junction-to-Ambient (Schottky)[b, g]	t ≤ 5 s	R_{thJA}	49	61	
Maximum Junction-to-Case (Drain) (Schottky)		R_{thJC}	13	16	

Notes:
a. Package limited.
b. Surface Mounted on FR4 board.
c. t ≤ 5 s.
d. See Solder Profile (*www.vishay.com/doc?73257*). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions for MOSFETS is 105 °C/W.
g. Maximum under Steady State conditions for Schottky is 110 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS/TJ}$	I_D = - 250 µA		- 19		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)/TJ}$			2.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.6		- 1.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	ns
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 4.5 V	- 20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 3.6 A		0.048	0.058	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.081	0.100	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 3.6 A		10		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		480		pF
Output Capacitance	C_{oss}			125		
Reverse Transfer Capacitance	C_{rss}			90		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 5 A		11	17	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 5 A		5.5	8.5	
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.8		
Gate Resistance	R_g	f = 1 MHz		9		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 2.5 Ω I_D ≅ - 4 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		11	20	ns
Rise Time	t_r			42	65	
Turn-Off Delay Time	$t_{d(off)}$			33	50	
Fall Time	t_f			50	75	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 2.5 Ω I_D ≅ - 4 A, V_{GEN} = - 10 V, R_g = 1 Ω		5	10	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			10	20	

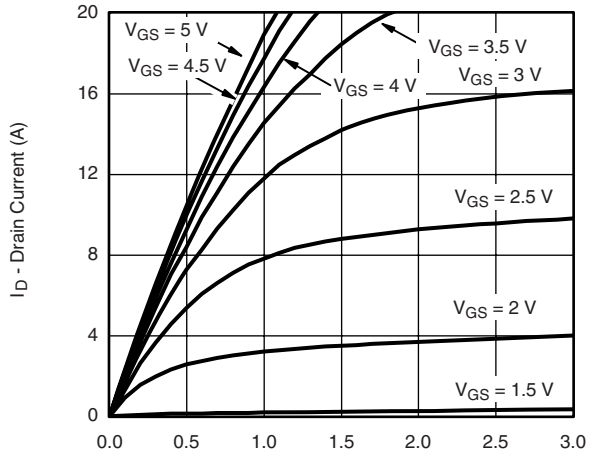
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 6	A
Pulse Diode Forward Current	I_{SM}				- 20	
Body Diode Voltage	V_{SD}	I_S = - 4 A, V_{GS} = 0 V		- 0.9	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 4 A dI/dt = 100 A/µs TJ = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	20	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			16		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

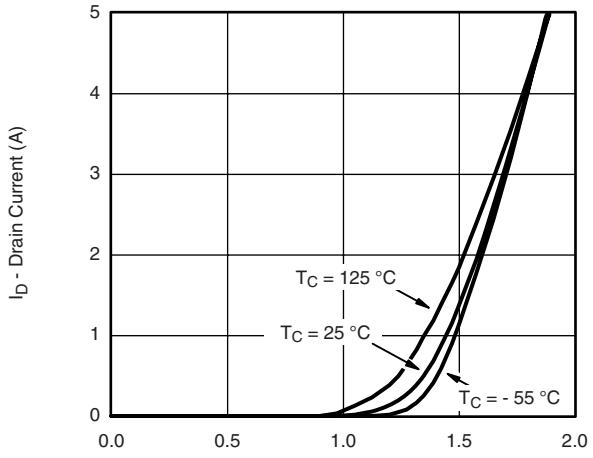
SCHOTTKY SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Forward Voltage Drop	V_F	I_F = 1 A		0.34	0.375	V
		I_F = 1 A, T_J = 125 °C		0.255	0.290	
Maximum Reverse Leakage Current	I_{rm}	V_R = 20 V		0.05	0.500	mA
		V_R = 20 V, T_J = 85 °C		2	20	
		V_R = 20 V, T_J = 125 °C		10	100	
Junction Capacitance	C_T	V_R = 10 V		90		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

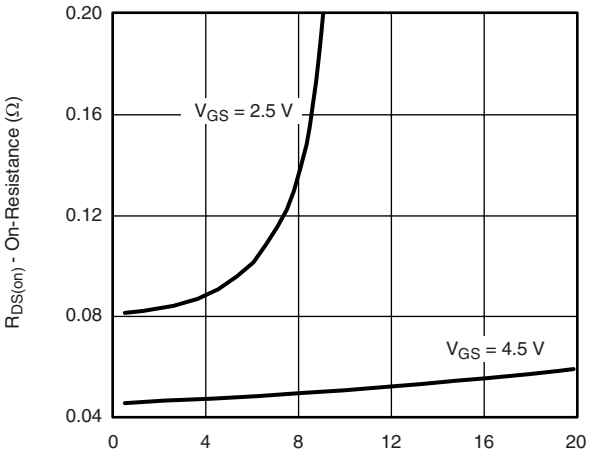
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



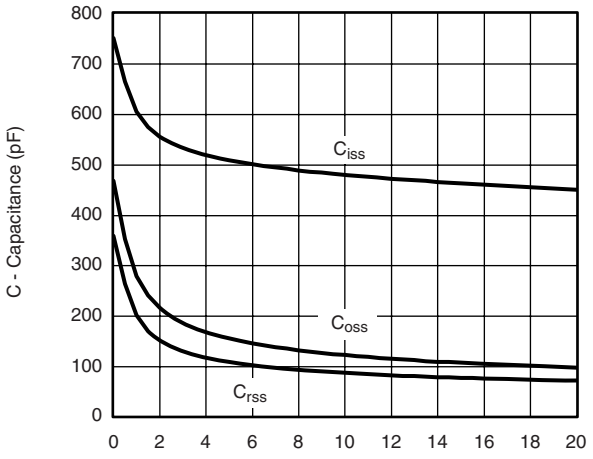
Output Characteristics



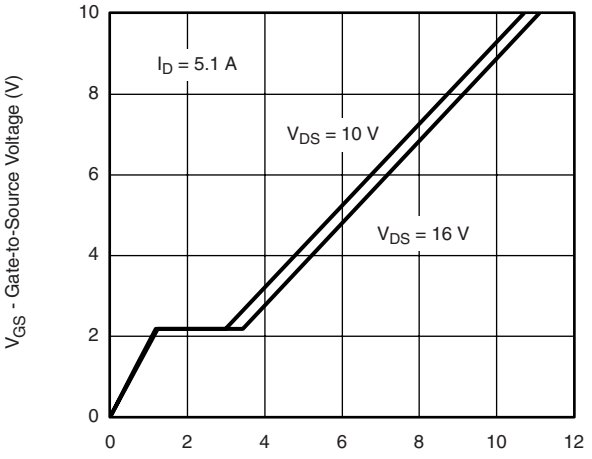
Transfer Characteristics



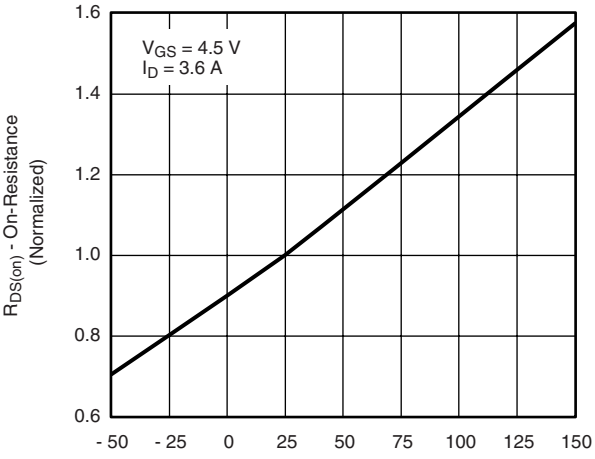
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

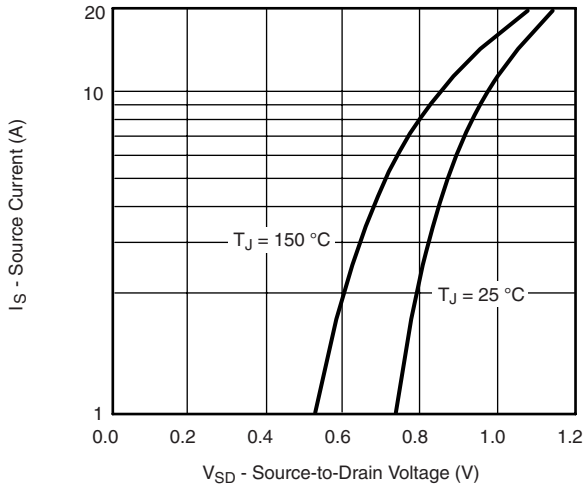


Gate Charge

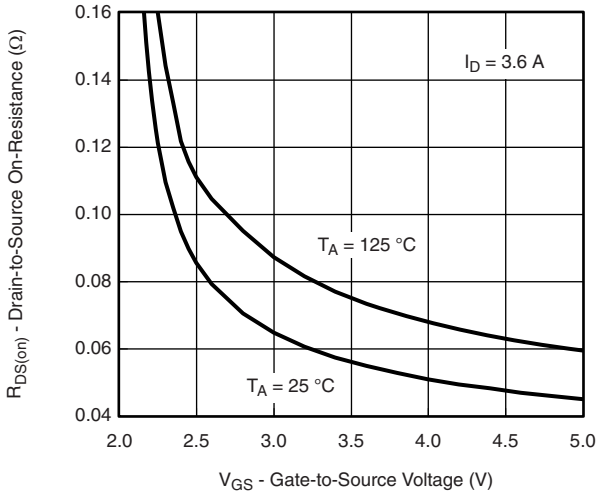


On-Resistance vs. Junction Temperature

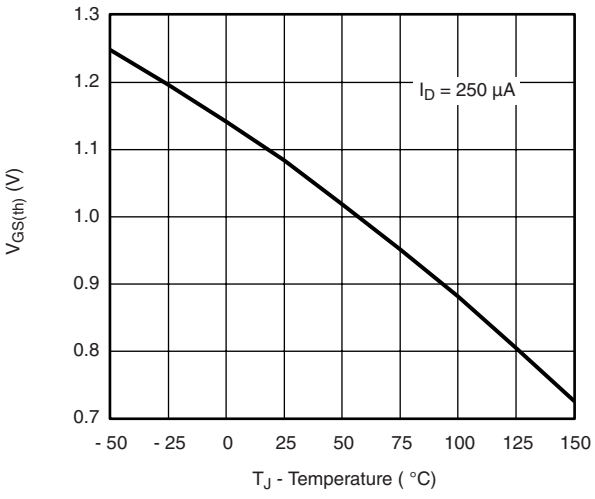
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



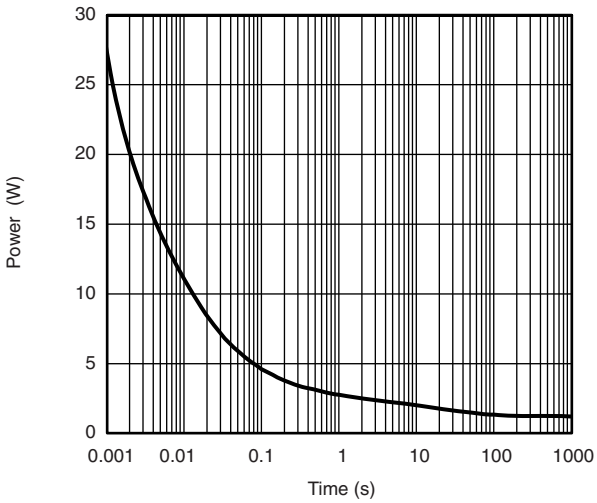
Source-Drain Diode Forward Voltage



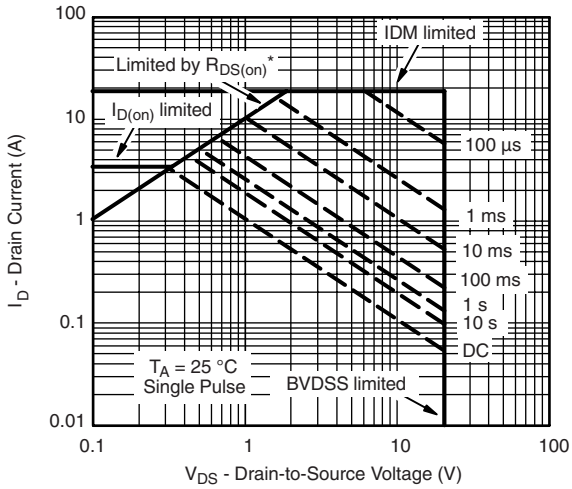
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



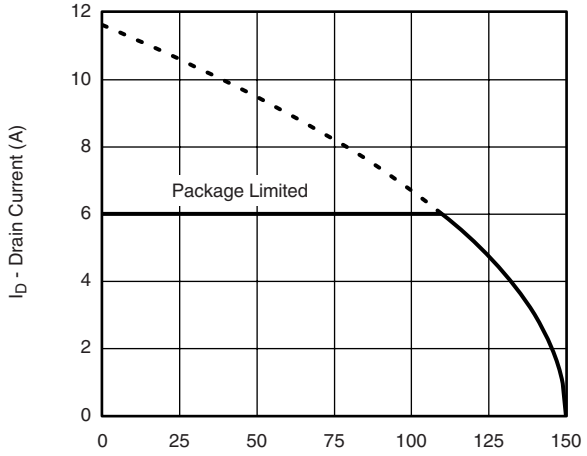
Single Pulse Power, Junction-to-Ambient



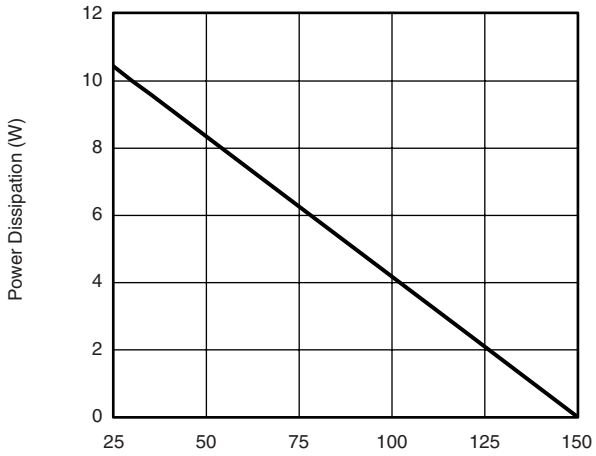
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



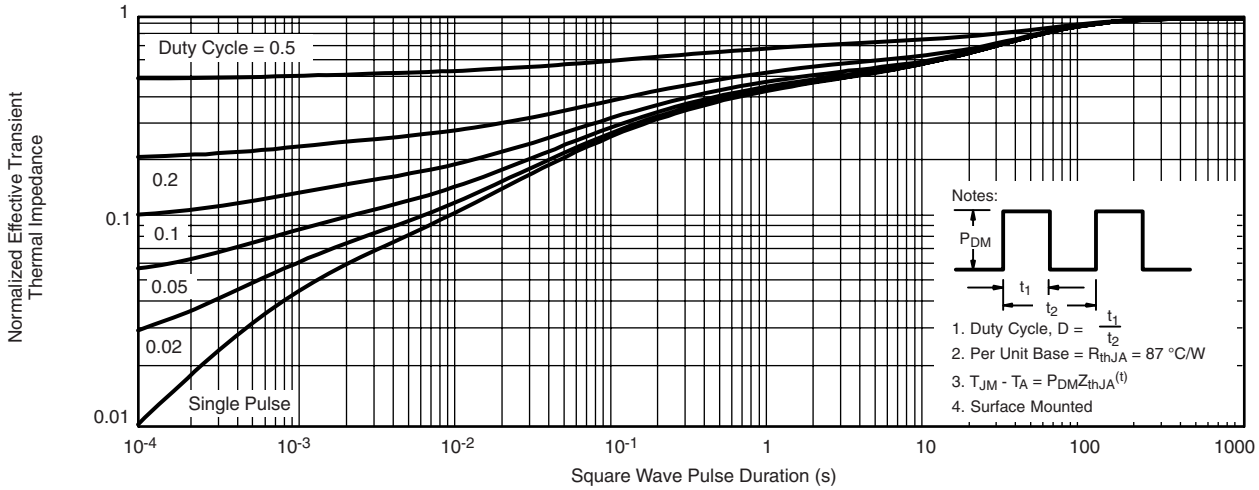
Current Derating*



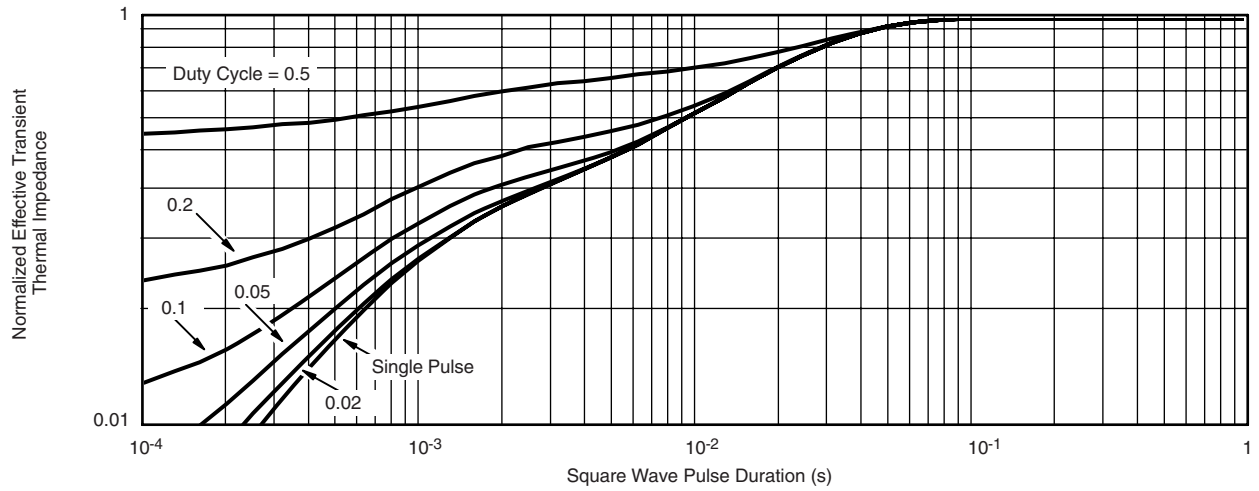
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

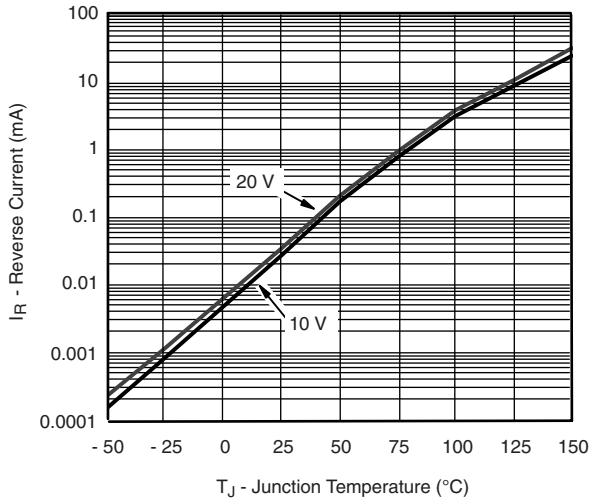


Normalized Thermal Transient Impedance, Junction-to-Ambient

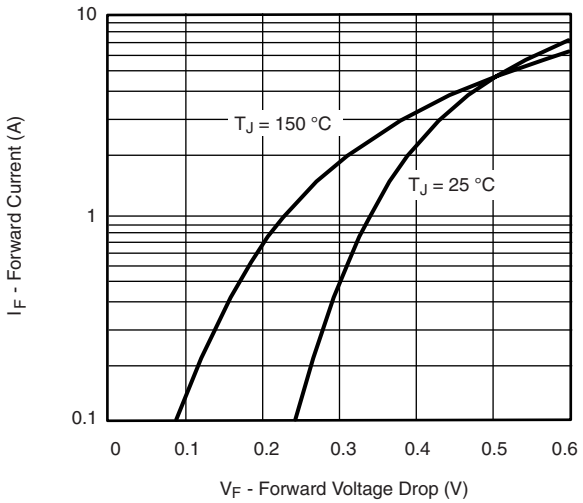


Normalized Thermal Transient Impedance, Junction-to-Case

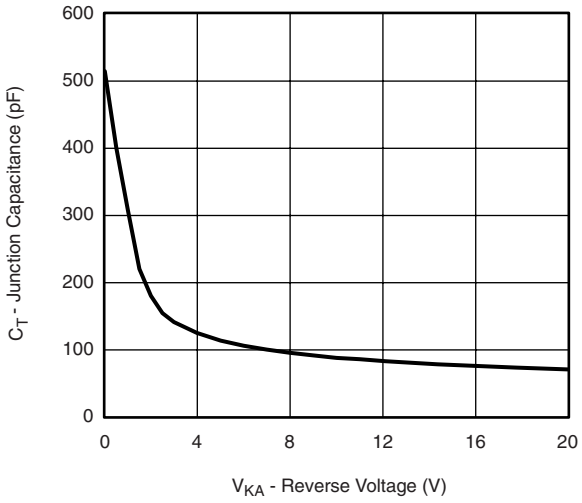
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Reverse Current vs. Junction Temperature

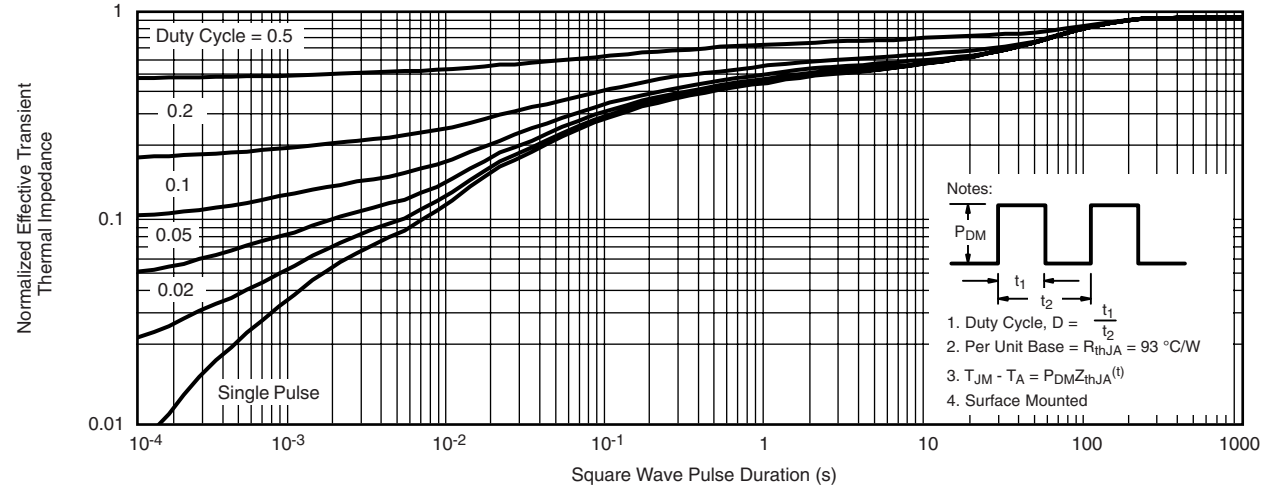


Forward Voltage Drop

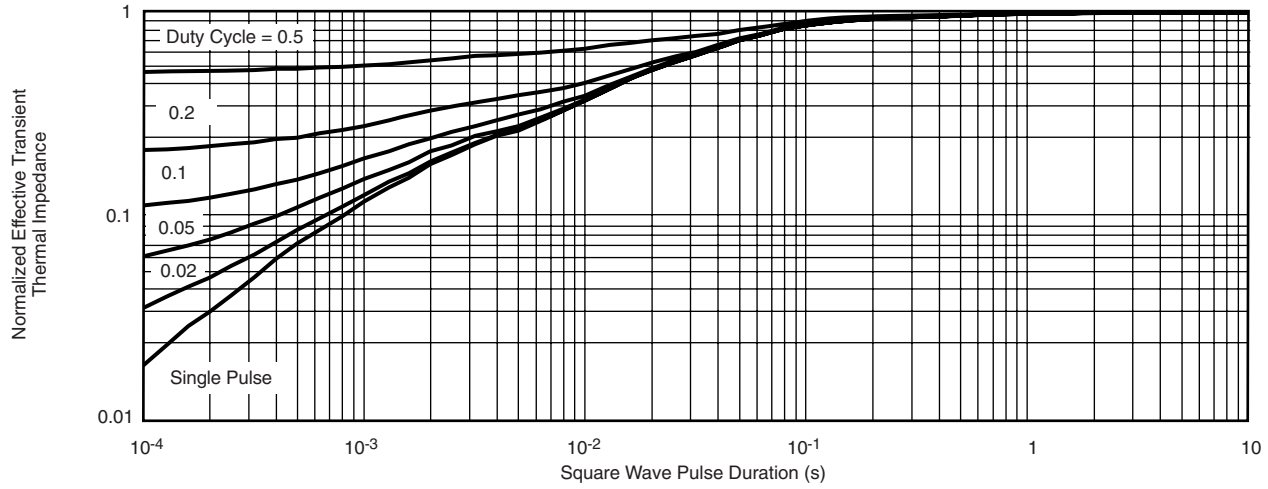


Capacitance

SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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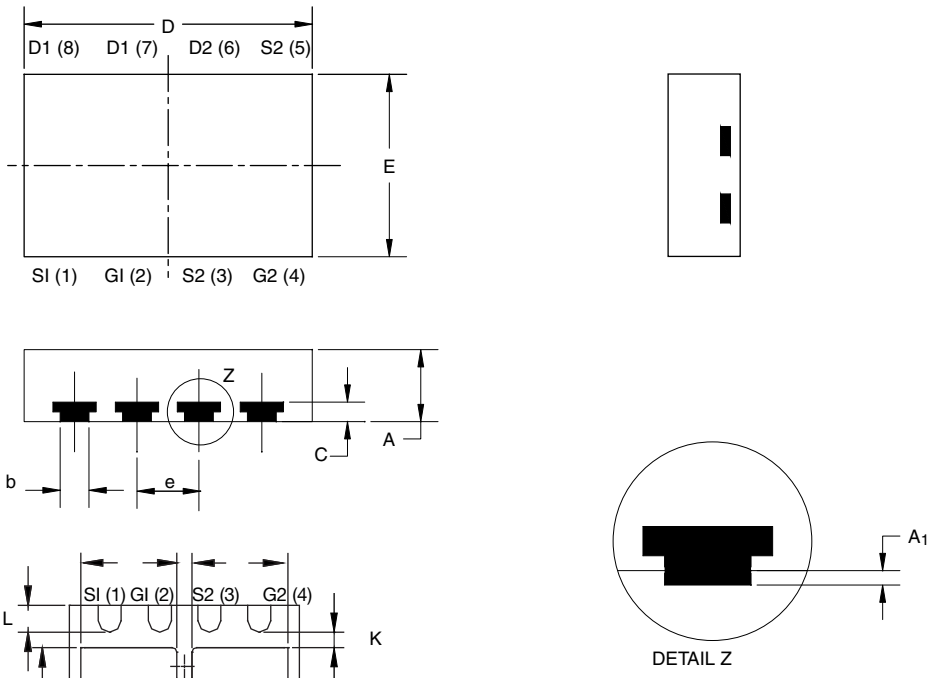
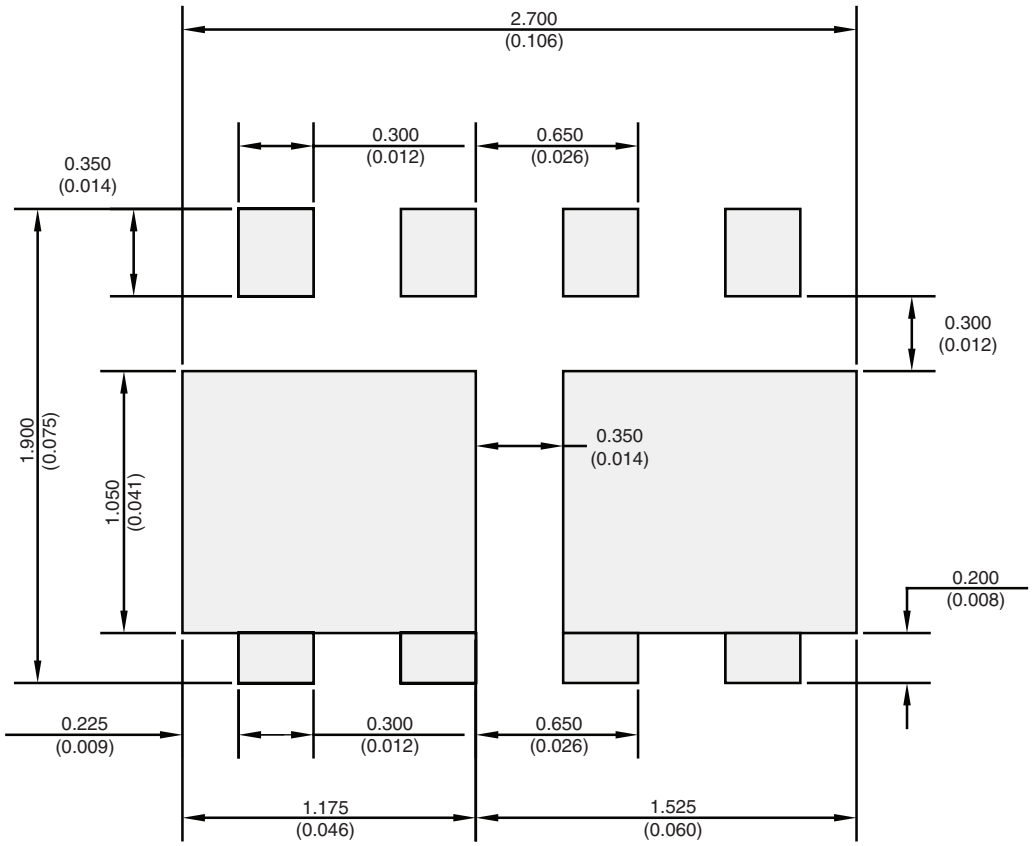
PowerPAK® ChipFET® DUAL PAD



Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A_1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D_2	1.07	1.20	1.32	0.042	0.047	0.052
E	1.82	1.90	1.98	0.072	0.075	0.078
E_2	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K_1	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
ECN: C10-0618-Rev. C, 19-Jul-10 DWG: 5940						

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner

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