

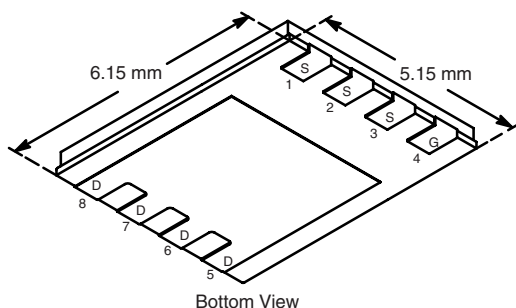


P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.00195 at $V_{GS} = -10$ V	- 60 ^d	183 nC
	0.0025 at $V_{GS} = -4.5$ V	- 60 ^d	
	0.0039 at $V_{GS} = -2.5$ V	- 60 ^d	

PowerPAK SO-8



Bottom View

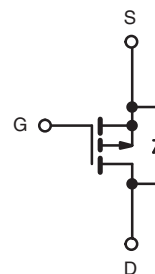
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Gen III P-Channel Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


 RoHS
 COMPLIANT
 HALOGEN
 FREE

APPLICATIONS

- Adaptor Switch
- Battery Switch
- Load Switch



P-Channel MOSFET

Ordering Information: Si7137DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	- 60 ^d	A
		- 60 ^d	
		- 42 ^{a, b}	
		- 33.7 ^{a, b}	
Pulsed Drain Current	I_{DM}	- 100	
Continuous Source-Drain Diode Current	I_S	- 60 ^d	A
		- 5.6 ^{a, b}	
Avalanche Current	I_{AS}	- 50	mJ
Single-Pulse Avalanche Energy	E_{AS}	125	
Maximum Power Dissipation	P_D	104	W
		66.6	
		6.25 ^{a, b}	
		4.0 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R_{thJA}	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Case	R_{thJC}	0.9	1.2	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. $t = 10$ s.c. Maximum under Steady State conditions is 54 $^\circ\text{C/W}$.

d. Package limited.

e. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

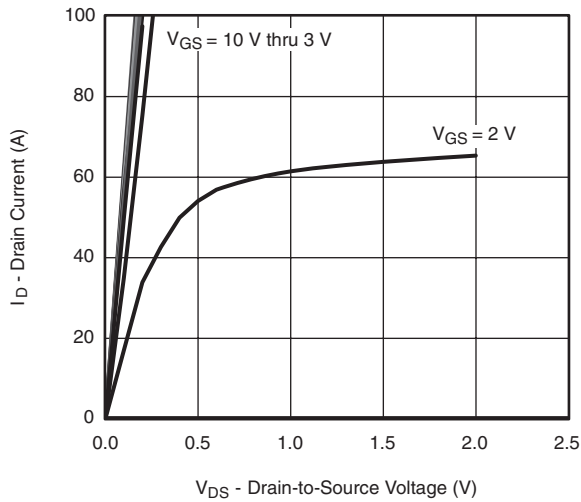
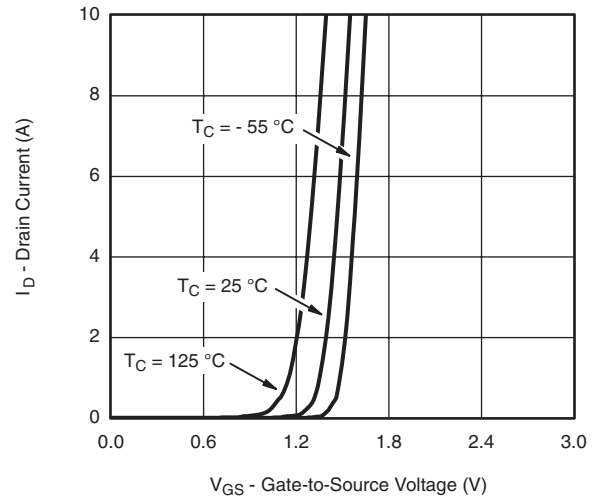
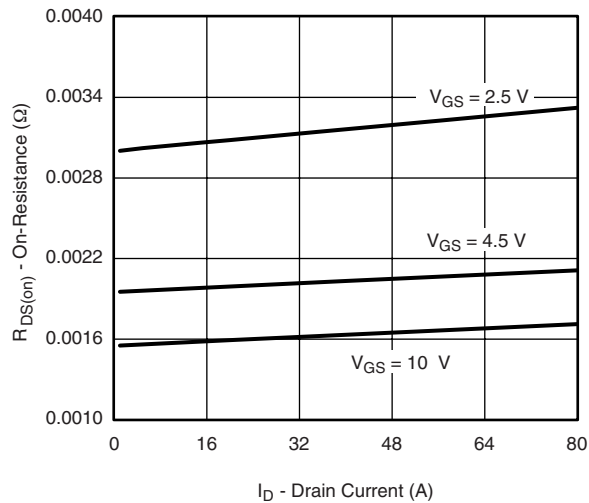
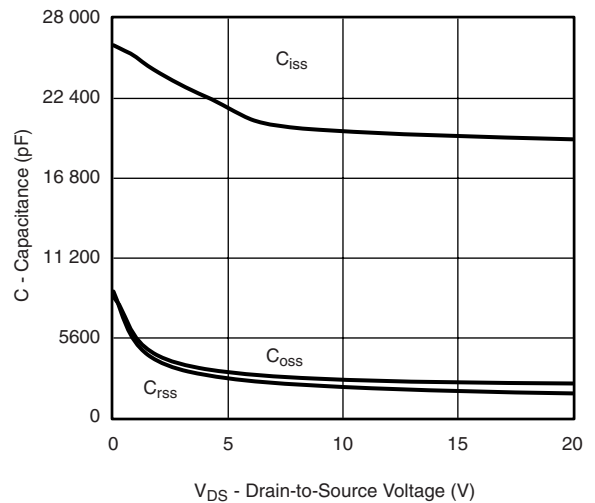
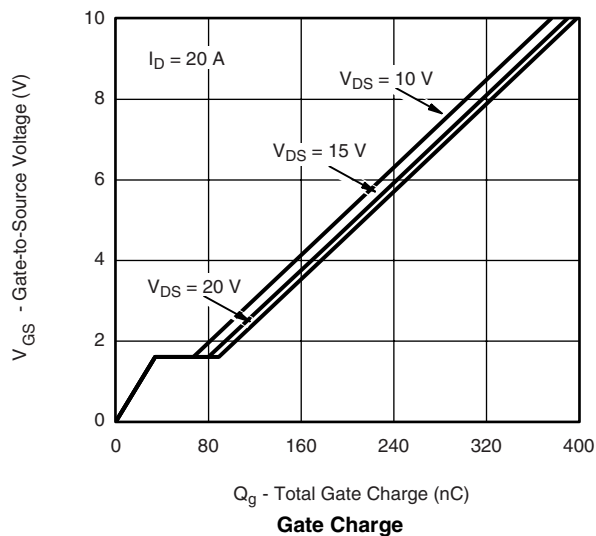
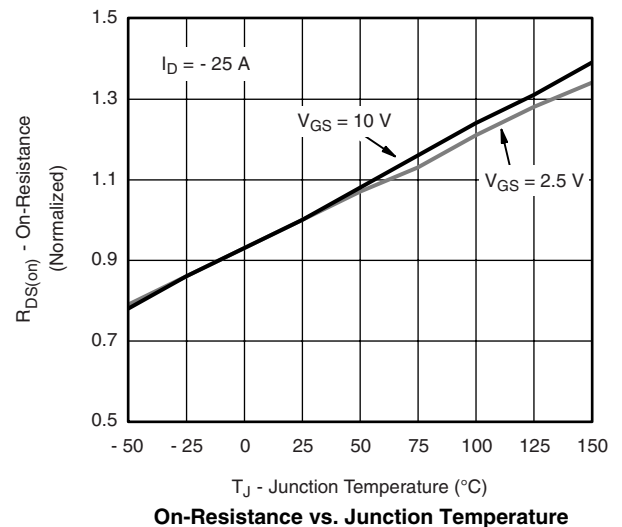
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 14.5		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			4.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.5		- 1.4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 40			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 25 A		0.0016	0.00195	Ω
		V _{GS} = - 4.5 V, I _D = - 20 A		0.002	0.0025	
		V _{GS} = - 2.5 V, I _D = - 15 A		0.0031	0.0039	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 25 A		95		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		20 000		pF
Output Capacitance	C _{oss}			2150		
Reverse Transfer Capacitance	C _{rss}			2650		
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 10 V, I _D = - 20 A		390	585	nC
Gate-Source Charge	Q _{gs}	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 20 A		188	282	
Gate-Drain Charge	Q _{gd}			33.6		
Gate Resistance	R _g		f = 1 MHz	0.9	1.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 1 Ω I _D ≅ - 10 A, V _{GEN} = - 10 V, R _g = 1 Ω		20	40	ns
Rise Time	t _r			14	28	
Turn-Off DelayTime	t _{d(off)}			230	400	
Fall Time	t _f			72	125	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 1 Ω I _D ≅ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		100	170	
Rise Time	t _r			150	255	
Turn-Off DelayTime	t _{d(off)}			230	390	
Fall Time	t _f			110	190	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 60	A
Pulse Diode Forward Current	I _{SM}				- 100	
Body Diode Voltage	V _{SD}	I _S = - 5 A, V _{GS} = 0 V		- 0.64	- 1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10 A, dI/dt = 100 A/μs, T _J = 25 °C		88	140	ns
Body Diode Reverse Recovery Charge	Q _{rr}			105	160	nC
Reverse Recovery Fall Time	t _a			25		ns
Reverse Recovery Rise Time	t _b			63		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

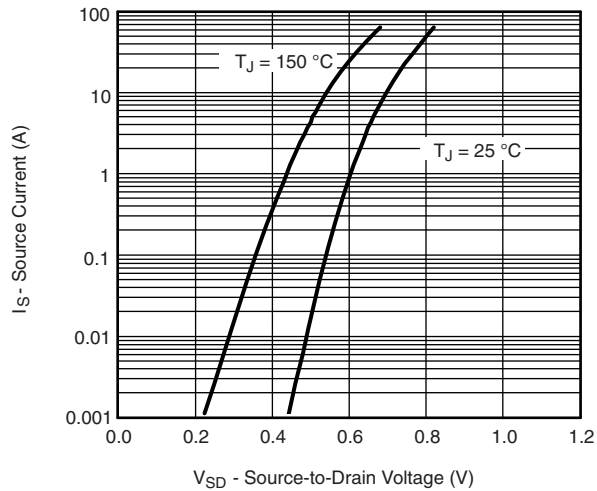
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

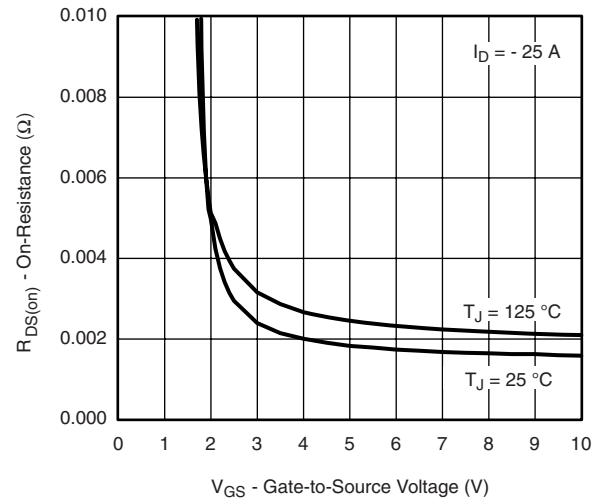

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Si7137DP

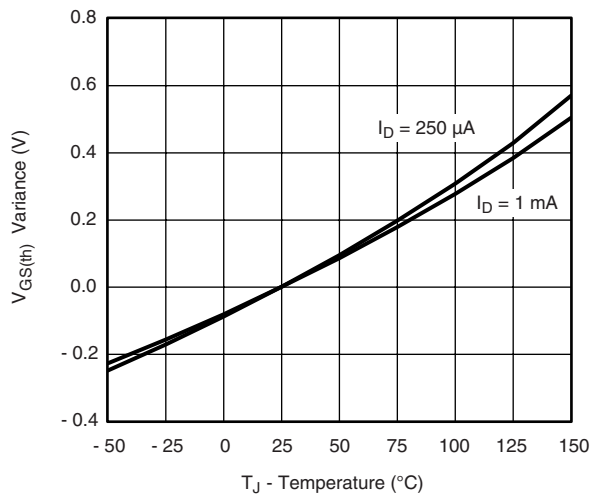
Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

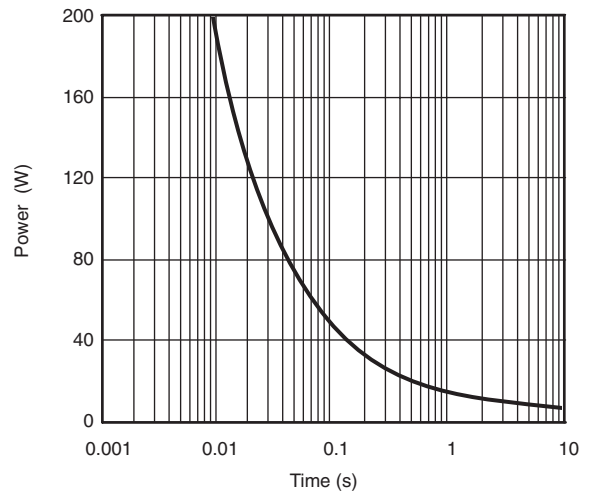
Source-Drain Diode Forward Voltage



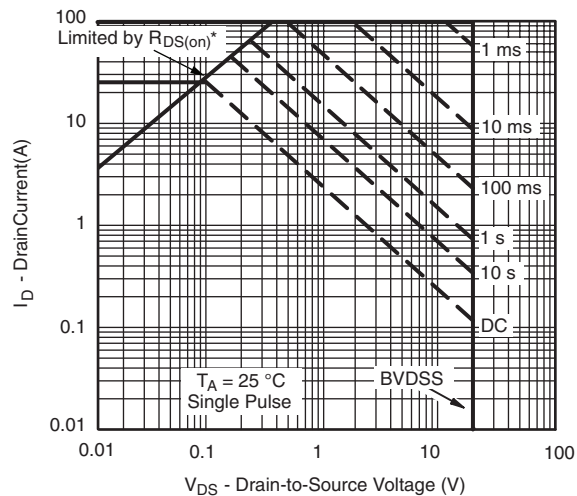
On-Resistance vs. Gate-to-Source Voltage



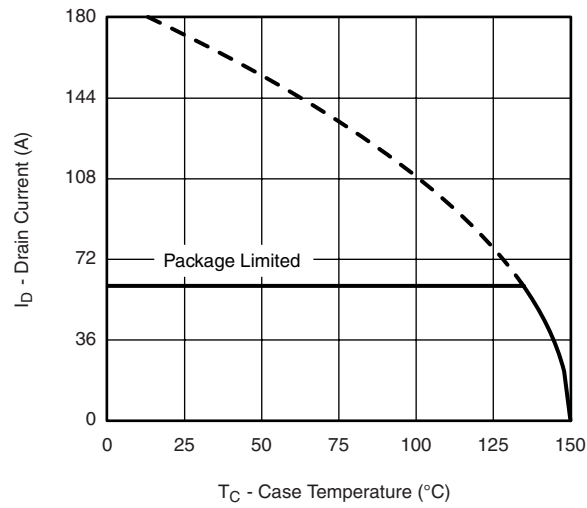
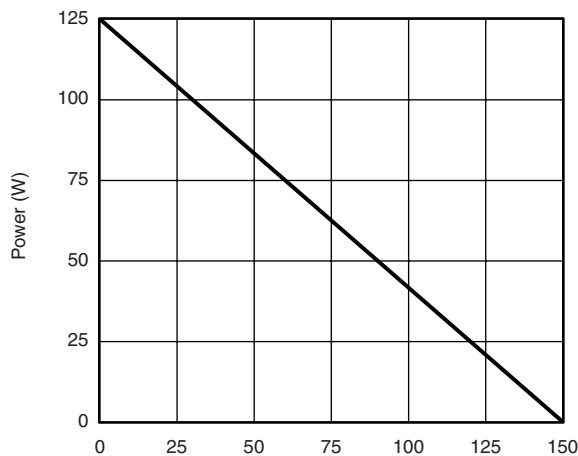
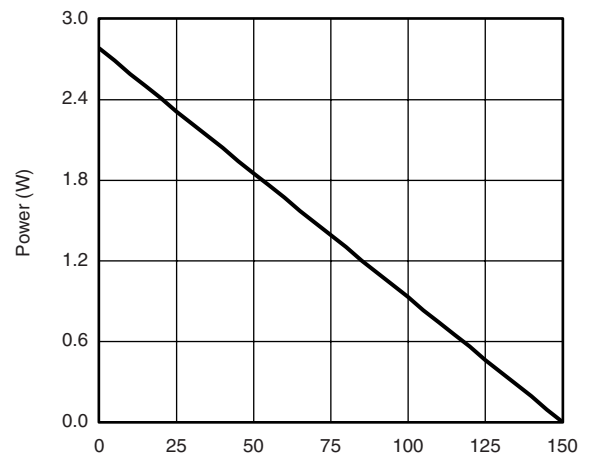
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

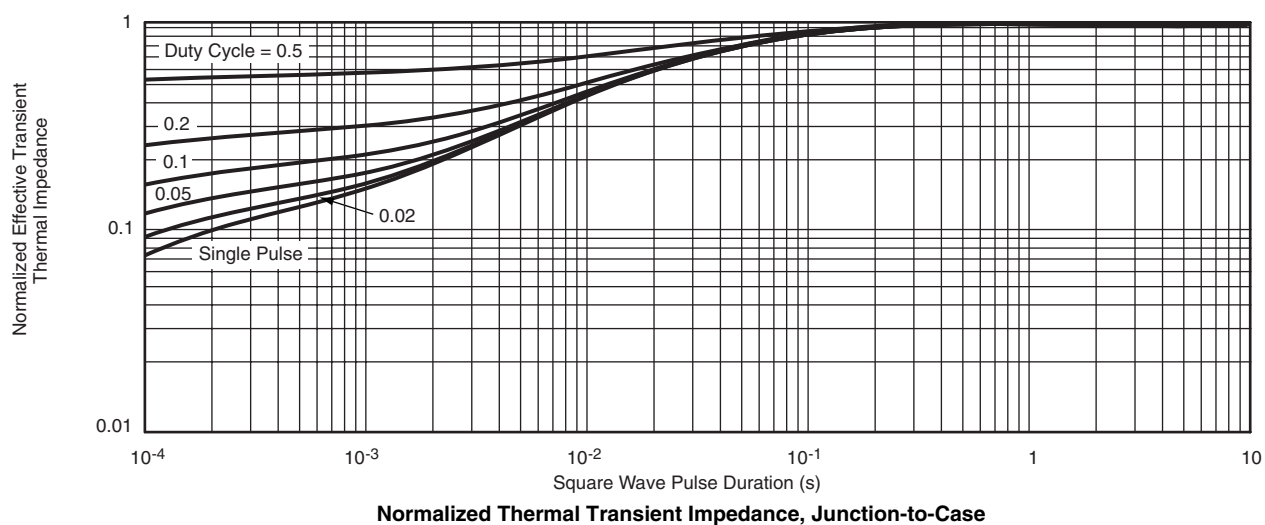
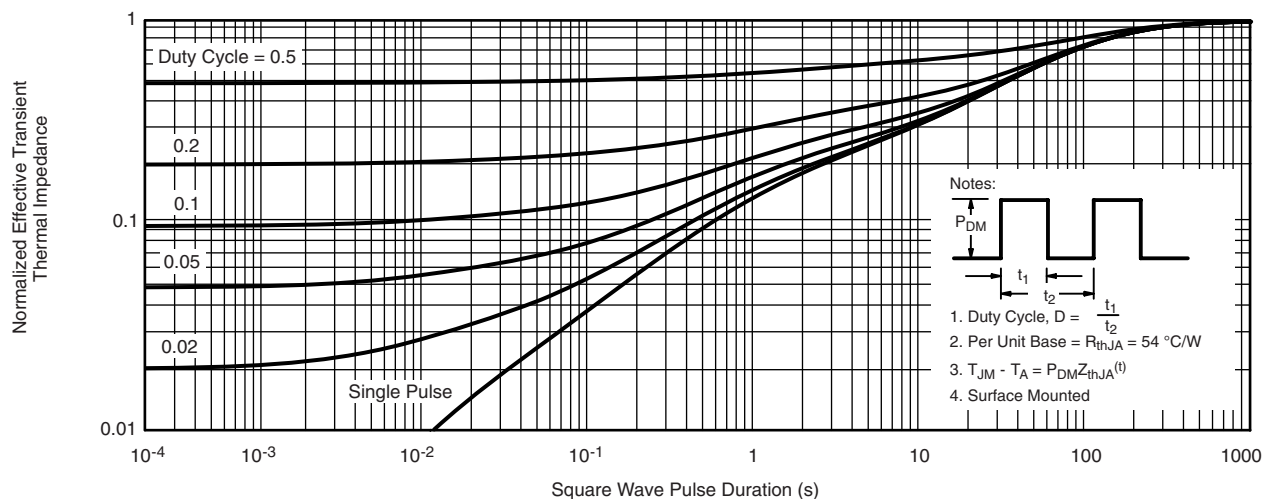
Safe Operating Area


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Current Derating*

Power, Junction-to-Case

Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

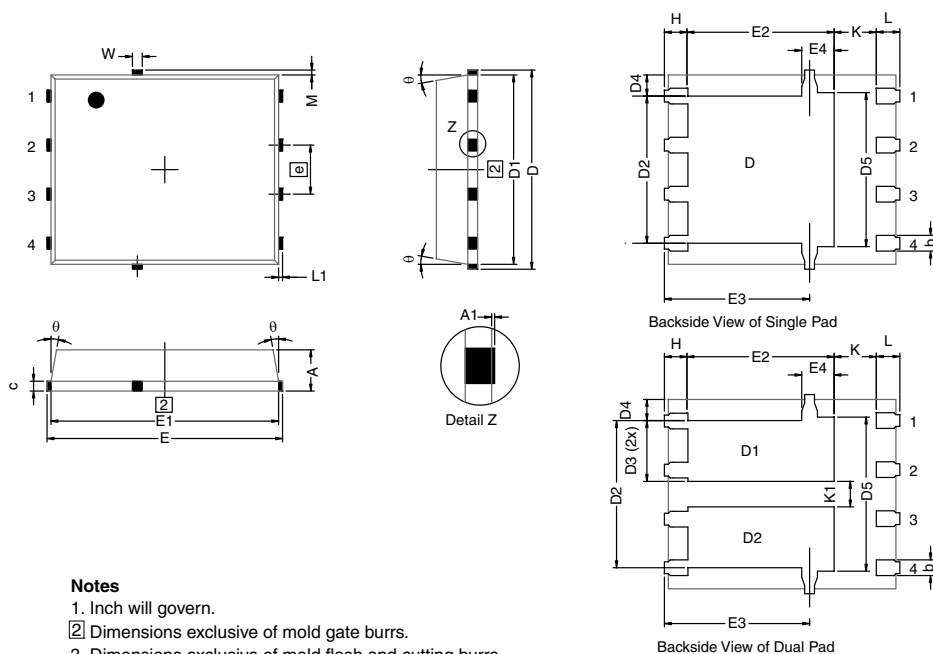
Si7137DP

Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69063.

PowerPAK® SO-8, (Single/Dual)



Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)	0.58 typ.			0.023 typ.		
E4 (for other product)	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K (for AL product)	1.45 typ.			0.057 typ.		
K (for other product)	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C13-0702-Rev. K, 20-May-13						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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