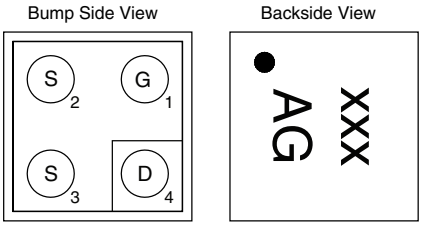
Si8812DB

Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)[a]	Q_g (Typ.)
20	0.059 at V_{GS} = 4.5 V	3.2	6.3 nC
	0.061 at V_{GS} = 3.7 V	3.1	
	0.065 at V_{GS} = 2.5 V	3.0	
	0.085 at V_{GS} = 1.8 V	2.7	

MICRO FOOT



Device Marking: xxx = Date/Lot Traceability Code
AG = Device Marking Code

Ordering Information: Si8812DB-T2-E1 (Lead (Pb)-free and Halogen-free)

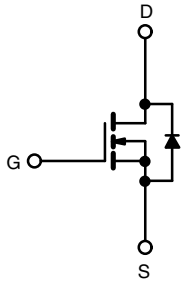
FEATURES

- TrenchFET® Power MOSFET
- Small 0.8 mm x 0.8 mm Outline Area
- Low 0.4 mm max. profile
- Low On-Resistance
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Load Switch with Low Voltage Drop
- Power Management
- For Smart Phones, Tablet PCs, Mobile Computing



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	3.2[a]	A
	T_A = 70 °C		2.6[a]	
	T_A = 25 °C		2.3[b]	
	T_A = 70 °C		1.8[b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	20	
Continuous Source-Drain Diode Current	T_A = 25 °C	I_S	0.7[a]	
	T_A = 25 °C		0.4[b]	
Maximum Power Dissipation	T_A = 25 °C	P_D	0.9[a]	W
	T_A = 70 °C		0.6[a]	
	T_A = 25 °C		0.5[b]	
	T_A = 70 °C		0.3[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[c]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, d]	t ≤ 5 s	R_{thJA}	105	135	°C/W
Maximum Junction-to-Ambient[b, e]			200	260	

Notes:
a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
d. Maximum under steady state conditions is 185 °C/W.
e. Maximum under steady state conditions is 330 °C/W.

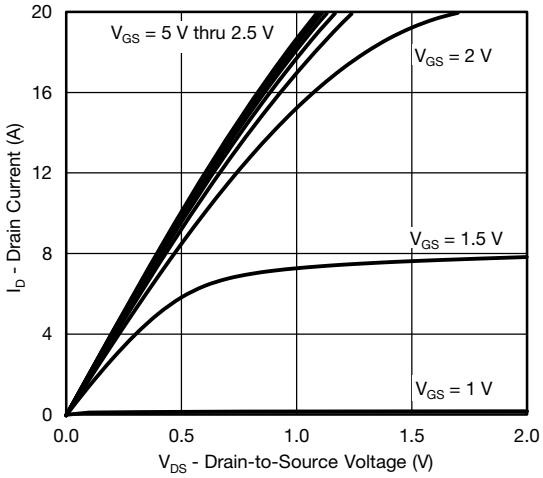
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		29		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1 A		0.048	0.059	Ω
		V_{GS} = 3.7 V, I_D = 1 A		0.049	0.061	
		V_{GS} = 2.5 V, I_D = 1 A		0.052	0.065	
		V_{GS} = 1.8 V, I_D = 0.5 A		0.060	0.085	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 1 A		12		S
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 8 V, I_D = 1 A		11	17	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 1 A		6.3	10	
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_g	f = 1 MHz		6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω $I_D \cong$ 1 A, V_{GEN} = 4.5 V, R_g = 1 Ω		10	20	ns
Rise Time	t_r			13	25	
Turn-Off Delay Time	$t_{d(off)}$			33	60	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω $I_D \cong$ 1 A, V_{GEN} = 8 V, R_g = 1 Ω		5	10	
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_A = 25 °C			0.7	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	I_S = 1 A, V_{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 1 A, dI/dt = 100 A/µs, T_J = 25 °C		10	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			3	10	nC
Reverse Recovery Fall Time	t_a			6		ns
Reverse Recovery Rise Time	t_b			4		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

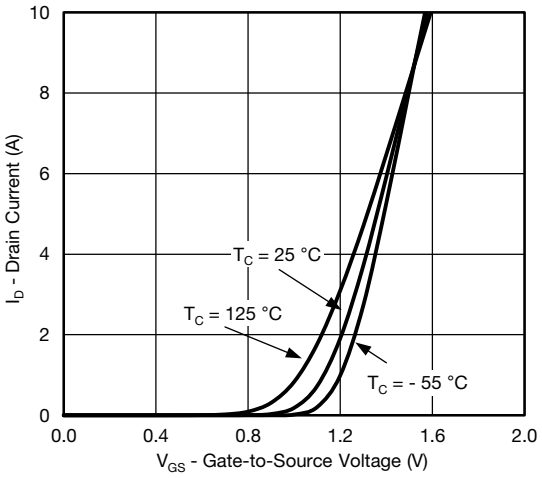
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 63682
S12-2050-Rev. A, 27-Aug-12

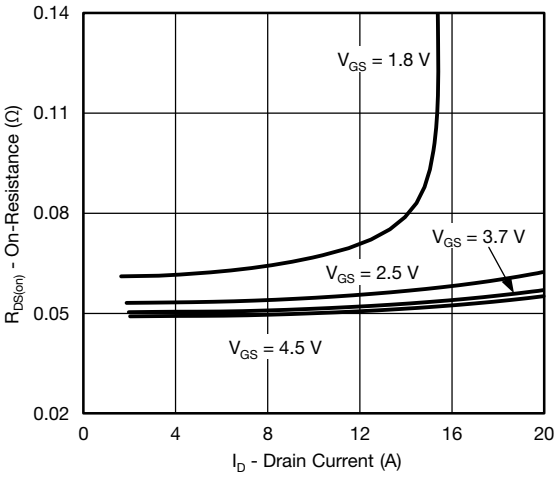
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



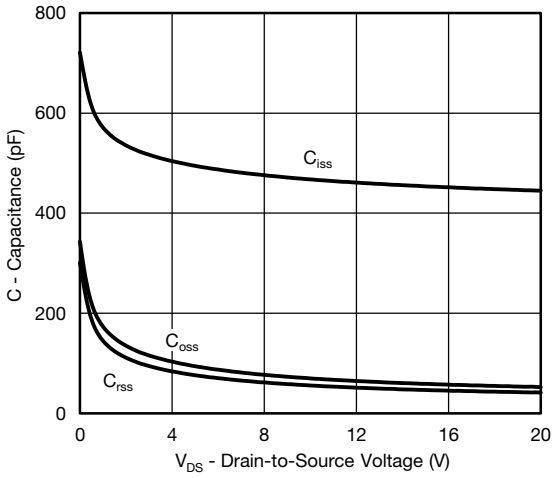
Output Characteristics



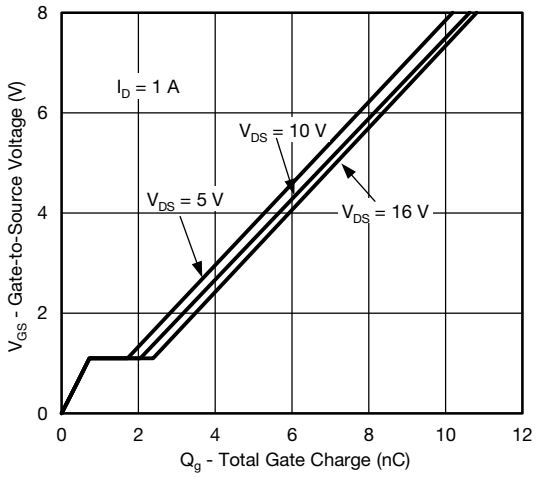
Transfer Characteristics



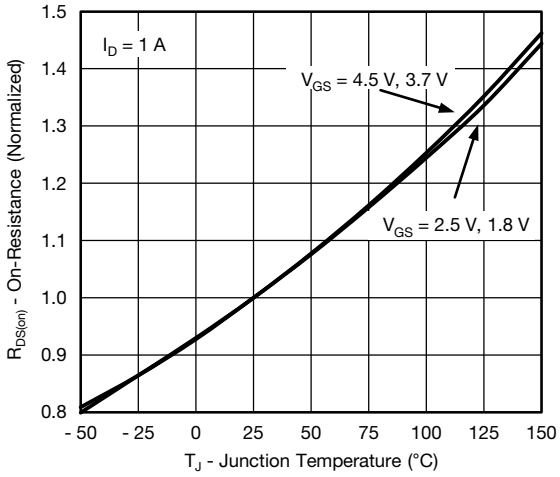
On-Resistance vs. Drain Current



Capacitance

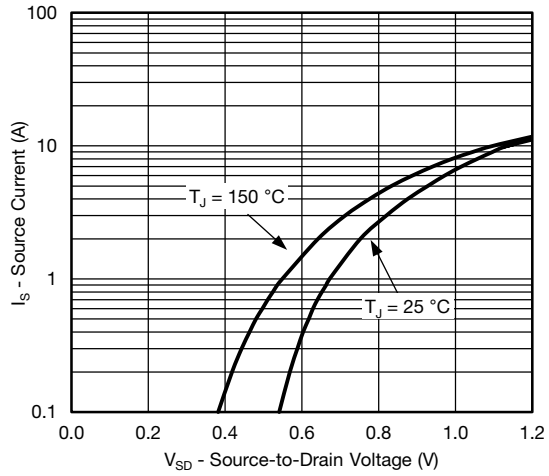


Gate Charge

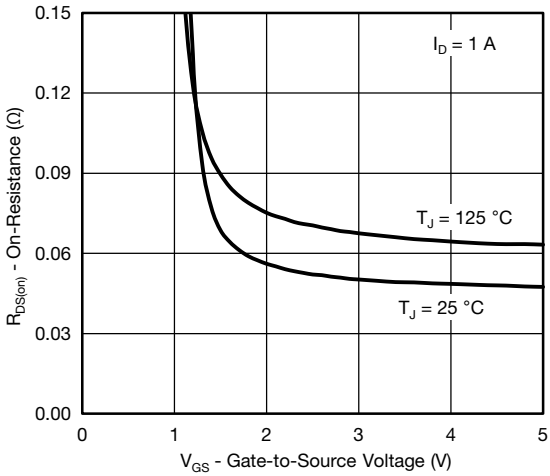


On-Resistance vs. Junction Temperature

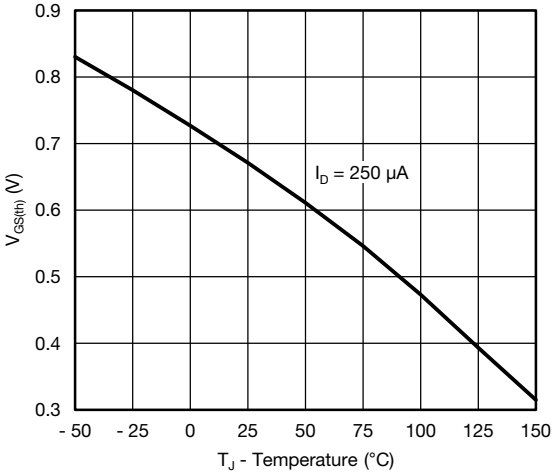
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



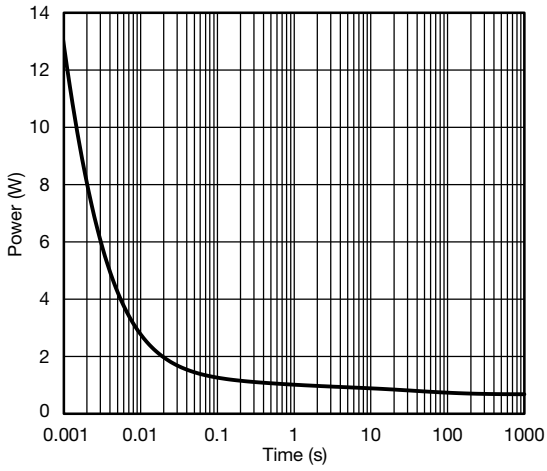
Source-Drain Diode Forward Voltage



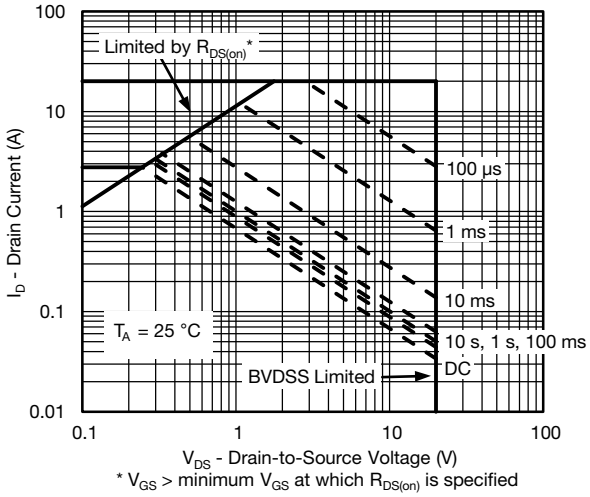
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

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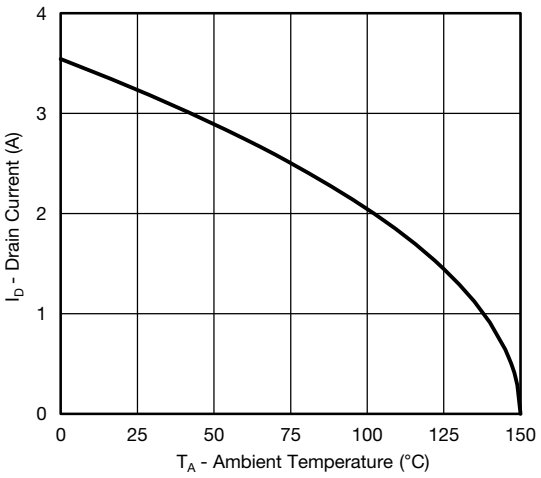
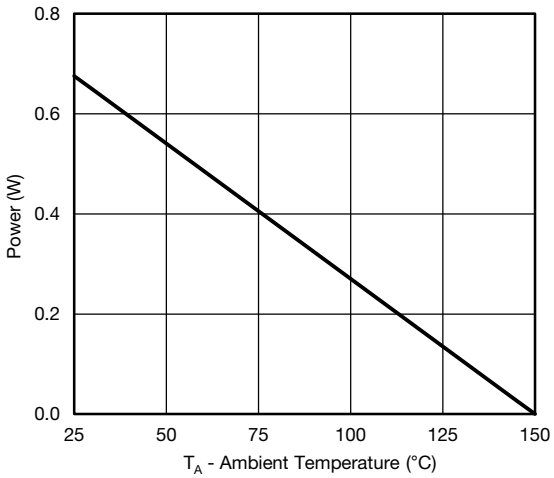


Current Derating*



Power Derating

Note:
When mounted on 1" x 1" FR4 with full copper.

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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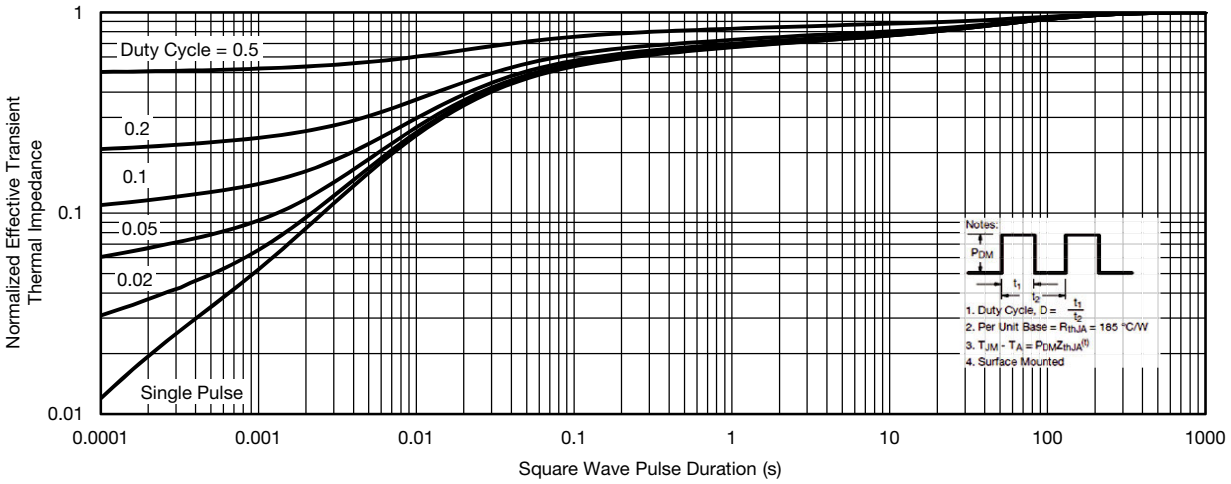
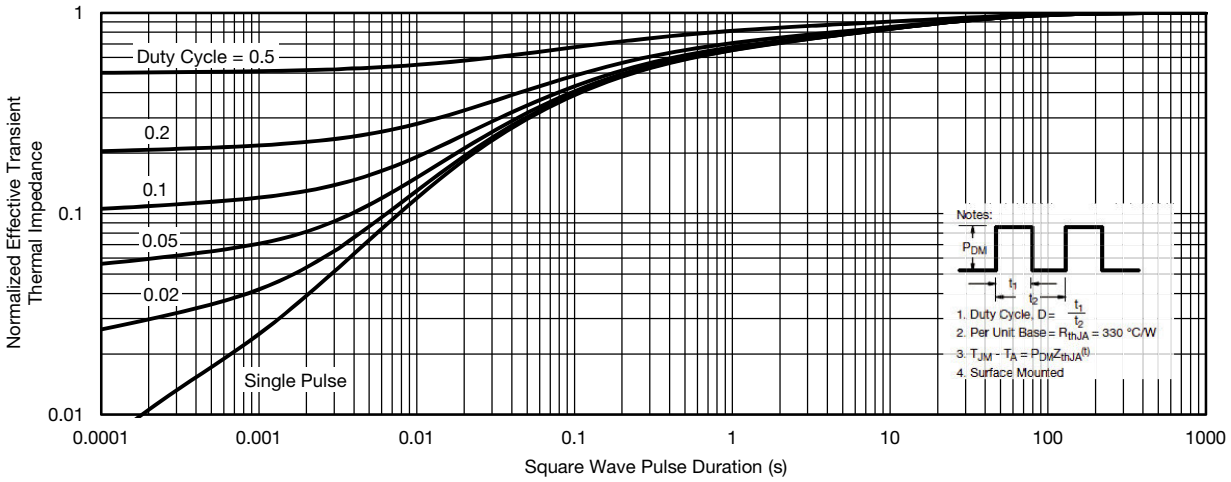


Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 board with maximum copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 board with minimum copper)

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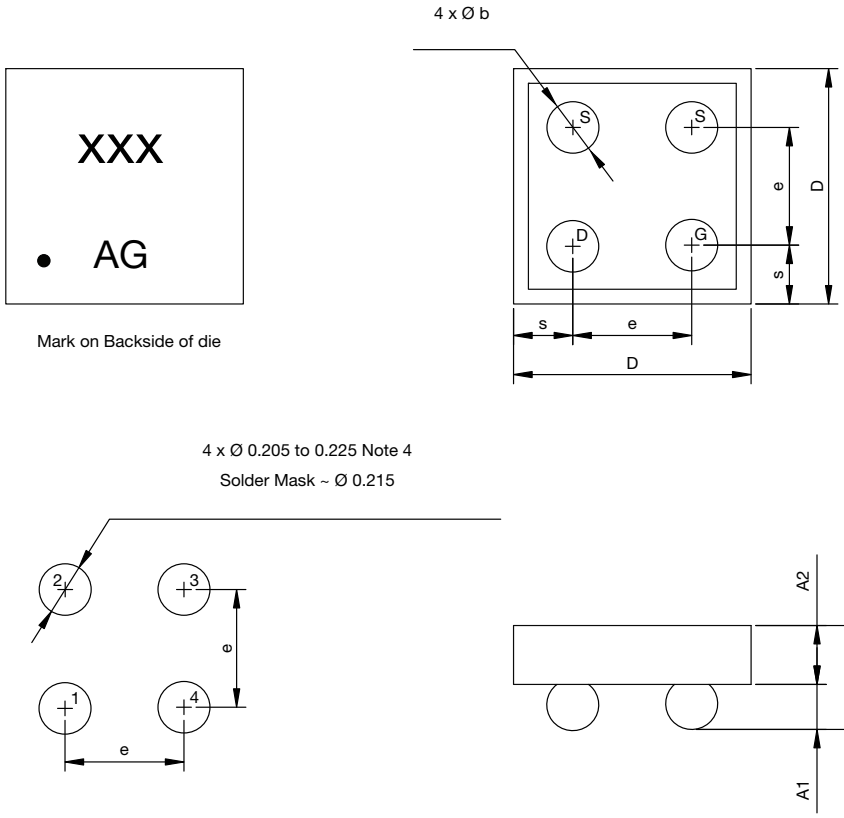
PACKAGE OUTLINE

MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



Notes (Unless otherwise specified):
1. All dimensions are in millimeters.
2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters[a]			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.314	0.357	0.400	0.0124	0.0141	0.0157
A_1	0.127	0.157	0.187	0.0050	0.0062	0.0074
A_2	0.187	0.200	0.213	0.0074	0.0079	0.0084
b	0.165	0.175	0.185	0.0064	0.0068	0.0072
e		0.400			0.0157	
s	0.180	0.200	0.220	0.0070	0.0078	0.0086
D	0.760	0.800	0.840	0.0299	0.0314	0.0330

Notes:
a. Use millimeters as the primary measurement.

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