

P-Channel 1.2-V (G-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 8	0.052 at $V_{GS} = - 4.5$ V	- g^a	7.78 nC
	0.070 at $V_{GS} = - 2.5$ V	- g^a	
	0.093 at $V_{GS} = - 1.8$ V	- 4.0	
	0.130 at $V_{GS} = - 1.5$ V	- 2.0	
	0.222 at $V_{GS} = - 1.2$ V	- 0.5	

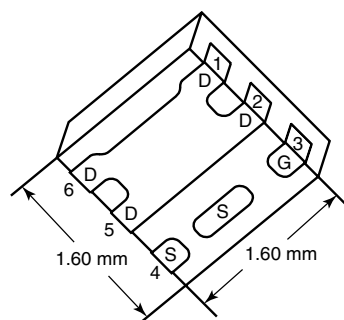
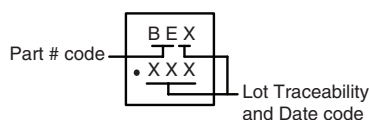
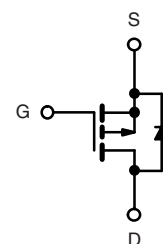
FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-75 Package
 - Small Footprint Area
 - Low On-Resistance


RoHS
COMPLIANT

APPLICATIONS

- Load Switch for Portable Devices

PowerPAK SC-75-6L-Single

Marking Code

Ordering Information: SiB417DK-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 8	V
Gate-Source Voltage	V_{GS}	± 5	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	- g^a
		$T_C = 70^\circ\text{C}$	- g^a
		$T_A = 25^\circ\text{C}$	- 5.6 ^{b, c}
		$T_A = 70^\circ\text{C}$	- 4.48 ^{b, c}
Pulsed Drain Current	I_{DM}	- 15	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	- g^a
		$T_A = 25^\circ\text{C}$	- 2 ^{b, c}
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	13
		$T_C = 70^\circ\text{C}$	8.4
		$T_A = 25^\circ\text{C}$	2.4 ^{b, c}
		$T_A = 70^\circ\text{C}$	1.6 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	41	51	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	7.5	9.5	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 105 $^\circ\text{C/W}$.

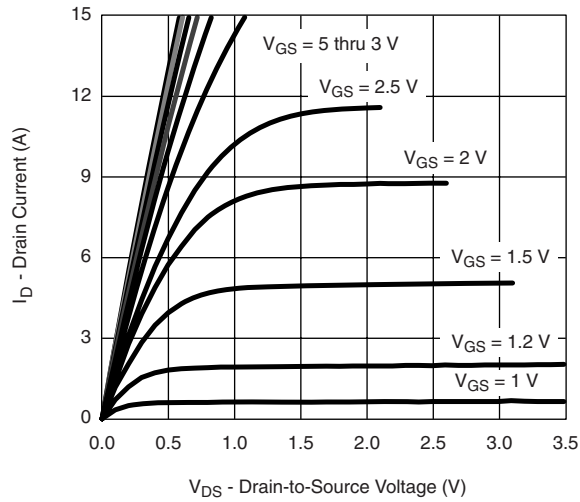
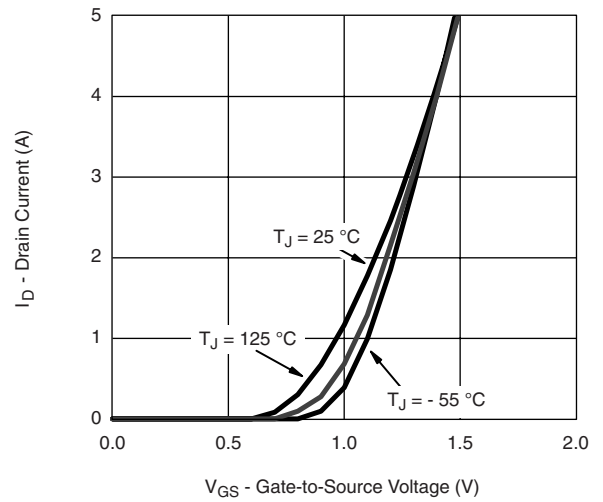
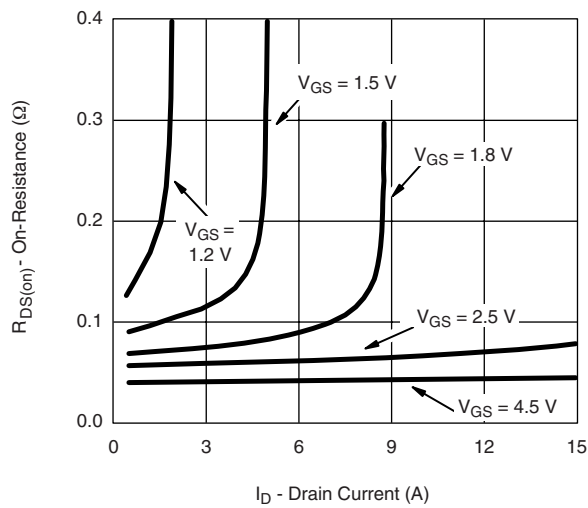
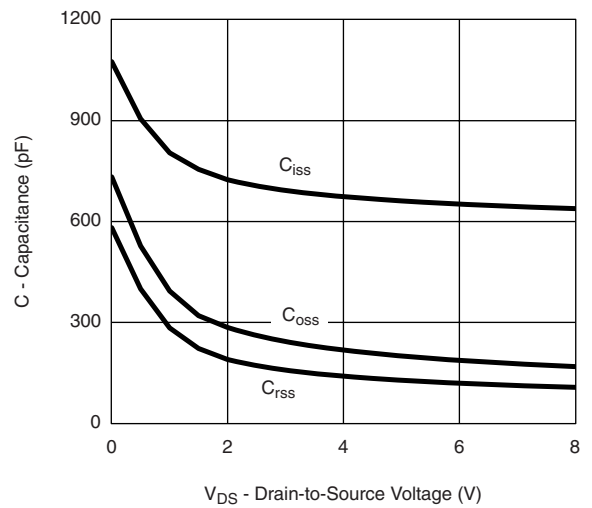
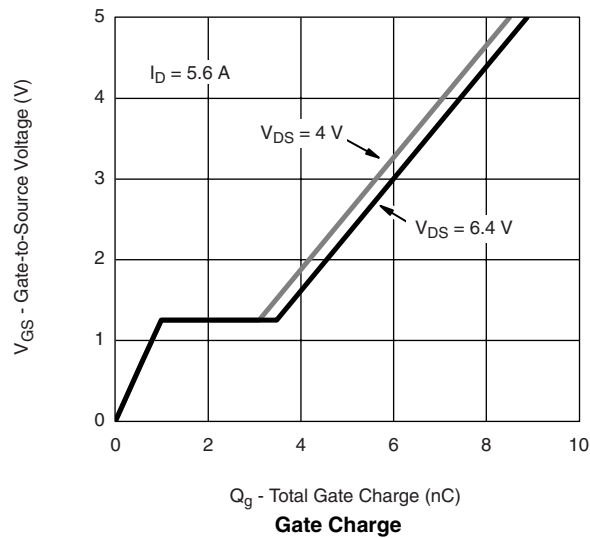
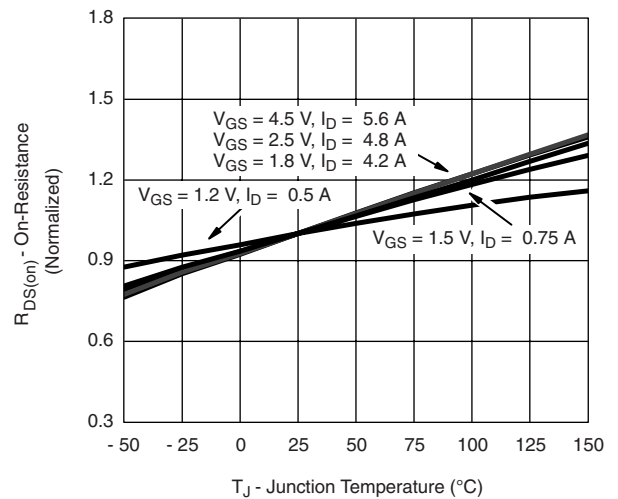
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 8			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 4.03		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			1.27		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.35		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 8 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 15			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 5.6 A		0.042	0.052	Ω
		V _{GS} = - 2.5 V, I _D = - 4.8 A		0.058	0.070	
		V _{GS} = - 1.8 V, I _D = - 4.2 A		0.076	0.093	
		V _{GS} = - 1.5 V, I _D = - 0.75 A		0.096	0.130	
		V _{GS} = - 1.2 V, I _D = - 0.50 A		0.148	0.222	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 4 V, I _D = - 5.6 A		12		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 4 V, V _{GS} = 0 V, f = 1 MHz		675		pF
Output Capacitance	C _{oss}			217		
Reverse Transfer Capacitance	C _{rss}			140		
Total Gate Charge	Q _g	V _{DS} = - 4 V, V _{GS} = - 5 V, I _D = - 5.6 A		8.5	12.75	nC
		V _{DS} = - 4 V, V _{GS} = - 4.5 V, I _D = - 5.6 A		7.78	11.67	
Gate-Source Charge	Q _{gs}			0.99		
Gate-Drain Charge	Q _{gd}			2.11		
Gate Resistance	R _g	f = 1 MHz		7.1		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 4 V, R _L = 0.89 Ω I _D ≅ - 4.48 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		13	19.5	ns
Rise Time	t _r			31	46.5	
Turn-Off Delay Time	t _{d(off)}			35	52.5	
Fall Time	t _f			18	27	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 9	A
Pulse Diode Forward Current	I _{SM}				- 15	
Body Diode Voltage	V _{SD}	I _S = - 3 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 3 A, di/dt = 100 A/μs, T _J = 25 °C		19.8	29.7	ns
Body Diode Reverse Recovery Charge	Q _{rr}			8	12	nC
Reverse Recovery Fall Time	t _a			15.8		ns
Reverse Recovery Rise Time	t _b			4		

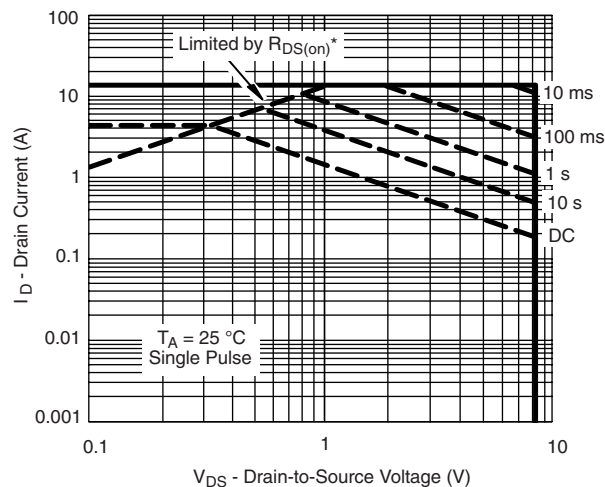
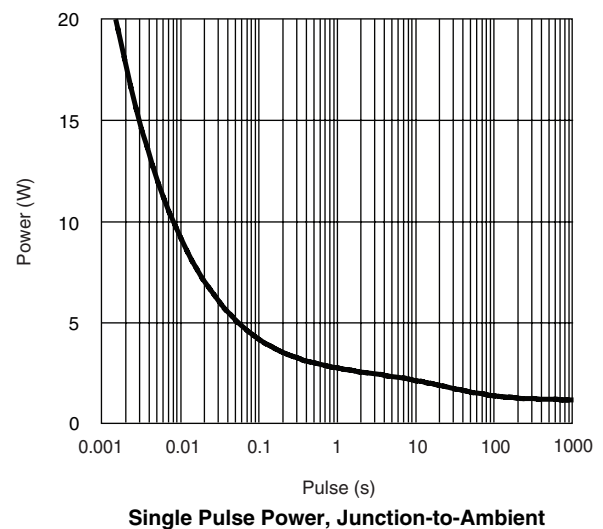
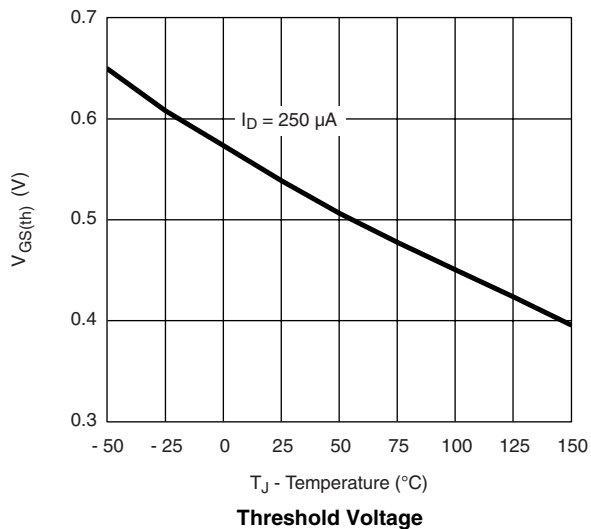
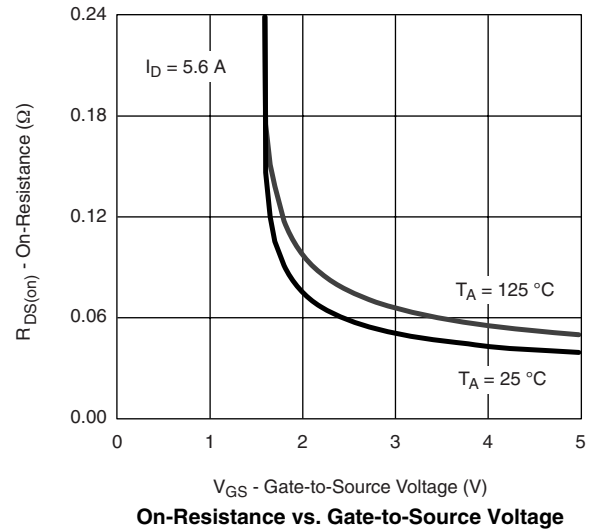
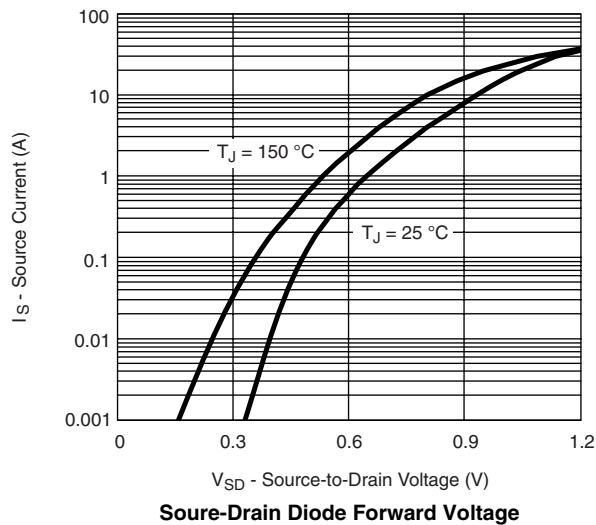
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

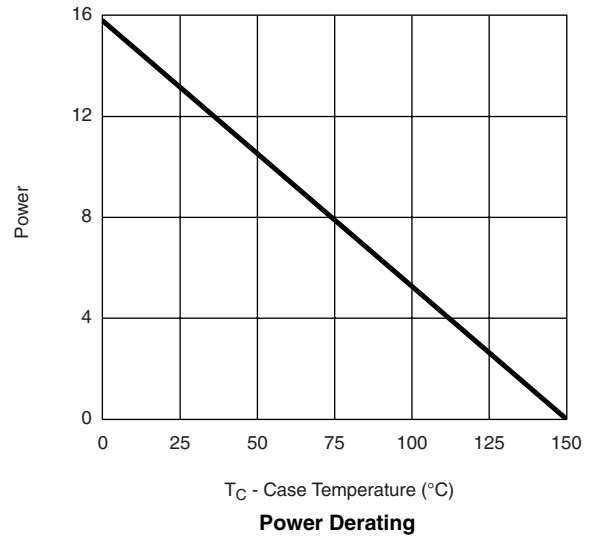
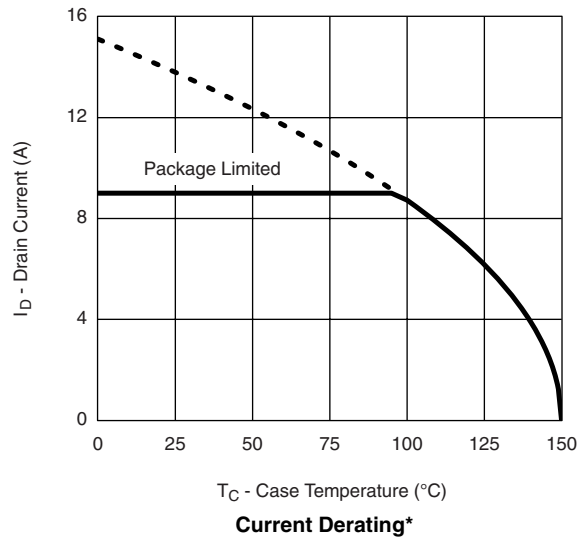
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

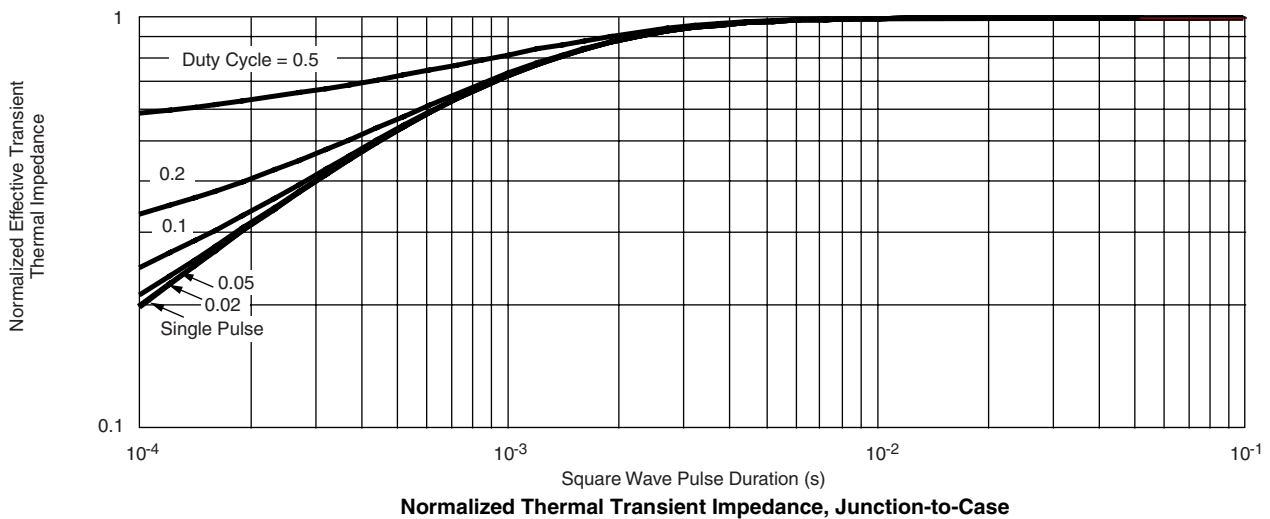
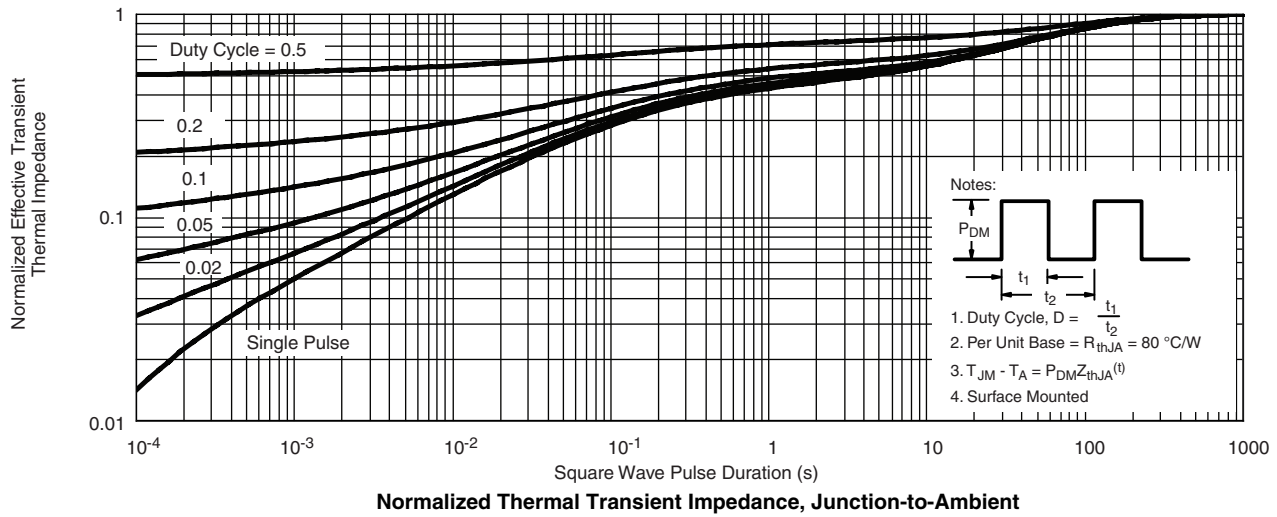
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74596>.



PowerPAK® SC75-6L

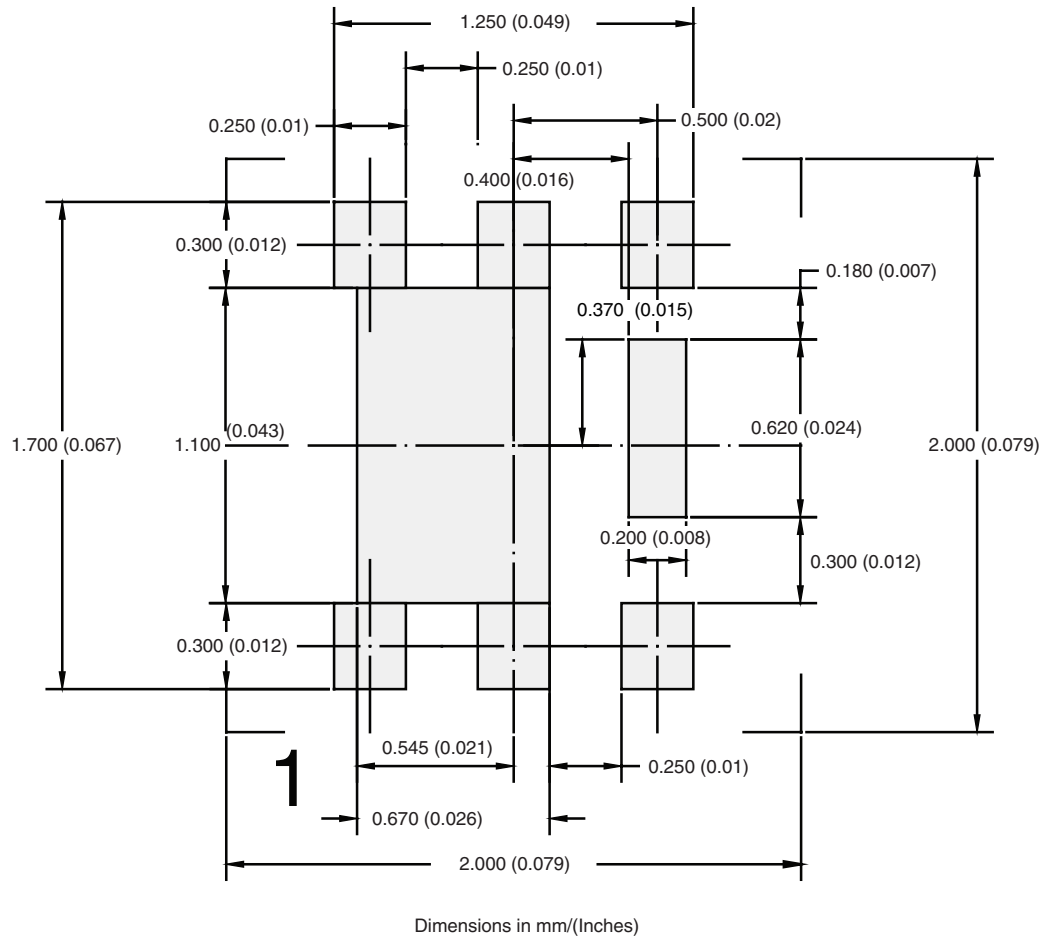


- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



[Return to Index](#)



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