6 A, microBUCK® SiC414, SiC424
Integrated Buck Regulator with 5 V LDO

DESCRIPTION

The Vishay Siliconix SiC414 and SiC424 are an advanced stand-alone synchronous buck regulator featuring integrated power MOSFETs, bootstrap switch, and an internal 5 V_{LDO} in a space-saving PowerPAK MLP44-28L package.

The SiC414 and SiC424 are capable of operating with all ceramic solutions and switching frequencies up to 1 MHz. The programmable frequency, synchronous operation and selectable power-save allow operation at high efficiency across the full range of load current. The internal LDO may be used to supply 5 V for the gate drive circuits or it may be bypassed with an external 5 V for optimum efficiency and used to drive external n-channel MOSFETs or other loads. Additional features include cycle-by-cycle current limit, voltage soft-start, under-voltage protection, programmable over-current protection, soft shutdown and selectable power-save. The Vishay Siliconix SiC414 and SiC424 also provides an enable input and a power good output.

PRODUCT SUMMARY	
Input Voltage Range	3 V to 28 V
Output Voltage Range	0.75 V to 5.5 V
Operating Frequency	200 kHz to 1 MHz
Continuous Output Current	6 A
Peak Efficiency	95 %
Package	PowerPAK MLP44-28L

FEATURES

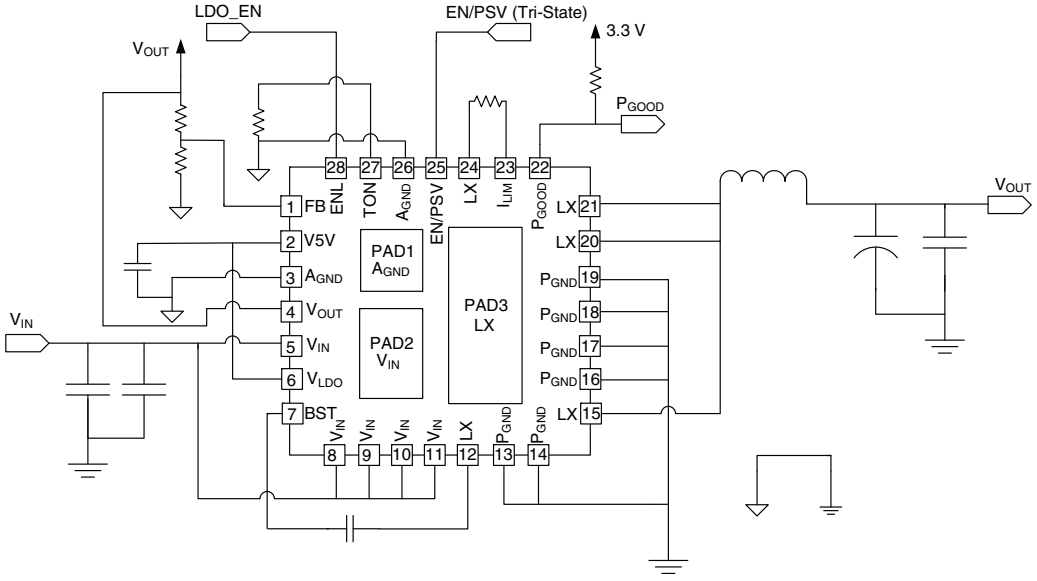
- High efficiency > 95 %
- 6 A continuous output current capability
- Integrated bootstrap switch
- Integrated 5 V/200 mA LDO with bypass logic
- Temperature compensated current limit
- Pseudo fixed-frequency adaptive on-time control
- All ceramic solution enabled
- Programmable input UVLO threshold
- Independent enable pin for switcher and LDO
- Selectable ultrasonic power-save mode (SiC414)
- Selectable power-save mode (SiC424)
- Internal soft-start and soft-shutdown
- 1 % internal reference voltage
- Power good output and over voltage protection
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

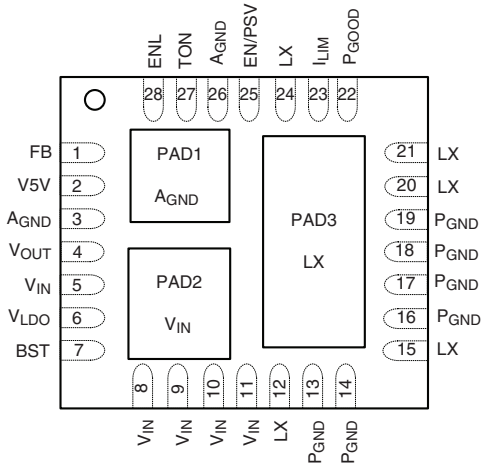
APPLICATIONS

- Notebook, desktop, and server computers
- Digital HDTV and digital consumer applications
- Networking and telecommunication equipment
- Printers, DSL, and STB applications
- Embedded applications
- Point of load power supplies

TYPICAL APPLICATION CIRCUIT AND PACKAGE OPTION



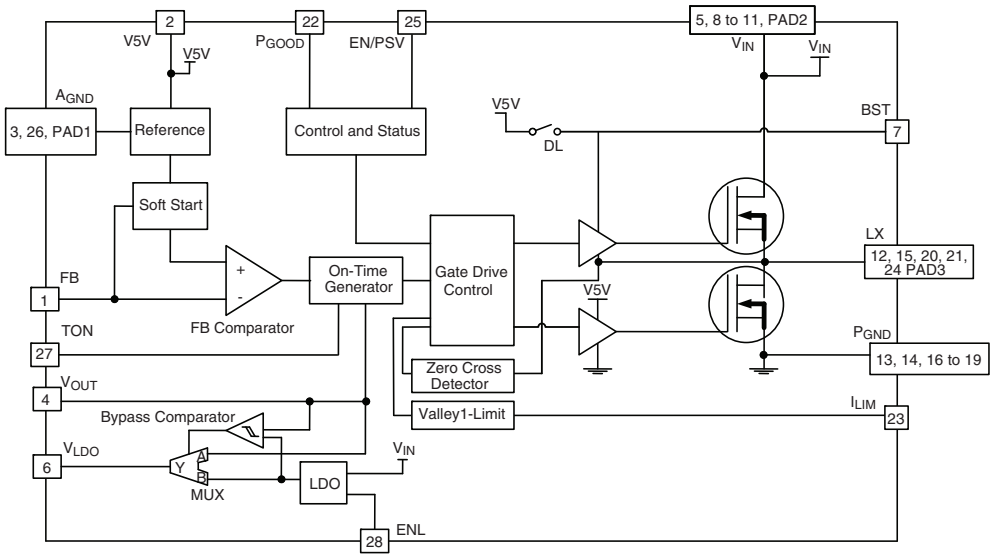
PIN CONFIGURATION (top view)



PIN DESCRIPTION		
Pin Number	**Symbol**	**Description**
1	FB	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from V_{OUT} to A_{GND}.
2	V5V	Bias input for internal analog circuits and gate drives - connect to external 3 V or 5 V supply or bias connection to V_{LDO}.
3, 26, PAD 1	A_{GND}	Analog ground.
4	V_{OUT}	Switcher output voltage sense pin, and also the input to the internal switch-over between V_{OUT} and V_{LDO}.
5, 8 to 11, PAD 2	V_{IN}	Input supply voltage.
6	V_{LDO}	5 V LDO output.
7	BST	Bootstrap pin - connect a capacitor from BST to LXBST to develop the floating supply for the high-side gate drive.
12	LXBST	LX Boost - connect to the BST capacitor.
15, 20, 21, PAD 3	LX	Switching (Phase) node.
13, 14, 16 to 19	P_{GND}	Power ground.
22	P_{GOOD}	Open-drain power good indicator. High impedance indicates power is good. An external pull-up resistor is required.
23	I_{LIM}	Current limit sense pin - used to program the current limit by connecting a resistor from I_{LIM} to LXS.
24	LXS	LX sense - connect to R_{ILIM} resistor.
25	EN/PSV	Enable/power save input for the switching regulator - connect to A_{GND} to disable the switching regulator. Float to operate in forced continuous mode (power save disabled). For SiC414, connect to V5V to operate with ultrasonic power save mode enabled. For SiC424, connect to V5V to operate with power save mode enabled with no minimum frequency.
27	t_{ON}	On-time programming input - set the on-time by connecting through a resistor to A_{GND}.
28	ENL	Enable input for the LDO - connect ENL to A_{GND} to disable the LDO. Drive with logic to + 3 V for logic control, or program the V_{IN} UVLO with a resistor divider between V_{IN}, ENL, and A_{GND}.

ORDERING INFORMATION	
Part Number	**Package**
SiC414CD-T1-GE3	PowerPAK MLP44-28
SiC424CD-T1-GE3	PowerPAK MLP44-28
SiC414DB	Reference board

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Electrical Parameter	**Conditions**	**Limits**	**Unit**
V_{IN}	to P_{GND}	- 0.3 to + 30	V
LX	to P_{GND}	- 0.3 to + 30	
LX (transient < 100 ns)	to P_{GND}	- 2 to + 30	
EN/PSV, P_{GOOD}, I_{LIM}	to GND	- 0.3 to + (V5V + 0.3)	
V_{OUT}, V_{LDO}, FB	to GND	- 0.3 to + (V5V + 0.3)	
V5V	to P_{GND}	- 0.3 to + 6	
t_{ON}	to P_{GND}	- 0.3 to + (V5V - 1.5)	
BST	to LX	- 0.3 to + 6	
	to P_{GND}	- 0.3 to + 35	
ENL		- 0.3 to V_{IN}	
A_{GND} to P_{GND}		- 0.3 to + 0.3	
Temperature			
Maximum Junction Temperature		150	°C
Storage Temperature		- 65 to 150	
Power Dissipation			
Junction to Ambient Thermal Impedance (R_{thJA})[b]	IC Section	43	°C/W
Maximum Power Dissipation	Ambient Temperature = 25 °C	3.4	W
	Ambient Temperature = 100 °C	1.3	
ESD Protection			
	HBM	2	kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)				
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
V_{IN}	3		28	V
V5V to P_{GND}	3		5.5	
V_{OUT} to P_{GND}	0.75		5.5	
Temperature				
Recommended Ambient Temperature	- 40 to 85			°C

Note:
For proper operation, the device should be used within the recommended conditions.

ELECTRICAL SPECIFICATIONS						
Parameter	**Symbol**	**Test Conditions Unless Specified** V_{IN} = 12 V, V5V = 5 V, T_A = + 25 °C for typ., - 40 °C to + 85 °C for min. and max., T_J = < 125 °C	**Min.**	**Typ.**	**Max.**	**Unit**
Input Supplies						
V_{IN} UVLO Threshold Voltage[a] (not available for V5V < 4.5 V)	V_{UVLO}	Sensed at ENL pin, rising edge	2.4	2.6	2.95	V
		Sensed at ENL pin, falling edge	2.23	2.4	2.57	
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.2		
V5V UVLO Threshold Voltage	V_{UVLO}	Measured at V_{DD} pin, rising edge	2.5	2.9	3.0	
		Measured at V_{DD} pin, falling edge	2.4	2.7	2.9	
V_{DD} UVLO Hysteresis	V_{UVLO_HYS}			0.2		
V_{IN} Supply Current	I_{IN}	EN/PSV, ENL = 0 V, V_{IN} = 28 V		8.5	20	µA
		Standby mode: ENL = V5V, EN/PSV = 0 V		130		
V5V Supply Current	I_{DD}	EN/PSV, ENL = 0 V, V5V = 5 V		3	7	
		EN/PSV, ENL = 0 V, V5V = 3 V		2		
		SiC414, EN/PSV = V5V, no load, (f_{sw} = 25 kHz), V_{FB} > 0.75 V[b]		1		mA
		SiC424, EN/PSV = V5V, no load, V_{FB} > 0.75 V[b]		0.4		
		V5V = 5 V, f_{sw} = 250 kHz, EN/PSV = floating, no load[b]		4		
		V5V = 5 V, f_{sw} = 250 kHz, EN/PSV = floating, no load[b]		2.5		
Controller						
FB Comparator Threshold	V_{FB}	Static V_{IN} and load, - 40 °C to + 85 °C, V5V = 3 V or 5 V	0.7425	0.750	0.7575	V
Frequency Range[b]	f_{sw}	Continuous mode	200		1000	kHz
		Minimum f_{SW}, (SiC414 only), EN/PSV= V5V, no load		25		
Bootstrap Switch Resistance				10		Ω
Timing						
On-Time	t_{ON}	Continuous mode operation V_{IN} = 15 V, V_{OUT} = 3 V, f_{SW} = 300 kHz, R_{ton} = 133 kΩ	1350	1500	1650	ns
Minimum On-Time[b]	$t_{ON, min.}$			80		
Minimum Off-Time[b]	$t_{OFF, min.}$	V5V = 5 V		320		
		V5V = 3 V		390		
Soft Start						
Soft Start Time[b]	t_{SS}			1.7		ms
Analog Inputs/Outputs						
V_{OUT} Input Resistance	R_{O-IN}			500		kΩ
Current Sense						
Zero-Crossing Detector Threshold Voltage	$V_{Sense-th}$	LX-P_{GND}	- 3	0	+ 3	mV

For technical questions, contact: powerictechsupport@vishay.com
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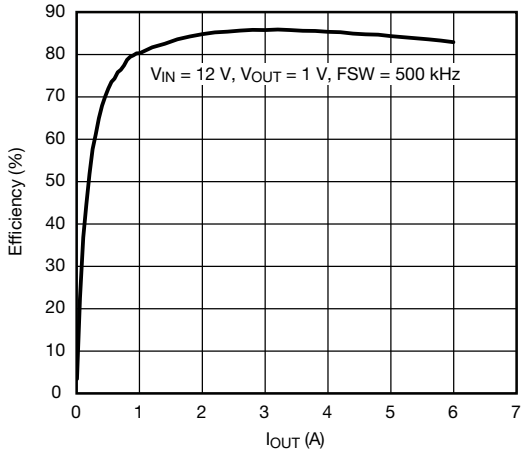
ELECTRICAL SPECIFICATIONS

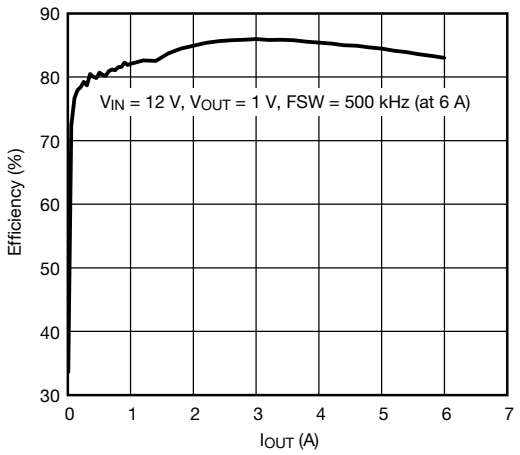
Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 12 V, V5V = 5 V, T_A = + 25 °C for typ., - 40 °C to + 85 °C for min. and max., T_J = < 125 °C	Min.	Typ.	Max.	Unit
Power Good						
Power Good Threshold Voltage	$PG\_V_{TH\_UPPER}$	Upper limit, V_{FB} > internal reference 750 mV		+ 20		%
		Lower limit, V_{FB} < internal reference 750 mV		- 10		
Start-Up Delay Time (between PWM enable and P_{GOOD} high)	PG_T_d	V5V = 5 V		4		ms
		V5V = 3 V		2		
Fault (noise-immunity) Delay Time[b]	PG_I_{CC}			5		µs
Power Good Leakage Current	PG_I_{LK}				1	µA
Power Good On-Resistance	PG_R_{DS-ON}			10		Ω
Fault Protection						
Valley Current Limit		V5V = 5 V, R_{ILIM} = 5 kΩ	3	4	5	A
I_{LIM} Source Current	I_{LIM}			8		µA
I_{LIM} Comparator Offset Voltage	V_{ILM-LK}	With respect to A_{GND}	- 8	0	+ 8	mV
Output Under-Voltage Fault	V_{OUV_Fault}	V_{FB} with respect to Internal 750 mV reference, 8 consecutive clocks		- 25		%
Smart Power-Save Protection Threshold Voltage[b]	P_{SAVE_VTH}	V_{FB} with respect to internal 750 mV reference		+ 10		
Over-Voltage Protection Threshold		V_{FB} with respect to internal 750 mV reference		+ 20		
Over-Voltage Fault Delay[b]	$t_{OV-Delay}$			5		µs
Over Temperature Shutdown[b]	T_{Shut}	10 °C hysteresis		150		°C
Logic Inputs/Outputs						
Logic Input High Voltage	V_{IH}	ENL	1			V
Logic Input Low Voltage	V_{IL}				0.4	
EN/PSV Input for PSAVE Operation[b]		% of V5V	45		100	%
EN/PSV Input for Forced Continuous Operation[b]			1V		42	
EN/PSV Input for Disabling Switcher			0		0.4	V
EN/PSV Input Bias Current	I_{EN}	EN/PSV = V5V or A_{GND}	- 10		+ 10	µA
ENL Input Bias Current		V_{IN} = 28 V		11	18	
FB Input Bias Current	FBL_I_{LK}	FB = V5V or A_{GND}	- 1		+ 1	
Linear Dropout Regulator						
V_{LDO} Accuracy	V_{LDO_ACC}	V_{LDO} load = 10 mA	4.9	5	5.1	V
LDO Current Limit	LDO_I_{LIM}	Start-up and foldback, V_{IN} = 12 V		115		mA
		Operating current limit, V_{IN} = 12 V	135	200		
V_{LDO} to V_{OUT} Switch-Over Threshold[c]	$V_{LDO-BPS}$		- 140		+ 140	mV
V_{LDO} to V_{OUT} Non-Switch-Over Threshold[c]	$V_{LDO-NBPS}$		- 450		+ 450	
V_{LDO} to V_{OUT} Switch-Over Resistance	R_{LDO}	V_{OUT} = 5 V		2		Ω
LDO Drop Out Voltage[d]		From V_{IN} to V_{VLDO} , V_{VLDO} = 5 V, I_{VLDO} = 100 mA		1.2		V

Notes:
a. $V_{IN\ UVLO}$ is programmable using a resistor divider from V_{IN} to ENL to A_{GND}. The ENL voltage is compared to an internal reference.
b. Guaranteed by design.
c. The switch-over threshold is the maximum voltage differential between the V_{LDO} and V_{OUT} pins which ensures that V_{LDO} will internally switch-over to V_{OUT}. The non-switch-over threshold is the minimum voltage differential between the V_{LDO} and V_{OUT} pins which ensures that V_{LDO} will not switch-over to V_{OUT}.
d. The LDO drop out voltage is the voltage at which the LDO output drops 2 % below the nominal regulation point.

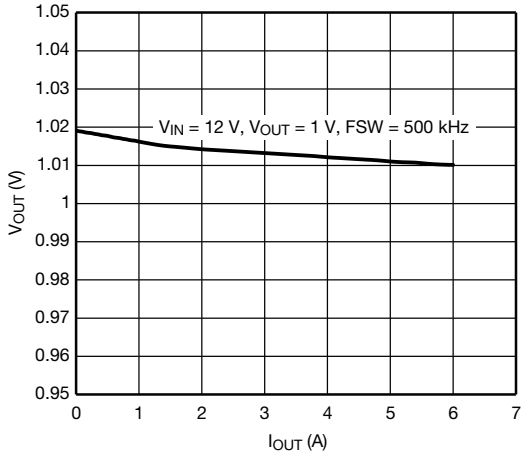
ELECTRICAL CHARACTERISTICS



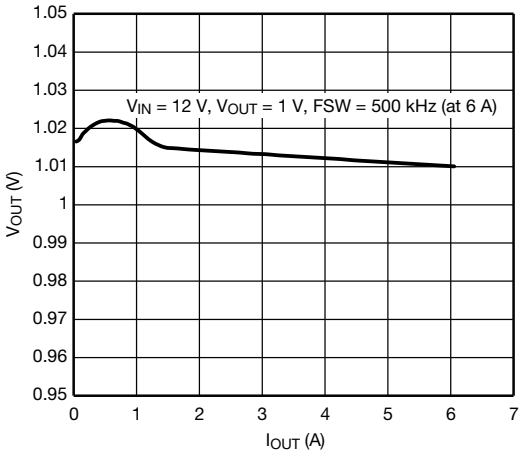
Efficiency vs. I_{OUT}
(in Continuous Conduction Mode)



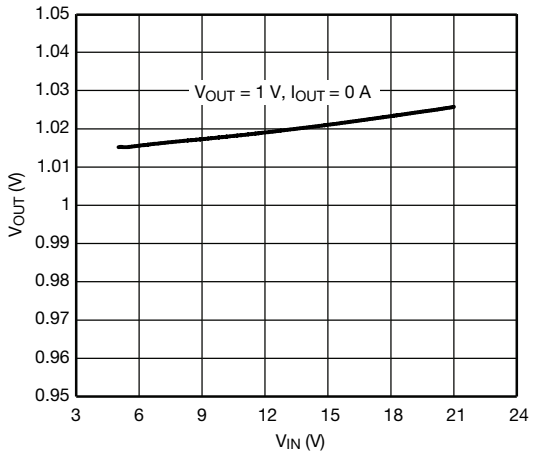
Efficiency vs. I_{OUT}
(in Power-Save-Mode)



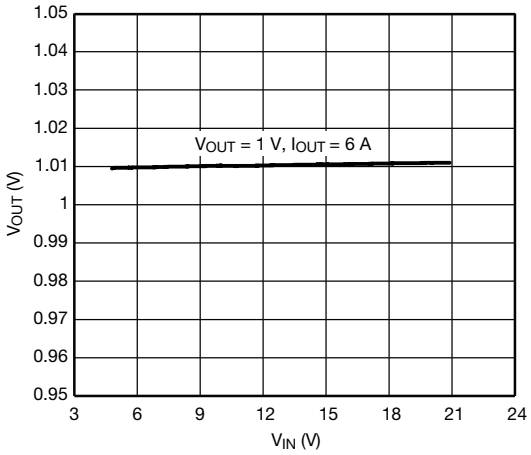
V_{OUT} vs. I_{OUT}
(in Continuous Conduction Mode)



V_{OUT} vs. I_{OUT}
(in Power-Save-Mode)

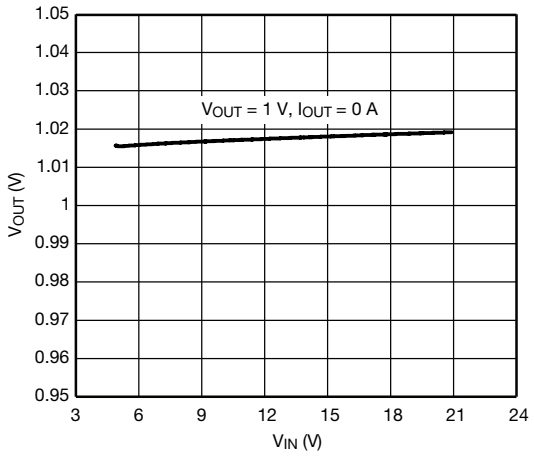


V_{OUT} vs. V_{IN} at I_{OUT} = 0 A
(in Continuous Conduction Mode, FSW = 500 kHz)

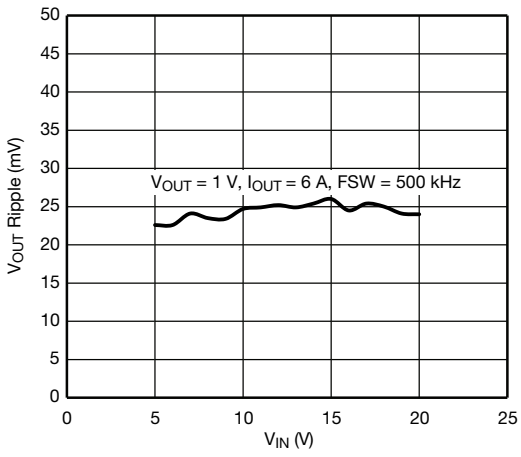


V_{OUT} vs. V_{IN} at I_{OUT} = 6 A
(in Continuous Conduction Mode, FSW = 500 kHz)

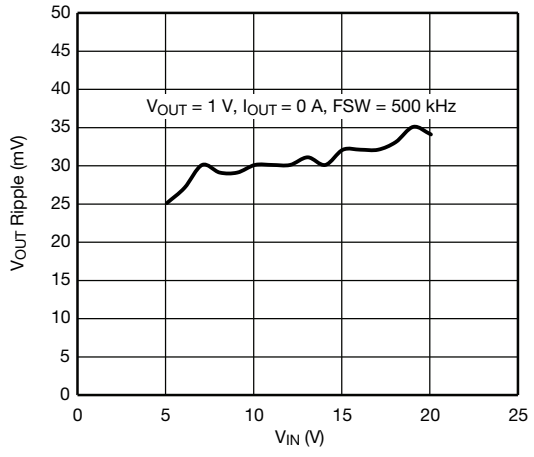
ELECTRICAL CHARACTERISTICS



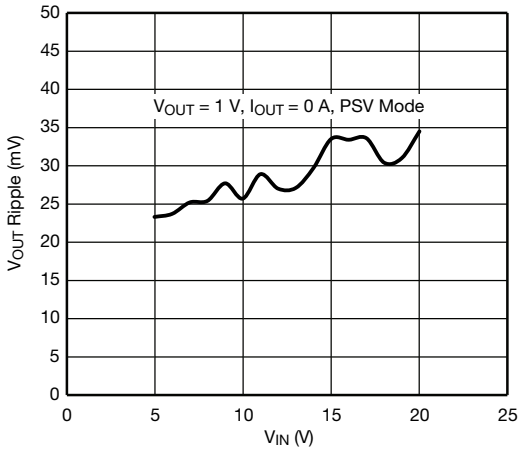
V_{OUT} vs. V_{IN}
(I_{OUT} = 0 A in Power-Save-Mode)



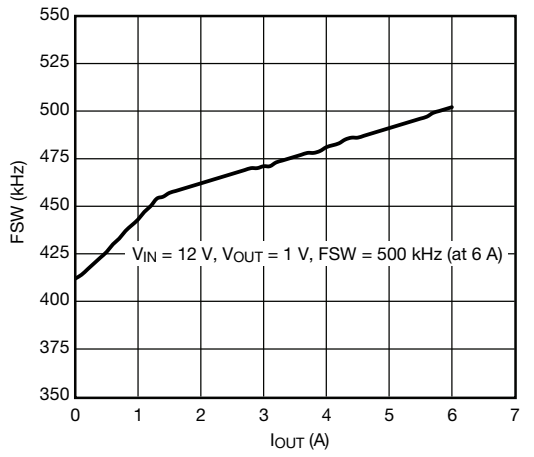
V_{OUT} Ripple vs. V_{IN}
(I_{OUT} = 6 A in Continuous Conduction Mode)



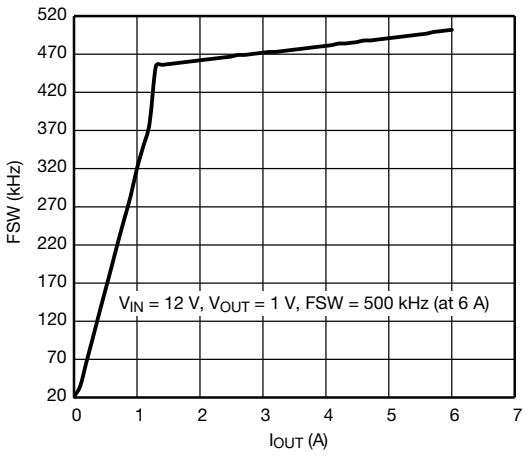
V_{OUT} Ripple vs. V_{IN}
(I_{OUT} = 0 A in Continuous Conduction Mode)



V_{OUT} Ripple vs. V_{IN}
(I_{OUT} = 0 A in Power-Save-Mode)

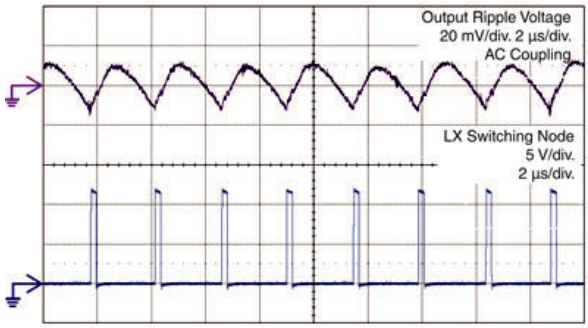


FSW vs. I_{OUT}
(in Continuous Conduction Mode)

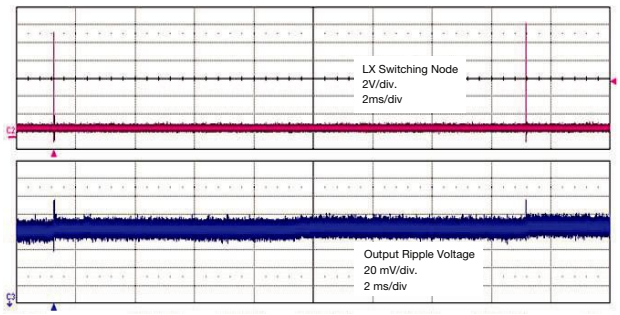


FSW vs. I_{OUT}
(in Power-Save-Mode)

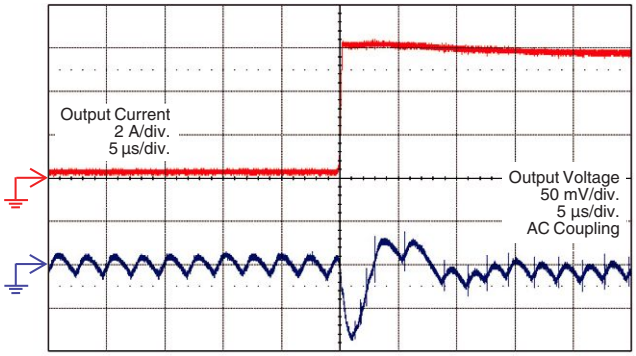
ELECTRICAL CHARACTERISTICS



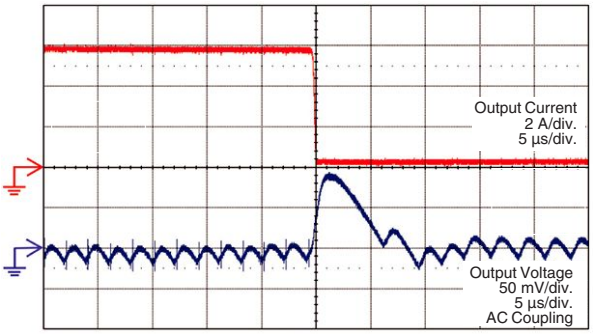
V_{OUT} Ripple in Continuous Conduction Mode (No Load)
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz)



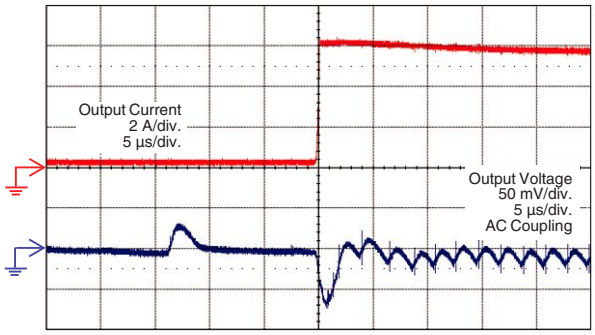
V_{OUT} Ripple in Power Save Mode (No Load)
(V_{IN} = 12 V, V_{OUT} = 1 V)



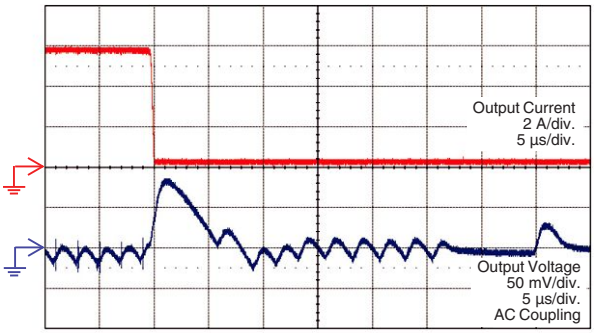
Transient Response in Continuous Conduction Mode
(0.2 A - 6 A)
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz)



Transient Response in Continuous Conduction Mode
(6 A - 0.2 A)
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz)

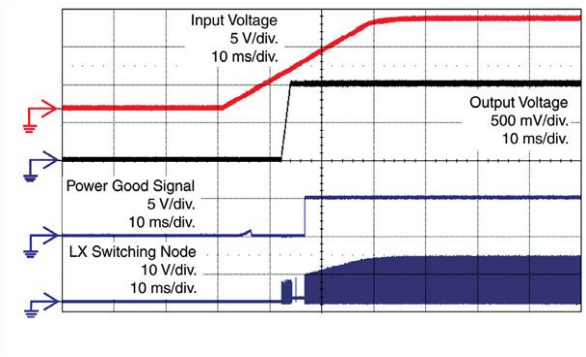


Transient Response in Power Save Mode
(0.2 A - 6 A)
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz at 6A)

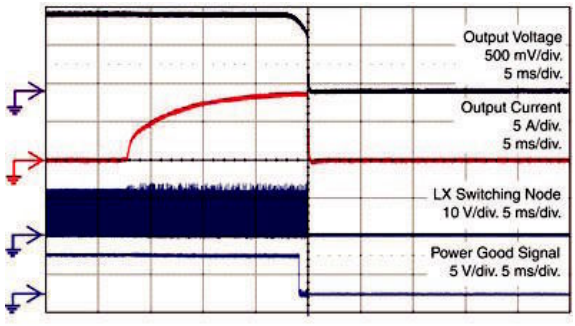


Transient Response in Power Save Mode
(6 A - 0.2 A)
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz at 6 A)

ELECTRICAL CHARACTERISTICS



Start-up with V_{IN} Ramping up
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz)



Over-Current Protection
(V_{IN} = 12 V, V_{OUT} = 1 V, FSW = 500 kHz)

APPLICATIONS INFORMATION

Device Overview

The SiC414 and SiC424 are a step down synchronous buck DC/DC converter with integrated power FETs and programmable LDO. The device is capable of 6 A operation at very high efficiency in a tiny 4 mm x 4 mm - 28 pin package. The programmable operating frequency range of 200 kHz to 1 MHz, enables the user to optimize the solution for minimum board space and optimum efficiency.

The buck controller employs pseudo-fixed frequency adaptive on-time control. This control scheme allows fast transient response thereby lowering the size of the power components used in the system.

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Input Voltage Range

The SiC414 and SiC424 requires two input supplies for normal operation: V_{IN} and V5V. V_{IN} operates over the wide range from 3 V to 28 V. V5V requires a 3.3 V or 5 V supply input that can be an external source or the internal LDO configured to supply 5 V.

Pseudo-Fixed Frequency Adaptive On-Time Control

The PWM control method used by the SiC414 and SiC424 is pseudo-fixed frequency, adaptive on-time, as shown in figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

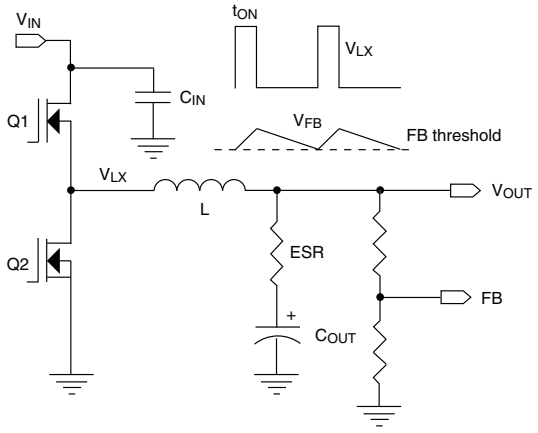


Figure 1 - PWM Control Method, V_{OUT} Ripple

The adaptive on-time control has significant advantages over traditional control methods used in the controllers today.

- Reduced component count by eliminating DCR sense or current sense resistor as no need of a sensing inductor current.
- Reduced saves external components used for compensation by eliminating the no error amplifier and other components.
- Ultra fast transient response because of fast loop, absence of error amplifier speeds up the transient response.
- Predictable frequency spread because of constant on-time architecture.
- Fast transient response enables operation with minimum output capacitance Overall, superior performance compared to fixed frequency architectures.

Overall, superior performance compared to fixed frequency architectures.

On-Time One-Shot Generator (t_{ON}) and Operating Frequency

The figure 2 shows the on-chip implementation of on-time generation. The FB Comparator output goes high when V_{FB} is less than the internal 750 mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

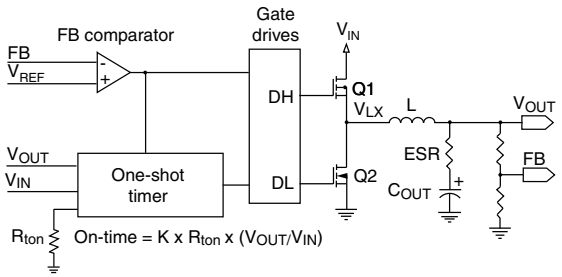


Figure 2 - On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{t_{ON} \times V_{IN}}$$

The SIC414 and SiC424 uses an external resistor to set the ontime which indirectly sets the frequency. The on-time can be programmed to provide operating frequency from 200 kHz to 1 MHz using a resistor between the t_{ON} pin and ground. The resistor value is selected by the following equation.

$$R_{tON} = \frac{1}{25\ pF \times f_{sw}} - 400\ \Omega \times \frac{V_{IN}}{V_{OUT}}$$

The maximum R_{tON} value allowed is shown by the following equation.

$$R_{ton\_MAX} = \frac{V_{IN\_MIN}}{15\ \mu A}$$

Immediately after the on-time, the DL (drive signal for the low side FET) output drives high to turn on the low-side MOSFET. DL has a minimum high time of ~ 320 ns, after which DL continues to stay high until one of the following occurs:

- V_{FB} falls below the 750 mV reference.
- The zero cross detector senses that the voltage on the LX node is below ground. Power save is activated when a zero crossing is detected.

t_{ON} limitations and V5V Supply Voltage

For V5V below 4.5 V, the t_{ON} accuracy may be limited by the input voltage.

The original R_{tON} equation is accurate if V_{IN} satisfies the below relation over the entire V_{IN} range:

$$V_{IN} < (V5V - 1.6\ V) \times 10$$

If V_{IN} exceeds (V5V - 1.6 V) x 10, for all or part of the V_{IN} range, the R_{tON} equation is not accurate. In all cases where $V_{IN} > (V5V - 1.6\ V) \times 10$, the R_{tON} equation must be modified as follows.

$$R_{tON} = \frac{1}{25\ pF \times f_{sw}} - 400\ \Omega \times \frac{(V5V - 1.6\ V) \times 10}{V_{OUT}}$$

Note that when $V_{IN} > (V5V - 1.6\ V) \times 10$, the actual on-time is fixed and does not vary with V_{IN}. When operating in this condition, the switching frequency will vary inversely with V_{IN} rather than approximating a fixed frequency.

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 750 mV reference voltage, see figure 3.

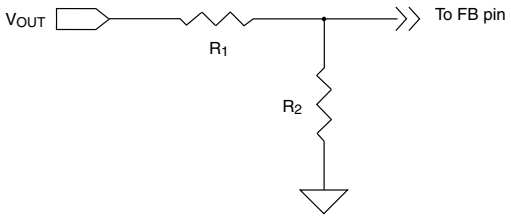


Figure 3 - Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.75 \times (1 + R_1/R_2) + V_{RIPPLE}/2$$

Enable and Power-Save Inputs

The EN/PSV and ENL inputs are used to enable or disable the switching regulator and the LDO. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 10 Ω internal resistor via the V_{OUT} pin. When EN/PSV is allowed to float, the pin voltage will float to 33 % of the voltage at V5V. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode. For V5V < 4.5 V, it is recommended to force 33 % of the V5V voltage on the EN/PSV pin to operate in forced continuous mode.

When EN/PSV is high (above 45 % of the voltage at V5V) for SiC414, the switching regulator turns on with ultrasonic

power-save enabled. The SiC414 ultrasonic power-save operation maintains a minimum switching frequency of 25 kHz, for applications with stringent audio requirements.

When EN/PSV is high (above 45 % of the voltage at V5V) for SiC424, the switching regulator turns on with power-save enabled. The SiC424 power-save operation is designed to maximize efficiency at light loads with no minimum frequency limits. This makes the SiC424 an excellent choice for portable and battery-operated systems.

The ENL input is used to control the internal LDO. This input provides a second function by acting as a V_{IN} ULVO sensor for the switching regulator. When ENL is low (grounded), the LDO is off. When ENL is a logic high but below the V_{IN} UVLO threshold (2.6 V typical), then the LDO is on and the switcher is off. When ENL is above the V_{IN} UVLO threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV pin is not grounded.

Forced Continuous Mode Operation

The SiC414 and SiC424 operates the switcher in Forced Continuous Mode (FCM) by floating the EN/PSV pin (see figure 4). In this mode of operation, the MOSFETs are turned on alternately to each other with a short dead time between them to avoid cross conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs.

For V5V < 4.5 V, it is recommended to force 33 % of the V5V voltage on the EN/PSV pin to operate in forced continuous mode.

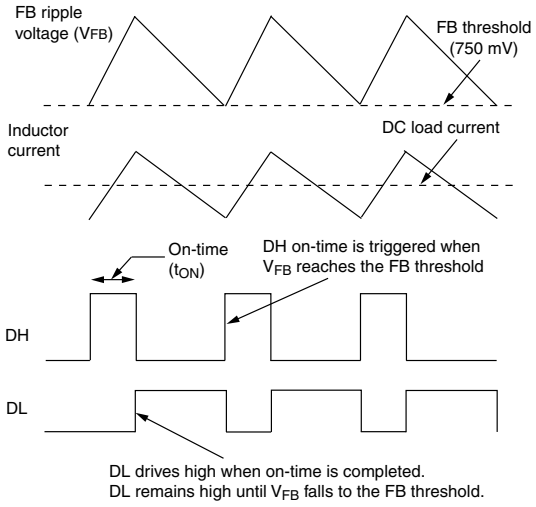


Figure 4 - Forced Continuous Mode Operation

Ultrasonic Power-Save Operation (SiC414)

The SiC414 provides ultrasonic power-save operation at light loads, with the minimum operating frequency fixed at slightly under 25 kHz. This is accomplished by using an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds 40 µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 750 mV threshold, the next DH (the drive signal for the high side FET) on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

Because the on-times are forced to occur at intervals no greater than 40 µs, the frequency will not fall far below 25 kHz. Figure 5 shows ultrasonic power-save operation.

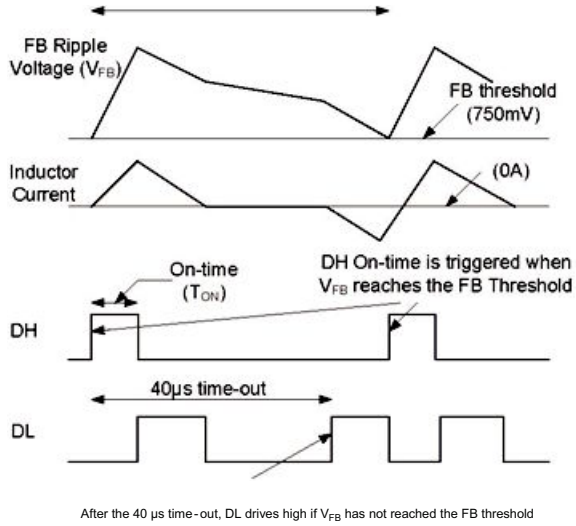


Figure 5 - Ultrasonic Power-Save Operation

Power-Save Mode Operation (SiC424)

The SiC424 provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 750 mV threshold. Because the MOSFETs are off , the load is supplied by the output capacitor. If the inductor current does not reach zero on any switching cycle, the controller immediately exits powersave and returns to forced continuous mode. Figure 6 shows power-save mode operation at light loads.

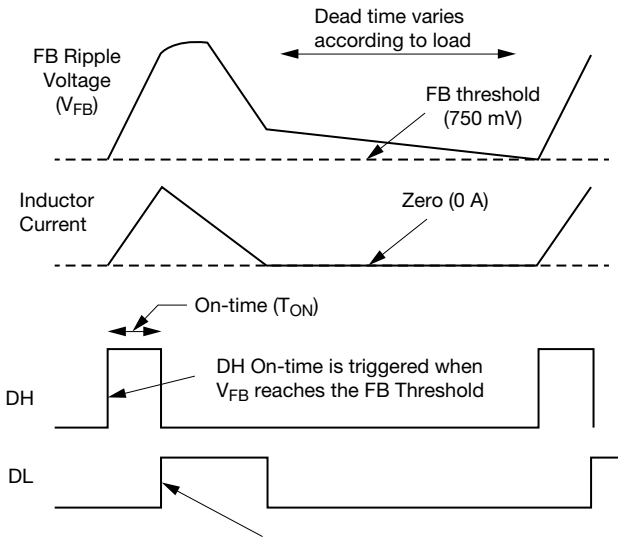


Figure 6 - Power-Save Mode Operation

Smart Power-Save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save mode enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutd-own. Smart power-save prevents this condition.

When the FB voltage exceeds 10 % above nominal, the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 750 mV trip point, a normal t_{ON} switching cycle begins.

This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 7 shows typical waveforms for the smart power-save feature.

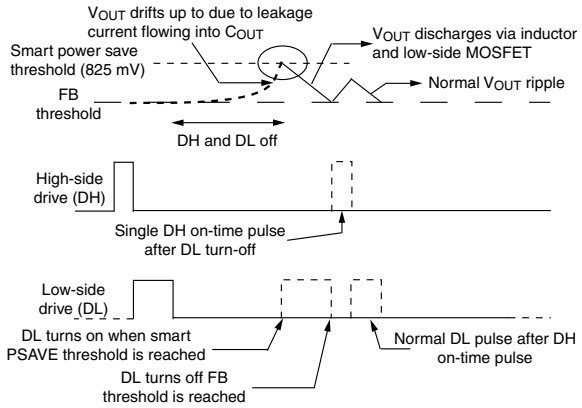


Figure 7 - Smart Power-Save

SmartDrive™

For each DH pulse the DH driver initially turns on the high side MOSFET at a lower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.5 V above P_{GND}, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching losses while maintaining high efficiency and also avoids the need for snubbers for the power MOSFETs.

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the $R_{DS(ON)}$ of the lower MOSFET for current sensing. The current limit is set by RILIM resistor. The R_{ILIM} resistor connects from the ILIM pin to the LXS pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~ 8 µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the $R_{DS(ON)}$. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by ILIM in figure 8.

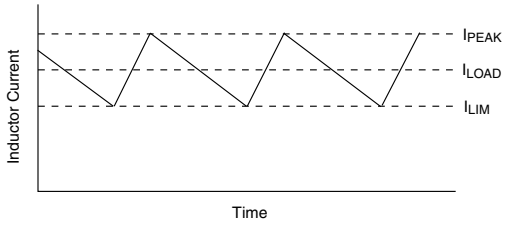


Figure 8 - Valley Current Limit

Setting the valley current limit to 6 A results in a 6 A peak inductor current plus peak ripple current. In this situation, the average (load) current through the inductor is 6 A plus one-half the peak-to-peak ripple current.

The internal 8 µA current source is temperature compensated at 4100 ppm in order to provide tracking with the $R_{DS(ON)}$. The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 1250 \times I_{LIM} \times [0.088 \times (5\ V - V5V) + 1]$$

When selecting a value for R_{ILIM} do not exceed the absolute maximum voltage value for the ILIM pin. Note that because the low-side MOSFET with low $R_{DS(ON)}$ is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. R_{ILIM} should be connected directly to LXS (pin 24).

Soft-Start of PWM Regulator

Soft-start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 750 mV in ~ 1.8 mV increments, using an internal ~ 500 kHz oscillator. When the ramp voltage reaches 750 mV, the ramp is ignored and the FB comparator switches over to a fixed 750 mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft-start profile for a wide range of applications. Typical soft-start ramp time is 1.7 ms.

During soft-start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output. This soft start operation is implemented even if FCM is selected. FCM operation is allowed only after P_{GOOD} is high.

Power Good Output

The power good (P_{GOOD}) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10 % below the nominal voltage, P_{GOOD} is pulled low. It is held low until the output voltage returns to the nominal voltage. P_{GOOD} is held low during start-up and will not be allowed to transition high until soft-start is completed (when V_{FB} reaches 750 mV) and typically 4 ms has passed.

P_{GOOD} will transition low if the V_{FB} pin exceeds + 20 % of nominal, which is also the over-voltage shutdown threshold (900 mV). P_{GOOD} also pulls low if the EN/PSV pin is low when V5V is present.

Output Over-Voltage Protection

Over-Voltage Protection (OVP) becomes active as soon as the device is enabled. The threshold is set at 750 mV + 20 % (900 mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or V5V is cycled. There is a 5 µs delay built into the OVP detector to prevent false transitions. P_{GOOD} is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls to 75 % of its nominal voltage (falls to 562.5 mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to turn off the MOSFETs. The controller stays off until EN/PSV is toggled or V5V is cycled.

V5V UVLO, and POR

Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until V5V rises above 2.9 V. An internal Power-On Reset (POR) occurs when V5V exceeds 2.9 V, which resets the fault latch and soft-start counter to begin the soft-start cycle. The SiC414 and SiC424 then begins a soft-start cycle. The PWM will shut off if V5V falls below 2.7 V.

LDO Regulator

The device features an integrated LDO regulator with a fixed output voltage of 5 V. There is also an enable pin (ENL) for the LDO that provides independent control. The LDO voltage can also be used to provide the bias voltage for the switching regulator.

A minimum capacitance of 1 µF referenced to A_{GND} is normally required at the output of the LDO for stability. If the LDO is providing bias power to the device, then a minimum 0.1 µF capacitor referenced to A_{GND} is required, along with a minimum 1 µF capacitor referenced to P_{GND} to filter the gate drive pulses. Refer to the layout guide-lines section.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. V_{LDO} output
3. V_{IN} input voltage

When the ENL pin is high, the LDO will begin start-up, see figure 9. During the initial phase, when the LDO output voltage is near zero, the LDO initiates a current-limited start-up (typically 85 mA) to charge the output capacitor. When V_{LDO} has reached 90 % of the final value, the LDO current limit is increased to ~ 200 mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator.

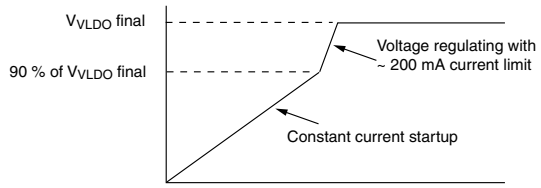


Figure 9 - LDO Start-Up

LDO Switch-over Function

The SiC414 and SiC424 includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient DC/DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the V_{LDO} pin directly to the V_{OUT} pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SiC414 and SiC424, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over logic waits for 32 switching cycles before it starts the switch-over. There are two methods that determine the switch-over of V_{LDO} to V_{OUT}.

In the first method, the LDO is already in regulation and the DC/DC converter is later enabled. As soon as the P_{GOOD} output goes high, the 32 cycle counter is started. The voltages at the V_{LDO} and V_{OUT} pins are then compared; if the

two voltages are within ± 300 mV (typically) of each other, within 32 cycles, the V_{LDO} pin connects to the V_{OUT} pin using an internal switch, and the LDO is turned off.

In the second method, the DC/DC converter is already running and the LDO is enabled. In this case the 32 cycles are started as soon as the LDO reaches 90 % of its final value. At this time, the V_{LDO} and V_{OUT} pins are compared, and if within ± 300 mV (typically) the switch-over occurs and the LDO is turned off.

Switch-Over Limitations on V_{OUT} and V_{LDO}

Because the internal switch-over circuit always compares the V_{OUT} and V_{LDO} pins at start-up, there are voltage limitations on permissible combinations of these pins. Consider the situation where V_{OUT} is programmed to 4.7 V. After start-up, the device would connect V_{OUT} to V_{LDO} and disable the LDO, since the two voltages are within the ± 300 mV switch-over window. To avoid unwanted switch-over, the minimum difference between the voltages for V_{OUT} and V_{LDO} should be ± 500 mV.

Switch-Over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in figure 10.

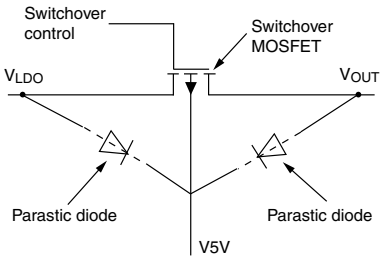


Figure 10 - Switch-Over MOSFET Parasitic Diodes

There are some important design rules that must be followed to prevent forward bias of these diodes. The following two conditions need to be satisfied in order for the parasitic diodes to stay off.

- $V5V \geq V_{LDO}$
- $V5V \geq V_{OUT}$

If either V_{LDO} or V_{OUT} is higher than V5V, then the respective diode will turn on and the SiC414 and SiC424 operating current will flow through this diode. This has the potential of damaging the device.

ENL Pin and V_{IN} UVLO

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. The V_{IN} UVLO voltage is programmable via a resistor divider at the V_{IN}, ENL, and A_{GND} pins. ENL is the enable/disable signal for the LDO. In order to implement the V_{IN} UVLO there is also a timing requirement that needs to be satisfied. If the ENL pin transitions low within 2 switching cycles and is < 1 V, then the LDO will turn off, but the switcher remains on. If ENL goes below the V_{IN} UVLO threshold and stays above 1 V, then the switcher will turn off but the LDO remains on. The V_{IN} UVLO function has a typical threshold of 2.6 V on the V_{IN} rising edge.The falling edge threshold is 2.4 V.

Note that it is possible to operate the switcher with the LDO disabled, but the ENL pin must be below the logic low threshold (0.4 V maximum). The table below summarizes the function of the ENL and EN pins, with respect to the rising edge of ENL.

EN	ENL	LDO	Switcher
Low	Low, < 0.4 V	Off	Off
High	Low, < 0.4 V	Off	On
Low	High, < 2.6 V	On	Off
High	High, < 2.6 V	On	Off
Low	High, > 2.6 V	On	Off
High	High, > 2.6 V	On	On

Figure 11 below shows the ENL voltage thresholds and their effect on LDO and switcher operation.

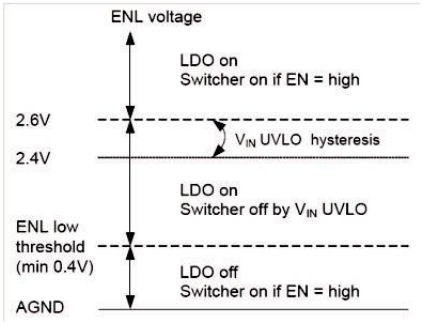


Figure 11 - ENL Thresholds

ENL Logic Control of PWM Operation

When the ENL input is driven above 2.6 V, it is impossible to determine if the LDO output is going to be used to power the device or not. In self-powered operation where the LDO will power the device, it is necessary during the LDO start-up to hold the PWM switching off until the LDO has reached 90 % of the final value. This prevents overloading the current-limited LDO output during the LDO start-up. However, if the switcher was previously operating (with EN/PSV high but ENL at ground, and V5V supplied externally), then it is undesirable to shut down the switcher. To prevent this, when the ENL input is above 2.6 V (above the V_{IN} UVLO threshold), the internal logic checks the P_{GOOD} signal. If P_{GOOD} is high, then the switcher is already running and the LDO will run through the start-up cycle without affecting the switcher. If P_{GOOD} is low, then the LDO will not allow any PWM switching until the LDO output has reached 90 % of its final value.

Using the On-chip LDO to Bias the SIC414/SIC424

The following steps must be followed when using the onchip LDO to bias the device.

- Connect V5V to V_{LDO} before enabling the LDO.
- Any external load on V_{LDO} should not exceed 40 mA until the LDO voltage has reached 90 % of final value.
- Do not connect the EN pin directly to the V5V or any other supply voltage if V_{OUT} is greater than or equal to 4.5 V.

Many applications connect the EN pin to V5V and control the on/off of the LDO and PWM simultaneously with the ENL pin. This allows one signal to control both the bias and power output of the SiC414 and SiC424. When V_{OUT} > 4.5 V this configuration can cause problems due to the parasitic diodes in the LDO switchover circuitry. After the V_{OUT} > 4.5 V PWM output is up and running the switchover diodes can hold up V5V > UVLO even if the ENL pin is grounded, turning off the LDO. Operating in this way can potentially damage the part.

Design Procedure

When designing a switch mode power supply, the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design:

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate - continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design:

- V_{IN} = 12 V ± 10 %
- V_{OUT} = 1.5 V ± 4 %
- f_{SW} = 250 kHz
- Load = 6 A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 250 kHz which results from using component selected for optimum size and cost.

A resistor (R_{tON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{tON} = \frac{1}{25\ pF \times f_{sw}} - 400\ \Omega \times \frac{V_{IN}}{V_{OUT}}$$

To select R_{tON}, use the maximum value for V_{IN}, and for t_{ON} use the value associated with maximum V_{IN}.

$$t_{ON} = \frac{V_{OUT}}{V_{INMAX.} \times f_{SW}}$$

t_{ON} = 303 ns at 13.2 V_{IN}, 1 V_{OUT}, 250 kHz

Substituting for R_{tON} results in the following solution

R_{tON} = 130.9 kΩ, use R_{tON} = 130 kΩ.

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4 A then Power-save operation will typically start for loads less than 2 A. If ripple current is set at 40 % of maximum load current, then power-save will start for loads less than 20 % of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25 % to 50 % of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50 % of the maximum load current. Therefore ripple current will be 50 % x 6 A or 3 A. To find the minimum inductance needed, use the V_{IN} and t_{ON} values that correspond to $V_{INMAX.}$

$$L = \frac{(13.2\ V - 1\ V) \times 318\ ns}{3\ A} = 1.26\ \mu H$$

A slightly larger value of 1.5 µH is selected. This will decrease the maximum I_{RIPPLE} to 2.53 A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current. The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$t_{ON\_VINMIN} = \frac{25\ pF \times R_{tON} \times V_{OUT}}{V_{INMIN}} + 10\ ns = 311\ ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(10.8 - 1\ V) \times 311\ ns}{1.5\mu H} = 2.03\ A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is for the output voltage regulation to be ± 4 % under static conditions. The internal 750 mV reference tolerance is 1 %. Assuming a 1 % tolerance from the FB resistor divider, this allows 2 % tolerance due to V_{OUT} ripple. Since this 2 % error comes from 1/2 of the ripple voltage, the allowable ripple is 4 %, or 40 mV for a 1 V output.

The maximum ripple current of 2.53 A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{40\ mV}{2.53\ A}$$

$$ESR_{MAX} = 15.8\ m\Omega$$

The output capacitance is chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1 µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$C_{OUT\_MIN} = \frac{L\ (I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX})^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (100 mV rise upon load release), and a 6 A load release, the required capacitance is shown by the next equation.

$$C_{OUT\_MIN} = \frac{1.5\ \mu H\ (6\ A + \frac{1}{2} \times 2.53)^2}{(1.05)^2 - (1\ V)^2}$$

$$C_{OUT\_MIN} = 772\ \mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 750 mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately - V_{OUT}. This causes a down-slope or falling dI/dt in the inductor. If the load dI/dt is not much faster than the - dI/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt:

Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 10 + 1/2 \times 2.53 = 7.26\ A$$

Rate of change of load current = dI_{LOAD}/dt

I_{MAX} = maximum load release = 6 A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2\ (V_{PK} - V_{OUT})}$$

Example

$$\text{Load } \frac{dI_{LOAD}}{dt} = \frac{1.25\ A}{1\ \mu s}$$

This causes the output current to move from 6 A to 0 A in 4.8 µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 7.26 \times \frac{1.5\ \mu H \times \frac{7.26}{1\ V} - \frac{6\ A}{1.25\ A} \times 1\ \mu s}{2\ (1.05\ V - 1\ V)}$$

$$C_{OUT} = 443\ \mu F$$

Note that C_{OUT} is much smaller in this example, 443 µF compared to 772 µF based on a worst-case load release. To meet the two design criteria of minimum 443 µF and maximum 15 mΩ ESR, select two capacitors rated at 220 µF and 15 mΩ ESR or less.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10 mV_{p-p}, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10 pF) capacitor across the upper feedback resistor, as shown in figure 12. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

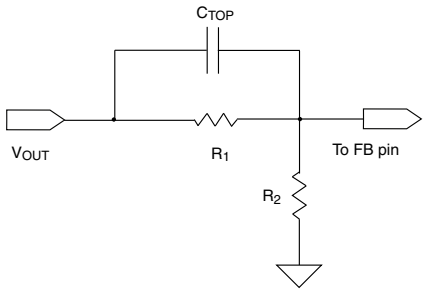


Figure 12 - Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is a decrease in load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10 mV_{p-p} at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications, the total output ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{SW}}$$

Using Ceramic Output Capacitors

When applications use ceramic output capacitors, the ESR is normally too small to meet the previously stated ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in figure 12. This network creates a ramp voltage across CL, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitive coupled into the FB pin via capacitor C_C.

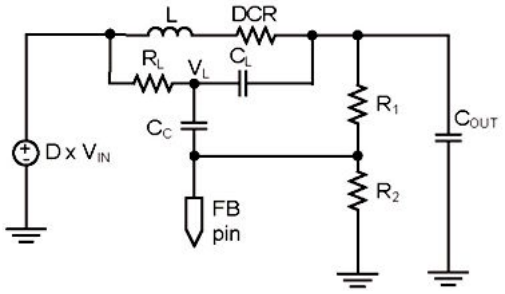


Figure 13 - Virtual ESR Ramp Circuit

Dropout Performance

The output voltage adjustment range for continuous conduction operation is limited by the fixed 250 ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} \times t_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator off set is trimmed so that under static conditions it trips when the feedback pin is 750 mV, 1 %.

The on-time pulse from the SiC414 and SiC424 in the design example is calculated to give a pseudo-fixed frequency of 250 kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, 1/2 of the output ripple appears as a DC regulation error. For example, if the output ripple is 50 mV with V_{IN} = 6 V, then the measured DC output will be 25 mV above the comparator trip point. If the ripple increases to 80 mV with V_{IN} = 25 V, then the measured DC output will be 40 mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive

droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1 % feedback resistors may result in up to an additional 1 % error. If tighter DC accuracy is required, resistors with lower tolerances should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage inductor. An adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

BILL OF MATERIALS

Qty.	Ref. Designator	Description	Value	Voltage	Footprint	Part Number	Manufacturer
1	U1	SiC424 COT Buck Converter			MLPQ-28 4 x 4 mm	SiC424	Vishay
4	C16, C18, C17, C23	220 µF, 10 V D	220 µF	10 V	SM593D	593D227X0010E2TE3	Vishay
4	C15, C20, C21, C22	10 µF, 16 V, X7R.B, 1206	10 µF	16 V	SM1206	GRM31CR71C106KAC7L	Murata
1	L1	1 µH	1 µH		IHLP2525	IHLP2525EZER1R0M01	Vishay
1	Q1	Si4812BDY-E3			SO-8	Si4812BDY	Vishay
5	C1, C2, C3, C4, C29	CAP. 22 µF, 16 V, 1210	22 µF	16 V	SM1210	GRM32ER71C226ME18L	Murata
3	C8, C9, C10	CAP. 10 µF, 25 V, 1210	10 µF	25 V	SM1210	TMK325B7106MM-T	Taiyo Yuden
1	C26	4.7 µF, 10 V, 0805	4.7 µF	10 V	SM0805	LMK212B7475KG-T	Taiyo Yuden
1	C12	CAP. Radial 150 µF, 35 V	150 µF	35 V	Radial	EU-FM1V151	Panasonic
1	R4	1 Ω, 2512	1 Ω	200 V	SM2512	CRCW25121R00FKEG	Vishay
2	R7, R11	Res. 0 Ω	0 Ω	50 V	SM0603	CRCW0603 0000ZOEA	Vishay
1	R39	0R, 50 V, 0402	0 Ω	50 V	SM0402	CRCW04020000ZOED	Vishay
1	R3	Res. 1K, 50 V, 0402	1K	50 V	SM0402	CRCW04021K00FKED	Vishay
2	R5, R6	Res. 100K, 0603	100K	50 V	SM0603	CRCW0603 100K FKEA	Vishay
3	R8, R10, R15	Res. 10K, 50 V, 0603	10K	50 V	SM0603	CRCW060310KFKED	Vishay
1	C6	CAP. CER 1 µF, 35 V, X7R 0805	1 µF	35 V	SM0805	GMK212B7105KG-T	Murata
1	R23	Res. 16.5 kΩ, 1/10 W, 1%, 0603 SMD	16.5K	50 V	SM0603	CRCW060316K5FKEA	Vishay
1	R13	Res. 1K, 50 V, 0402	1K	50 V	SM0402	CRCW04021K00FKED	Vishay
1	C30	CAP. 180 pF, 0402	180 pF	50 V	SM0402	VJ0402A181JXACW1BC	Vishay
1	R30	Res. 78.7 kΩ, 1/10 W, 1 %, 0603 SMD	78.7k	50 V	SM0603	CRCW060378K7FKEA	Vishay
4	C7, C11, C14, C28	CAP. 0.1 µF, 50 V, 0603	0.1 µF	50 V	SM0603	VJ0603Y104KXACW1BC	Vishay
1	C5	CAP. 0.1 µF, 10 V, 0402	0.1 µF	10 V	SM0402	VJ0402Y104MXQCW1BC	Vishay
4	B1, B2, B3, B4	Solder Banana				575-6	Keystone
1	C13	CAP. 0.01 µF, 50 V, 0402	0.01 µF	50 V	SM0402	VJ0402Y103KXACW1BC	Vishay
12	P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12	Probe Hook			Terminal	0	Keystone
4	M1, M2, M3, M4	Nylon on Stand off				8834	Keystone

PCB LAYOUT OF THE EVALUATION BOARD

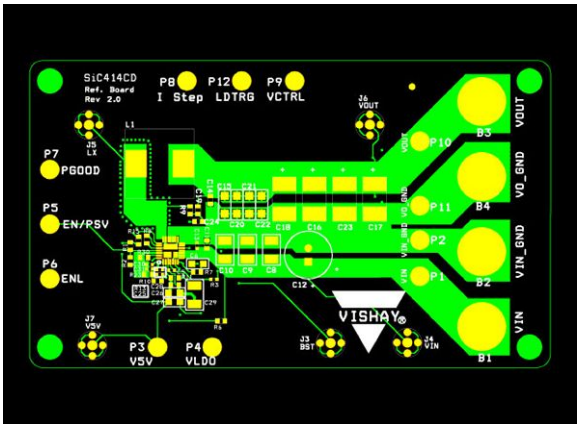


Figure 14. Top Layer

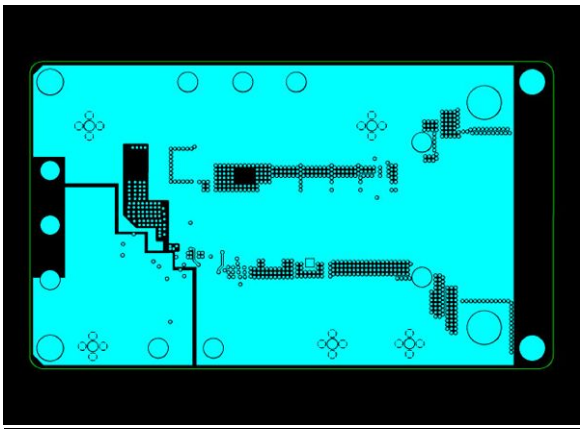


Figure 15. Mid Layer1

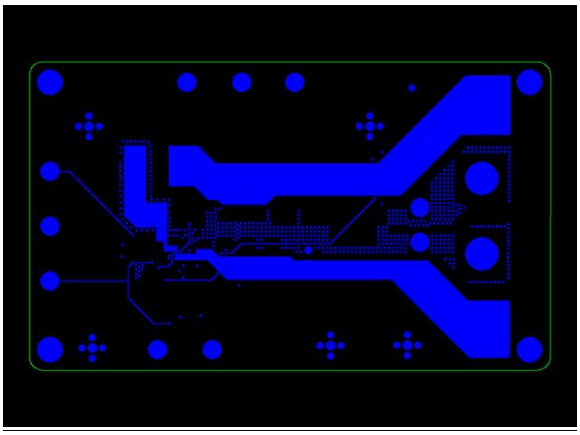


Figure 16. Mid Layer2

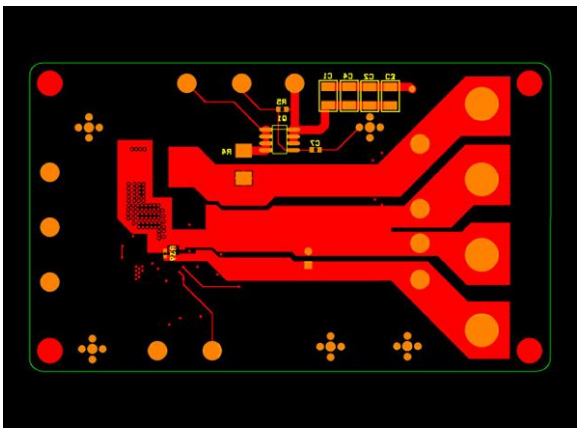
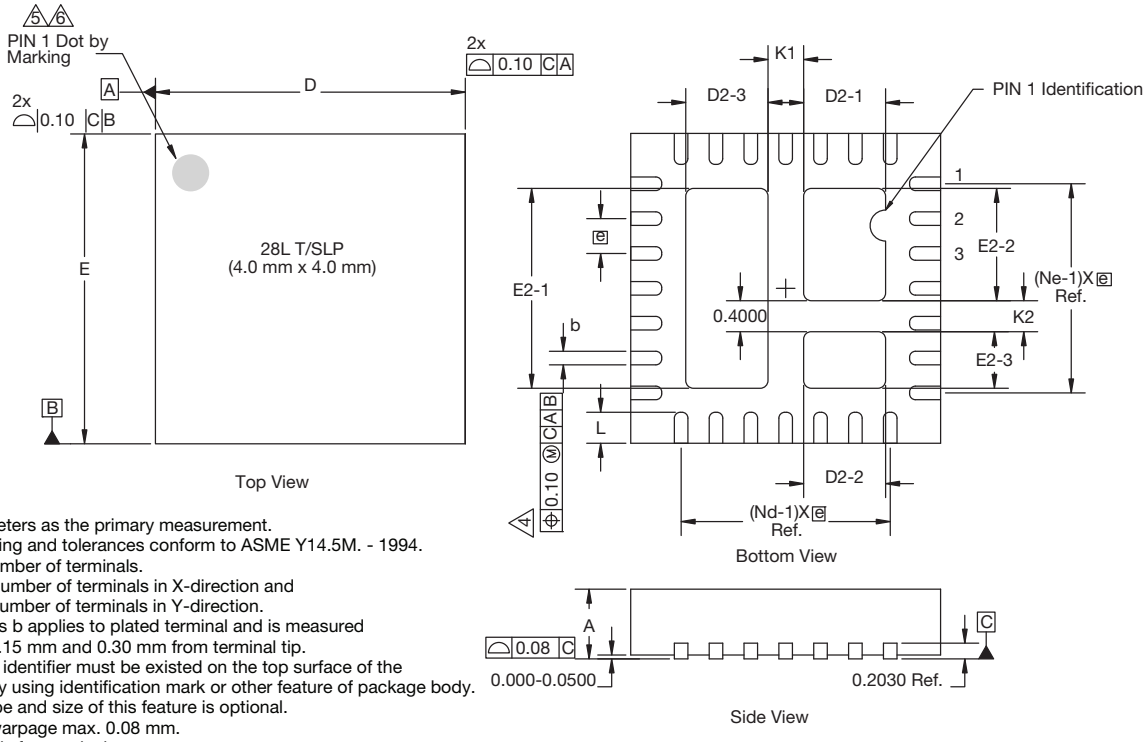


Figure 17. Bottom Layer

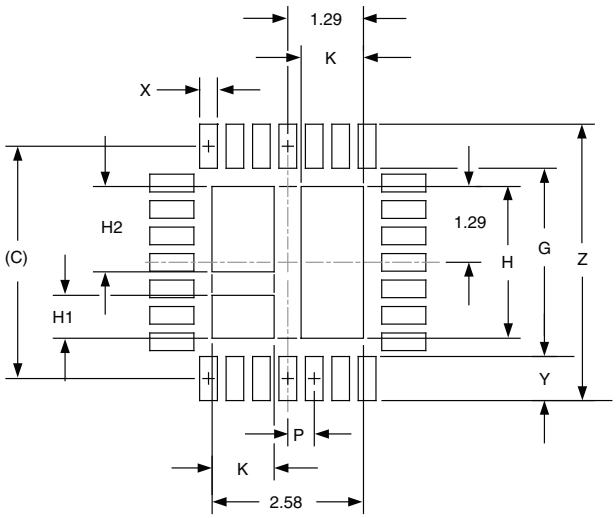
PACKAGE DIMENSIONS AND MARKING INFO



Notes:
1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and
   Ne is the number of terminals in Y-direction.
4. Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max. 0.08 mm.
8. Applied only for terminals.

Dimensions	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A(8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 Ref.			0.008 Ref.	
b(4)	0.175	0.225	0.275	0.007	0.009	0.011
D		4.00 BSC			0.157 BSC	
e		0.45 BSC			0.018 BSC	
E		4.00 BSC			0.157 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
N(3)		28			28	
Nd(3)		7			7	
Ne(3)		7			7	
D2-1	0.912	1.062	1.162	0.036	0.042	0.046
D2-2	0.908	1.058	1.158	0.036	0.042	0.046
D2-3	0.908	1.058	1.158	0.036	0.042	0.046
E2-1	2.43	2.58	2.68	0.096	0.102	0.105
E2-2	1.30	1.45	1.55	0.051	0.057	0.061
E2-3	0.58	0.73	0.83	0.023	0.029	0.033
K1		0.46 BSC			0.018 BSC	
K2		0.40 BSC			0.016 BSC	

RECOMMENDED LAND PATTERN



Dimensions	Millimeters
C	(3.95)
G	3.20
H	2.58
H1	0.73
H2	1.45
K	1.06
P	0.45
X	0.30
Y	0.75
Z	4.70

Notes:
a. Controlling dimensions are in millimeters (angles in degrees).
b. This land pattern is for reference purposes only. Consult your manufacturing group to ensure your company's manufacturing guidelines are met.
c. Square package-dimensions apply in both X and Y directions.

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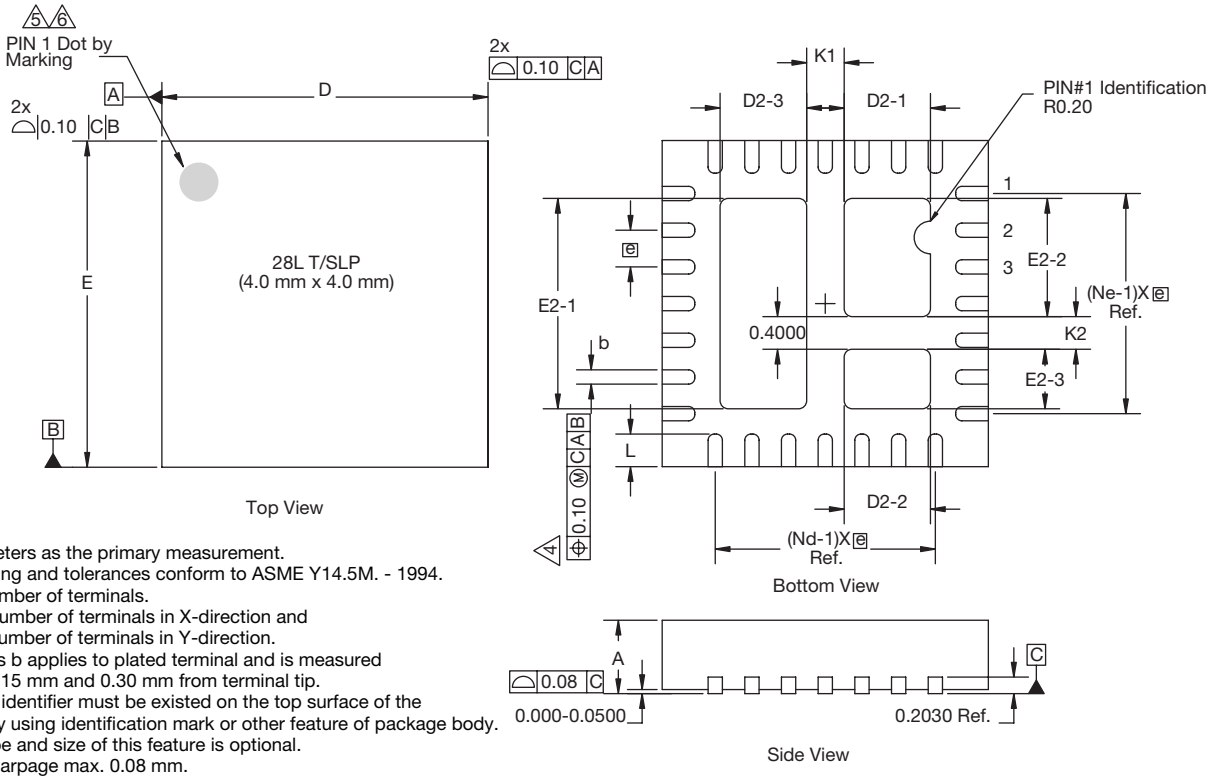
PowerPAK® MLP44-28L CASE OUTLINE

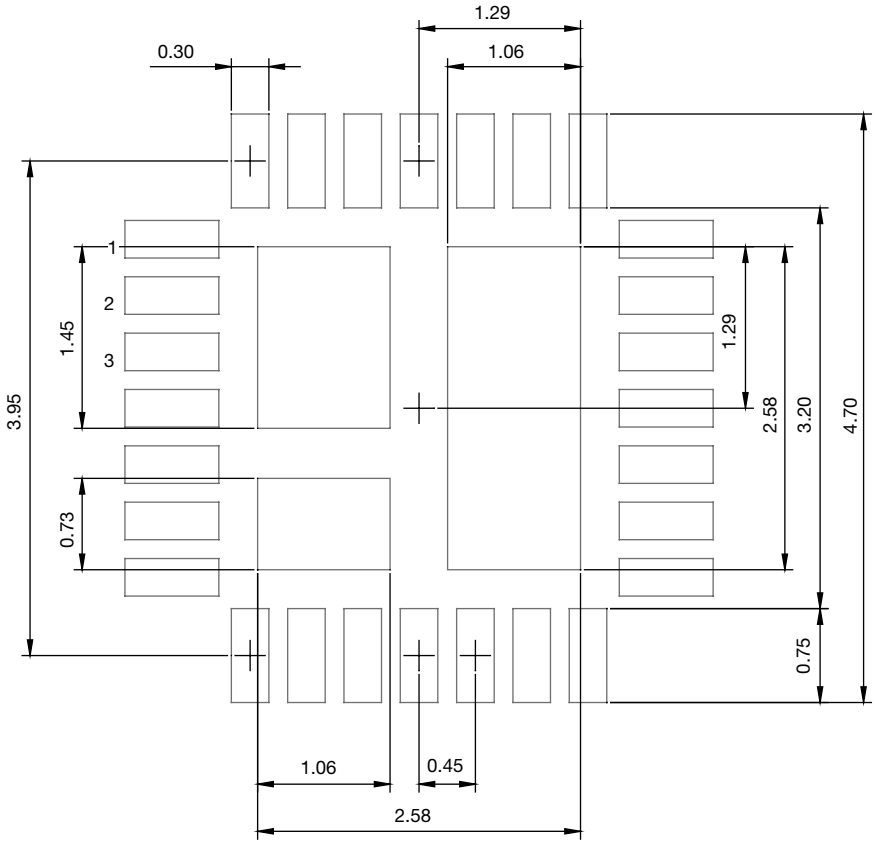


Notes:
1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and
   Ne is the number of terminals in Y-direction.
4. Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max. 0.08 mm.
8. Applied only for terminals.

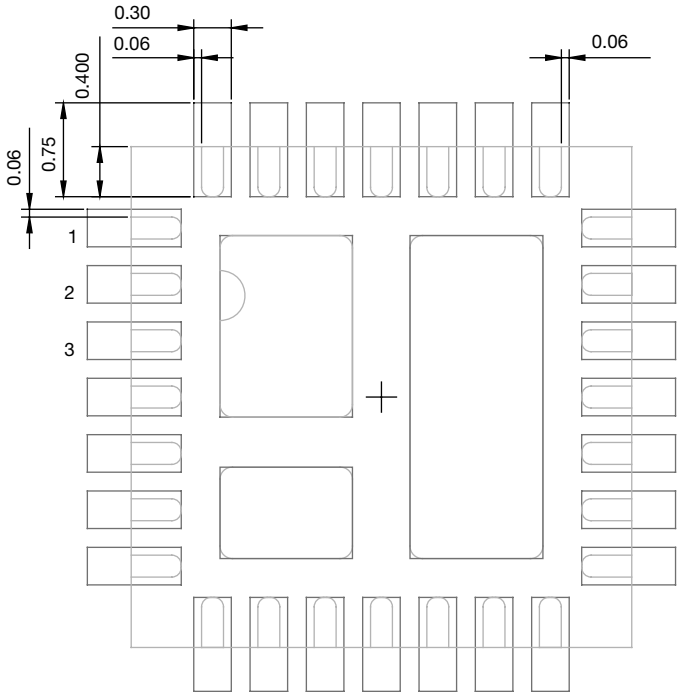
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 REF			0.008 REF	
b (4)	0.175	0.225	0.275	0.007	0.009	0.011
D		4.00 BSC			0.157 BSC	
e		0.45 BSC			0.018 BSC	
E		4.00 BSC			0.157 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
N (3)		28			28	
Nd (3)		7			7	
Ne (3)		7			7	
D2-1	0.908	1.058	1.158	0.036	0.042	0.046
D2-2	0.908	1.058	1.158	0.036	0.042	0.046
D2-3	0.912	1.062	1.162	0.036	0.042	0.046
E2-1	2.43	2.58	2.68	0.096	0.102	0.105
E2-2	1.30	1.45	1.55	0.051	0.057	0.061
E2-3	0.58	0.73	0.83	0.023	0.029	0.033
K1		0.46 BSC			0.018 BSC	
K2		0.40 BSC			0.016 BSC	
ECN: T10-0056-Rev. A, 22-Feb-10 DWG: 5996						

PowerPAK® MLP44-28L Land Pattern

Recommended Land Pattern



Recommended Land Pattern vs. Case Outline



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