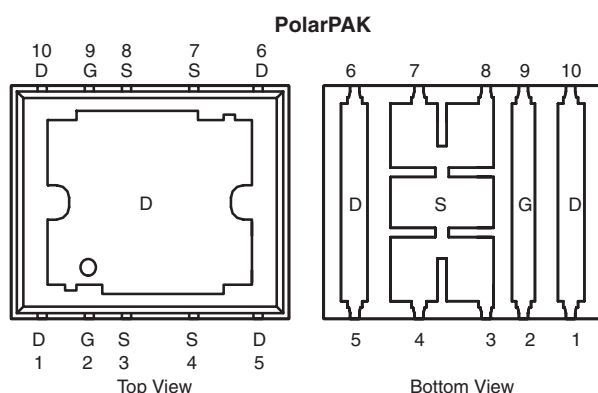


N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)		Q_g (Typ.)
		Silicon Limit	Package Limit	
100	0.0142 at $V_{GS} = 10$ V	64	60 ^a	50 nC

Package Drawing
www.vishay.com/doc?72945



Top surface is connected to pins 1, 5, 6, and 10

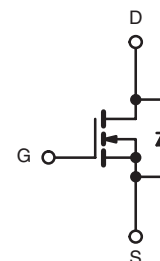
Ordering Information: SiE854DF-T1-E3 (Lead (Pb)-free)
SiE854DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- Primary Side Switch
- Half-Bridge



N-Channel MOSFET
For Related Documents
www.vishay.com/ppg?69824

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	64 (Silicon Limit)	A
		60 ^a (Package Limit)	
		52	
		13.2 ^{b, c}	
		10.5 ^{b, c}	
Pulsed Drain Current	I_{DM}	60	A
Continuous Source-Drain Diode Current	I_S	60 ^a	A
		4.3 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	40	A
Single Pulse Avalanche Energy	E_{AS}	80	mJ
Maximum Power Dissipation	P_D	125	W
		80	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	$^\circ\text{C}$

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	R_{thJC} (Drain)	0.8	1	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 68 °C/W.

c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		120		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 10		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	25			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 13.2 A		0.0117	0.0142	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 13.2 A		30		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		3100		pF
Output Capacitance	C _{oss}			250		
Reverse Transfer Capacitance	C _{rss}			95		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 13.2 A		50	75	nC
Gate-Source Charge	Q _{gs}			16		
Gate-Drain Charge	Q _{gd}			13		
Gate Resistance	R _g	f = 1 MHz		1	1.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		15	25	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			30	45	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	A
Pulse Diode Forward Current ^a	I _{SM}				60	
Body Diode Voltage	V _{SD}	I _S = 10 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C		70	110	ns
Body Diode Reverse Recovery Charge	Q _{rr}			195	300	nC
Reverse Recovery Fall Time	t _a			56		ns
Reverse Recovery Rise Time	t _b			14		

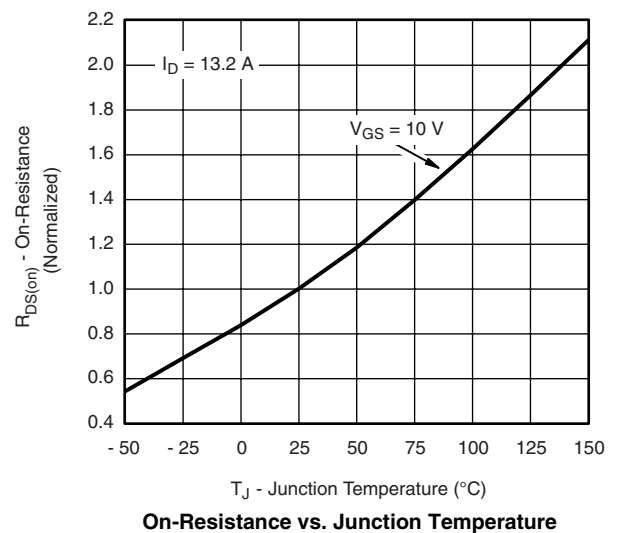
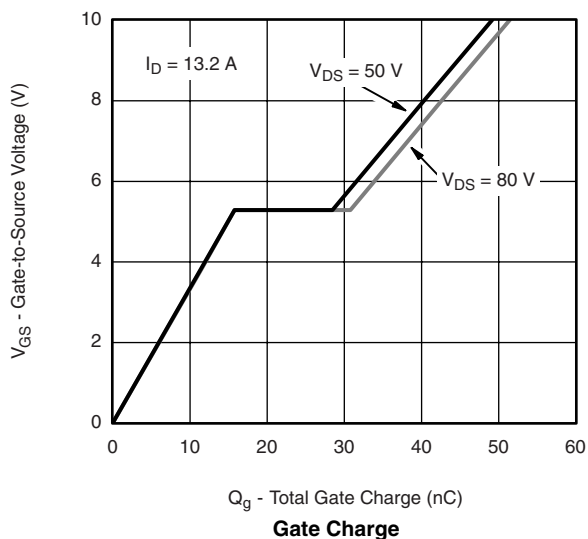
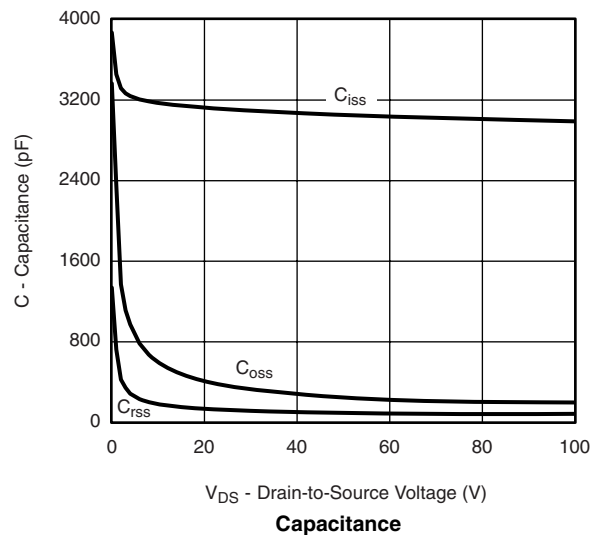
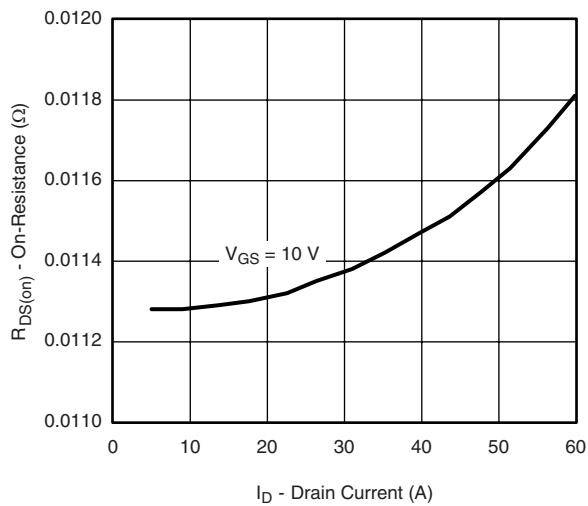
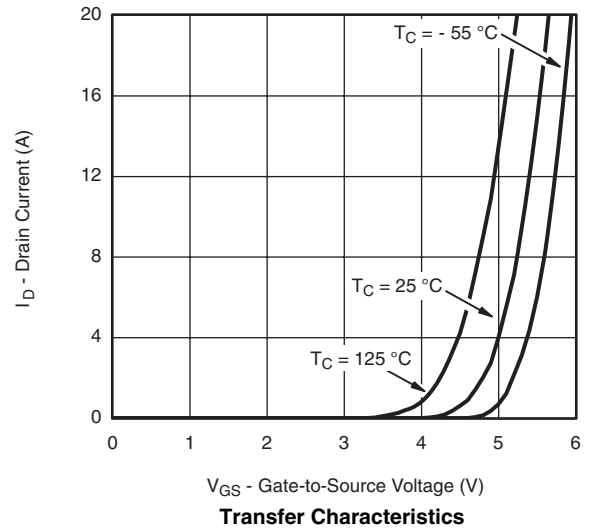
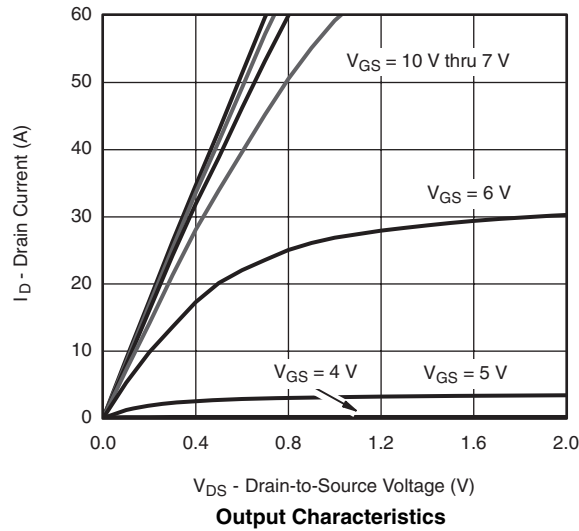
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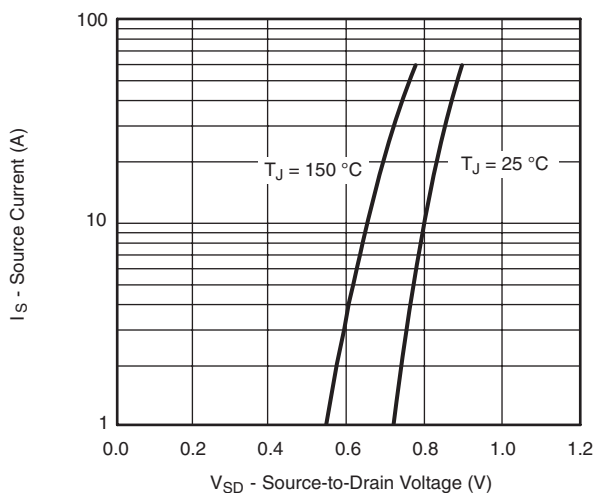
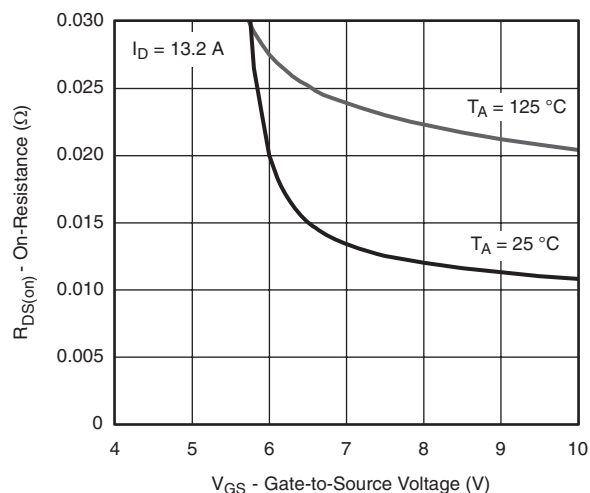
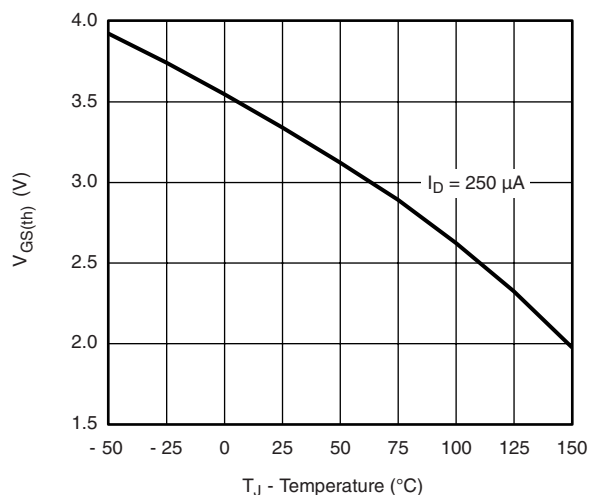
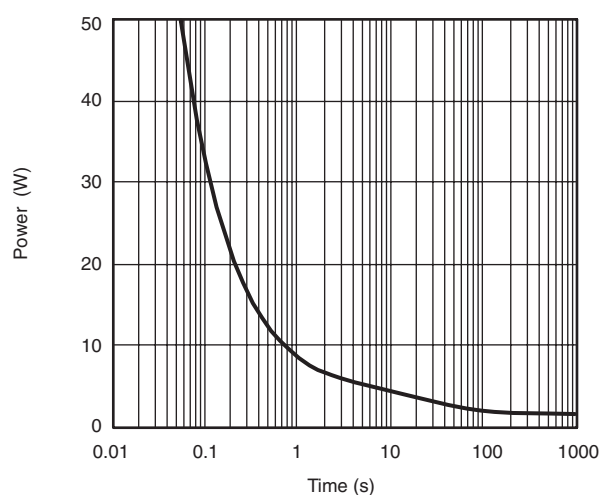
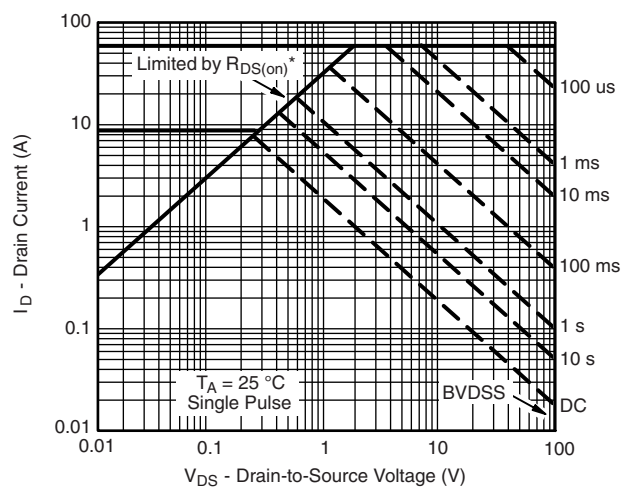
a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing.

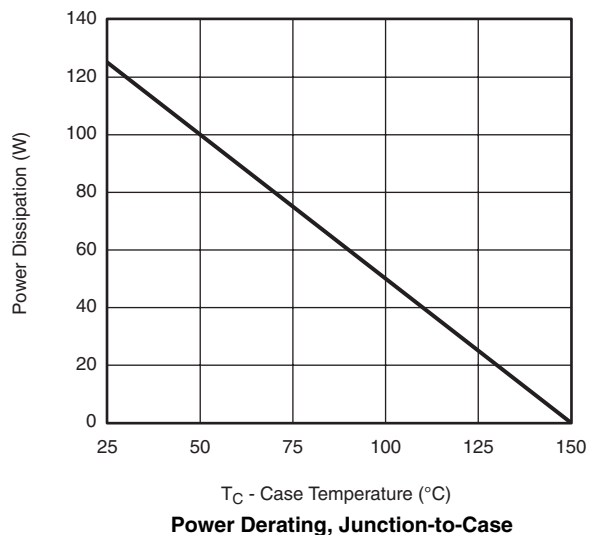
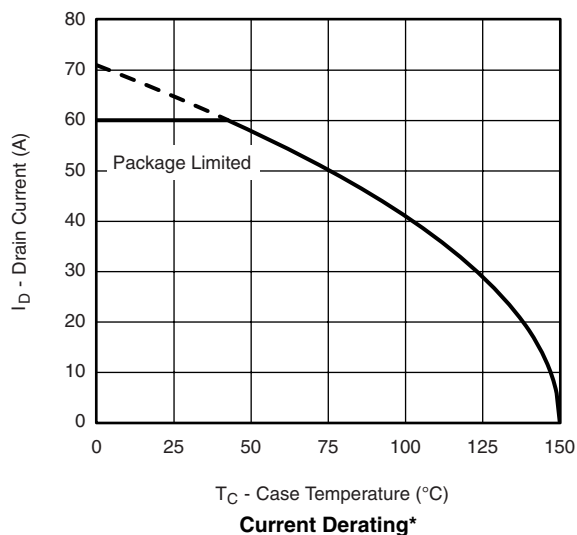
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

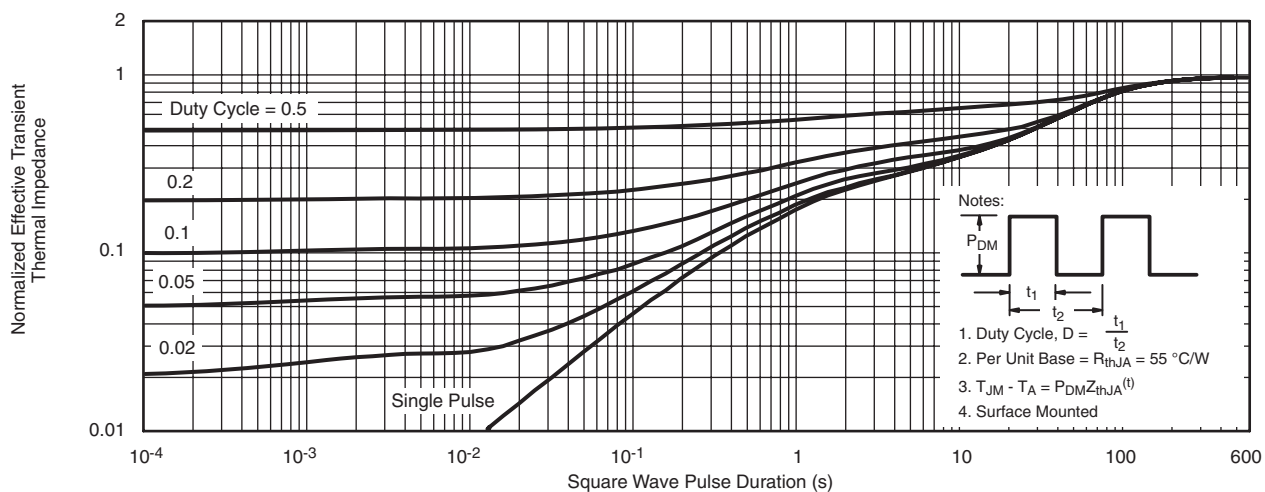
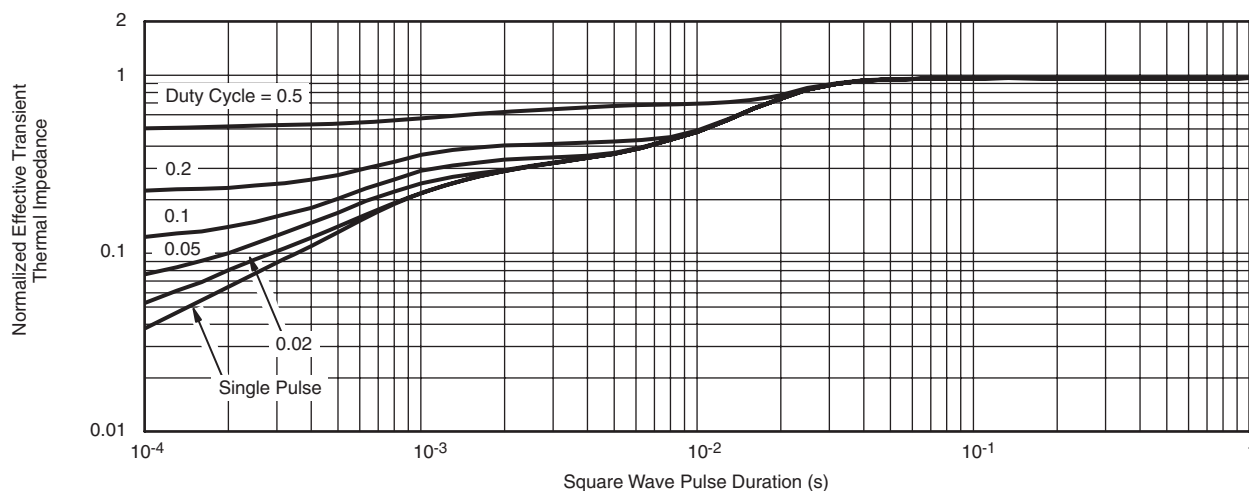
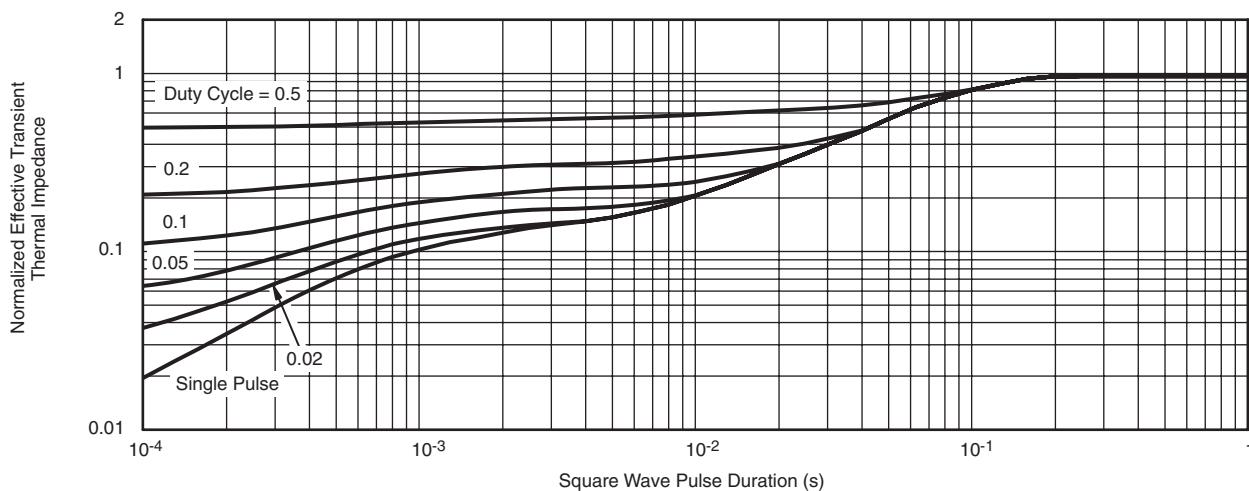


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

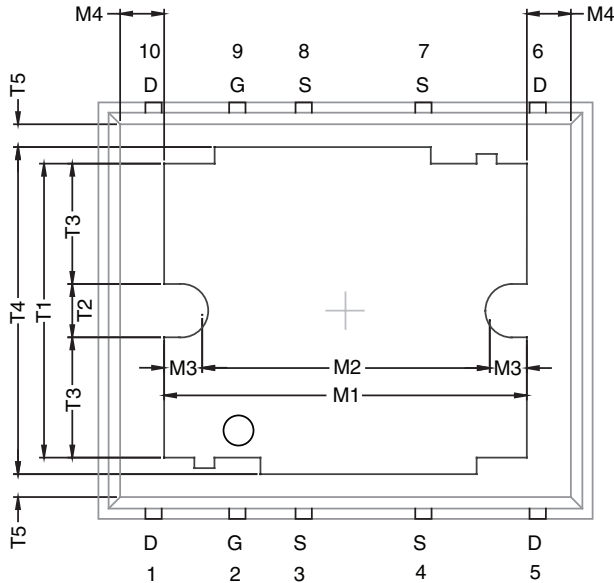


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

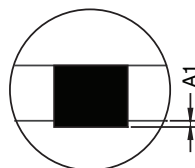
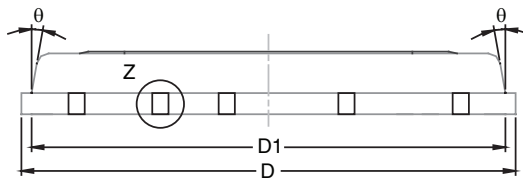
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)****Normalized Thermal Transient Impedance, Junction-to-Source**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69824.

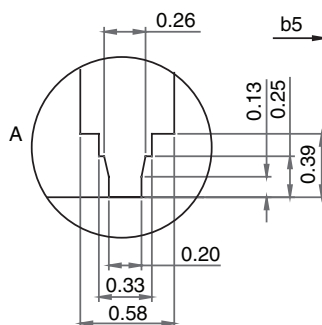
POLARPAK™ OPTION L



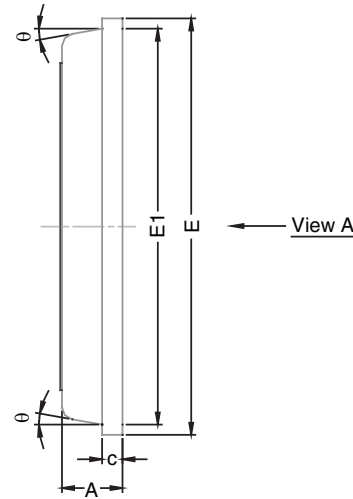
(Top View)



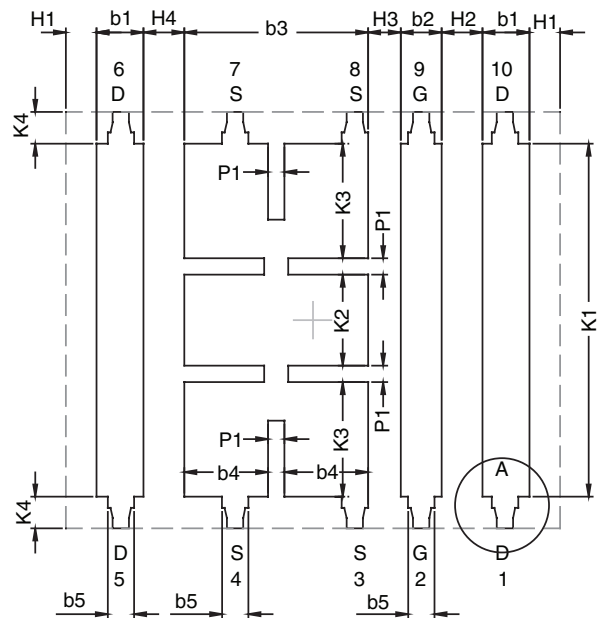
DETAIL Z



Product datasheet/information page contain links to applicable package drawing.



View A



View A
(Bottom View)

Package Information

Vishay Siliconix

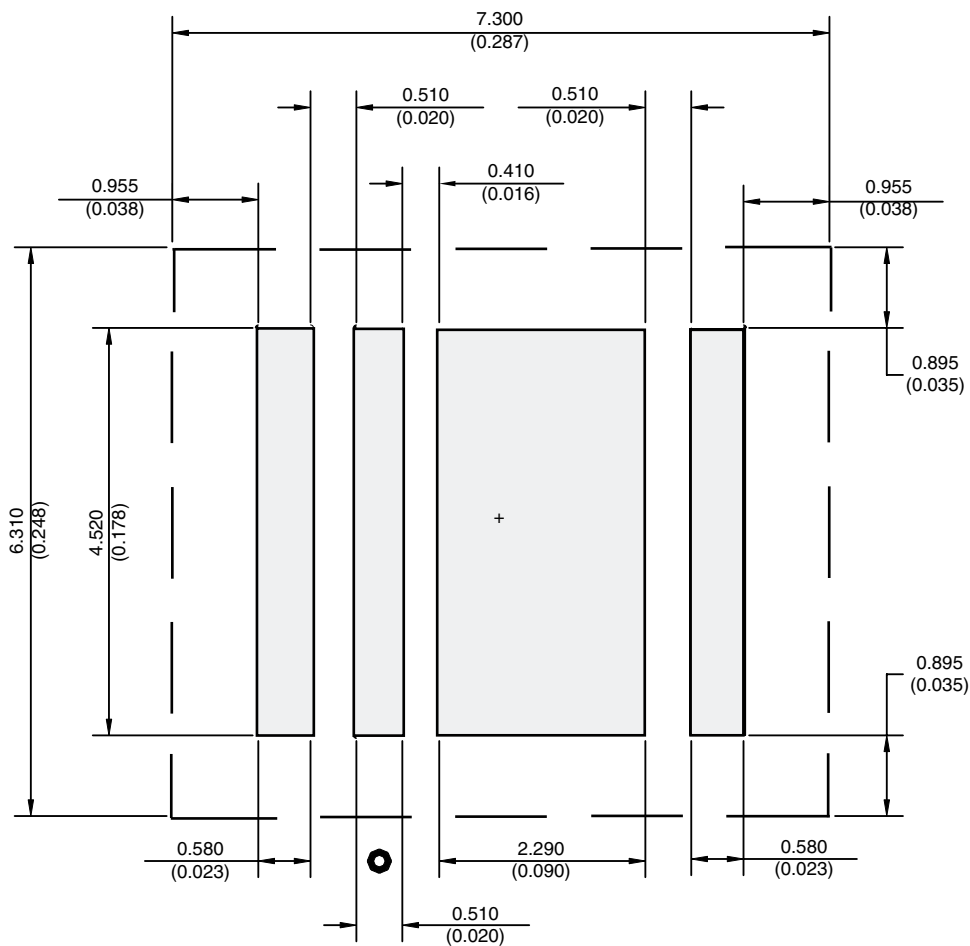


DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	-	0.05	0.000	-	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	-	-	0.009	-	-
H2	0.45	-	0.56	0.018	-	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	-	0.56	0.018	-	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37	-	-	0.054	-	-
K4	0.24	-	-	0.009	-	-
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	-	-	0.009	-	-
M4	0.05	-	-	0.002	-	-
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20	-	-	0.047	-	-
T4	3.90	-	-	0.153	-	-
T5	0	0.18	0.36	0.000	0.007	0.014
θ	0°	10°	12°	0°	10°	12°
ECN: T-08441-Rev. C, 11-Aug-08 DWG: 5946						

Notes

Millimeters govern over inches.

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S
 Dimensions in mm/(Inches)
 No External Traces within Broken Lines
 Dot indicates Gate Pin (Part Marking)



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