

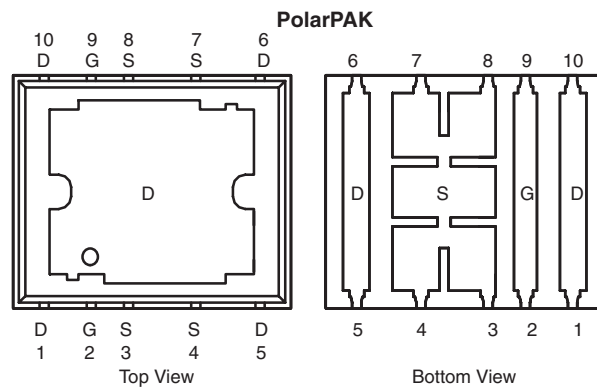


N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a		Q _g (Typ.)
		Silicon Limit	Package Limit	
25	0.0014 at V _{GS} = 10 V	229	60	46 nC
	0.0018 at V _{GS} = 4.5 V	202	60	

Package Drawing
www.vishay.com/doc?72945



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE882DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

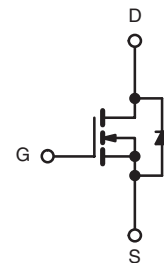
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Gen III Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size, ≤ 100 V
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- VRM
- DC/DC Conversion: Low-Side
- Server Vcore



N-Channel MOSFET
 For Related Documents
www.vishay.com/ppg?65002

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	25	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	229 (Silicon Limit)	A
		60 ^a (Package Limit)	
		60 ^a	
		47 ^{b, c}	
		41 ^{b, c}	
Pulsed Drain Current	I _{DM}	100	
Continuous Source-Drain Diode Current	I _S	60 ^a	
		4.3 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	50	
Avalanche Energy	E _{AS}	125	mJ
Maximum Power Dissipation	P _D	125	W
		80	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

- Package limited is 60 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SiE882DF

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THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	R_{thJC} (Drain)	0.8	1	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 68 °C/W.

c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

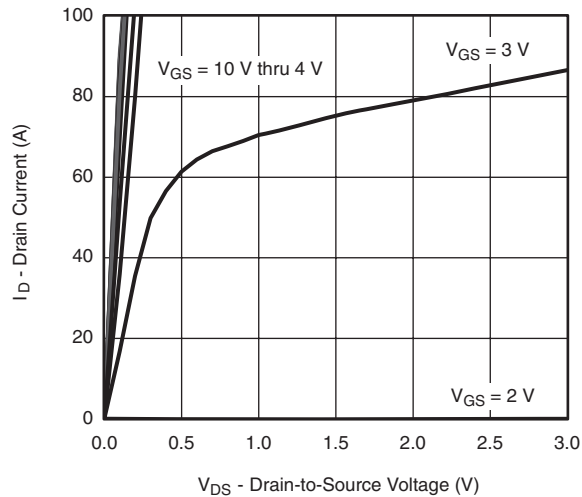
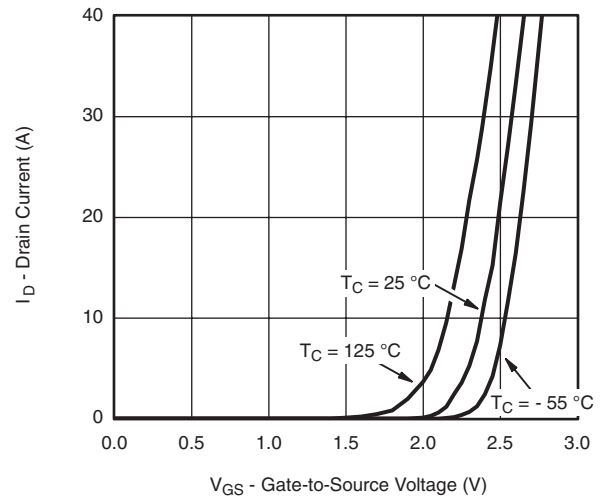
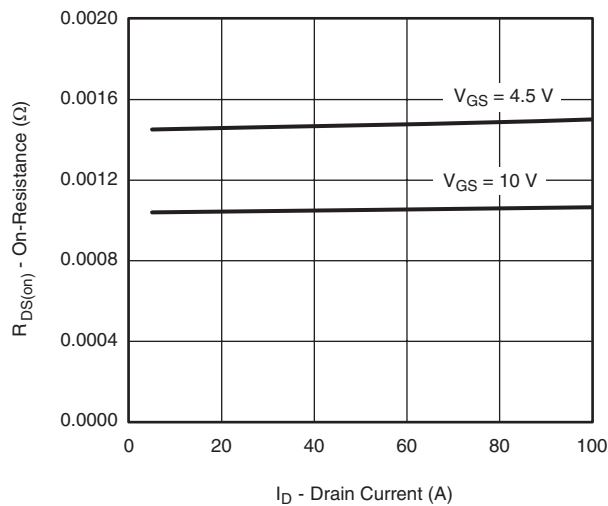
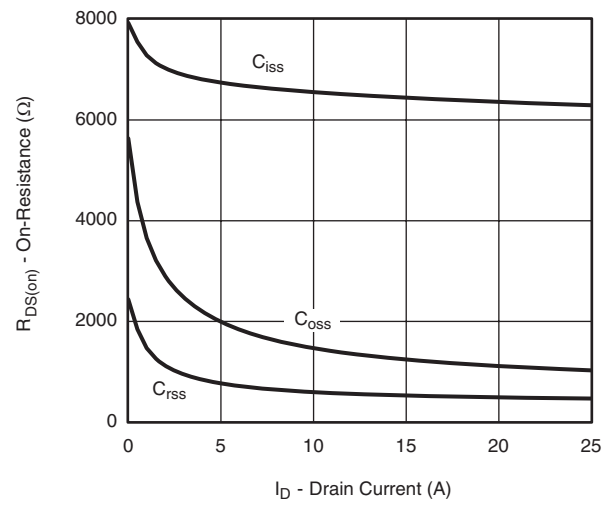
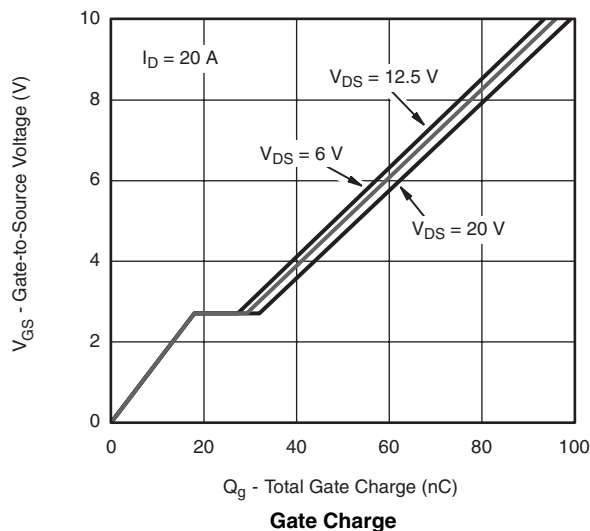
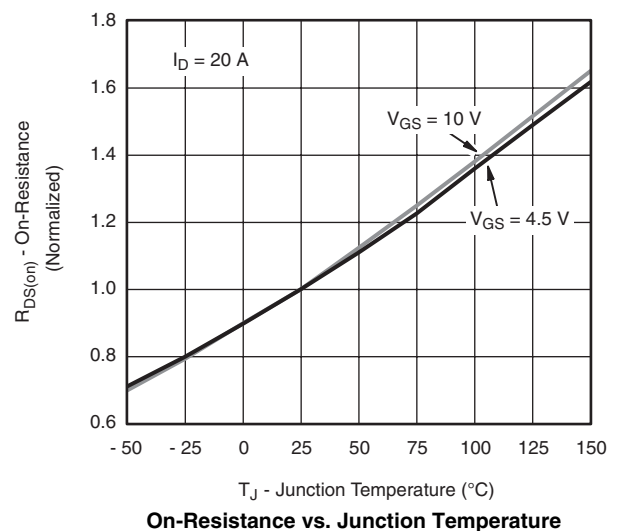
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	25			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		25		mV/°C	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.0			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.7	2.2	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	25			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$		0.0011	0.0014	Ω	
		$V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$		0.0015	0.0018		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 20\text{ A}$		125		S	
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{DS} = 12.5\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		6400		pF	
Output Capacitance	C_{oss}			1400			
Reverse Transfer Capacitance	C_{rss}			550			
Total Gate Charge	Q_g	$V_{DS} = 12.5\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$		96	145	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 12.5\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$		46	70		
Gate-Drain Charge	Q_{gd}			18			
Gate Resistance	R_g			12			
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$	0.2	1.1	2.2	Ω	
Rise Time	t_r		$V_{DD} = 12.5\text{ V}$, $R_L = 1.25\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		45	70	ns
Turn-Off Delay Time	$t_{d(off)}$				170	255	
Fall Time	t_f				65	100	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 12.5\text{ V}$, $R_L = 1.25\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$			85	130	
Rise Time	t_r			20	30		
Turn-Off Delay Time	$t_{d(off)}$			15	25		
Fall Time	t_f			45	70		
				10	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			60	A	
Pulse Diode Forward Current ^a	I_{SM}				100		
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		55	85	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			70	105	nC	
Reverse Recovery Fall Time	t_a			25		ns	
Reverse Recovery Rise Time	t_b			30			

Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

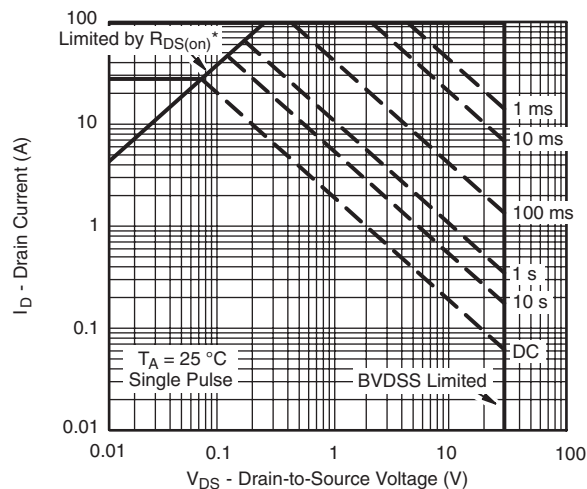
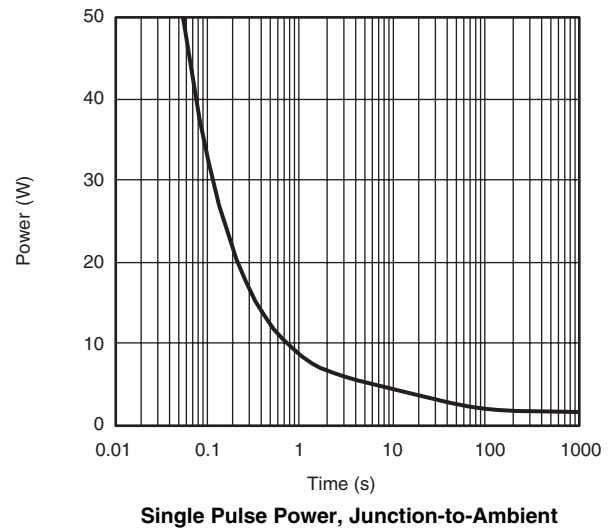
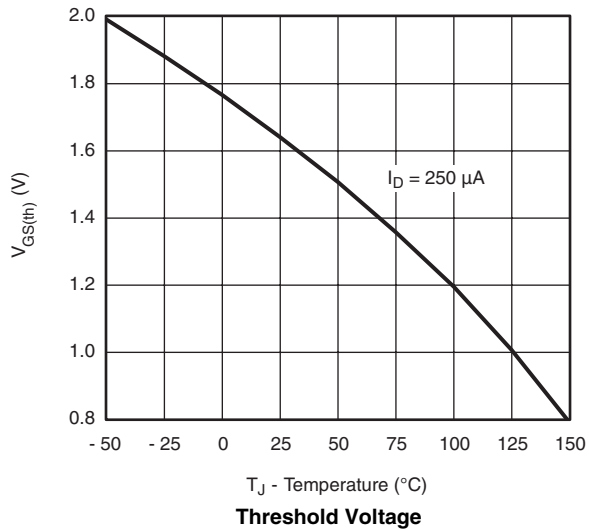
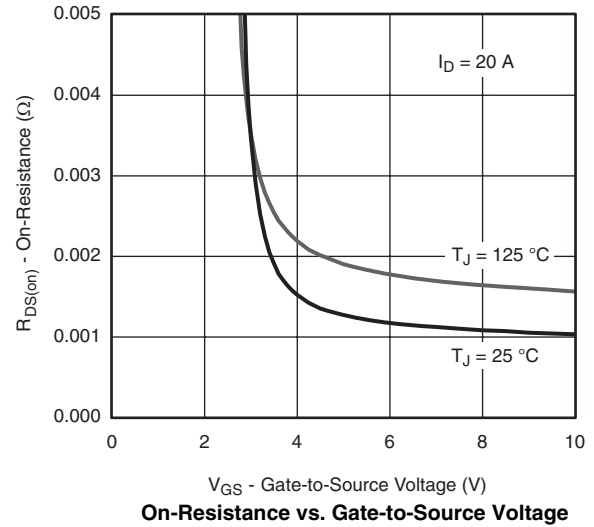
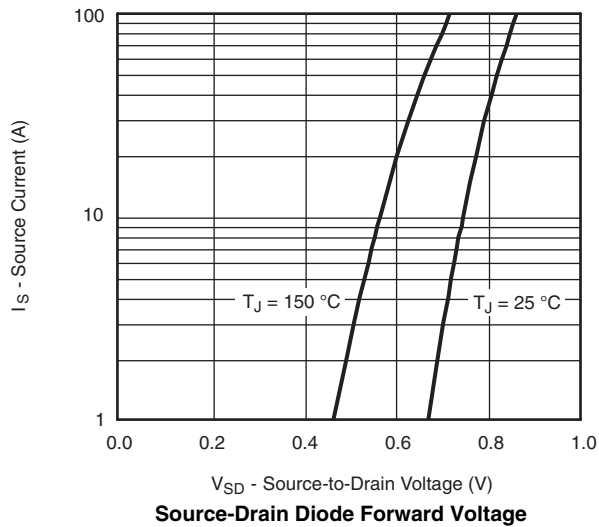
b. Guaranteed by design, not subject to production testing.

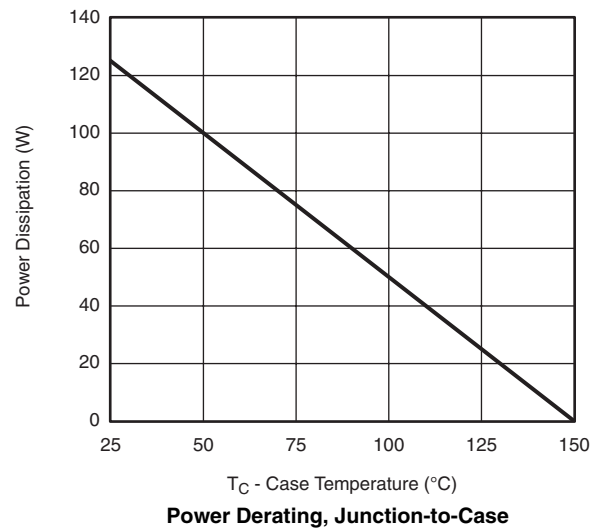
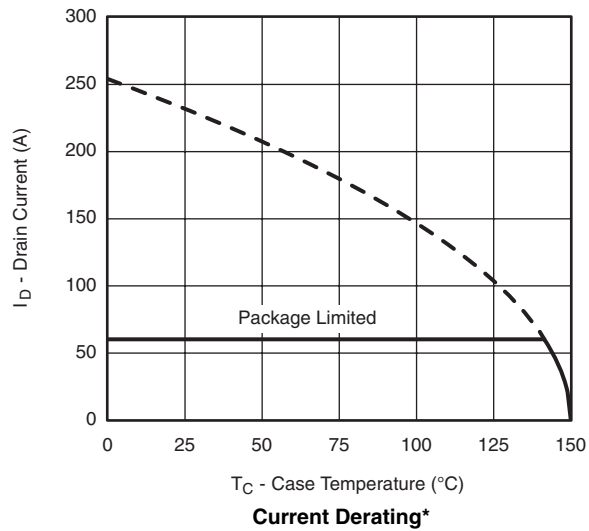
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

SiE882DF

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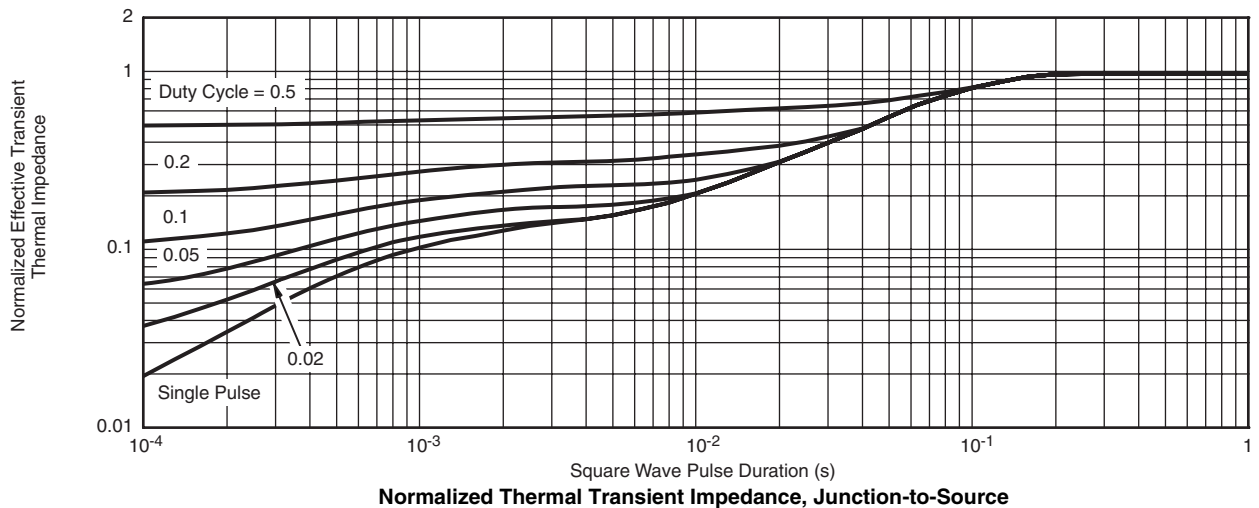
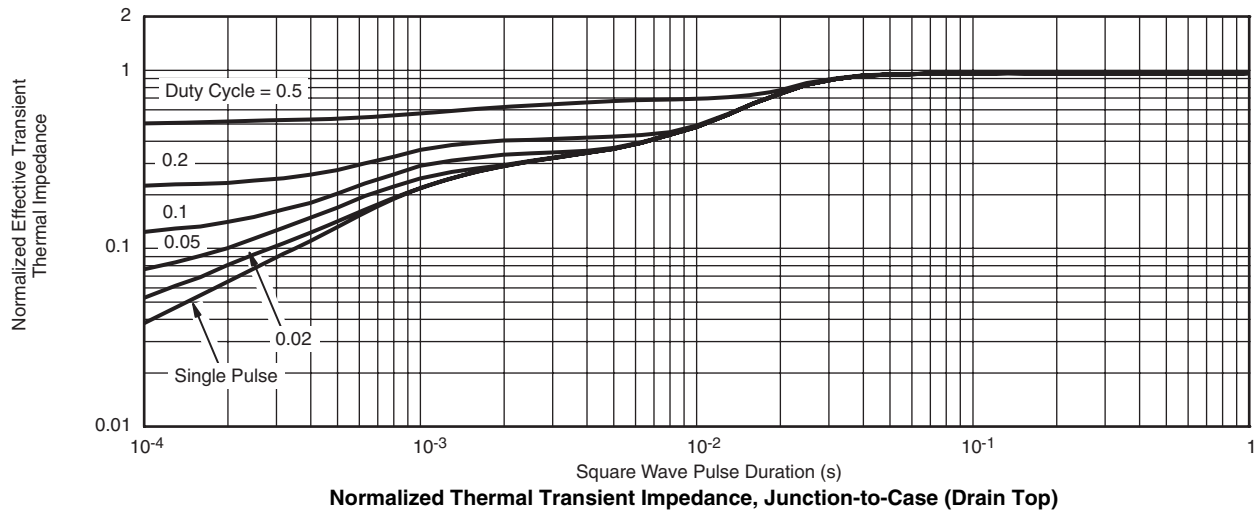
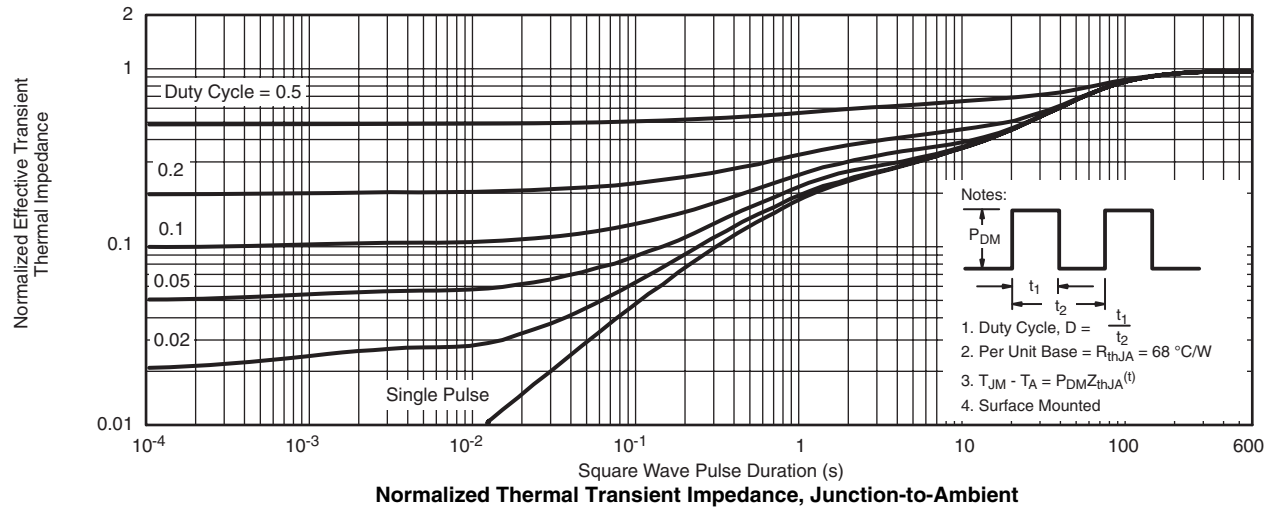
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

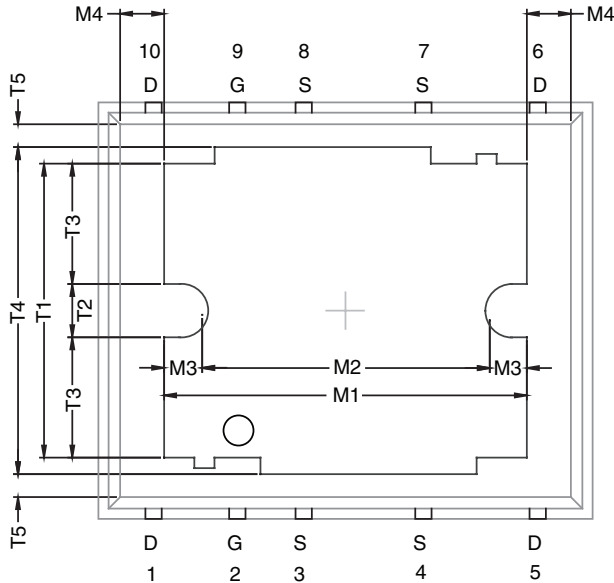
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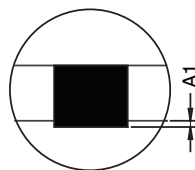
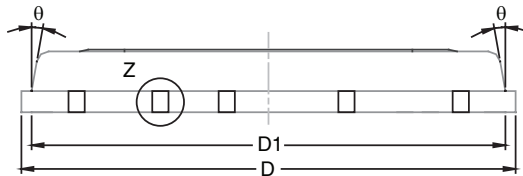
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?65002.

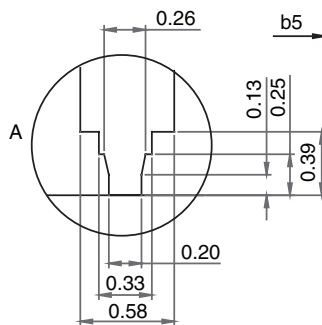
POLARPAK™ OPTION L



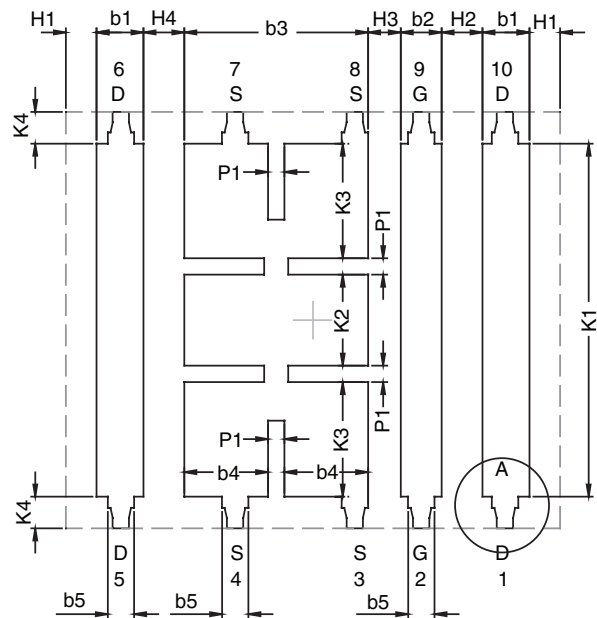
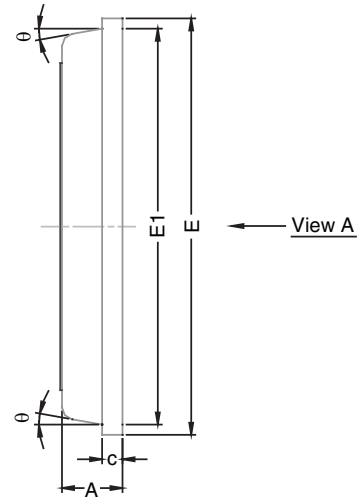
(Top View)



DETAIL Z



Product datasheet/information page contain links to applicable package drawing.



View A
(Bottom View)

Package Information

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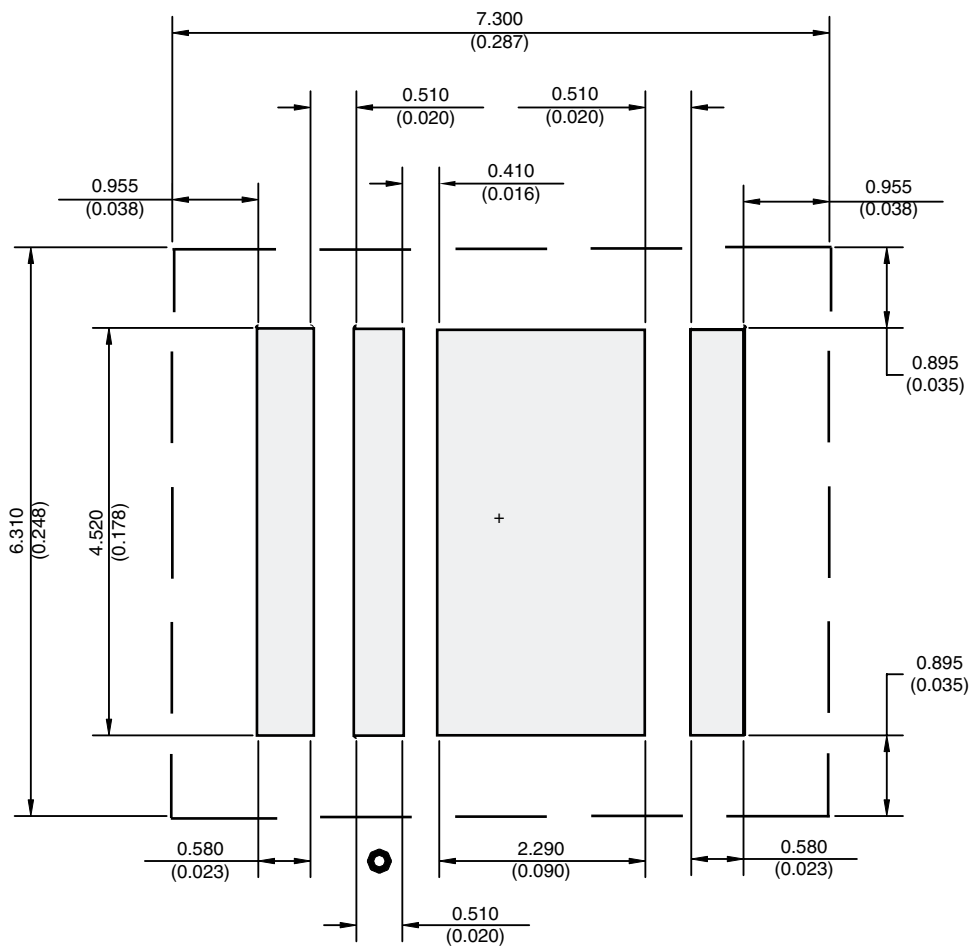


DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	-	0.05	0.000	-	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	-	-	0.009	-	-
H2	0.45	-	0.56	0.018	-	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	-	0.56	0.018	-	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37	-	-	0.054	-	-
K4	0.24	-	-	0.009	-	-
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	-	-	0.009	-	-
M4	0.05	-	-	0.002	-	-
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20	-	-	0.047	-	-
T4	3.90	-	-	0.153	-	-
T5	0	0.18	0.36	0.000	0.007	0.014
θ	0°	10°	12°	0°	10°	12°
ECN: T-08441-Rev. C, 11-Aug-08 DWG: 5946						

Notes

Millimeters govern over inches.

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S
 Dimensions in mm/(Inches)
 No External Traces within Broken Lines
 Dot indicates Gate Pin (Part Marking)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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