



Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
Channel-1	30	0.0240 at V _{GS} = 10 V	11	3.5 nC
		0.0320 at V _{GS} = 4.5 V	11	
Channel-2	30	0.0110 at V _{GS} = 10 V	28	6.8 nC
		0.0165 at V _{GS} = 4.5 V	28	

FEATURES

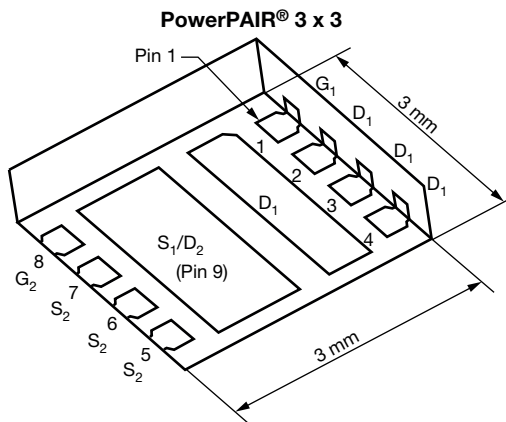
- PowerPAIR Optimizes High-Side and Low-Side MOSFETs for Synchronous Buck Converters
- TrenchFET® Power Mosfets
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



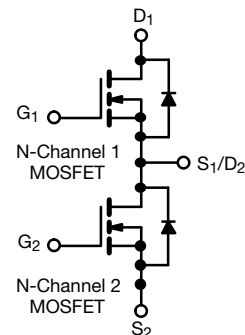
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Computing System Power
- POL
- Synchronous Buck Converter



Ordering Information:
SiZ300DT-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage		V _{DS}	30		V	
Gate-Source Voltage		V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	11 ^a	28 ^a	A	
	T _C = 70 °C		11 ^a	28 ^a		
	T _A = 25 °C		9.8 ^{b, c}	14.9 ^{b, c}		
	T _A = 70 °C		7.8 ^{b, c}	11.9 ^{b, c}		
Pulsed Drain Current (t = 300 μs)		I _{DM}	30	40		mJ
Continuous Source Drain Diode Current	T _A = 25 °C	I _S	11 ^a	26		
	T _A = 25 °C		3.2 ^{b, c}	3.8 ^{b, c}		
Avalanche Current	L = 0.1 mH	I _{AS}	12	15		
Single Pulse Avalanche Energy		E _{AS}	7	11		
Maximum Power Dissipation	T _C = 25 °C	P _D	16.7	31	W	
	T _C = 70 °C		10.7	20		
	T _A = 25 °C		3.7 ^{b, c}	4.2 ^{b, c}		
	T _A = 70 °C		2.4 ^{b, c}	2.7 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260			

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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THERMAL RESISTANCE RATINGS

Parameter		Symbol	Channel-1		Channel-2		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	27	34	24	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6	7.5	3.2	4	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 69 °C/W for channel-1 and 64 °C/W for channel-2.

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA	Ch-1	30		V		
		V _{GS} = 0 V, I _D = 250 μA	Ch-2	30				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	Ch-1		24	mV/°C		
		I _D = 250 μA	Ch-2		30			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	Ch-1		- 4.1			
		I _D = 250 μA	Ch-2		- 5			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1		2.4	V	
		V _{DS} = V _{GS} , I _D = 250 μA	Ch-2	1		2.2		
Gate Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	Ch-1			± 100	nA	
			Ch-2			± 100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	Ch-1			1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V	Ch-2			1		
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	Ch-1			5		
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	Ch-2			5		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1	10			A	
		V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-2	10				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 9.8 A	Ch-1		0.0200	0.0240	Ω	
		V _{GS} = 10 V, I _D = 15 A	Ch-2		0.0090	0.0110		
		V _{GS} = 4.5 V, I _D = 8.5 A	Ch-1		0.0265	0.0320		
		V _{GS} = 4.5 V, I _D = 12 A	Ch-2		0.0135	0.0165		
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 9.8 A	Ch-1		30		S	
		V _{DS} = 15 V, I _D = 15 A	Ch-2		30			
Dynamic ^a								
Input Capacitance	C _{iss}	Channel-1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		400		pF	
			Ch-2		730			
Output Capacitance	C _{oss}	Channel-2 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		125			
			Ch-2		155			
Reverse Transfer Capacitance	C _{rss}		Ch-1		25			
			Ch-2		65			
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 9.8 A	Ch-1		7.4	12	nC	
		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 15 A	Ch-2		14.2	22		
		Channel-1 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 9.8 A	Ch-1		3.5	5.3		
			Ch-2		6.8	11		
Gate-Source Charge	Q _{gs}	Channel-2 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15 A	Ch-1		1.5			
			Ch-2		2.2			
Gate-Drain Charge	Q _{gd}		Ch-1		1.1			
			Ch-2		2.3			
Gate Resistance	R _g	f = 1 MHz	Ch-1	0.5	2.6	5.2	Ω	
			Ch-2	0.5	2.6	5.2		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Dynamic ^a								
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.9 Ω I _D ≅ 8 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1		25	50	ns	
			Ch-2		25	50		
Rise Time	t _r		Ch-1		45	90		
			Ch-2		80	160		
Turn-Off Delay Time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1		10	20		
			Ch-2		20	40		
Fall Time	t _f		Ch-1		10	20		
			Ch-2		40	80		
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.9 Ω I _D ≅ 8 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1		5	10		
			Ch-2		5	10		
Rise Time	t _r		Ch-1		10	20		
			Ch-2		20	40		
Turn-Off Delay Time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1		10	20		
			Ch-2		15	30		
Fall Time	t _f		Ch-1		7	15		
			Ch-2		10	20		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1			11	A	
			Ch-2			26		
Pulse Diode Forward Current ^a	I _{SM}		Ch-1			30		
			Ch-2			40		
Body Diode Voltage	V _{SD}	I _S = 8 A, V _{GS} = 0 V	Ch-1		0.84	1.2	V	
		I _S = 10 A, V _{GS} = 0 V	Ch-2		0.82	1.2		
Body Diode Reverse Recovery Time	t _{rr}	Channel-1 I _F = 8 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		17	35	ns	
			Ch-2		20	40		
Body Diode Reverse Recovery Charge	Q _{rr}		Channel-2 I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		9	20	nC
				Ch-2		14	30	
Reverse Recovery Fall Time	t _a			Ch-1		9.5		ns
				Ch-2		12.5		
Reverse Recovery Rise Time	t _b			Ch-1		7.5		
				Ch-2		7.5		

Notes:

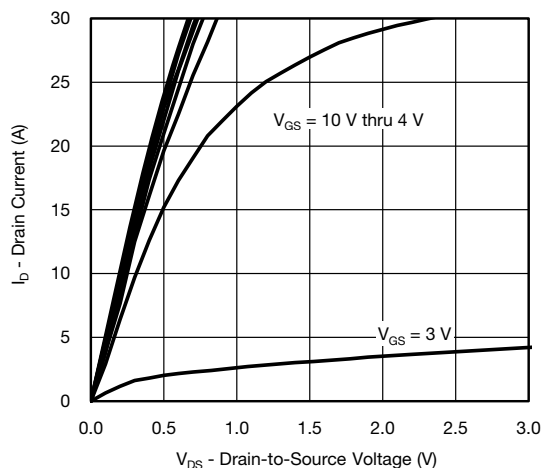
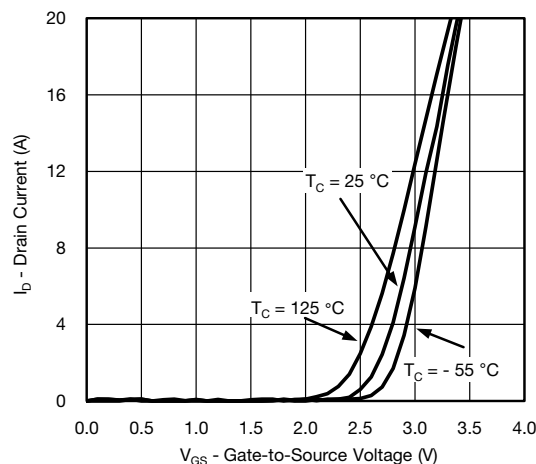
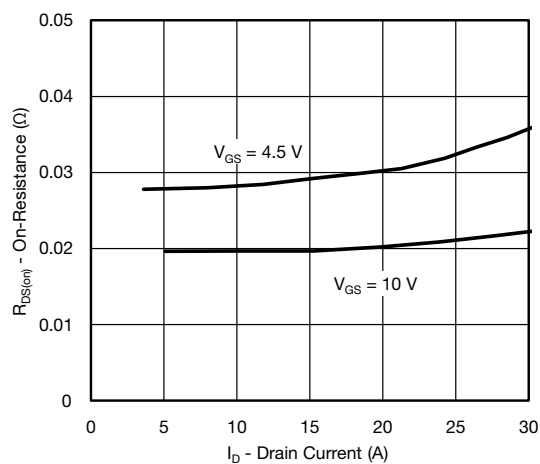
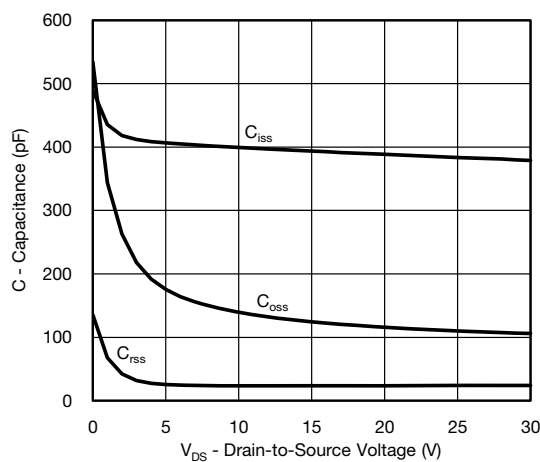
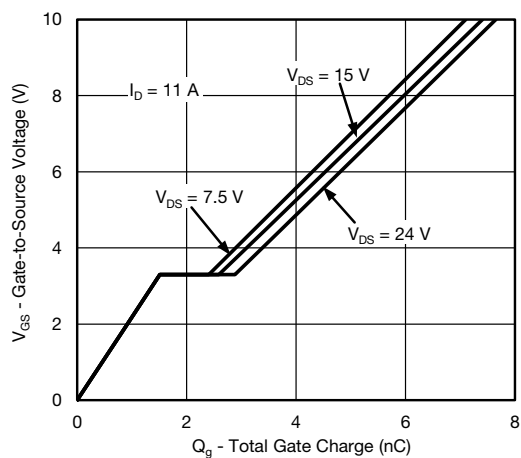
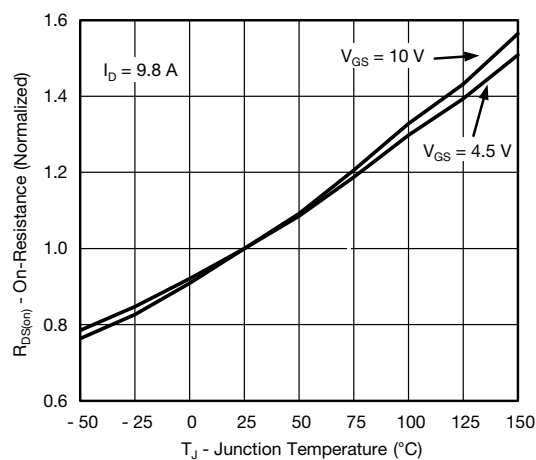
a. Guaranteed by design, not subject to production testing.

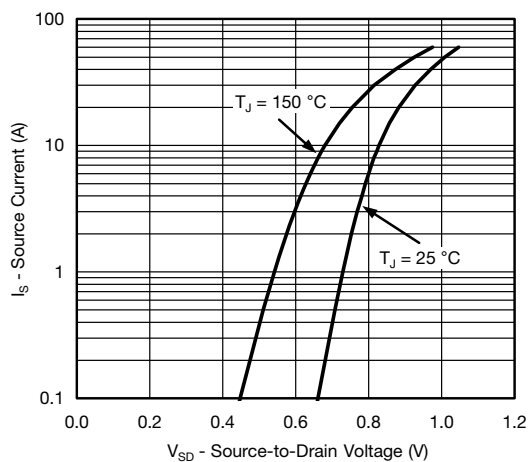
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

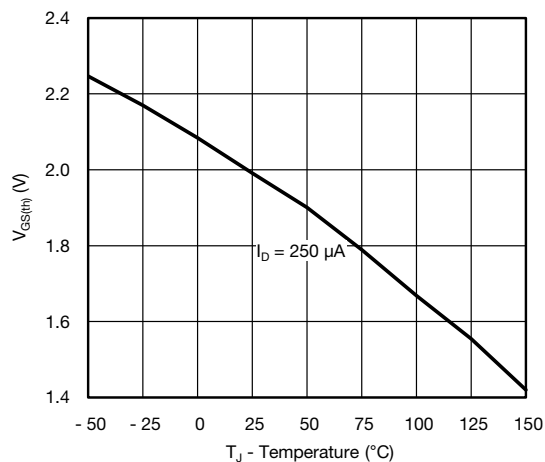
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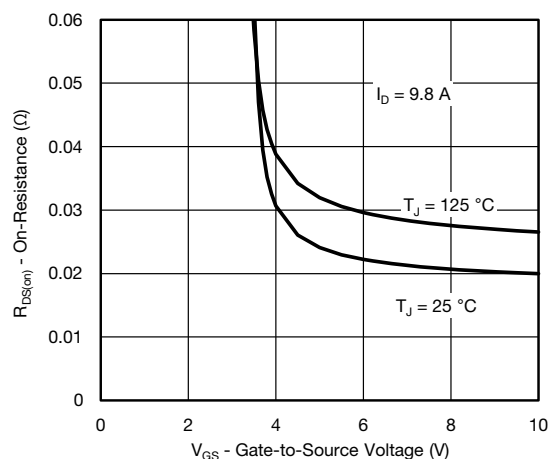
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**


CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


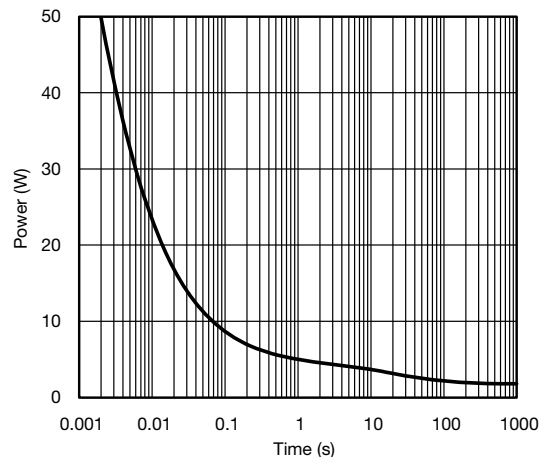
Source-Drain Diode Forward Voltage



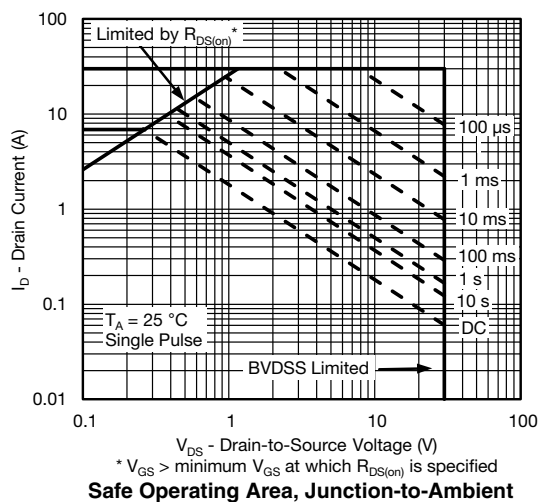
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



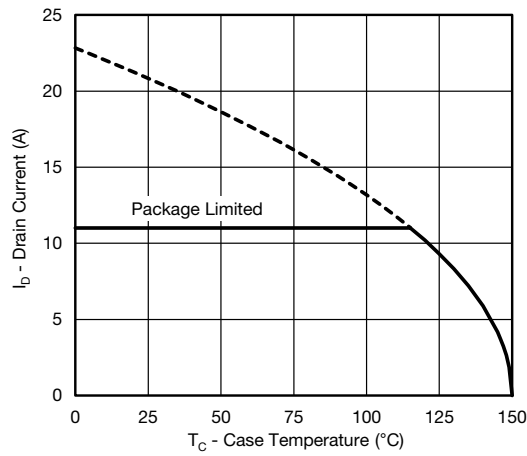
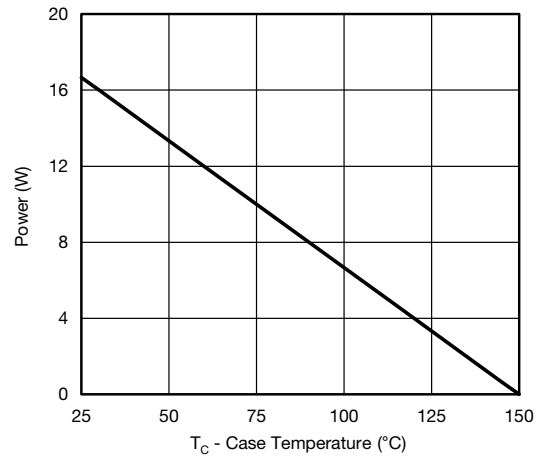
Single Pulse Power



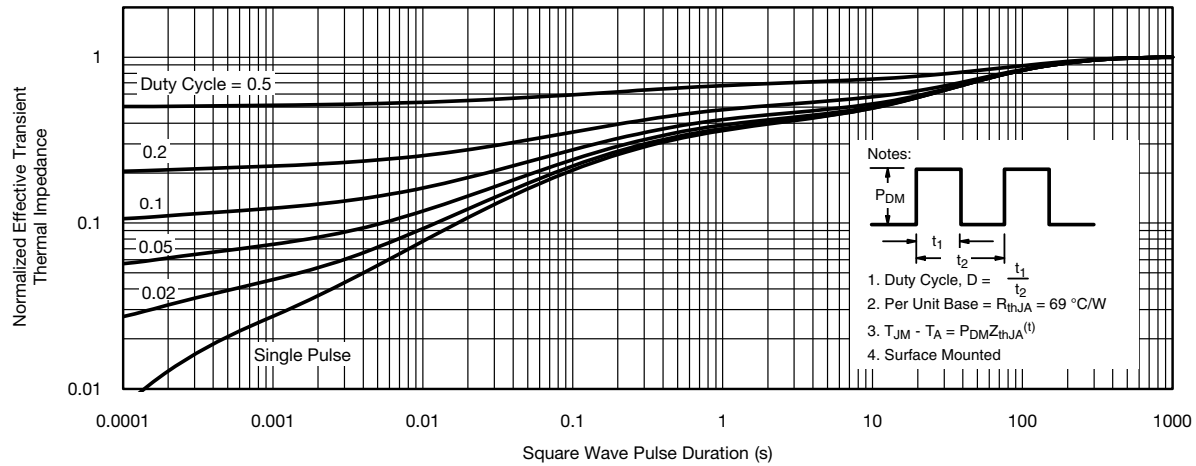
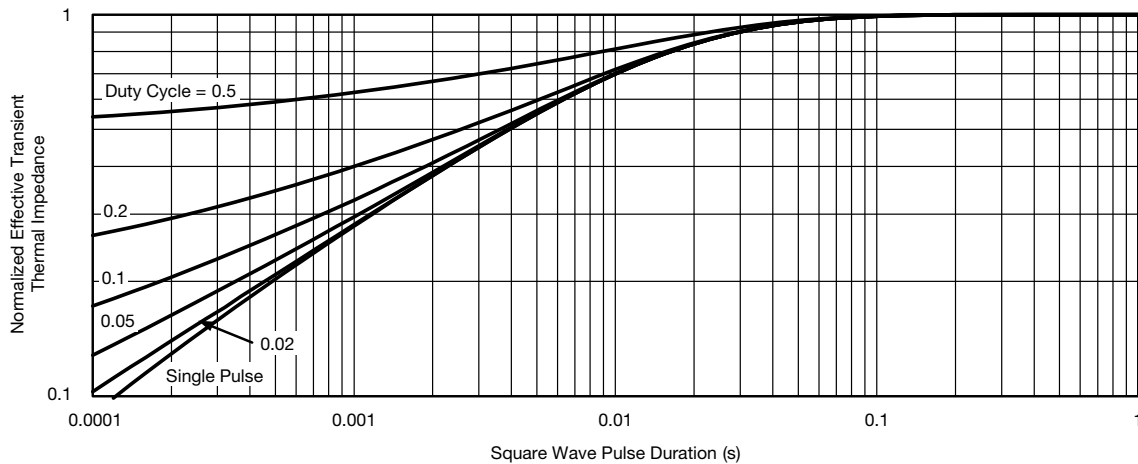
Safe Operating Area, Junction-to-Ambient

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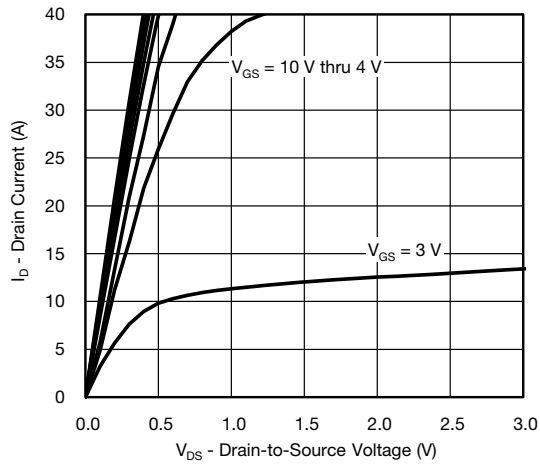
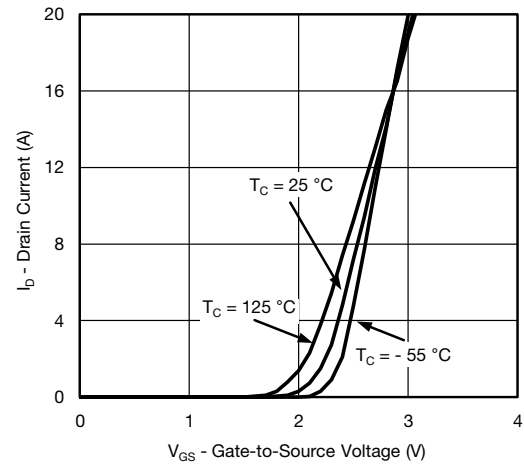
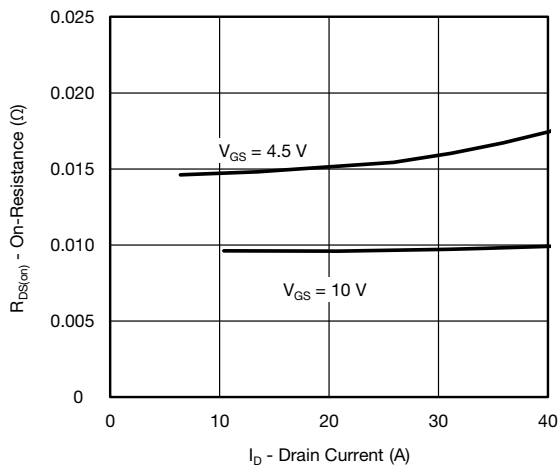
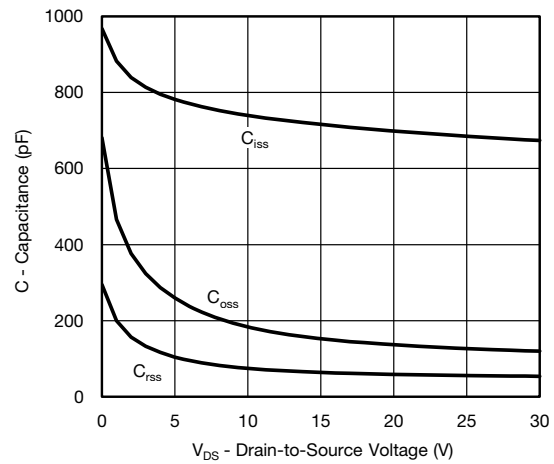
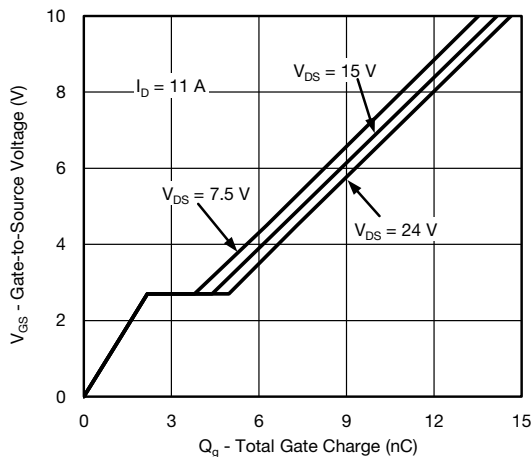
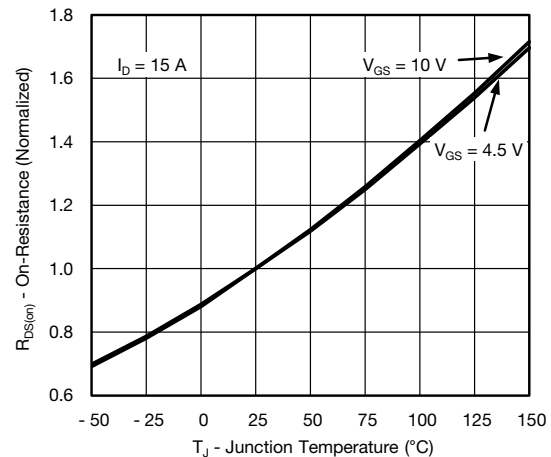
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Current Derating*****Power, Junction-to-Case**

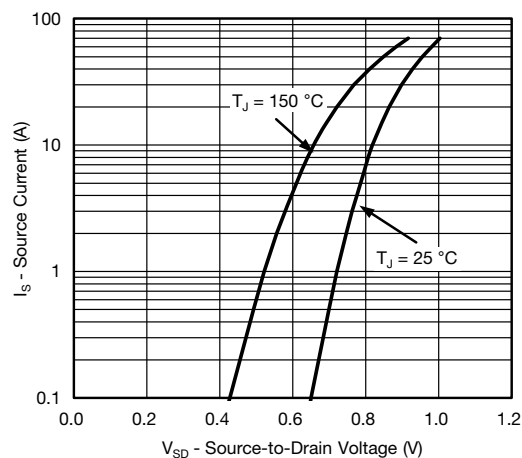
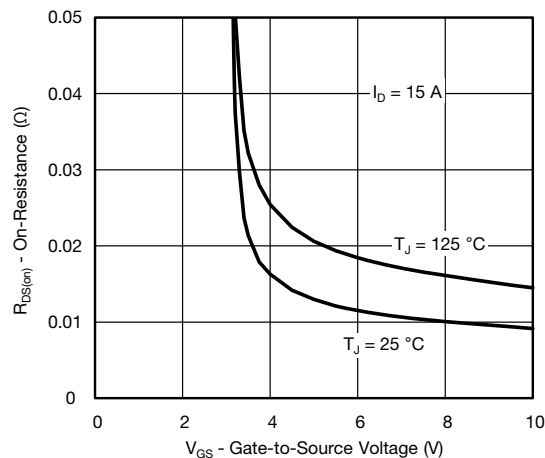
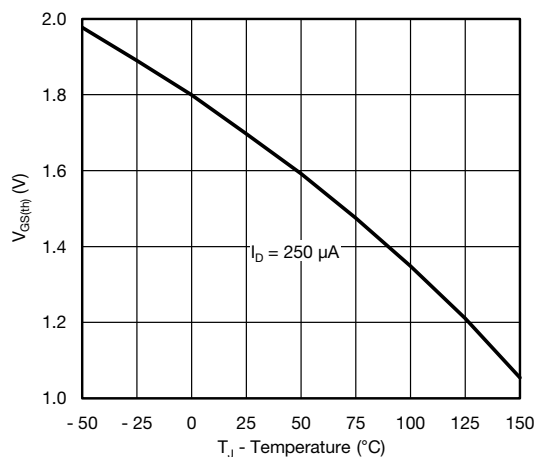
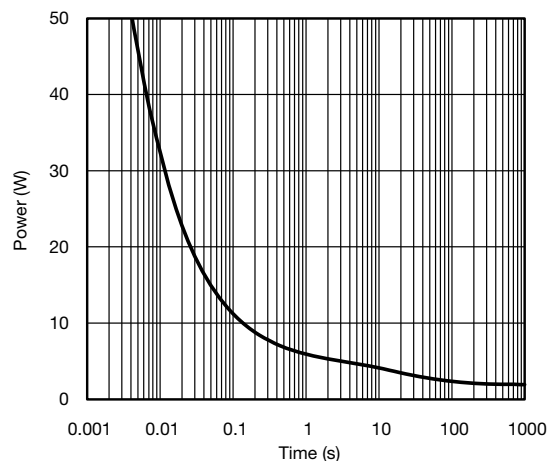
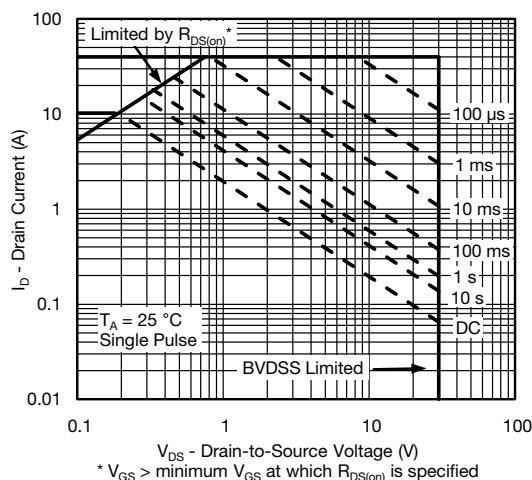
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

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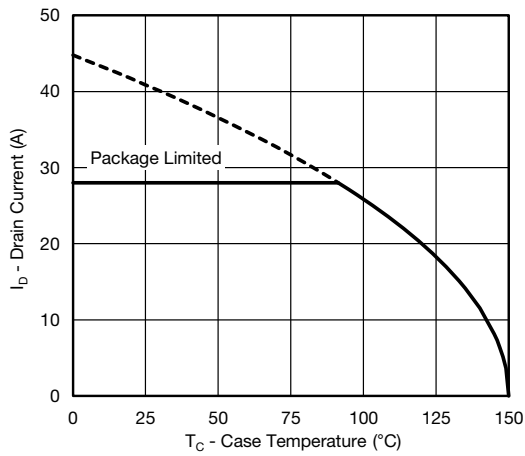
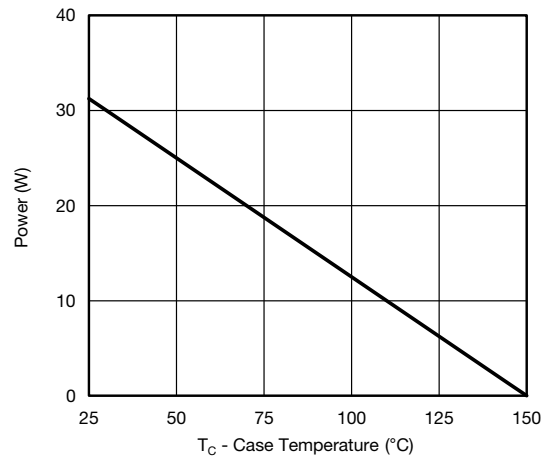
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**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

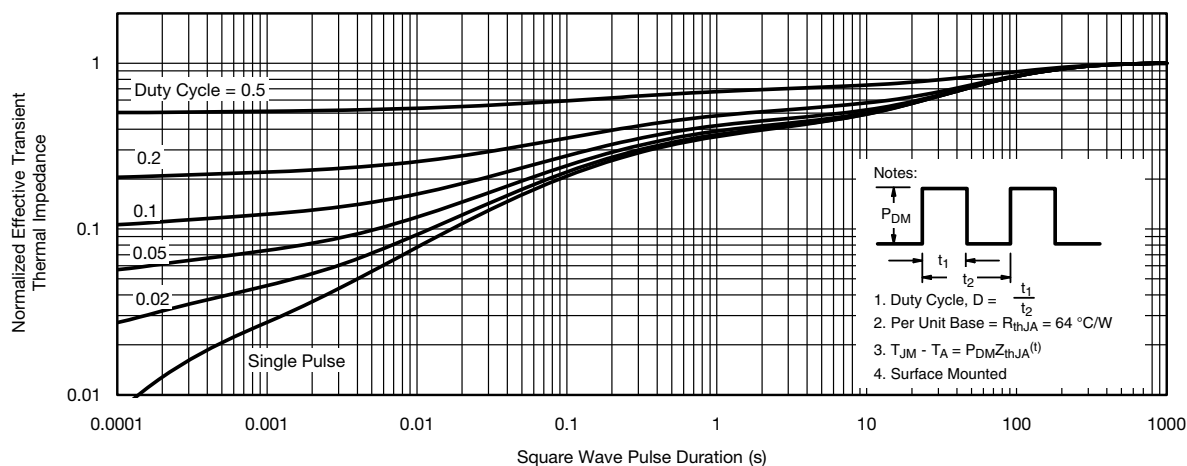
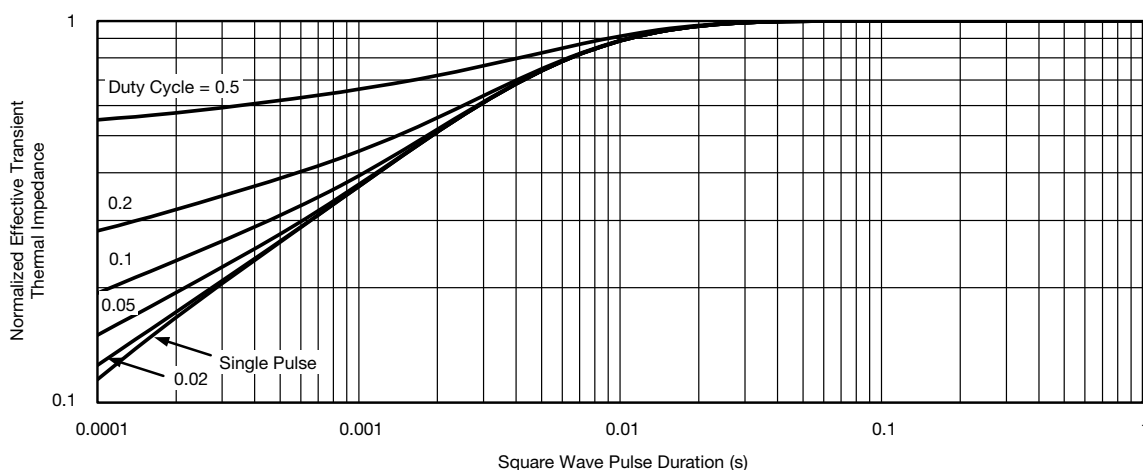

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

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**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Current Derating*****Power, Junction-to-Case**

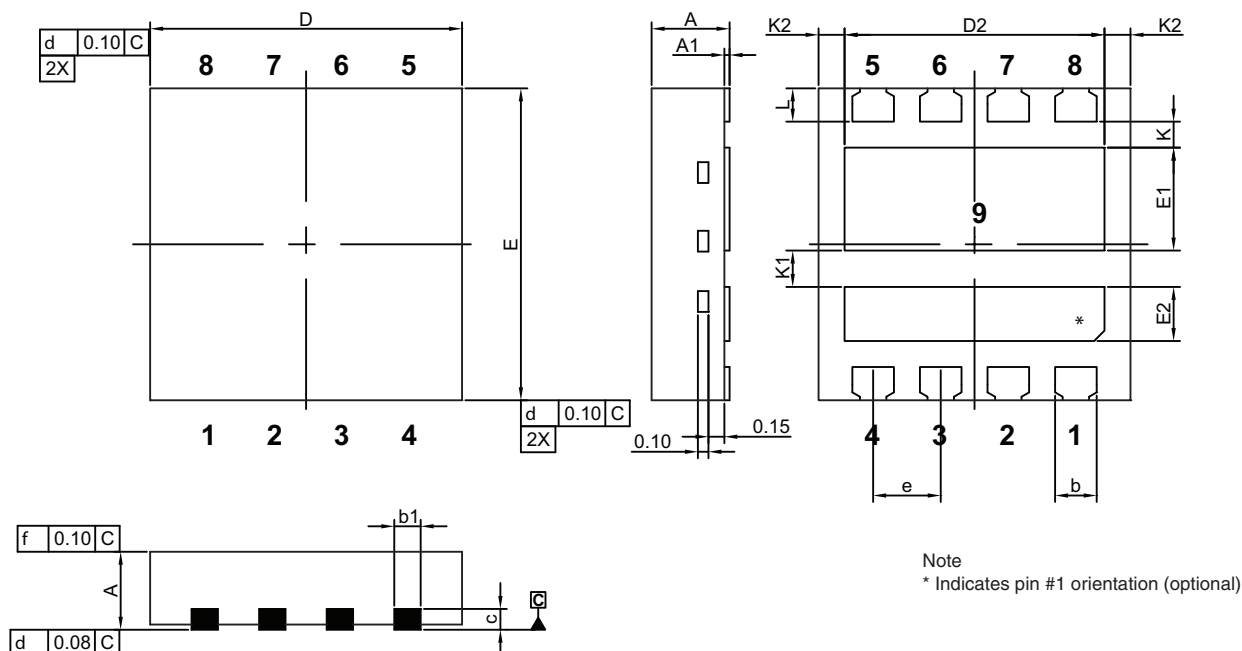
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CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?267715.

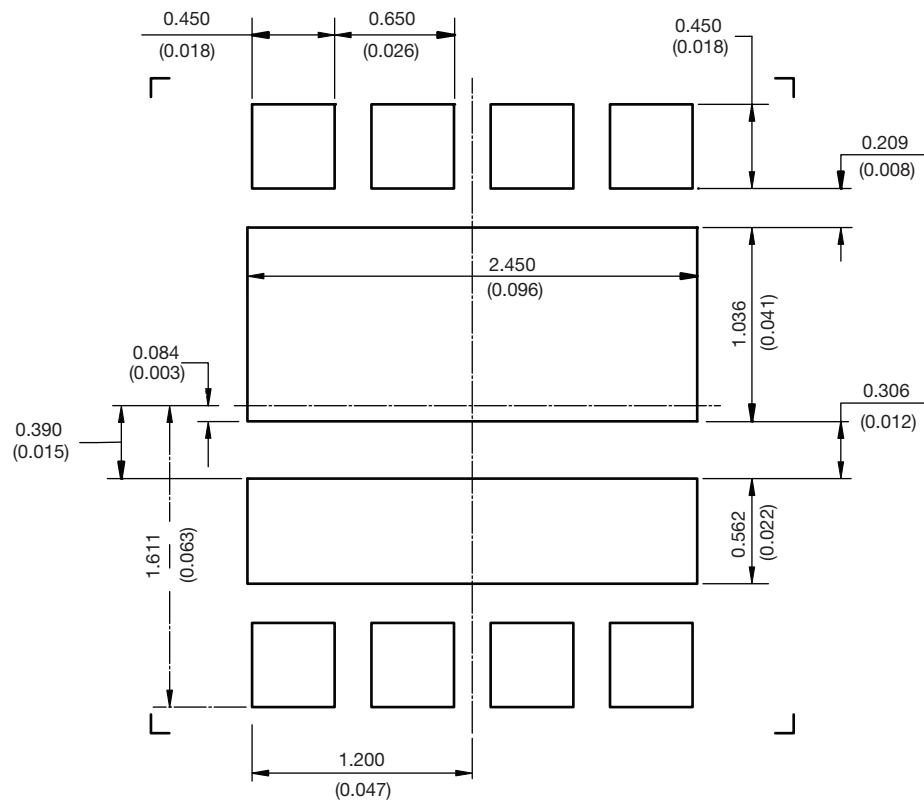


PowerPAIR® 3 x 3 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.