VISHAY

SiZ904DT

Vishay Siliconix

Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)	Q_g (Typ.)
Channel-1	30	0.024 at V_{GS} = 10 V	12[a]	3.8 nC
		0.030 at V_{GS} = 4.5 V	12[a]	
Channel-2	30	0.0135 at V_{GS} = 10 V	16[a]	7.3 nC
		0.017 at V_{GS} = 4.5 V	16[a]	

FEATURES

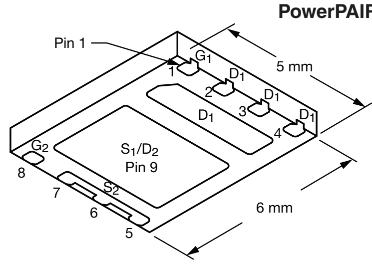
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

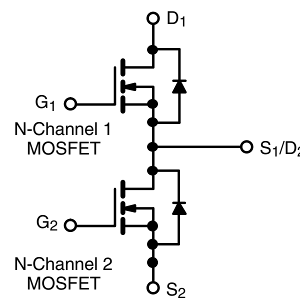
APPLICATIONS

- Notebook System Power
- POL
- Low Current DC/DC

PowerPAIR® 6 x 5



Ordering Information: SiZ904DT-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**Channel-1**	**Channel-2**	**Unit**
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	12[a]	16[a]	A
	T_C = 70 °C		12[a]	16[a]	
	T_A = 25 °C		9.5[b, c]	14.5[b, c]	
	T_A = 70 °C		7.6[b, c]	11.6[b, c]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	30	40	
Source Drain Current Diode Current	T_C = 25 °C	I_S	12[a]	16[a]	
	T_A = 25 °C		3.2[b, c]	4[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	10	15	
Single Pulse Avalanche Energy		E_{AS}	5	11	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	20	33	W
	T_C = 70 °C		12.9	21	
	T_A = 25 °C		3.8[b, c]	4.8[b, c]	
	T_A = 70 °C		2.4[b, c]	3.1[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d, e]			260		

THERMAL RESISTANCE RATINGS							
Parameter		**Symbol**	**Channel-1**		**Channel-2**		**Unit**
			Typ.	**Max.**	**Typ.**	**Max.**	
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	25	33	20	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.7	6.2	3	3.8	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (*www.vishay.com/doc?73257*). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 68 °C/W for Channel-1 and 61 °C/W for Channel-2.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	Ch-1	30			V
		V_{GS} = 0 V, I_D = 250 µA	Ch-2	30			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	Ch-1		35		mV/°C
		I_D = 250 µA	Ch-2		33		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	Ch-1		- 4.5		
		I_D = 250 µA	Ch-2		- 5		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1		2.5	V
		V_{DS} = V_{GS}, I_D = 250 µA	Ch-2	1.2		2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	Ch-1			± 100	nA
			Ch-2			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	Ch-1			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V	Ch-2			1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-1			5	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-2			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	Ch-1	20			A
		$V_{DS} \geq$ 5 V, V_{GS} = 10 V	Ch-2	20			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7.8 A	Ch-1		0.020	0.024	Ω
		V_{GS} = 10 V, I_D = 10 A	Ch-2		0.0105	0.0135	
		V_{GS} = 4.5 V, I_D = 7 A	Ch-1		0.024	0.030	
		V_{GS} = 4.5 V, I_D = 7 A	Ch-2		0.0135	0.017	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 7.8 A	Ch-1		17		S
		V_{DS} = 10 V, I_D = 10 A	Ch-2		24		
Dynamic[a]							
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1		435		pF
		Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-2		846		
Output Capacitance	C_{oss}		Ch-1		95		
			Ch-2		187		
Reverse Transfer Capacitance	C_{rss}		Ch-1		42		
			Ch-2		72		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 7.8 A	Ch-1		8	12	nC
		V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	Ch-2		15.4	23	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 7.8 A	Ch-1		3.8	6	
		Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	Ch-2		7.3	11	
Gate-Source Charge	Q_{gs}		Ch-1		1.4		
			Ch-2		2.3		
Gate-Drain Charge	Q_{gd}		Ch-1		1.1		
			Ch-2		2.2		
Gate Resistance	R_g	f = 1 MHz	Ch-1	0.6	3.2	6.4	Ω
			Ch-2	0.2	0.8	1.6	

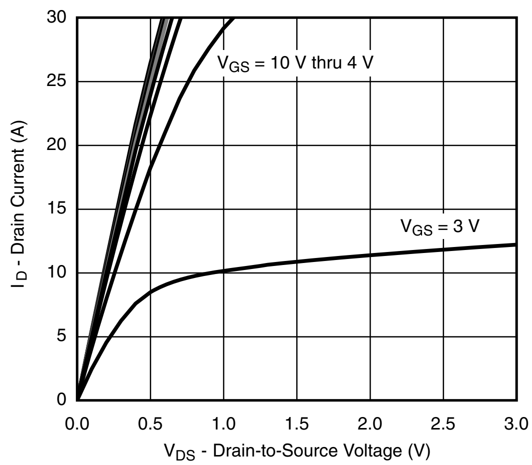
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 2.4 Ω $I_D \cong$ 6.3 A, V_{GEN} = 4.5 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1		15	30	ns
			Ch-2		15	30	
Rise Time	t_r		Ch-1		12	24	
			Ch-2		12	24	
Turn-Off Delay Time	$t_{d(off)}$		Ch-1		13	26	
			Ch-2		13	26	
Fall Time	t_f		Ch-1		10	20	
			Ch-2		10	20	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 2.4 Ω $I_D \cong$ 6.3 A, V_{GEN} = 10 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1		5	10	
			Ch-2		9	18	
Rise Time	t_r		Ch-1		10	20	
			Ch-2		9	18	
Turn-Off Delay Time	$t_{d(off)}$		Ch-1		15	30	
			Ch-2		14	28	
Fall Time	t_f		Ch-1		10	20	
			Ch-2		8	16	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	Ch-1			12	A
			Ch-2			16	
Pulse Diode Forward Current[a]	I_{SM}		Ch-1			30	
			Ch-2			40	
Body Diode Voltage	V_{SD}	I_S = 6.3 A, V_{GS} = 0 V	Ch-1		0.8	1.2	V
		I_S = 3 A, V_{GS} = 0 V	Ch-2		0.78	1.2	
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 I_F = 6.3 A, dI/dt = 100 A/µs, T_J = 25 °C Channel-2 I_F = 10 A, dI/dt = 100 A/µs, T_J = 25 °C	Ch-1		15	30	ns
			Ch-2		17	34	
Body Diode Reverse Recovery Charge	Q_{rr}		Ch-1		7	15	nC
			Ch-2		9.5	19	
Reverse Recovery Fall Time	t_a		Ch-1		9		ns
			Ch-2		10		
Reverse Recovery Rise Time	t_b		Ch-1		6		
			Ch-2		7		

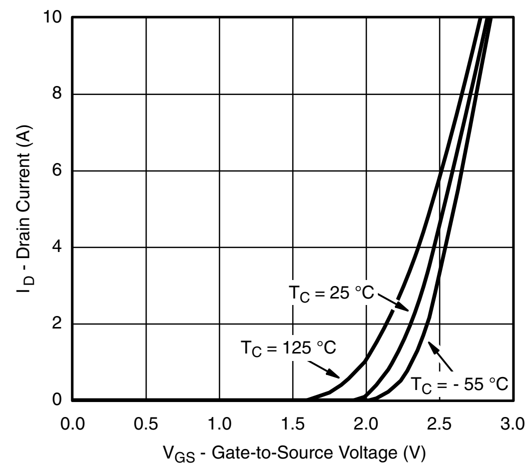
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

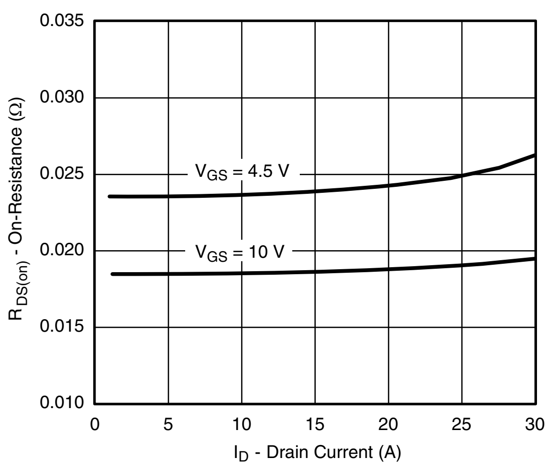
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



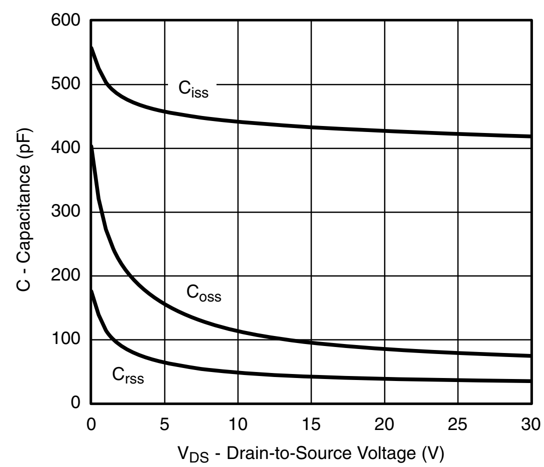
Output Characteristics



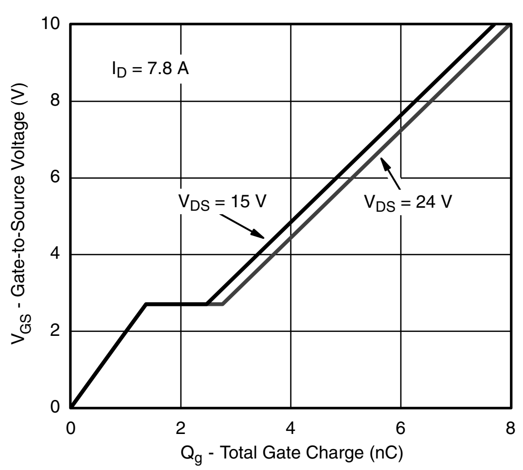
Transfer Characteristics



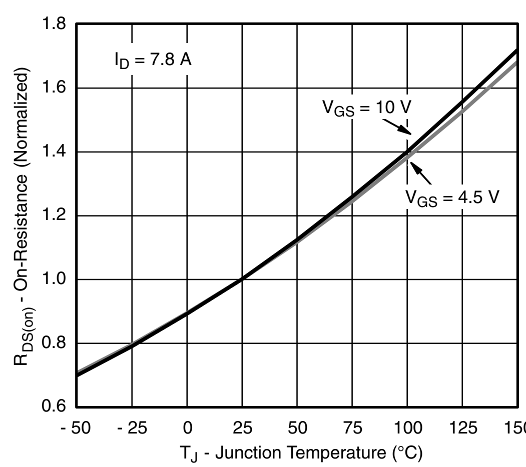
On-Resistance vs. Drain Current



Capacitance

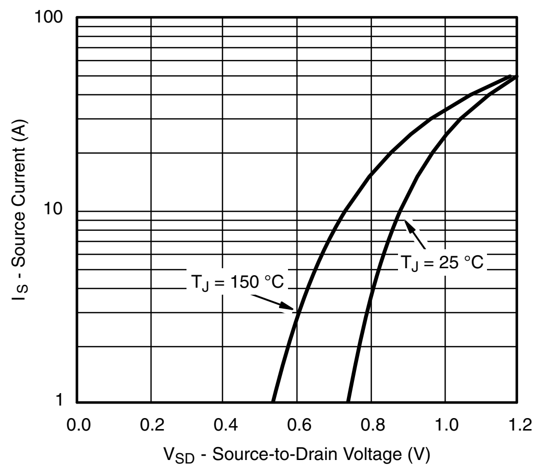


Gate Charge

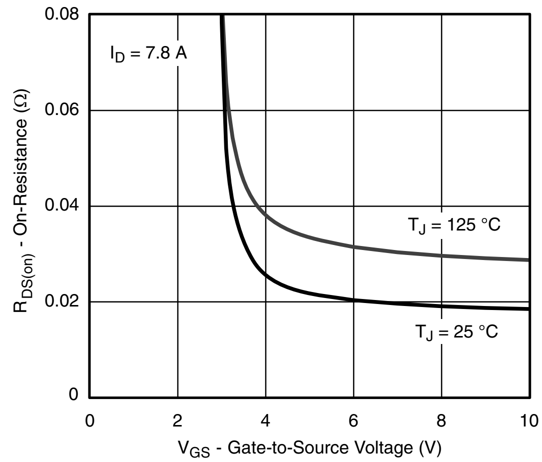


On-Resistance vs. Junction Temperature

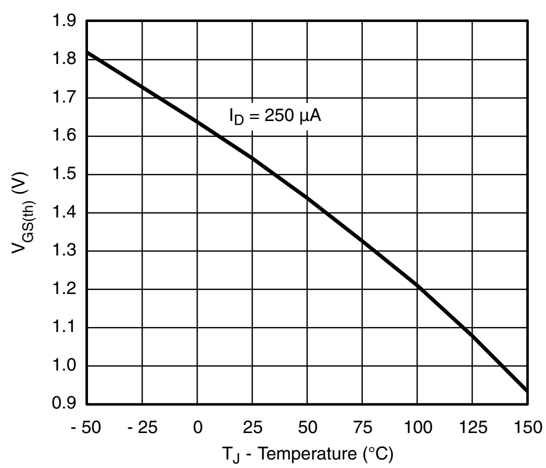
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



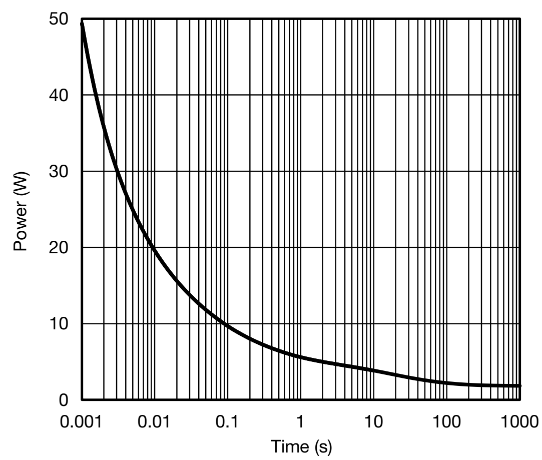
Source-Drain Diode Forward Voltage



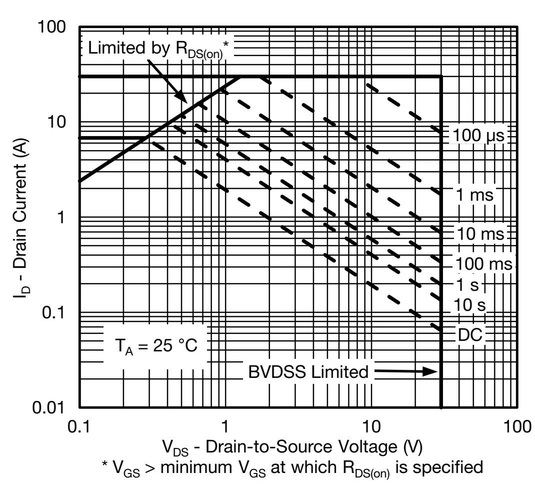
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

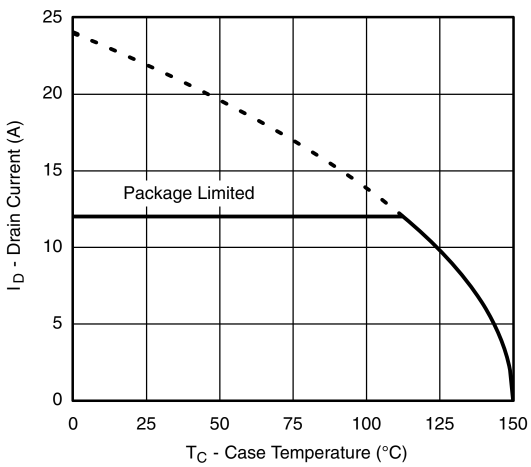


Single Pulse Power

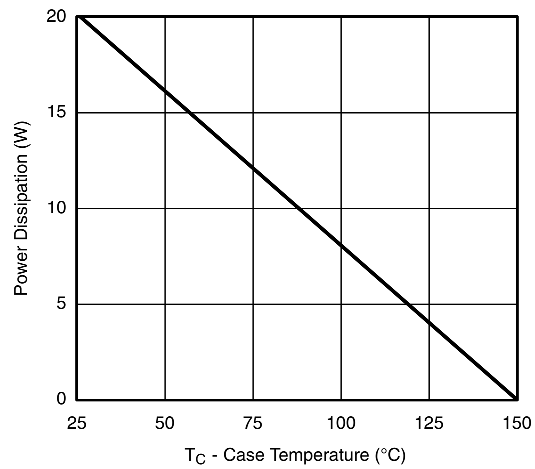


Safe Operating Area, Junction-to-Ambient

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



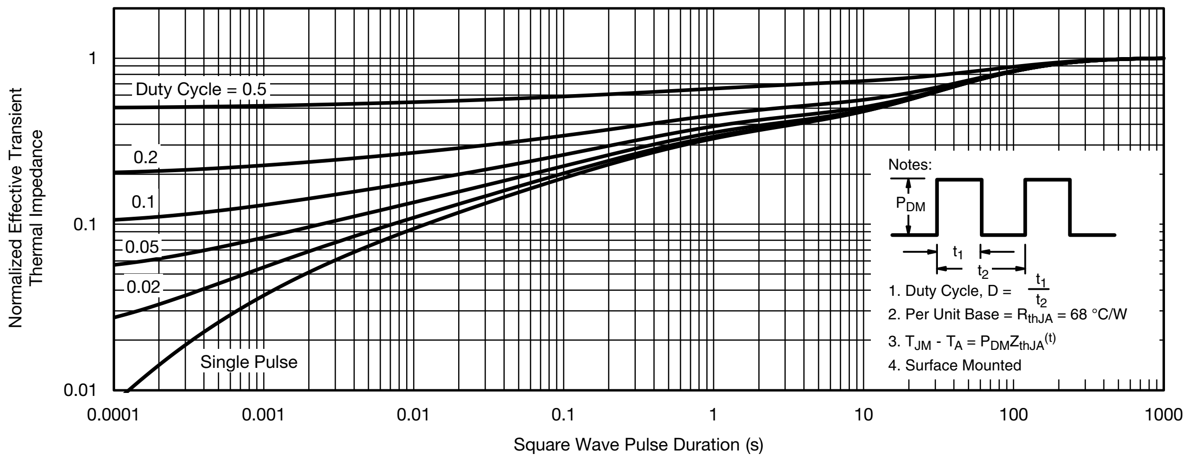
Current Derating*



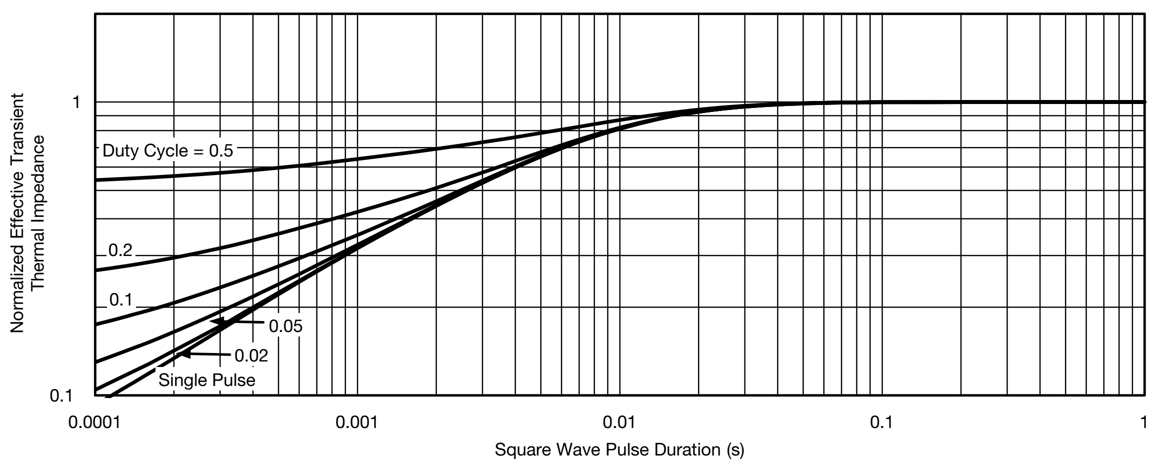
Power, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

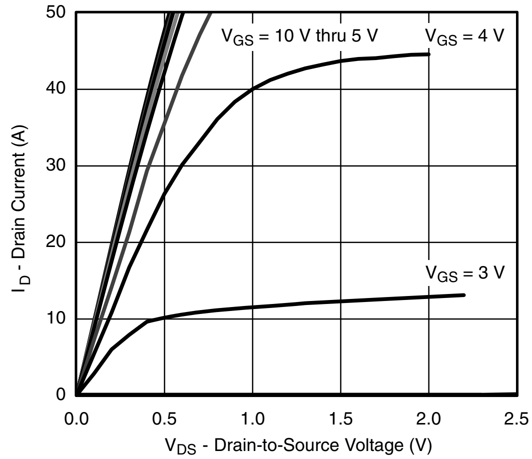


Normalized Thermal Transient Impedance, Junction-to-Ambient

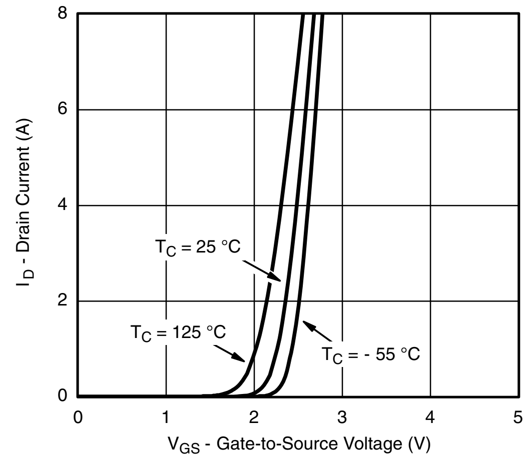


Normalized Thermal Transient Impedance, Junction-to-Case

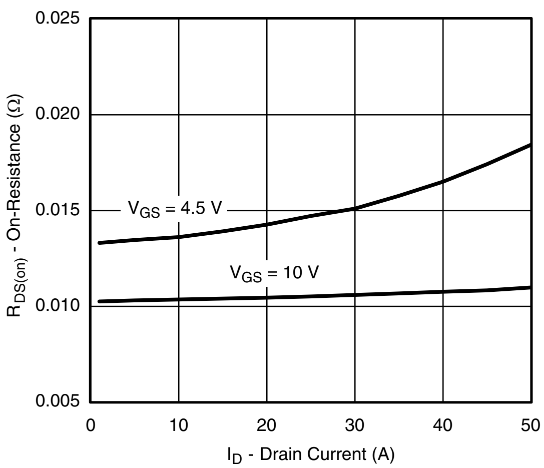
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



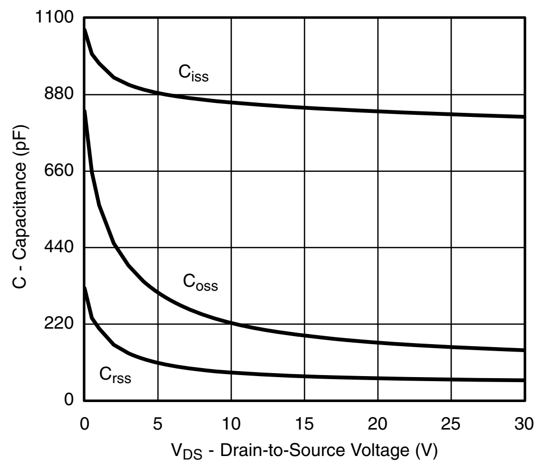
Output Characteristics



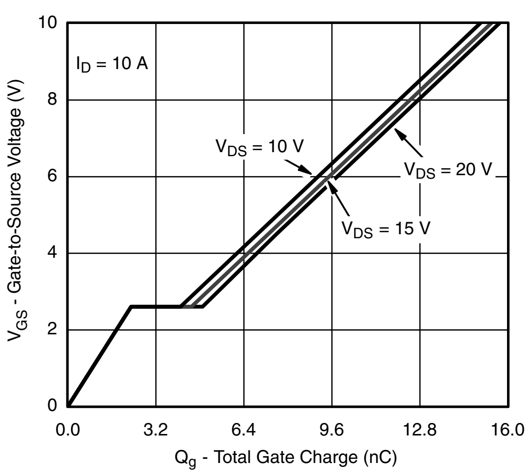
Transfer Characteristics



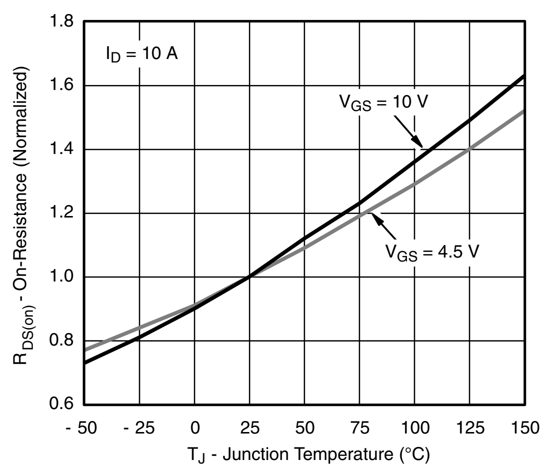
On-Resistance vs. Drain Current



Capacitance

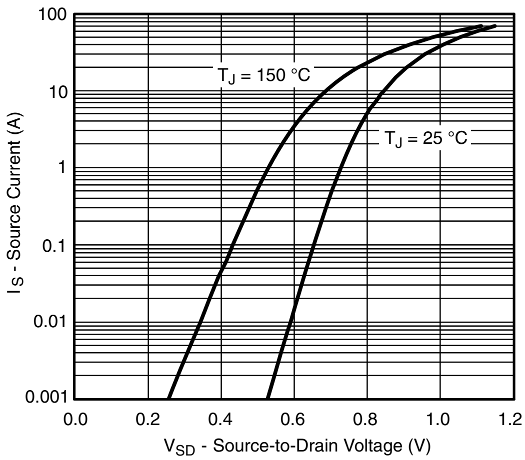


Gate Charge

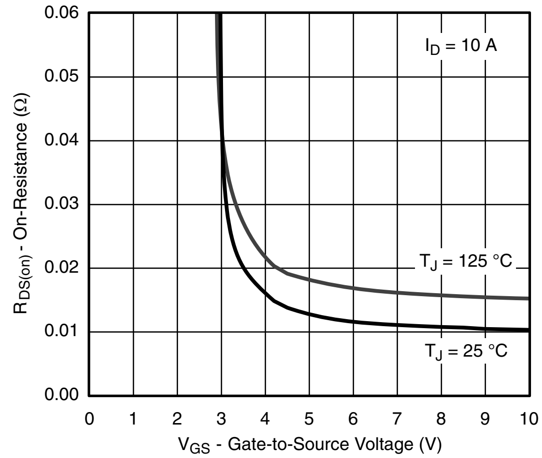


On-Resistance vs. Junction Temperature

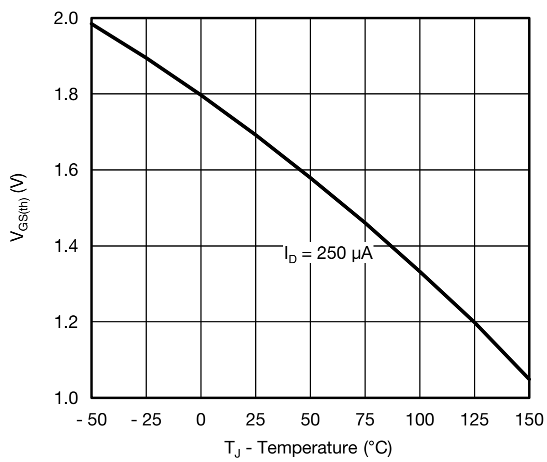
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



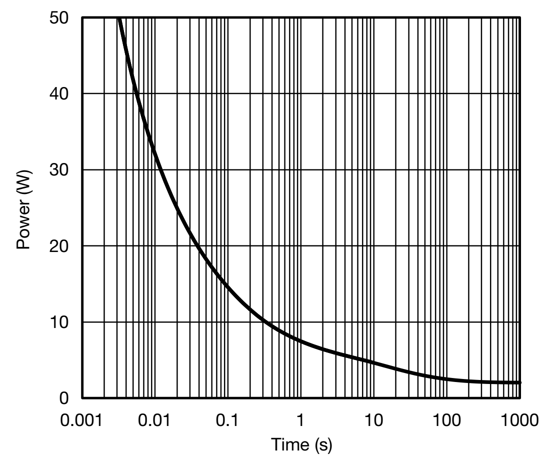
Source-Drain Diode Forward Voltage



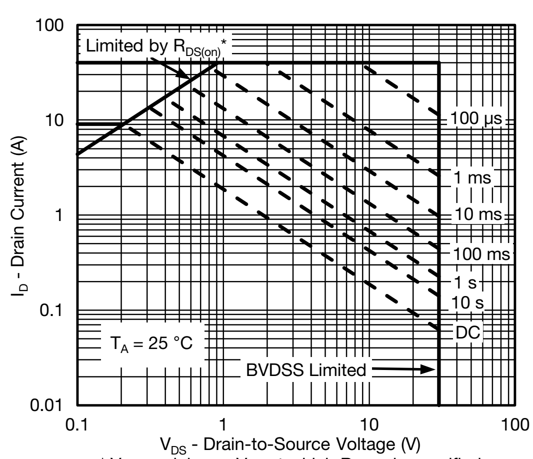
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



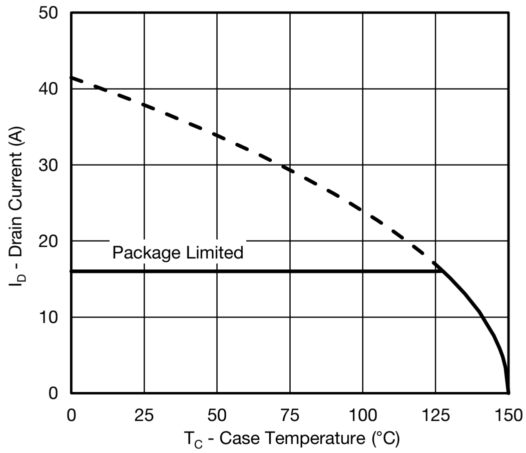
Single Pulse Power



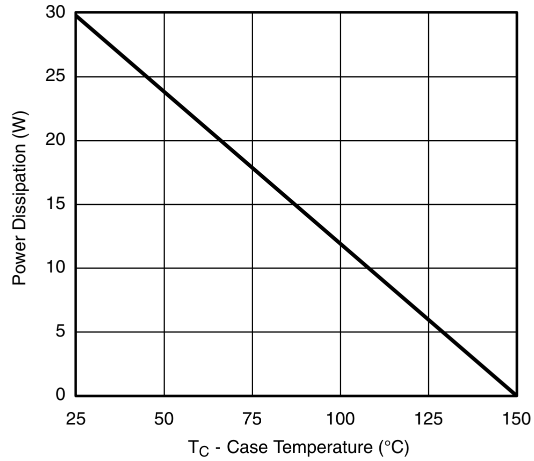
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



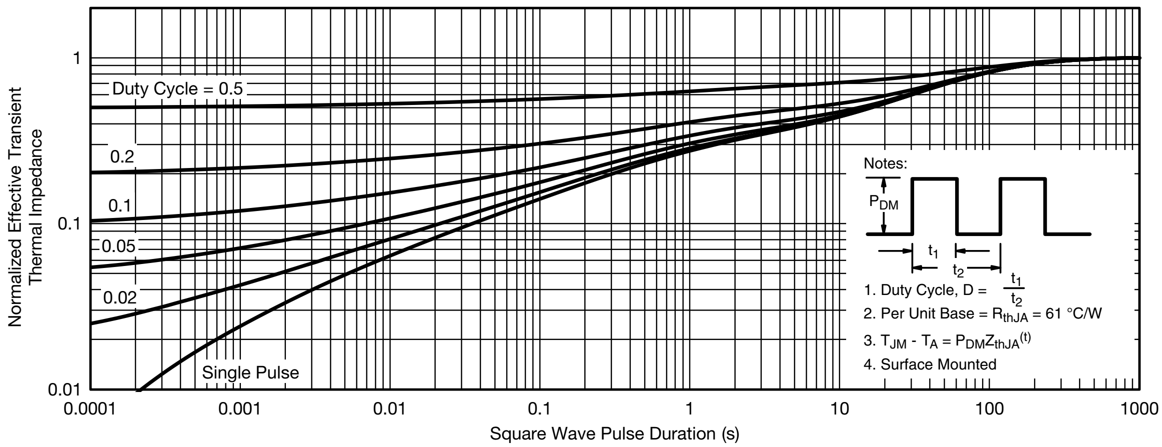
Current Derating*



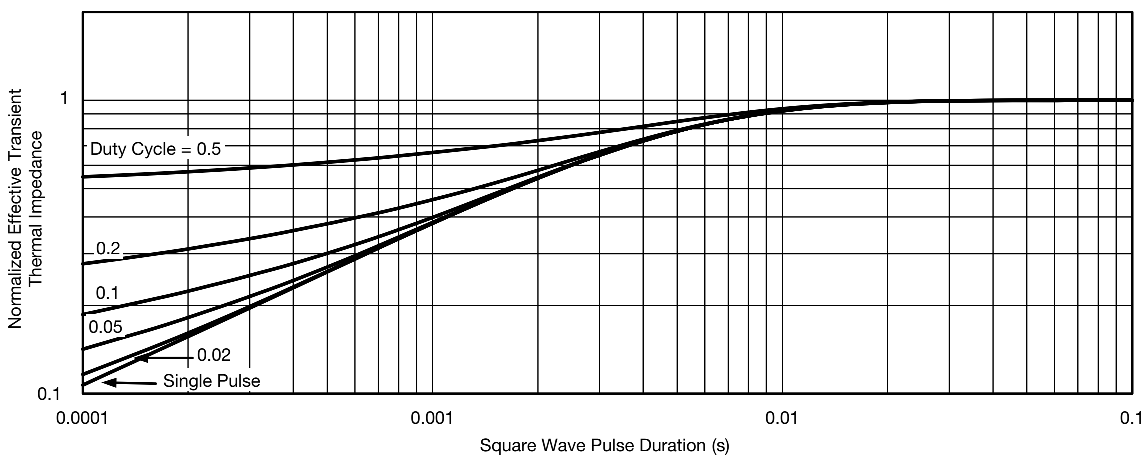
Power, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



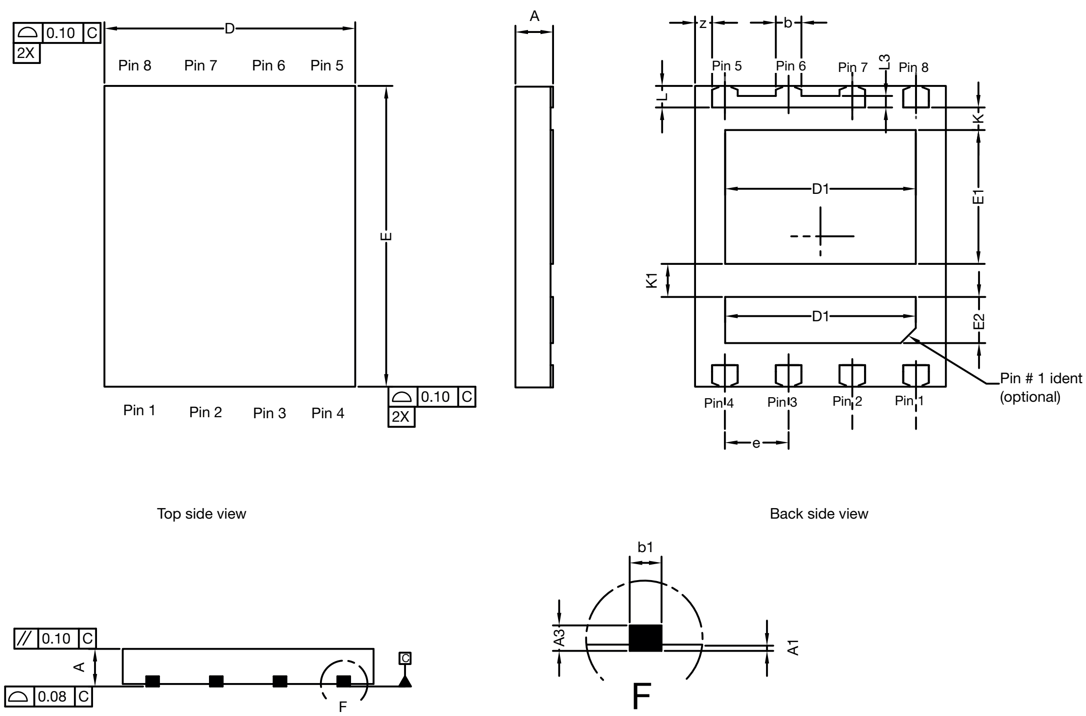
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63482.

PowerPAIR® 6 x 5 Case Outline



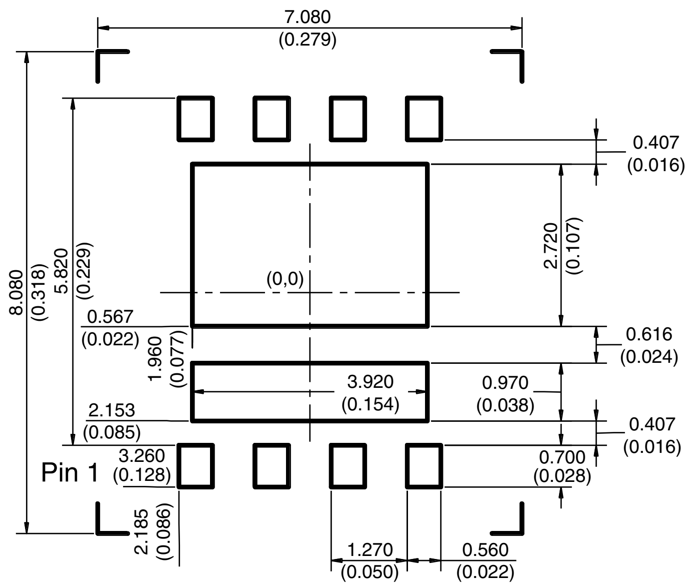
Top side view

Back side view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.15	0.20	0.25	0.006	0.007	0.009
b	0.43	0.51	0.61	0.017	0.020	0.024
b1		0.25 BSC			0.010 BSC	
D	4.90	5.00	5.10	0.192	0.196	0.200
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	5.90	6.00	6.10	0.232	0.236	0.240
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099
E2	0.87	0.92	0.97	0.034	0.036	0.038
e		1.27 BSC			0.005 BSC	
K Option AA (for W/B)		0.45 typ.			0.018 typ.	
K Option AB (for BWL)		0.65 typ.			0.025 typ.	
K1		0.66 typ.			0.025 typ.	
L	0.33	0.43	0.53	0.013	0.017	0.020
L3		0.23 BSC			0.009 BSC	
z		0.34 BSC			0.013 BSC	

ECN: T13-0354-Rev. B, 20-May-13
DWG: 6005

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 6 x 5



Recommended Minimum Pad
Dimensions in mm (inches)

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