DEM-DAI1738 Instruction Manual

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ABSTRACT

This user's guide describes the DEM-DAI1738 evaluation fixture for the PCM1738 stereo digital-to-analog (D/A) converter.

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Features and Description

The DEM-DAI1738 is an evaluation fixture for the PCM1738 24-bit, 192-kHz sampling stereo D/A converter. This evaluation fixture utilizes a DEM-DAI1738 demonstration board and demonstration software for function and operation control of the PCM1738.

The DEM-DAI1738 consists of a DAI (S/PDIF) section that uses a DIR1703 DAI receiver, a PCM1738 DAC section, a differential I/V section, and a balanced amplifier with post LPF section.

The DEM-DAI1738 requires a 5-V digital power supply for its digital circuits, a 5-V analog power supply for the PCM1738, and ±15-V analog power supply for the I/V and balanced amplifier circuits.

The DAI section has both coax and optical inputs that can be selected by a mounted switch and are capable of handling sampling rates up to 96 kHz.

The PCM1738 accepts up to 192-kHz sampling PCM audio data input and 64 f_S DSD signal input through function control and jumper connection on board.
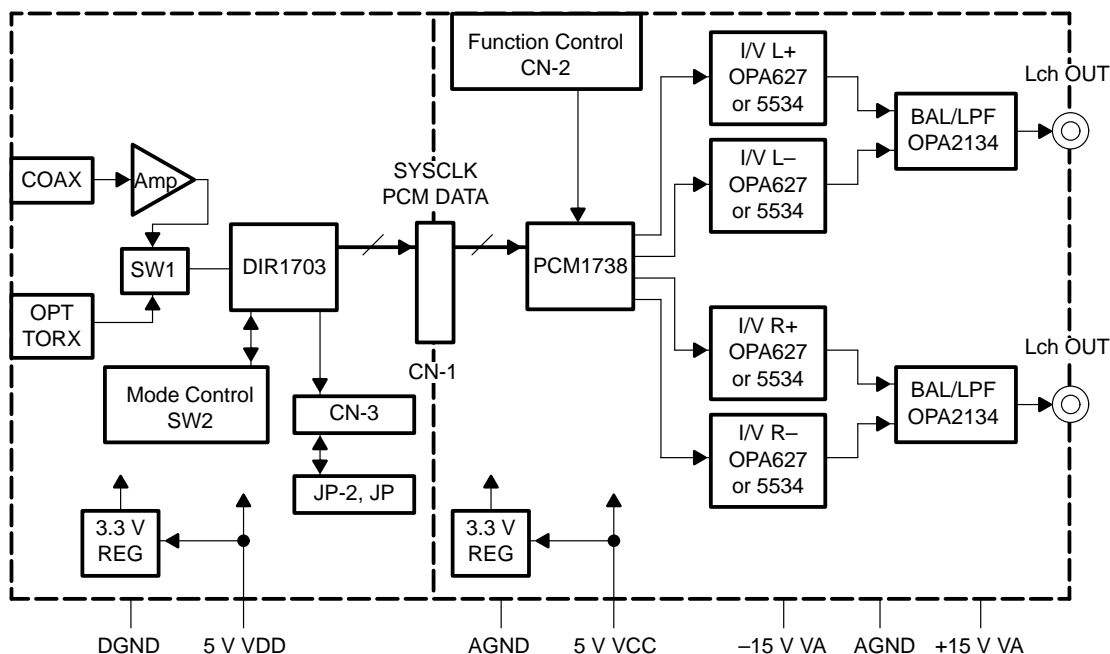
Figure 1. Block Diagram

Operation and Function Control of DAI Section

- **optical/coax input selection**

  SW1 is the optical/coax S/PDIF digital input selection switch. This switch is illustrated in Figure 2.

  1 ↑ COAX

  3 ↓ OPT

  Figure 2. Optical/Coax Input Selection

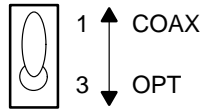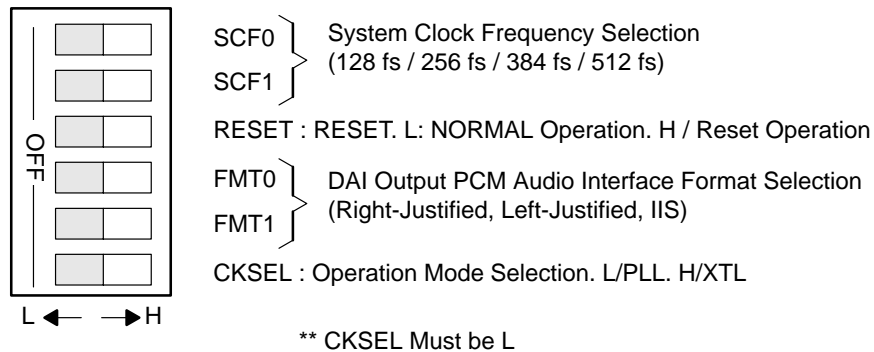- **function and operation control of DIR1738**

  SW2 is the function and operation control switch for the DIR1738. This switch is illustrated in Figure 3.

  SCF0 ⎫ System Clock Frequency Selection
  SCF1 ⎬ (128 fs / 256 fs / 384 fs / 512 fs)

  RESET : RESET. L: NORMAL Operation. H / Reset Operation

  FMT0 ⎫ DAI Output PCM Audio Interface Format Selection
  FMT1 ⎬ (Right-Justified, Left-Justified, IIS)

  CKSEL : Operation Mode Selection. L/PLL. H/XTL

  ** CKSEL Must be L

  Figure 3. Function and Operation Control of DIR1738

  Table 1. System Clock Frequency

SCF0	SCF1	SYSTEM CLOCK FREQUENCY
L	L	128 f_S
L	H	256 f_S
H	L	384 f_S
H	H	512 f_S

  Table 2. Audio Interface Format

FMT0	FMT1	AUDIO INTERFACE FORMAT
L	L	16-bit, MSB first, right-justified
L	H	24-bit, MSB first, left-justified
H	L	24-bit, MSB first, right-justified
H	H	24-bit, IIS

- **JP–2 Connection**

  JP-2 is used to enable CKSEL. Jumper on 3–4 enables CKSEL. This jumper connection is illustrated in Figure 4.

  1   3 3-4 Jumper Connection : Normal (Enable CKSEL)
  2   4

  JP-2
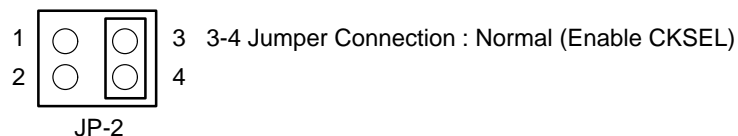
  Figure 4. JP-2 Connection

Crystal/External Clock Selection

Jumper JP-3 is used for selection of crystal oscillator or external clock frequency. This jumper connection is shown in Figure 5. Table 3 gives the external clock frequencies that can be selected using JP–3 for different sampling rates.

Figure 5. Crystal/External Clock Selection

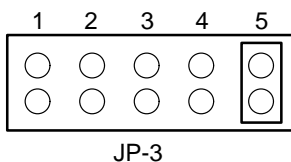**Table 3. External Clock Selection**

SAMPLING RATE	128 f_S	256 f_S	384 f_S	512 f_S	BRSEL CONNECTED TO	
32 kHz	4.096 MHz	8.192	12.288	16.384	BFRAME	$\rightarrow$ 1
44.1 kHz	5.6448	11.2896	16.9344	22.5792	EMFLG	$\rightarrow$ 2
48 kHz	6.144	12.288	18.432	24.576	Open	$\rightarrow$ 5
88.2 kHz	11.2896	22.5792	33.8688	45.1584	URBIT	$\rightarrow$ 3
96 kHz	12.288	24576	36.864	49.152	CSBIT	$\rightarrow$ 4

PCM Audio Interface

The PCM audio data and system clock from the DIR1701 can be connected to the digital input of the PCM1738 by a jumper connection on CN–1.

External audio data input can be interfaced using the right side pins on CN–1. Refer to the current version of the PCM1738 data sheet, TI literature number SBAS174, for interface connections of digital filter (DF) and direct stream digital (DSD) modes.
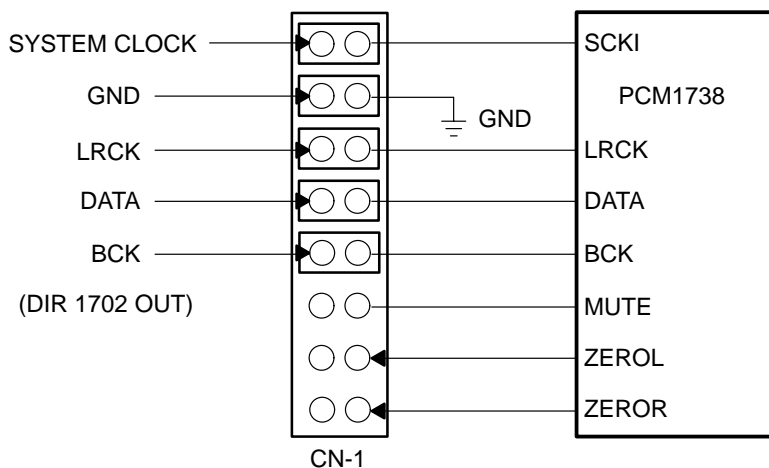
Figure 6. PCM Audio Interface

5-V Power Supply for Digital VDD

The DEM–DAI1738 requires 5-V digital and analog power supplies. These supplies must be kept separate to prevent interference between the digital and DAC/analog sections.

The JP–1 connection allows common connection of the 5-V V_{DD} and 5-V V_{CC} supplies for limited power supply availability during actual evaluation.
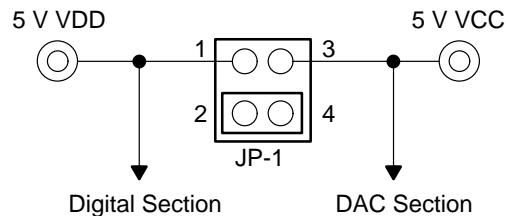
Figure 7. 5-V Power Supply

AC/DC Coupling Selection

Jumpers 4 and 5 are used for dc or ac-coupling selection between I/V converter output and balanced amplifier input.
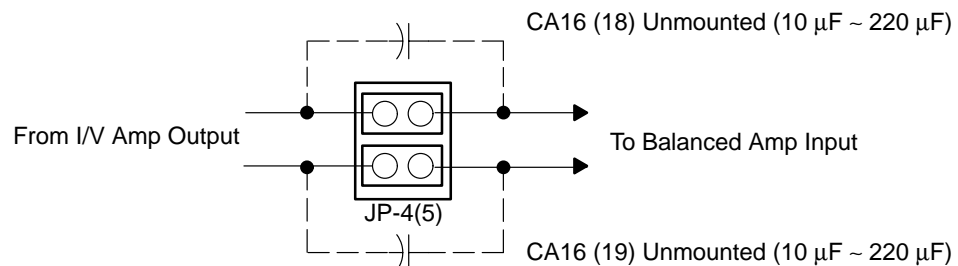
Figure 8. AC/DC Coupling Selection

Schematic Diagram—DIR Section

Figure 9 shows the schematic diagram for the DIR section.

Figure 9. DIR Section

(*1) : Silk Shows EMFLG/FLT
(*2) : Silk Shows PEFLG

Schematic Diagram—DAC, Analog, and Power Supply Section

Figure 10 shows the schematic diagram for the DAC, analog, and power supply section.

Figure 10. DAC, Analog, and Power Supply Section
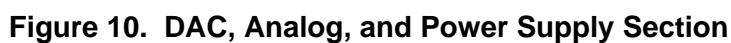
Table 4 presents the component values for the DAC, analog, and power supply section.

Table 4. Component Values for DAC, Analog, and Power Supply Section
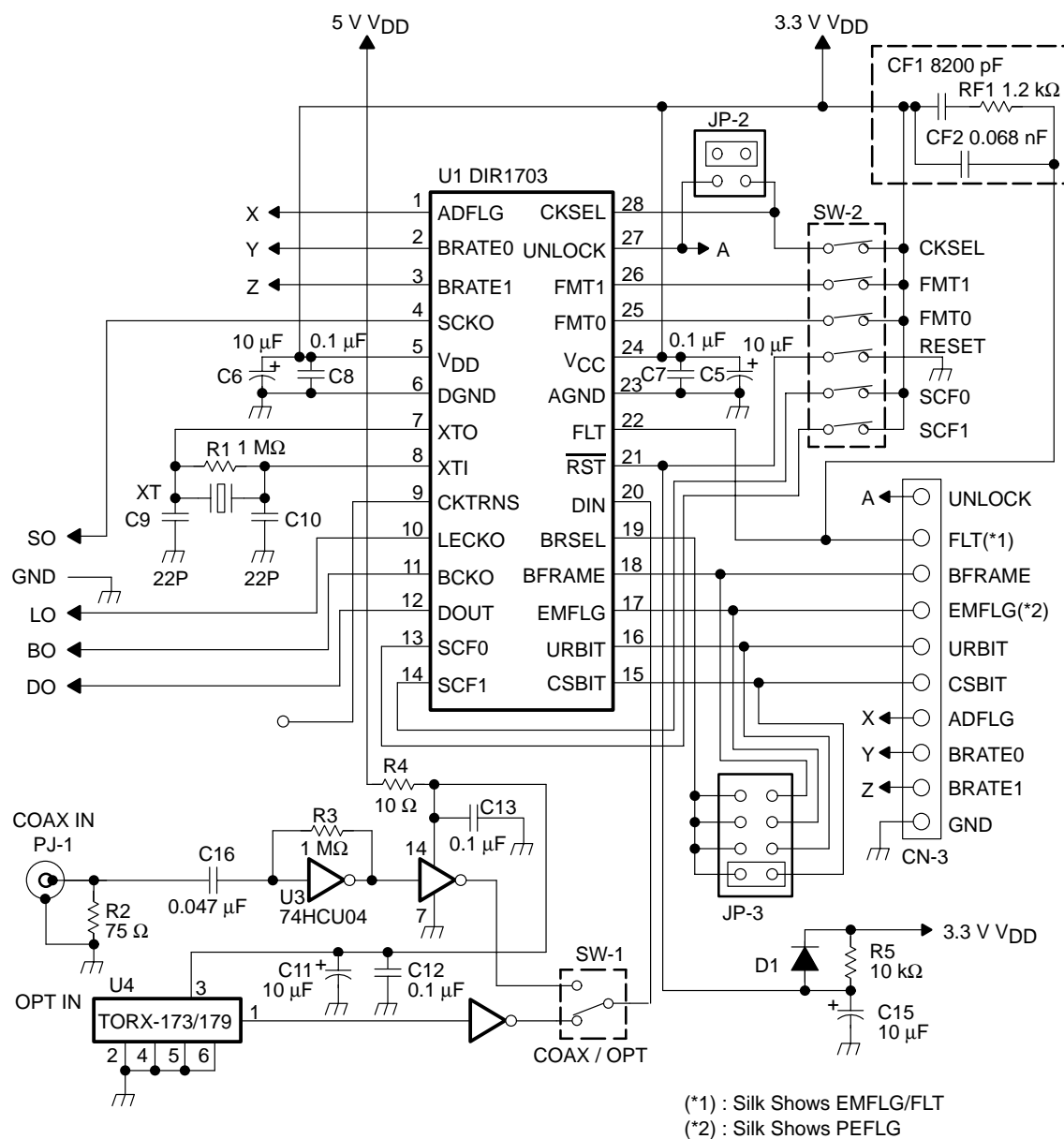
COMPONENT NUMBER	COMPONENT VALUE
CP1, CP2, CP3	220 µF, 25 V
CP7, CP11–CP20	1 µF, 25 V
CP8, CPD1	100 µF, 16 V
CA2, CA4, CA5, CA6, CA7, CP11, CP12	10 µF, 16 V
CA16–CA19	47 µF, 25 V
CP4, CP5, CP6, CP9, CA1, CA3	0.047 µF
CA8, CA9, CA10, CA11	5600 pF
CA20, CA21	8200 pF
CA22–CA25	1800 pF
CP10, CPD2	0.1 µF
LP1	47 µF
RP1	10 Ω, 1/4 W
RA1	16 kΩ, 1/8 W
RA2, RA3, RA20, RA21	100 Ω, 1/8 W
RA4–RA19	620 Ω, 1/8 W
RP2	330 Ω, 1/8 W
RAC, RAM	10 kΩ, 1/8 W

CA16, CA17, and CA18 are not mounted

Schematic Diagram—Power Supply for Operational Amplifier and CN–1/CN–2 Connectors Section

Figure 11 shows the schematic diagram for the power supply for the operational amplifier, CN–1, and CN–2 connector section.
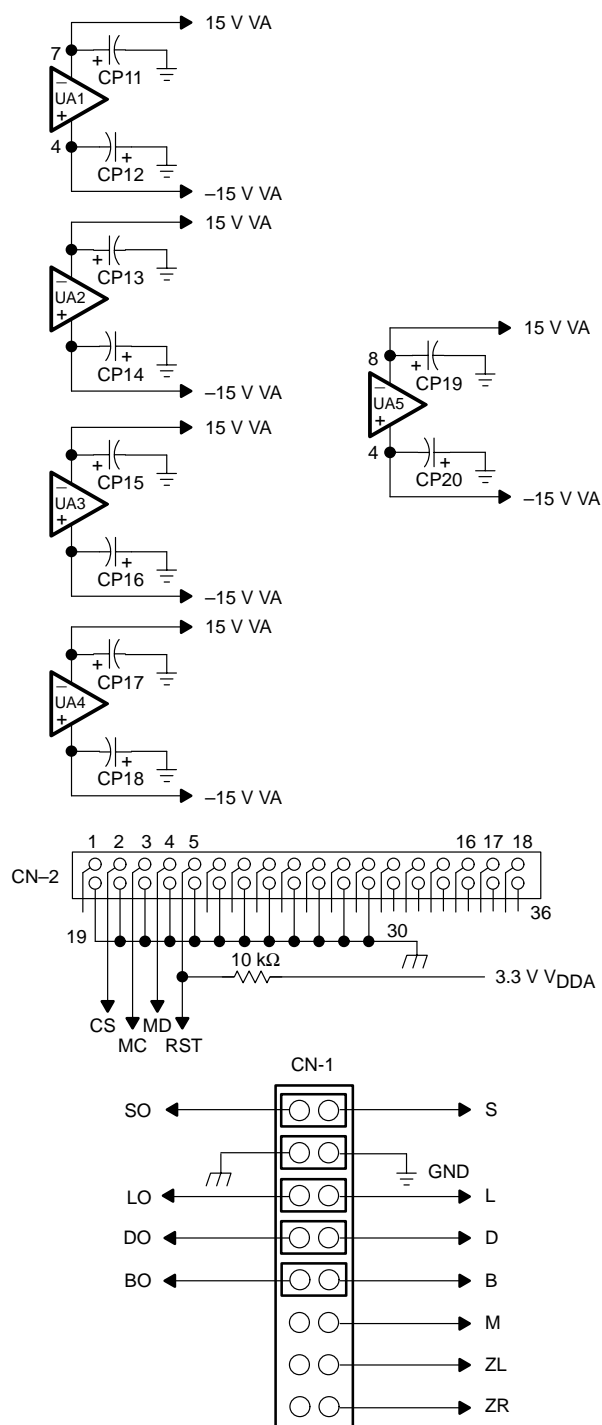
Figure 11. Power Supply for Operational Amplifier and CN–1/CN–2 Connectors Section

Printed-Circuit Board

Figure 12 shows the printed-circuit board.
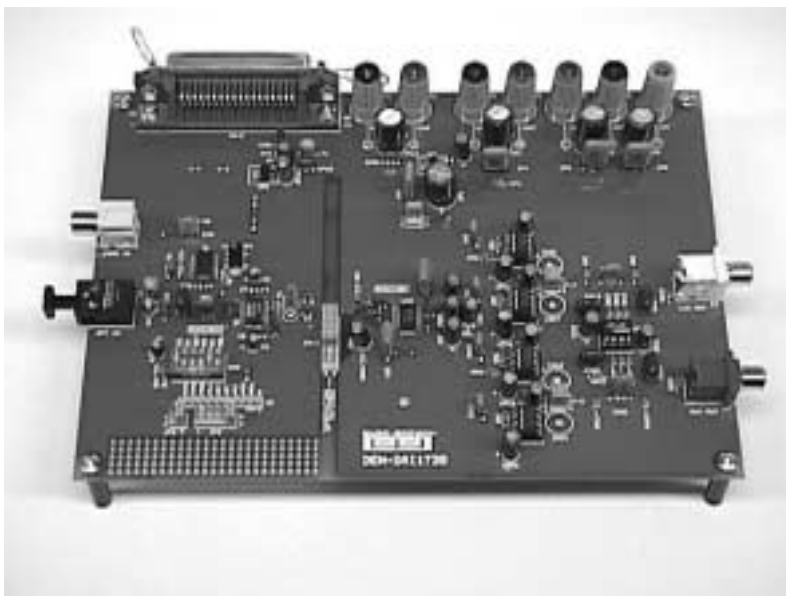
Figure 12. Printed-Circuit Board

- **parts location**

Figure 13 shows the printed circuit layout.
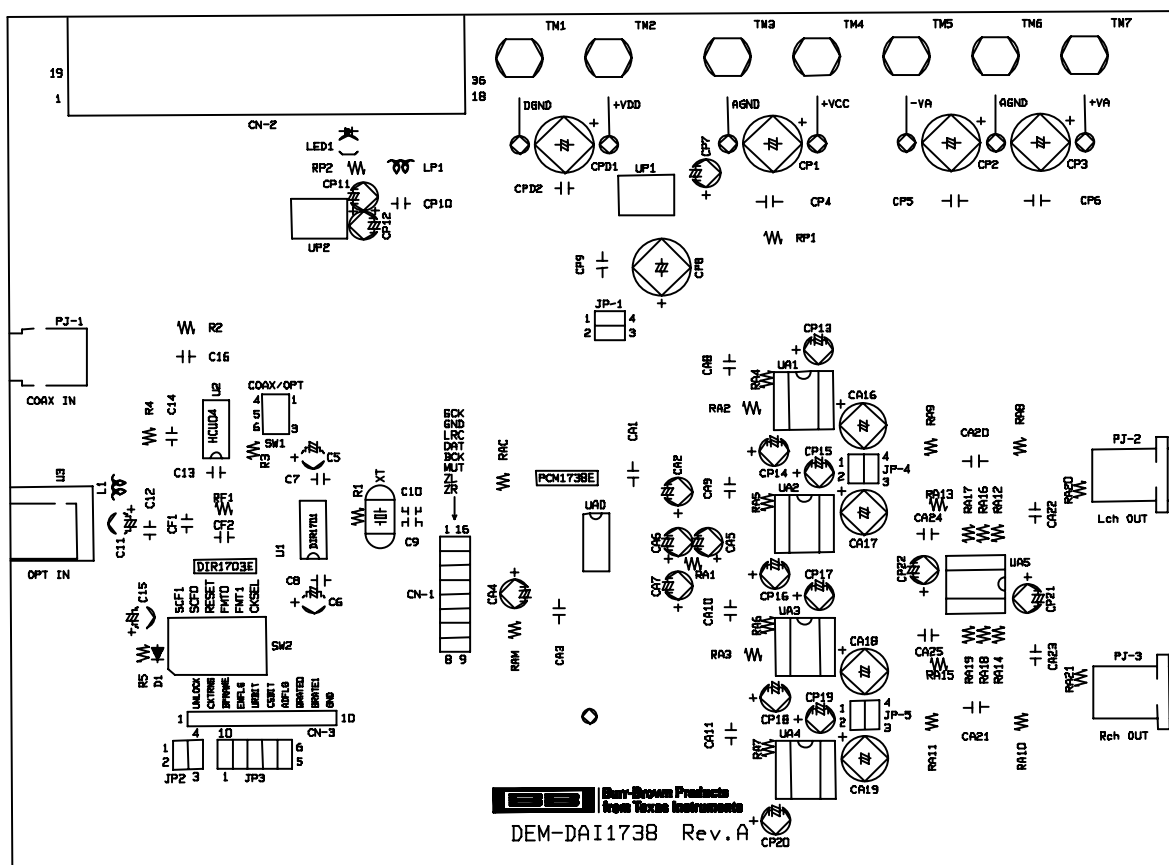
TOP SILK   DEM-DAI1738

Figure 13. Printed-Circuit Layout—Parts Location

- **top-side layer**

Figure 14 shows the top-side layer of the DEM–DAI1738 printed-circuit board.
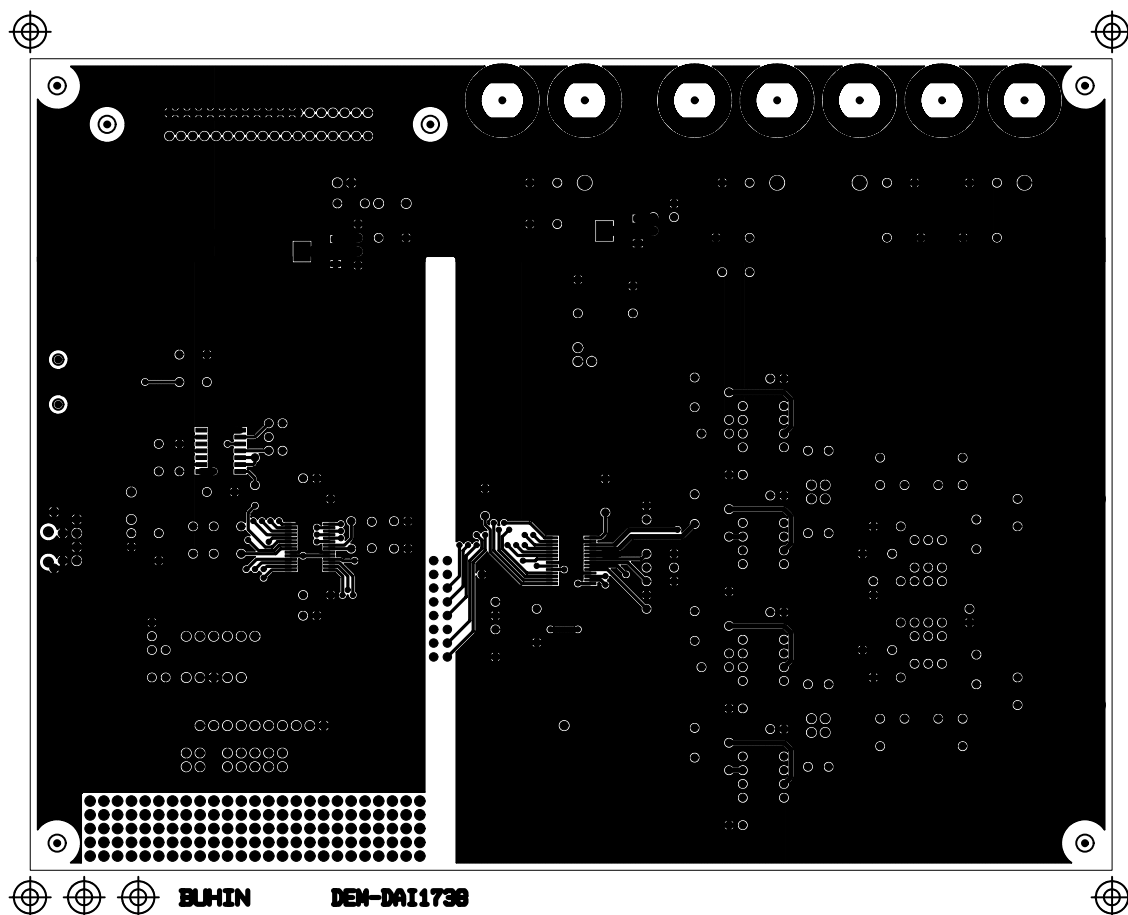
Figure 14. Top-Side Layer

- **bottom-side layer**

Figure 15 shows the bottom-side layer of the DEM–DAI1738 printed-circuit board.
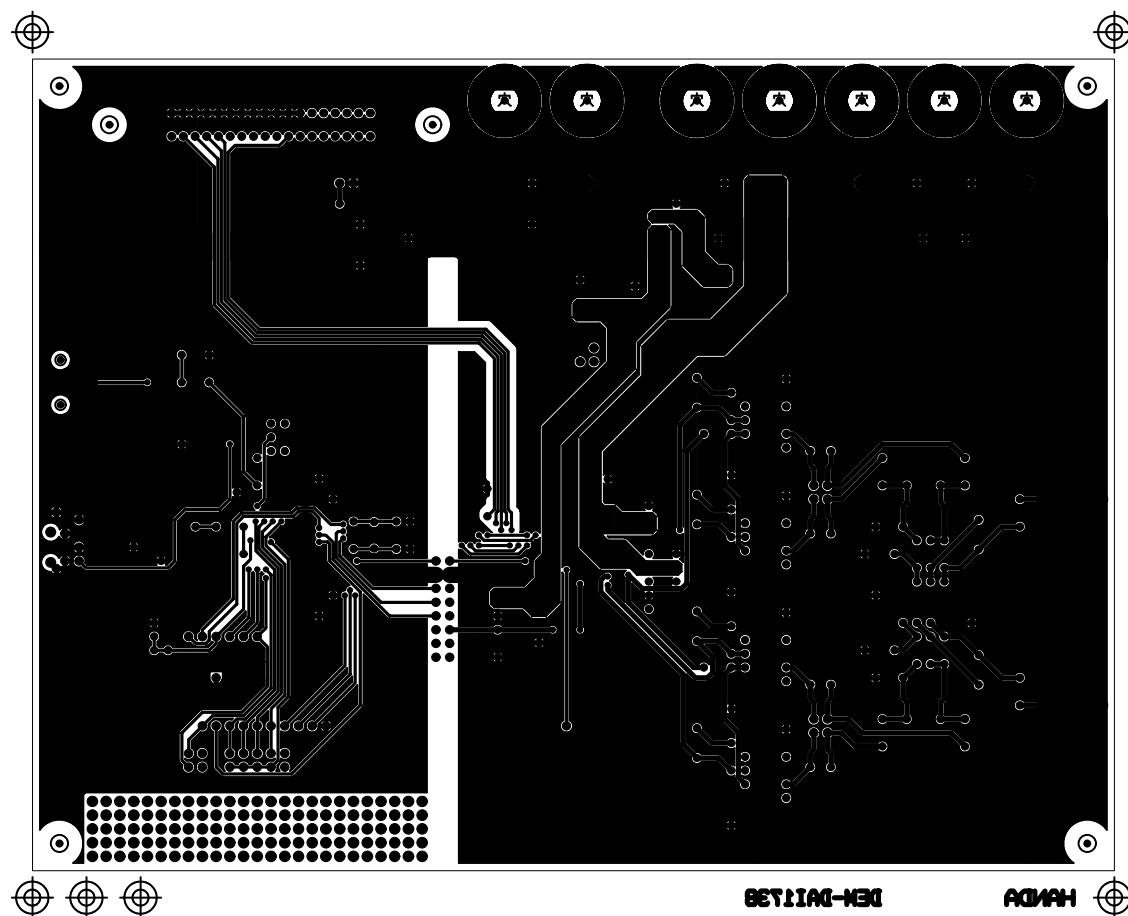
Figure 15. Bottom-Side Layer

Demonstration Software

Software is provided with the DEM–DAI1738 to allow programming of the PCM1738's internal registers. The software operates on computers running Microsoft Windows™ 3.1, 95, or 98.

The demonstration software requires connection of the PC printer port to CN–2 of the DEM–DAI1738 using a standard printer cable.

- **installation**

The demonstration software is distributed on a 3.5-inch floppy disk.

To install the software on your PC computer, first create a new folder on your hard drive with an appropriate name (such as *DEM1738*). Then open the *Dem1738* folder on the installation floppy disk and copy all its files to your new folder.

Open the configuration setting file named *# Dem1738* using a text editor, such as Notepad™. After the file opens, search for the following line:

PCMIFADR = &h378

The &h378 indicates the printer port address that the demonstration software uses to communicate with the DEM–DAI1738.

This address must be set to %h378, &h278, or &h3BC. Most PCs use &h378 as the default printer port address. If your printer port is not located at &h378, edit the address to match your computer's port address.

- **using the demonstration software**

Double-click on the application file named DEM1738. A window appears on your screen, as shown in Figure 16. There are two menu selections (Execute and Window) near the top of the window.

The Execute menu includes three selections: Initialize, Reset, and Exit. Selecting Initialize instructs the program to write all of the PCM1738's internal registers with the default values.

Reset instructs the program to rewrite the PCM1738's internal registers with the data currently selected in the application windows. Exit closes the application.

The Window menu includes four selections: Attenuation control, Operation control, Function control, and Register read. The following sections provide an explanation of each window.

- **HOLD and PASS**

Each window has a button near the top which is labeled either HOLD or PASS. The current setting is toggled by clicking on this button. When set to HOLD, the settings in a window can be changed, but are not written to the register(s) until the OK button (which appears at the bottom of the window) is pressed.

When set to PASS, any setting changes made in a window are immediately written to the corresponding register(s).

- **function control**

Enable operation and function control of the DEM–DAI1738 are shown in the following table.

Table 5. Function Control

FUNCTION	DEFAULT	REGISTER	BIT
Functions available for both write and read			
Digital attenuation control 0 dB to 120 dB and mute, 0.5 dB step	0 dB	Register 16 for L-channel Register 16 for L-channel	ATL[7:0] ATR[7:0]
Attenuation load control Disable, enable	Attenuation disable	Register 18	ATLD
Attenuation speed selection $\times$1 f_S speed selection	$\times$ 1 fx	Register 19	ATS[1:0]
Soft mute control Mute disable, enable	Mute disable	Register 18	MUTE
Infinite zero mute control Disable, enable	Disable	Register 19	INZD

Input audio data format selection
    16/20/24-bit standard (right-justified)
    24-bit MSB-first left-justified
    16/24-bit standard (right-justified)
	16-bit standard format	Register 18	FMT[2:0]

De-emphasis control Disable, enable	De-emphasis disable	Register 18	DME
Sampling rate selection for de-emphasis Disable, 44.1 kHz, 48 kHz, 32 kHz	De-emphasis disable	Register 18	DMF[1:0]
Digital filter rolloff selection Sharp rolloff, slow rolloff	Sharp rolloff	Register 19	FLT
Output phase reversal Normal, reverse	Normal	Register 19	REV
DAC operation control Enable, disable	DAC operation enabled	Register 19	OPE
System clock (SCKO) output control Output enable, disable	Output enabled	Register 19	CLKE
System clock (SCKO) rate control SCK1, SCK2	SCKI	Register 19	CLKD
System reset control Reset operation, normal operation	Normal operation	Register 20	SRST
Mode register reset control Reset operation, normal operation	Normal operation	Register 20	MRST
Digital filter bypass control DF enable, DF bypass	DF enabled	Register 20	DFTH
Delta-Sigma oversampling rate selection $\times$64 f_S, $\times$128 f_S, $\times$32 f_S	$\times$ 64 f_S	Register 20	OS[1:0]
Delta-Sigma order selection 3rd order, 5th order	3rd order	Register 20	DSOS
Monaural mode selection Stereo, monaural	Stereo	Register 20	MONO
Channel selection of monaural mode data L-channel, R-channel	L-channel	Register 20	CHSL
Functions available only for read			
Zero-detection flag Not zero, zero detected	Not-zero = 0 Zero detected = 1	Register 21	ZFGL for L-channel ZFGR for R-channel

TEXAS
INSTRUMENTS

• **PCM1738 demonstration software window**
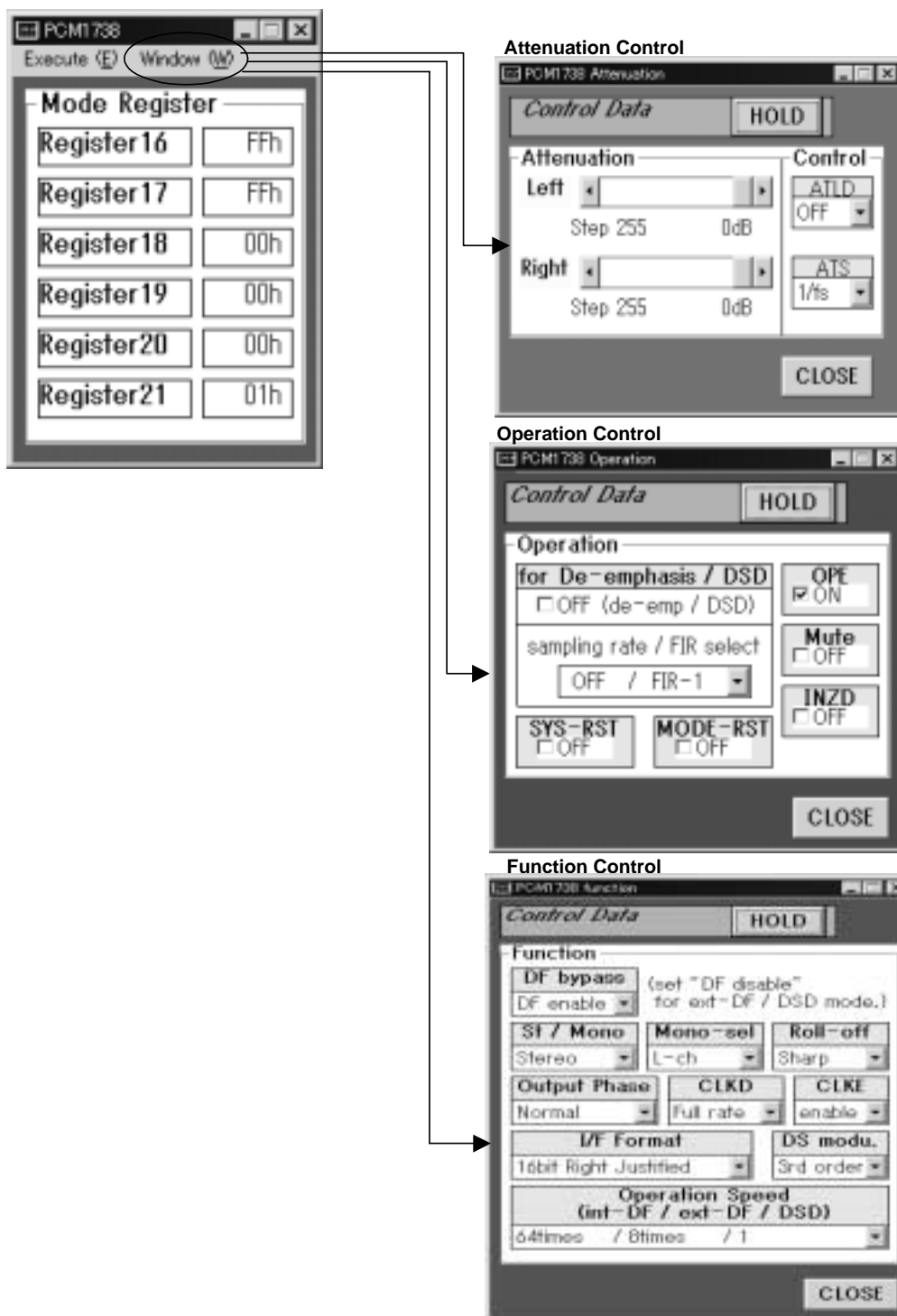
Figure 16. Demonstration Software Window

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