![Texas Instruments logo] **TEXAS INSTRUMENTS**

THS1040/41 Evaluation Module for the THS1040/THS1041 10-Bit ADC

User's Guide

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This manual describes the physical characteristics, functions, modes of operation, and configuration of the THS1040/41EVM evaluation module (EVM).

How to Use This Manual

❑ Chapter 1 – Overview

❑ Chapter 2 – Physical Description

❑ Chapter 3 – Circuit Description

❑ Chapter 4 – Modes of Operation

❑ Chapter 5 – Schematics

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Overview

This chapter gives a general overview of the THS1040/41EVM evaluation module (EVM), and describes some of the factors that must be considered in using this module.

1.1   Purpose

The THS1040/41EVM evaluation module (EVM) provides a platform for evaluation of the THS1040 and THS1041 10-bit analog-to-digital converters (ADC) under various signal, reference, and supply conditions. Unless stated explicitly, the functionality described in this user's guide applies to both THS1040 and THS1041 devices.

1.2   EVM Basic Functions

Analog input to the THS1040/41 is provided by external SMA connectors. The input can be configured onboard to be ac, dc, or transformer-coupled to the input of the device.

An external SMA connector is provided on the THS1041 for the clamp input. This allows external digital control of the ADC's clamping function. The ADC can be clamped either to an external reference voltage or from the on-chip DAC.

The EVM provides an external SMA connection for ADC clock input. The user can send this clock to the output connector with the digital data or provide a second clock source to be sent in place of the ADC clock. This allows the user to provide the required setup and hold times of the output data with respect to the output clock. Refer to the clock section for proper configuration and operation.

In addition to the internal reference from the THS1040/41 device, options are provided on the EVM to allow adjustment of the ADC reference via an onboard reference circuit.

Output from the EVM is via a 40-pin header connector. The digital lines from the THS1040/41 are buffered using the SN74LVTH162244 before going to the header.

Power connections to the EVM are via 4-mm banana sockets. Separate connectors are provided for the analog and digital supply to the device.

The THS1041 has a number of programmable registers that can be programmed using DIL switches on the EVM.

1.3   Power Requirements

The EVM has 2 main dc-power supply connections: 3.3 V for the analog and 3.3-V digital supplies to the ADC. Each of these supplies is independent, but it should be noted that the input thresholds of the ADC varies dependent on the digital and analog supply voltages, as per the data sheet specification. A 5-V connector is also provided to allow the user to reprogram the CPLD (THS1041 EVM only).

Voltage Limits

Exceeding the 3.3-V maximum can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 THS1040/41EVM Operational Procedure

The THS1040/41EVM provides a flexible means of evaluating the THS1040 and THS1041 in a number of modes of operation. These are described more fully in Chapter 4. The following basic setup procedure can be used as a board-confidence check:

❏ Verify all jumper settings against the following schematic jumper table:

Device	Jumper Table (connection)
THS1040	SJP1 OUT, SJP2 pin 1–2, SJP3 OUT, SJP4 OUT, SJP5 OUT, SJP6 pin 1–2, SJP7 pin 2–3, SJP8 pin 2–3, SJP9 pin 2–3, SJP10 pin 2–3
	W1 pin 1–2, W2 pin 1–2, W3 pin 1–2, W4 pin 2–3, W5 pin 1–2, W6 OUT, W7 IN, W8 OUT, W9 OUT, W10 OUT, W11 OUT, W12 OUT
THS1041	SJP1 OUT, SJP2 pin 1–2, SJP3 OUT, SJP4 OUT, SJP5 OUT, SJP6 pin 1–2, SJP7 pin 1–2, SJP8 pin 1–2, SJP9 pin 1–2, SJP10 pin 1–2
	W1 pin 1–2, W2 pin 1–2, W3 OUT, W4 OUT, W5 pin 1–2, W6 OUT, W7 IN, W8 OUT, W9 OUT, W10 OUT, W11 OUT, W12 OUT

❏ Connect supplies to the EVM as follows:

■ 3.3 V analog supply to J8 and return to J7.

■ 3.3 V digital supply to J10 and return to J11.

❏ Switch power supplies on.

❏ Use a function generator with 50-Ω output to input a 40-MHz, 1.5-V offset, 3-Vp-p amplitude square wave signal into J4 to be used as the ADC clock. The frequency of the clock must be within the specification for the device speed grade.

❏ Use a function generator with 50-Ω output to input a 40-MHz, 1.5-V offset, 3-Vp-p amplitude square wave signal into J14 to be used as the buffered output clock and the PLD input clock (THS1041 EVM only). This signal must be the same frequency and synchronized with the ADC clock.

❏ Use a frequency generator with 50-Ω output to input a 1.5-MHz, 0-V offset, 1.5-Vp-p amplitude sine wave signal into analog input SMA J2. This provides a transformer coupled differential signal to the ADC.

❏ The digital pattern on the output connector J12 should now represent a sine wave and can be monitored using a logic analyzer.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM, and lists the components used on the module.

2.1 PCB Layout

The EVM is constructed on a 4-layer, 4.15″ × 4.5″, 0.062″ thick PCB using FR-4 material. Figures 2–1 through 2–4 show the individual layers.
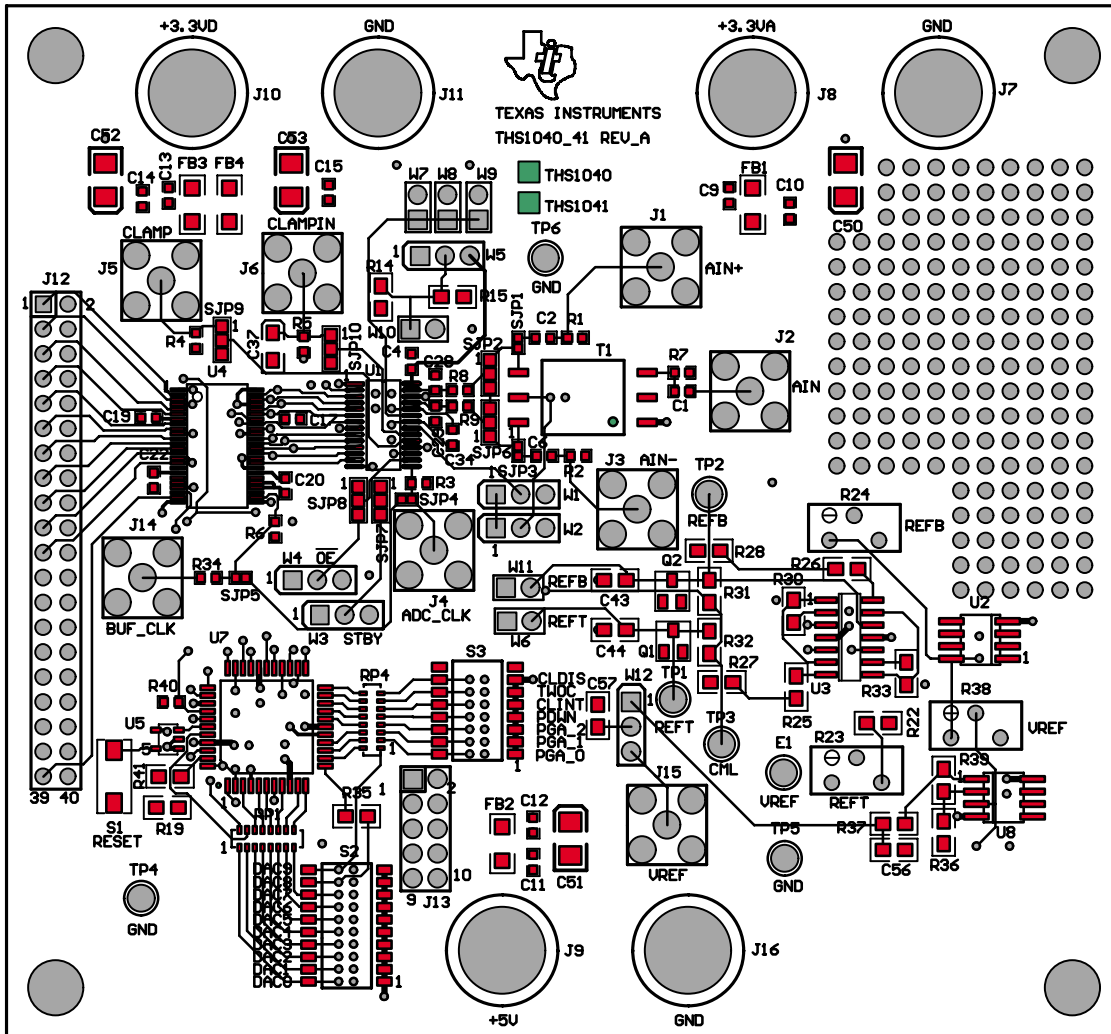
Figure 2–1. Top Layer
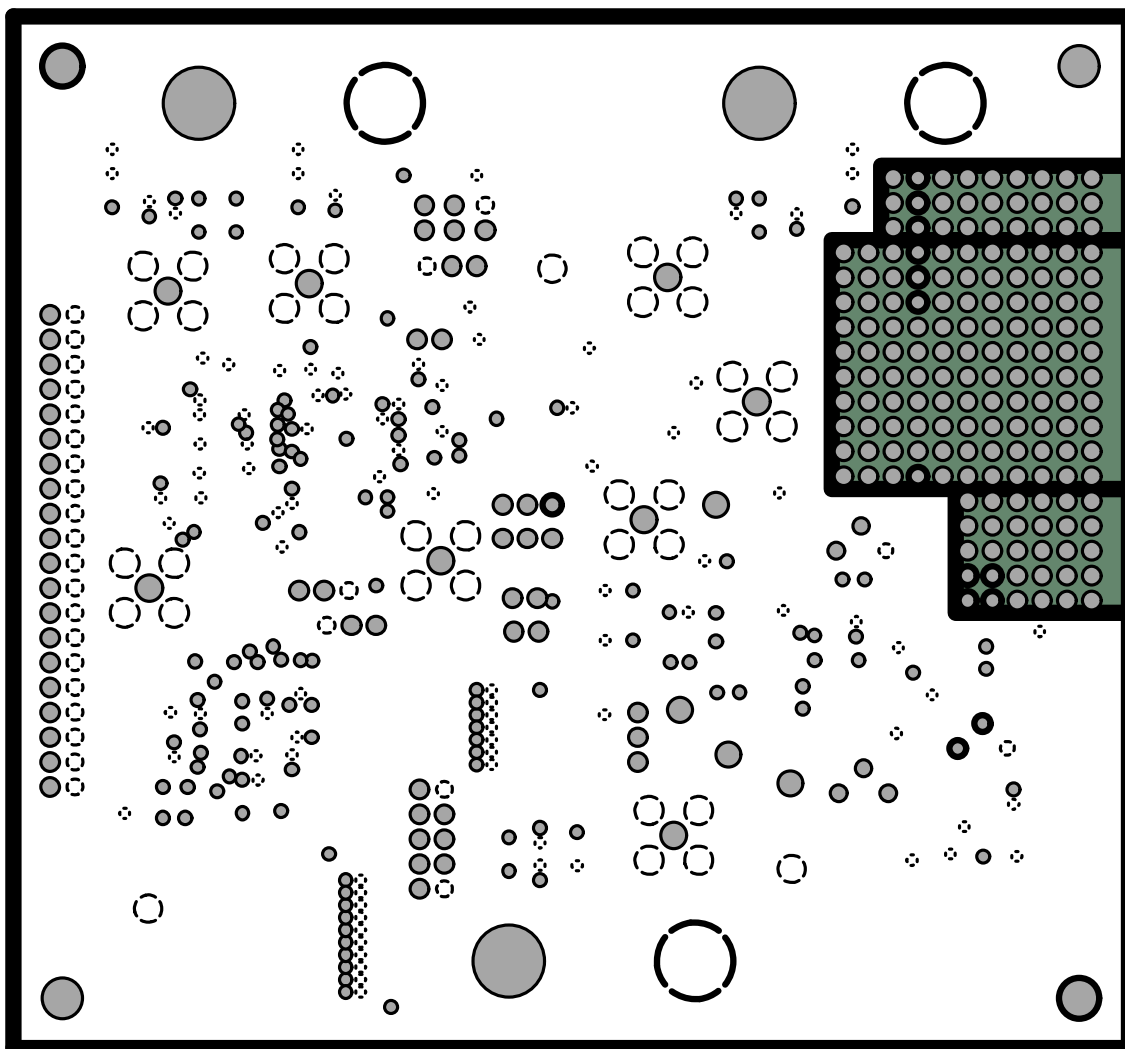
Figure 2–2. Layer 2—Ground Plane
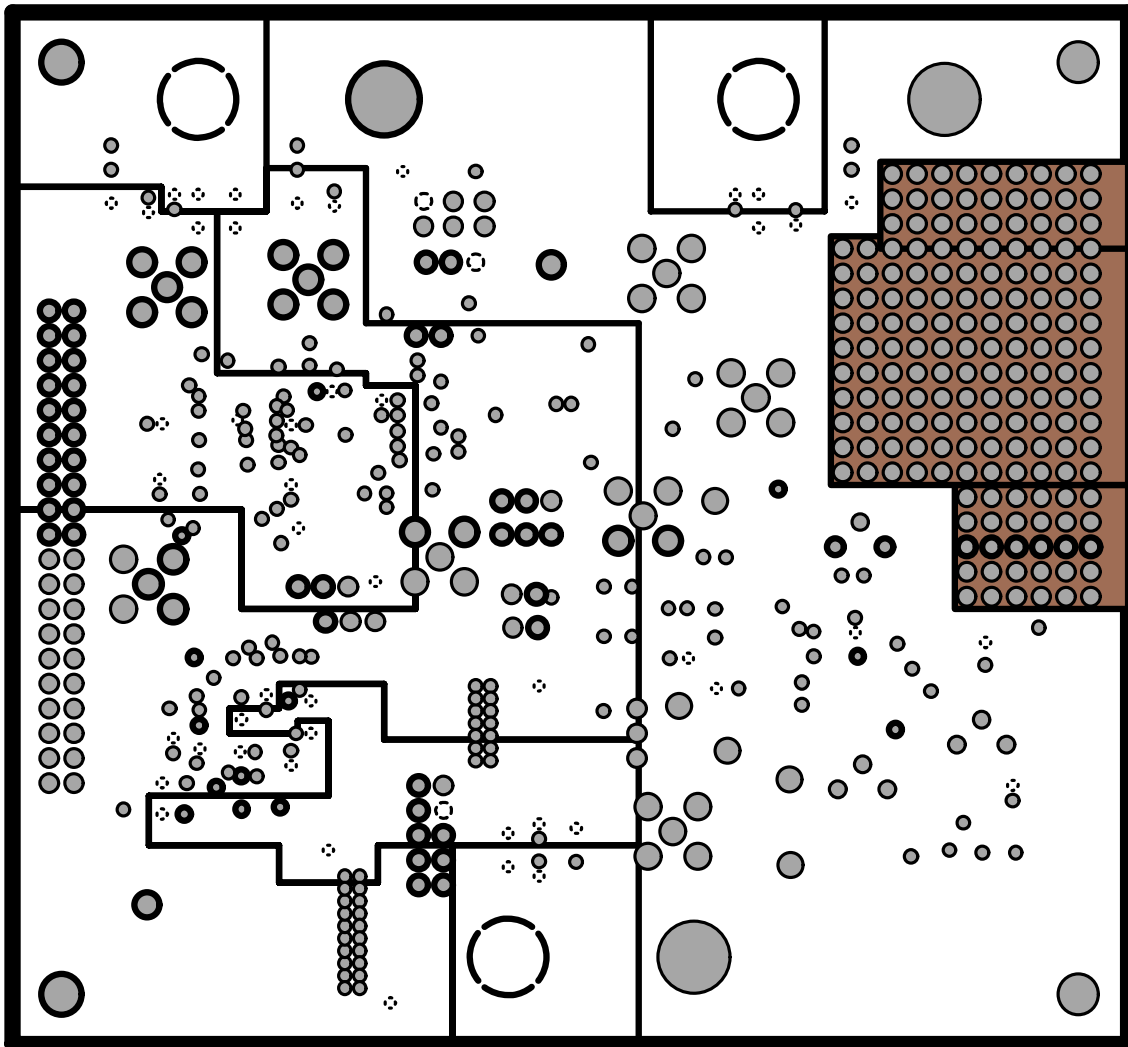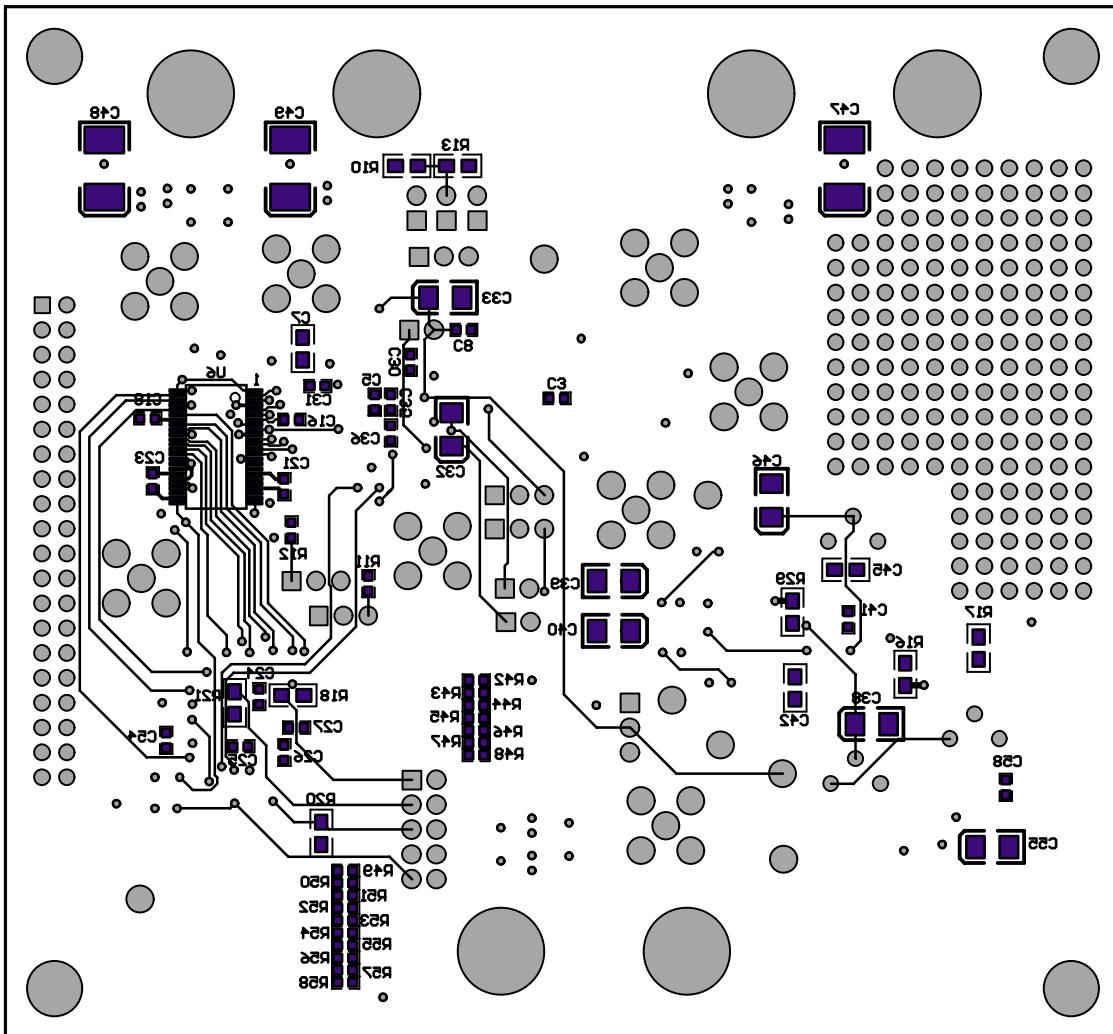
Figure 2–3. Layer 3—Power Plane

Figure 2–4. Bottom Layer

2.2 Parts List

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. Parts List

Description	Qty	Part Number	Manufacturer	Reference Description
47-µF tantalum, 10% 10 V	3	10TPA47M	Sanyo	C47, C48, C49
10-µF, 10-V, 10% capacitor	9	GRM42X5R106K10	Murata	C38–C40, C46, C50–53, C55
1-µF, 10-V, 10% capacitor	2		Murata	C32, C33
0.1-µF, 16-V, 10% capacitor	32	ECJ-1VB1C104K	Panasonic	C1–C6, C8–C27, C34–C36, C41, C54, C58
0.1-µF, 16-V, 10% capacitor	7		Panasonic	C7, C42–C45, C56, C57
20-pF, 50-V, 5% capacitor	2		AVX	C28, C29
10-µF, 50-V, 10% capacitor	1			C37
470-pF, 50-V, 10% capacitor	2			C30, C31
Ferrite bead	4			FB1–FB4
0-Ω resistor, 1.16 W, 1%	1	ERJ-3EKF0R00V	Panasonic	R34
1.5-kΩ resistor, 1/16 W, 1%	1			R22
10-Ω resistor, 1/16 W, 1%	2			R8, R9
100-kΩ resistor, 1/16 W, 1%	17			R42–R58
432-Ω resistor, 1/16 W, 1%	2	ERJ-3EKF432R0V	Panasonic	R25, R26
49.9-Ω resistor, 1/16 W, 1%	8	ERJ-3EKF49R9V	Panasonic	R1–R7, R40
5.1-kΩ resistor, 1/16 W, 1%	1			R29
10-kΩ resistor, 1/16 W, 1%	0			*Not installed*: R11, R12
10-kΩ resistor	4			R10, R13, R16, R36 *Not installed: R14, R15*
11-kΩ resistor, 1/16 W, 1%	1			R33
15-kΩ resistor, 1/16 W, 1%	1			R30
1-kΩ resistor, 1/16 W, 1%	6			R17–R21, R37
180-Ω resistor	2			R31, R32
330-Ω resistor	2			R27, R28
4.7-kΩ resistor	2			R35, R41
730-Ω resistor	1			R39
10-KΩ Pot	3	3296Y-101	Bourns	R23, R24, R38
100-Ω resistor	2	742C163101JCT	Bourns	RP1, RP4
Transformer	1	T1-6T-KK81	Mini-Circuits	T1
SMA connectors	8	713-4339	ALLIED	J1–J6, J14, J15
Black test point	3	5001K	Keystone	TP4–TP6
Red test point	3	5000K	Keystone	TP1–TP3
2POS_header	6	TSW-150-07-L-S	Samtec	W6–W11
3POS_header	4	TSW-150-07-L-S	Samtec	W1, W2, W5, W12 *Not installed*: W3, W4
2POS_CONNECTOR SMT	4			SJP1, SJP3–SJP5
3POS_CONNECTOR SMT	6			SJP2, SJP6–SJP10
40-PIN_IDC	1			J12
5-PIN_IDC	1			J13
Red banana jacks	3	ST-351A	Allied	J8–J10
Black banana jacks	3	ST351B	Allied	J7, J11, J16
MMBT3904	1			Q2
MMBT3906	1			Q1
EVQ-PJ_SWITCH	1			S1

Table 2–1. Parts List (Continued)

Description	Qty	Part Number	Manufacturer	Reference Description
SWITCH_10POS_SMT	1			S2
SWITCH_8POS_SMT	1			S3
THS1041	1	THS1041CPW	TI	U1
LT1004-1.2	1	LT1004CD–1.2	TI	U2
TLV2464	1	TLV2464CD	TI	U3
SN74AVC162244	2	SN74AVC162244DGG	TI	U4, U6
TPS3801	1	TPS3801K33DCK	TI	U5
EPM7032AETC44	1		Altera	U7
TLV2462D	1	TLV2462CD	TI	U8
Stand off hex (1/4 × 1")	4	219-2063	Allied	

Chapter 3

Circuit Description

This chapter discusses the various functions on the EVM.

3.1 Circuit Function

The following paragraphs describe the function of individual circuits. Refer to Chapter 4 for jumper configurations for various modes of operation, and to the relevant data sheet for device operating characteristics.

3.1.1 Inputs

The ADC has either transformer-coupled input from a single-ended source, true differential analog inputs, or a single-ended input. These inputs are provided via SMA connectors J1, J2, and J3 on the EVM and can be configured in three ways as discussed in the following sections.

3.1.1.1 Differential Interface

For true differential input, the positive differential signal is connected to J1 and the negative differential signal is connected to J3. The jumpers on the board are then configured as follows: SJP1 IN, SJP2 pin 1–2, SJP3 IN, SJP6 pin 1–2, W1, W2, and T1 removed. The inputs have 50-Ω terminators and are ac-coupled.

3.1.1.2 Single-Ended Transformer Coupled Interface

For transformer-coupled ADC input using a single ended source, a positive signal is applied to SMA J2. The jumpers on the board are then configured as follows: SJP1 OUT, SJP2 pin 1–2, SJP3 OUT, SJP6 pin 1–2, W1 pin 1–2, and W2 pin 1–2. Transformer T1 performs the single ended to differential signal conversion.

3.1.1.3 Single-Ended Interface

For single-ended input, a positive signal is applied to SMA J1. The jumpers on the board are then configured as follows: SJP1 IN, SJP2 pin 1–2, SJP3 IN, SJP6 pin 1–2, C6 replaced with a short, W1, W2, and T1 removed. A dc source is then applied to SMA J3 to provide the midscale voltage for the positive input signal at J1.

3.1.1.4 Clock Inputs

The EVM provides separate inputs for the ADC clock and output buffer clock. This allows the user to send a modified version of the ADC clock (inverted, delayed, etc.) with the output data to generate the required setup and hold times for the users interface. The ADC clock input is SMA connector J4 with 50-Ω termination. The buffered output clock input is SMA connector J14 with 50-Ω termination. The clock inputs should be 50-Ω square wave signals, 3.3 V referenced to ground, with a duty cycle of 50 ±5%. The EVM can operate with only one clock input by installing SJP4 and SJP5, and removing R34. Since the input clock will now be terminated at both loads, the clock signal amplitude should be adjusted to provide the appropriate levels at the loads.

3.1.1.5 Control Inputs

The THS1040 has two discrete inputs to control the operation of the device. Table 3–1 describes the operation of the EVM jumpers for THS1040 operation.

Table 3–1. THS1040 Jumper Settings for Control Inputs

Jumper	Function	Location: Pins 1–2	Location: Pins 2–3
W3	Power down select	Operate mode	Power down mode
W4	Output enable select	Data bus 3-state	Data bus enabled

The THS1041 has three internal control registers that put the device into various modes of operation (see data sheet). Writing to the registers is accomplished on the EVM by using the two banks of DIL switches S2 and S3 and reset switch S1. A write operation to the THS1041 is performed as follows:

1) Set the DIL switches to the value to be programmed into the THS1041 registers. Each individual DIL switch is referenced to a register bit in either clamp register #1, clamp register #2, or the control register. DAC0 DIL switch through DAC7 DIL switch refers to bits 0–7 of clamp register #1. DAC8 and DAC9 DIL switches refer to bits 0 and 1 of clamp register #2. The DIL labels on S3 map directly to the control register. A DIL switch in the ON position represents a logic 1. Register bits 9 and 8 are automatically set by the PLD during programming.

2) Press and release the push button switch S1. All THS1041 registers are now programmed with the DIL switch values by the PLD.

Note:

After first application of power, the values of the DIL switches are automatically programmed into the THS1041 registers.

3.1.1.6 Clamp Interface

The THS1041 has a built-in clamp amplifier whose clamp input level can be driven from an external dc source (SMA connector J6) or from an internal high-precision 10-bit digital clamp level DAC, programmable via an internal clamp register. The clamp function is enabled by inputting a logic high level (AV_{DD}) input to SMA connector J5. The internal register is written to by the DIL switches and the PLD on the EVM. To enable the clamp interface, the following THS1041 internal control register bits and EVM jumpers must be configured as follows:

Table 3–2. THS1041 Internal Control Register Bits and EVM Jumpers

Clampout Source	Internal Register Bit CLINT	Internal Register Bit CLDIS	Jumper Table (Connection)
Clampin pin	0	0	SJP9 pin 1–2, SJP10 pin 1–2, W7 OUT, W8 OUT, W9 IN or W8 IN, W9 OUT
Internal DAC	1	0	

3.1.1.7 Programmable Gain Amplifier (PGA)

The THS1041 has a built-in 3-bit programmable gain amplifier operated by the internal control register. The gain range is from 0.5 to 4.0. See the data sheet for control register values used to select available gain settings.

3.1.2 References

In addition to the capability to configure the on-chip reference via jumpers, a reference circuit has been included on the EVM. This uses a 1.2-V shunt reference diode (U2) as its primary source, and allows adjustment of the REFT and REFB signals to the ADC using potentiometers R23 and R24, respectively. The ranges of the external reference signals are: REFT, 0.60 V to 2.68 V, REFB, 0 V to 1.79 V. See Chapter 4 for further details on the jumper settings required to use this mode.

3.1.3 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a 3.3-V analog supply (J8 and J7) and 3.3-V digital supply (J10 and J11). J9 and J16 are only used when reprogramming the PLD device (not required by the user).

3.1.4 Outputs

The data outputs from the ADC are buffered using SN74LVTH162244 before going to header J12. Header J12 is a standard 40-pin device on a 100-mil grid, and allows easy connection to a logic analyzer. The connector pinouts are listed in Table 3–1.

Table 3–3. Output Connector J4

J4 Pin	Description	J4 Pin	Description
1	Data bit 0 (LSB)	21	OVR
2	GND	22	GND
3	Data bit 1	23	
4	GND	24	GND
5	Data bit 2	25	
6	GND	26	GND
7	Data bit 3	27	
8	GND	28	GND
9	Data bit 4	29	
10	GND	30	GND
11	Data bit 5	31	
12	GND	32	GND
13	Data bit 6	33	
14	GND	34	GND
15	Data bit 7	35	
16	GND	36	GND
17	Data bit 8	37	
18	GND	38	GND
19	Data bit 9 (MSB)	39	CLK
20	GND	40	GND

Modes of Operation

The EVM can be easily configured, via jumper connections, to operate the THS1040/41 in various modes of operation. Figures 4–1 to 4–4 depict various modes of operation, with Table 4–1 listing the corresponding jumper settings. For further information on these modes of operation, refer to the relevant device data sheet.

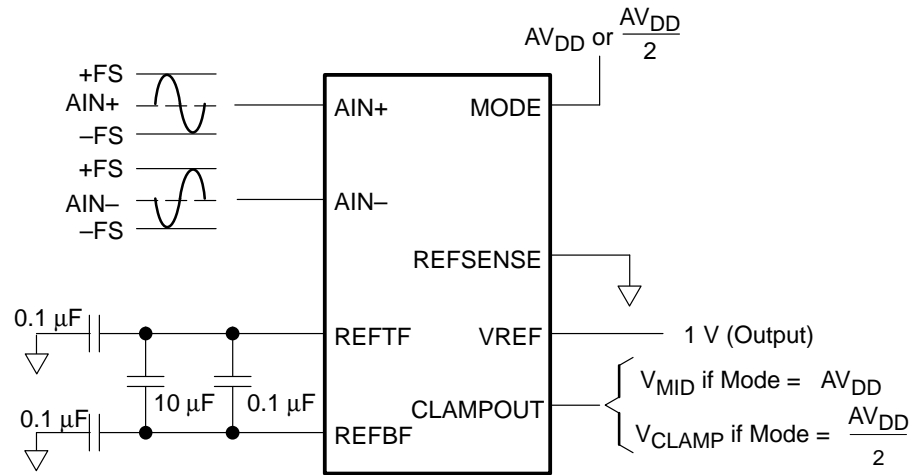*Figure 4–1. Differential Input, Internal Reference Mode, 1-V Reference Span*

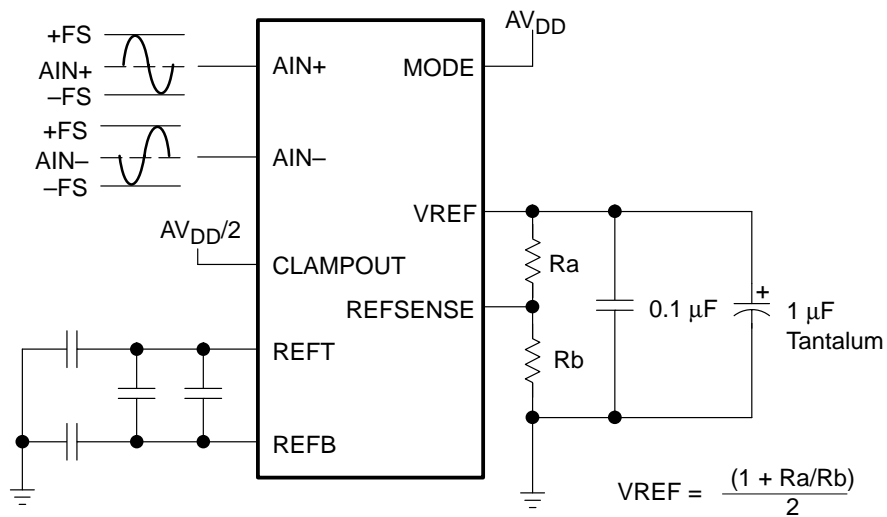*Figure 4–2. Differential Input, Internal Reference Mode, Adjustable Reference Span*

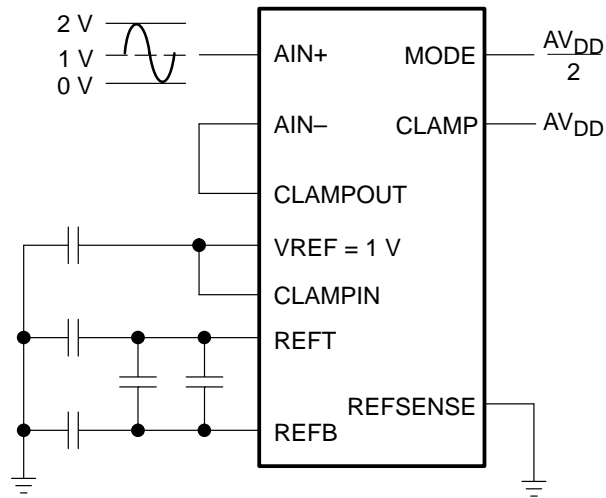Figure 4–3. Single-Ended Input, Internal ADC References

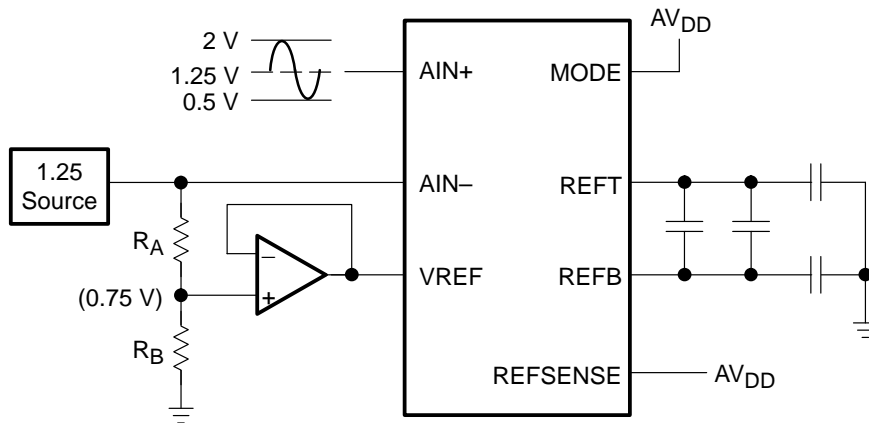Figure 4–4. Single-Ended Input, External VREF Source

Table 4–1. Board Jumper Settings for Various Modes of Operation

MODE	SJP1	SJP2	SJP3	SJP6	SJP9	SJP10	W1	W2	W5	W6	W7	W8	W9	W10	W11	W12	R14	R15	T1
Differential input, internal reference mode, 1-V reference span	OUT	1-2	OUT	1-2	OUT	OUT	1-2	1-2	1–2	OUT	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
Differential input, internal reference mode, 0.5 to 1-V reference span (adjustable)	OUT	1-2	OUT	1-2	OUT	OUT	1-2	1-2	OUT	OUT	IN	OUT	OUT	IN	OUT	OUT	IN	IN	IN
Sinlge-ended input, internal reference mode, 1-V reference span	IN	1-2	OUT	2-3	1–2†	1–2‡	2-3	OUT	1-2	OUT	OUT	IN	OUT	OUT	OUT	2–3‡	OUT	OUT	OUT
Sinlge-ended input, external VREF	IN	1-2	1-2§	2–3	OUT	OUT	OUT	OUT	2-3	OUT	IN	OUT	OUT	OUT	OUT	1–2 or 2–3	OUT	OUT	OUT
Differential input, internal reference mode, 0.5-V reference span	OUT	1-2	OUT	1-2	OUT	OUT	1-2	1-2	OUT	OUT	IN	OUT	OUT	IN	OUT	OUT	OUT	OUT	IN
Differential input, external reference mode	OUT	1-2	OUT	1-2	OUT	OUT	OUT	2-3	2-3	IN	OUT	OUT	IN	OUT	IN	OUT	OUT	OUT	IN

† Apply AVDD to J5
‡ Connect J15 to J6
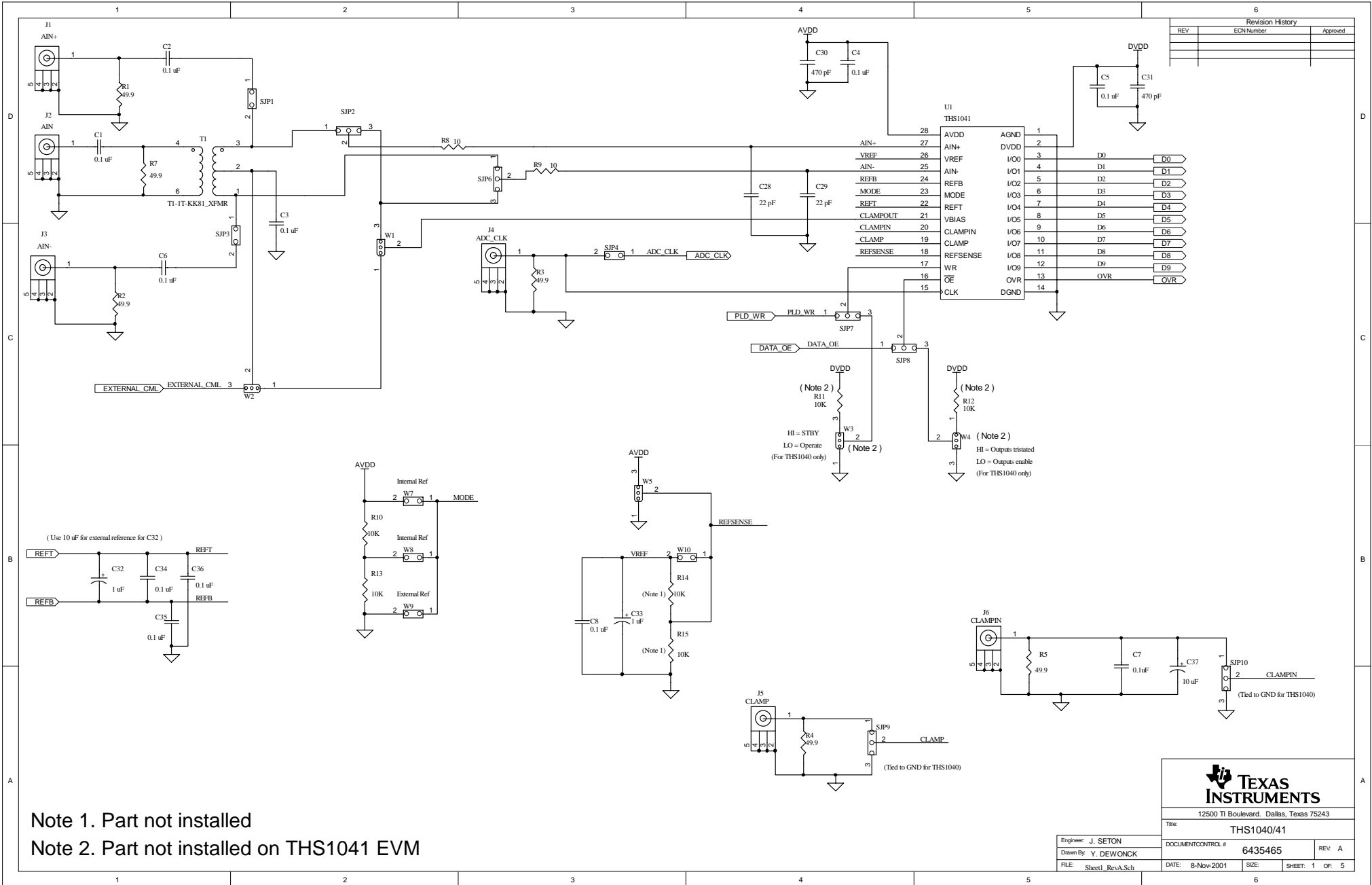§ C6 replaced with a short

Chapter 5

Schematics

This chapter contains the EVM schematic diagrams.

Figures 5–1 through 5–5 show the schematic diagram for the EVM.

Note 1. Part not installed

Note 2. Part not installed on THS1041 EVM

AVDD
R17 1K
R23 10K
AVDD
C41 0.1 uF
U3A
TLV2464CD
U3B
TLV2464CD
R25 432
C42 0.1uF
R27 330
E Q1 MMBT3906
B
C
TP1
W6
REFT
REFT (2.0V TYP)
U2 LT1004-1.2
R22 1.5K
C38 10uF
R30 15K
R29 5.1K
C40 10uF
C44 0.1uF
R32 180
TP3
EXTERNAL_CML
EXTERNAL_CML (1.5V TYP)
R24 10K
C46 10uF
U3C TLV2464CD
R33 11K
R16 10K
U3D TLV2464CD
R26 432
C45 0.1uF
R28 330
B Q2 MMBT3904
C
E
R31 180
TP2
C39 10uF
C43 0.1uF
W11
REFB
REFB (1.0V TYP)
R38 10K
C55 10uF
AVDD
C58 0.1 uF
U8A TLV2462D
R37 1K
C56 0.1uF
W12 EXTIO
E1 RED
J15
VREF
VREF
R39 730
R36 10K
C57 0.1uF

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title: THS1040/41
Engineer: J. SETON
Drawn By: Y. DEWONCK
DOCUMENTCONTROL # 6435465
REV. A
FILE:
DATE: 8-Nov-2001
SIZE:
SHEET: 2 OF: 5

+3.3VA-PS
ADC Analog Supply (+3.3V)
FB1
AVDD
J8 BANANA_JACK
J7 BANANA_JACK
C9 0.1 uF
C47 47 uF
C50 10uF
C10 0.1 uF

+5VD-PS
Digital Supply for Altera Byteblaster cable
FB2
+5V
J9 BANANA_JACK
J16 BANANA_JACK
C11 0.1 uF
C51 10uF
C12 0.1 uF
NOTE 1

+3.3VD-PS
ADC Digital Supply (+3.3V)
FB3
DVDD
J10 BANANA_JACK
J11 BANANA_JACK
C13 0.1 uF
C48 47 uF
C52 10uF
C14 0.1 uF

Altera Digital Supply (+3.3V)
FB4
VCC
C49 47 uF
C53 10uF
C15 0.1 uF

TP4 TP5 TP6

Note 1. Part not installed on THS1040 EVM

DATA OUT

DVDD

C16 0.1 uF C17 0.1 uF C18 0.1 uF C19 0.1 uF

U4
VCC /OE1 7
VCC /OE2 18
VCC /OE3 31
VCC /OE4 42

J12
40PIN_IDC

BD0 2 1Y1 1A1 47 D0 — LSB
BD1 3 1Y2 1A2 46 D1
BD2 5 1Y3 1A3 44 D2
BD3 6 1Y4 1A4 43 D3
BD4 8 2Y1 2A1 41 D4
BD5 9 2Y2 2A2 40 D5
BD6 11 2Y3 2A3 38 D6
BD7 12 2Y4 2A4 37 D7
BD8 13 3Y1 3A1 36 D8 — MSB
BD9 14 3Y2 3A2 35 D9
BOVR 16 3Y3 3A3 33 OVR

17 3Y4 3A4 32
19 4Y1 4A1 30
20 4Y2 4A2 29
PLD_CLK 22 4Y3 4A3 27
BCLK 23 4Y4 4A4 26

15 GND GND 34
45 GND GND 28
4 GND GND 10
39 GND GND 21

SN74LVTH162244DGG

J14
OUTPUT CLOCK
R34 0 BUF_CLK
SJP5
R6 49.9
ADC_CLK

(Note 2) DVDD
C20 0.1 uF C21 0.1 uF C22 0.1 uF C23 0.1 uF

U6
VCC /OE1 7
VCC /OE2 18
VCC /OE3 31
VCC /OE4 42

REG_OE

2 1Y1 1A1 47 R0
3 1Y2 1A2 46 R1
5 1Y3 1A3 44 R2
6 1Y4 1A4 43 R3
8 2Y1 2A1 41 R4
9 2Y2 2A2 40 R5
11 2Y3 2A3 38 R6
12 2Y4 2A4 37 R7
13 3Y1 3A1 36 R8
14 3Y2 3A2 35 R9

16 3Y3 3A3 33
17 3Y4 3A4 32
19 4Y1 4A1 30
20 4Y2 4A2 29
22 4Y3 4A3 27
23 4Y4 4A4 26

15 GND GND 34
45 GND GND 28
4 GND GND 10
39 GND GND 21

SN74LVTH16244ADGG
(Note 2)

(Note 2)
S1
VCC
C54 0.1 uF (Note 2)

U5
MR GND 1
GND 2
VDD RESET 3
TPS3801
(Note 2)

VCC
R41 4.7K
(NOTE 2)

DATA_OE — DATA_OE

(Note 2) +5V
R18 1K R19 1K R20 1K R21 1K

(Note 2)
J13
TCK 1 2
TDO 3 4
TMS 5 6
7 8
TDI 9 10
5X2X.1

(Note 2) R40 49.9
PLD_CLK
PLD_0 — PLD_0
PLD_1 — PLD_1

VCC

U7
EPM7032AETC44

I/O 34
I/O 35
GND 36
GCLK1/IN 37
OE1/IN 38
OE2/IN 39
I/O 40
I/O 41
I/O 42
I/O 43
I/O 44

R9 33 I/O I/O(TDI) 1 PLD_WR — PLD_WR
R8 32 I/O(TDO) I/O 2 PLD_2 — PLD_2
R7 31 I/O GND 3
R6 30 I/O I/O 4 PLD_3 — PLD_3
R5 29 VCC I/O 5 PLD_4 — PLD_4
28 I/O I/O 6
27 I/O VCC 7
R4 26 I/O(TCK) I/O(TMS) 8 PLD_5 — PLD_5
25 I/O I/O 9
R3 24 GND I/O 10 PLD_6 — PLD_6
23 I/O I/O 11 PLD_7 — PLD_7

22 21 20 19 18 17 16 15 14 13 12

(Note 2)

PLD_8 — PLD_8
PLD_9 — PLD_9
PLD_PGA_0 — PLD_PGA_0
PLD_PGA_1 — PLD_PGA_1

PLD_PGA_2 — PLD_PGA_2
PLD_PDWN — PLD_PDWN
PLD_CLINT — PLD_CLINT
PLD_TWOC — PLD_TWOC
PLD_CLDIS — PLD_CLDIS

VCC (Note 2)
C24 0.1 uF C25 0.1 uF C26 0.1 uF C27 0.1 uF

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title: THS1040/41
Engineer: J. SETON
Drawn By: Y. DEWONCK
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DATE: 8-Nov-2001 SIZE: SHEET: 4 OF. 5

Note 2. Part not installed on THS1040 EVM

TEXAS INSTRUMENTS

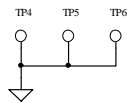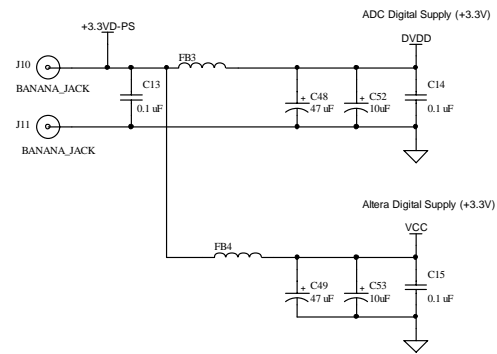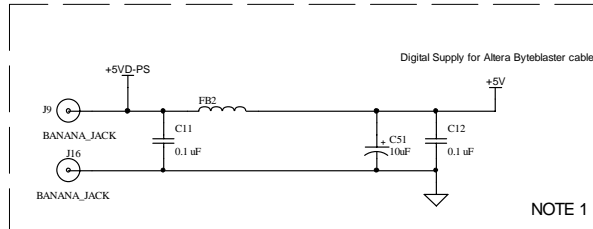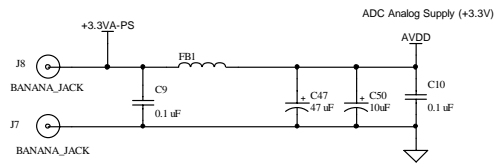12500 TI Boulevard. Dallas, Texas 75243

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