TEXAS INSTRUMENTS

DAC7731 Evaluation Module

User's Guide

March 2003

DAP EVMs

SLAU099

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage ranges specified in the EVM user's guide. The DC power supply for the digital section should not exceed +5 V. The DC power supply for the analog section should not exceed +15 V to –15 V. If used, the external reference voltage input should not exceed 10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the DAC7731 evaluation module. It covers all pertinent areas involved in properly using this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

Chapter 1—EVM Overview

Chapter 2—PCB Design and Performance

Chapter 3—EVM Operation

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Data Sheets:	**Literature Number:**
DAC7731	SBAS249
REF102	SBCS022
OPA627	SBOS165

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Chapter 1

EVM Overview

This chapter gives a general overview of the DAC7731 evaluation module (EVM) and describes some of the factors that must be considered when using the module.

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1.1 Features

This EVM features the DAC7731 digital-to-analog converter. The DAC7731EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the high resolution, single-channel, and serial input DAC. This EVM features a serial interface to communicate with any host microprocessor or TI DSP (with SPI capability) base system.

1.2 Power Requirements

The following sections describe the power requirements of the EVM.

1.2.1 Supply Voltage

The dc power-supply requirement for the digital section of the EVM is typically 5 V connected to the J3-1 or via J6-10 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J3-2 and J6-5 terminal. The dc power-supply requirement for the analog section (V_{CC} and V_{SS}) of this EVM range is from 15.75 V to -15.75 V maximum. The analog section connects through J1-3 and J1-1 respectively, or through J6-1 and J6-2 terminals and are referenced to analog ground through J1-2 and J6-6 terminals.

The V_{CC} supply source is also used to provide the positive rail of the external output op amp while the negative rail can be selected between V_{SS} and AGND via the W5 jumper. The external op amp is installed as an option to provide output signal conditioning or boost capacitive load drive and for other output mode requirements.

CAUTION

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

Although the DAC7731 has a built-in 10-V reference, an external reference circuit is provided in the EVM board. The external reference circuit can be isolated if the internal reference voltage is selected.

The 10-V precision voltage reference is provided to supply the external voltage reference for the DAC through REF102, U3, via jumper W4 by shorting pins 1 and 2. An adjustable 100-kΩ potentiometer, R11, is installed in series with 20 kΩ, R10, to allow the user to adjust the reference voltage to its desired settings. TP1 and TP2 are also provided, as well as J4-20, to allow the user to connect other external reference source if the onboard reference circuit is not desired. The external voltage reference must not exceed 10 V dc.

The REF102 precision reference is powered by V_{CC} (15 V) supply through J1-3 or J6-1 terminal.

The DAC7731 has a REFEN_ pin to enable the internal reference circuit or to disable it and select an external reference source. The REFEN_ pin can be hardware-driven through W2 jumper. Likewise, it can also be software-driven through J2-19 terminal via W2 jumper by shorting pins 1 and 2. The REF_{OUT} pin of the DAC7731 must be connected to the REF_{IN} pin to use the internal voltage reference. This can be done through W3 jumper by shorting pins 1 and 2. Shorting pins 2 and 3 of W3 selects the external voltage reference source.

The on-chip reference buffer output is channeled out through V_{REF} pin, which is used to set up the DAC7731 output amplifier into one of three voltage output modes (refer to the data sheet). V_{REF} can also be used to drive other system components that require external voltage reference.

When applying an external voltage reference through TP1 or J4-20, make sure that it does not exceed 10 V maximum. Otherwise, this can permanently damage the DAC7731, U1, device under test.

1.3 EVM Basic Functions

The DAC7731 EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC7731 digital-to-analog converter. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TI DSP (with SPI capability), or some sort of a waveform generator.

The headers J2 and P2 are the connectors provided which allow control signals and data required to interface a host processor or a waveform generator using a customized cable.

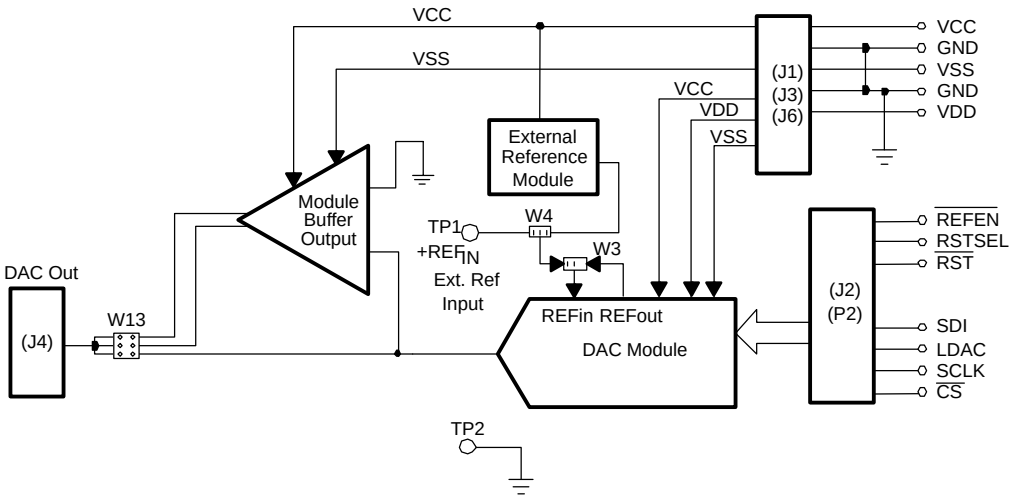
A specific adapter interface card is also available for most of TI's DSP starter kits (DSK) and the card model depends on the type of the TI DSP starter kit used. Specify the DSP with which you are interfacing to ensure acquiring the right adapter interface card. In addition, an MSP430 microprocessor-based motherboard platform is available for connection and interface with this EVM, provided a 5-V level shifter is used for stable operation. The 5-V level shifter is also available upon request. For more details or information regarding the adapters mentioned above or the MSP430 motherboard platform, call or email Texas Instruments. Use email address dataconvapps@list.ti.com for fast response.

The output of the DAC can be monitored via W13. The 6-pin header, W13, provides different options of the DAC output, but requires the output op amp, U2, to be configured correctly first for the desired waveform characteristic. Because of the headroom issue with the op amp, the reference voltage must be adjusted to prevent the output from clipping. If the internal reference voltage

of the DAC is used, then the output op amp can only be configured for unity gain. Shorting pins 1 and 2 of W13 allows the user to monitor the raw output of the DAC7731. The J4 header is also used to monitor the output signal through the external op amp for cascading or daisy-chaining up to three DAC7731 EVMs. This can be done by properly configuring the W13 header to route the DAC output of each respective EVM so that the output signal does not stack up on top of the other. Of course it is also possible to stack more than three EVMs as long as the W13 is left open and the output signal is monitored through this same header in each respective EVM.

A block diagram of the EVM is shown in Figure 1-1.

Figure 1-1. EVM Block Diagram



Chapter 2

PCB Design and Performance

The layout design of the PCB, describing the physical and mechanical characteristics of the EVM, is presented in this chapter. This section also shows the resulting performance of the EVM, which can be compared to the device specification listed in the data sheet. The list of components used on the module is also included in this section.

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2.1 PCB Layout

The DAC7731 EVM is designed to preserve the performance quality of the DAC under test, as specified in the data sheet. Carefully analyzing the EVM physical restrictions and knowing the elements that contribute to the EVM performance degradation are keys to a successful design implementation. These obvious EVM performance degraders can be alleviated during the schematic design phase by properly selecting the right components and building the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and knowing and understanding the components mechanical attributes.

The obscure part of the design is the layout process, where lack of knowledge and inexperience can present a problem. The main concern here is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals must be properly separated from each other. The power and ground plane is very important and are carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane does the job as well. When considering a split-plane design, analyze the component placement and carefully split the board into its analog and digital sections, starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contribute to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections—meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces, but maximize trace widths where possible in the design. This can be seen in the layout figures presented on the following pages.

The DAC7731 EVM board is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 42,8625 mm (1.6875 inch) $\times$ 80,9625 mm (3.1875 inch), and the board thickness is 1,57 mm (0.062 inch). Figure 2-1 through Figure 2-5 show the individual artwork layers.

Figure 2-1. Top Silkscreen

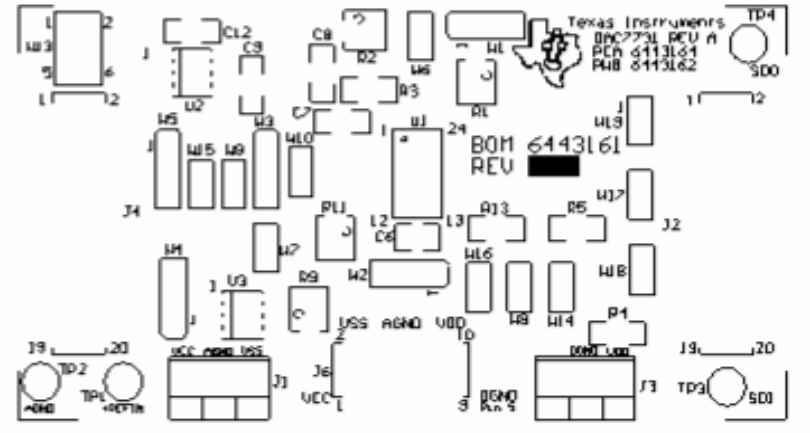


Figure 2-2. Layer 1 (Top Signal Plane)

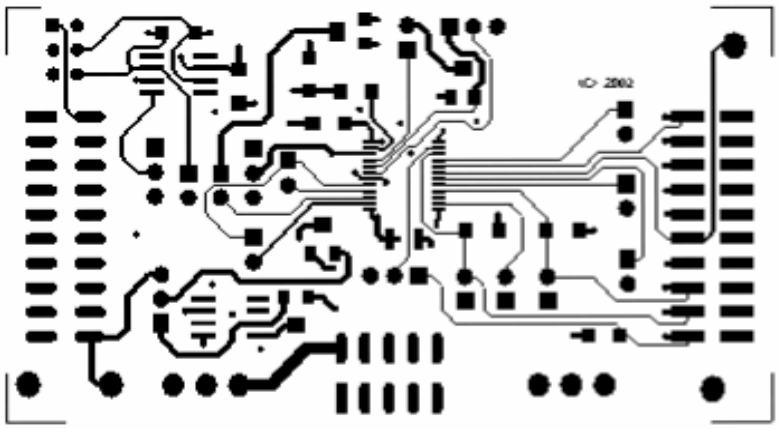


Figure 2-3. Layer 2 (Ground Plane)

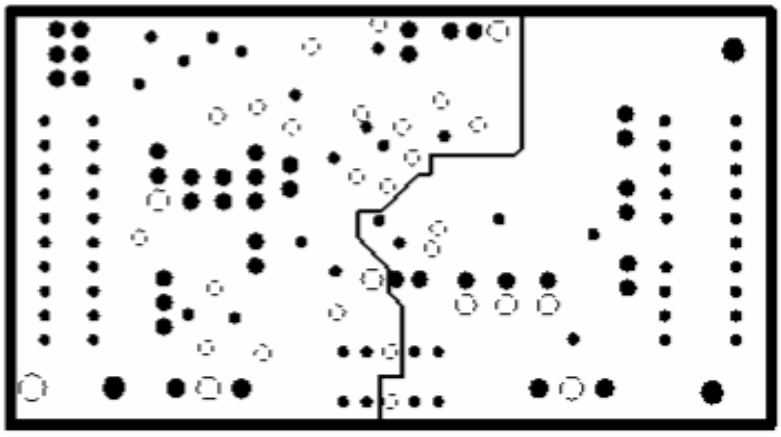


Figure 2-4. Layer 3 (Power Plane)

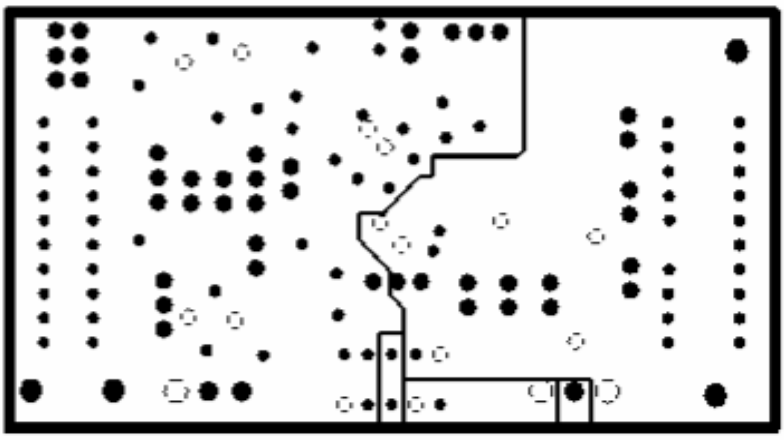


Figure 2-5. Layer 4 (Bottom Signal Plane)

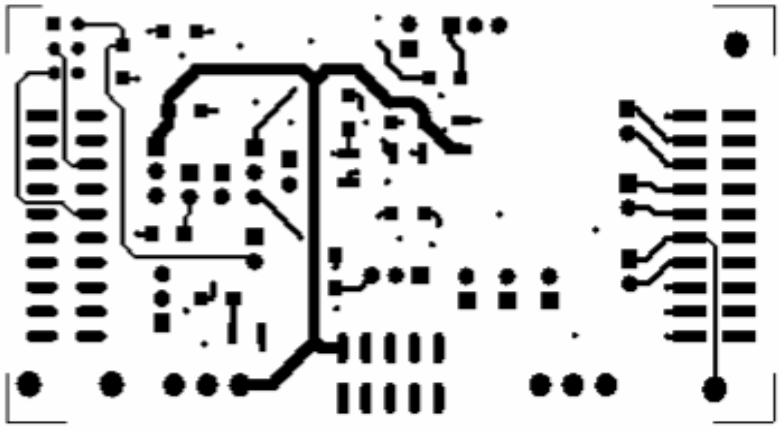


Figure 2-6. Bottom Silkscreen

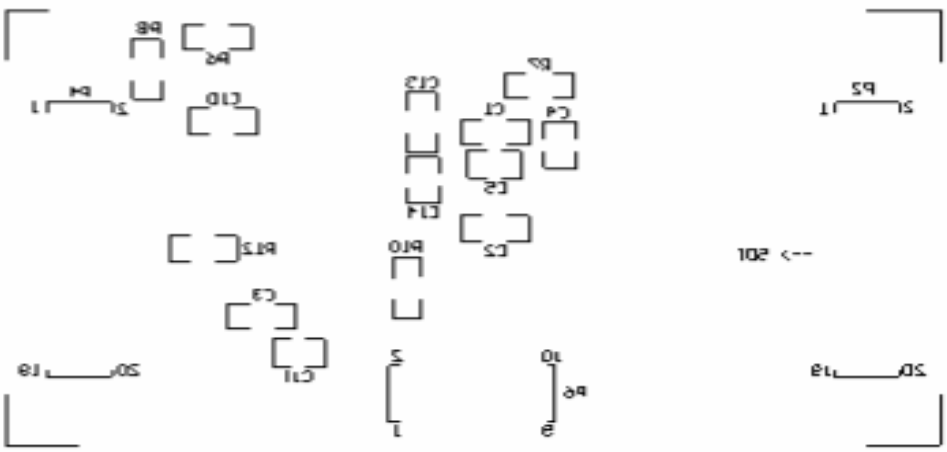
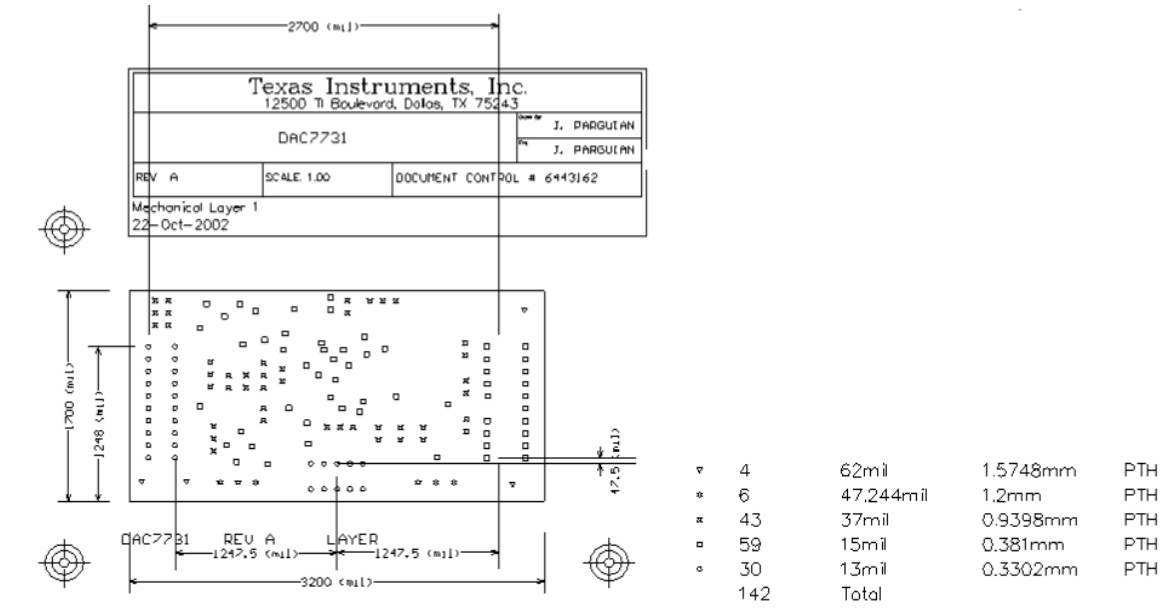


Figure 2-7. Drill Drawing



Notes:

1) PWB to be fabricated to meet or exceed IPC-6012, Class 3 standards and workmanship shall conform to IPC-A-600, Class 3—Current revisions
2) Board material and construction to be UL approved and marked on the finished board.
3) Laminate material: Copper-clad FR-4
4) Copper weight: 1 oz. finished
5) Finished thickness: 0.062 ± 0.010
6) MIN plating thickness in through holes 0.001”
7) SMCBC/HASL
8) LPI soldermask both sides using appropriate layer artwork: color = green
9) LPI silkscreen as required: color = white
10) Vender information to be incorporated on back side whenever possible
11) Minimum copper conductor width is 10 mils; minimum conductor spacing is 8 mils
12) Number of finished layers: 4

2.2 EVM Performance

The EVM performance test is conducted using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running the LABVIEW software. The EVM board is tested for all codes of 65535 and the device under test (DUT) is allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the INL and DNL results and is shown in Figure 2-9.

The parameters and results of the DAC7731 EVM characterization test can be seen in Figure 2-8 and Figure 2-9.

Figure 2-8. DAC7731EVM Test Parameters

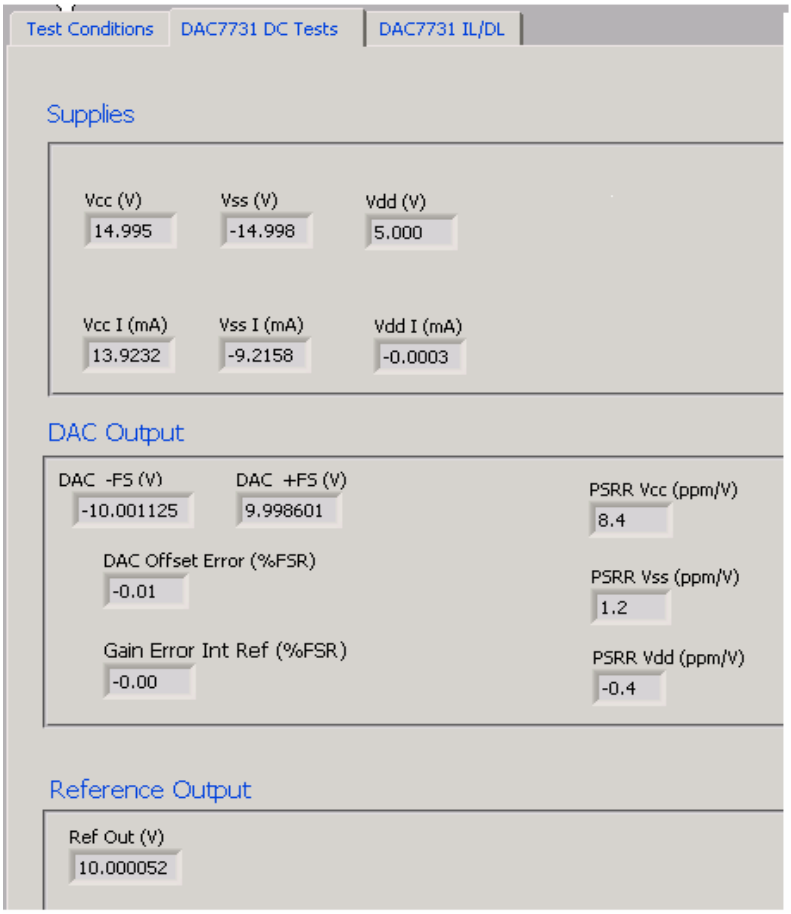
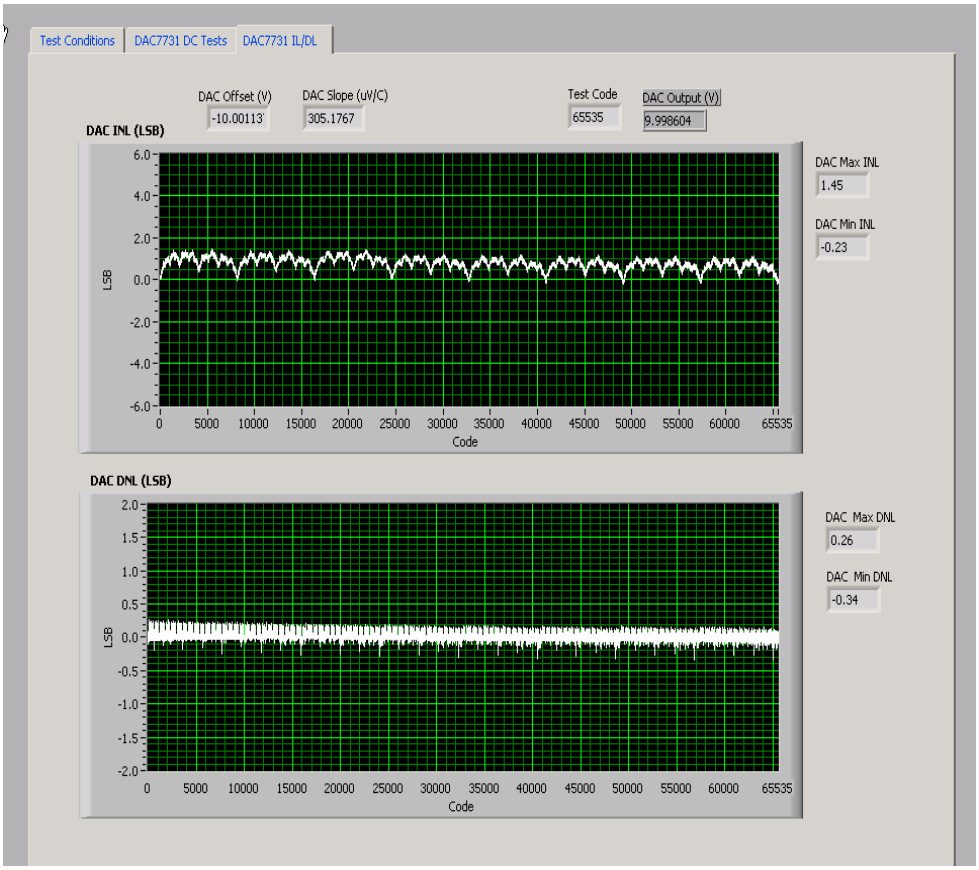


Figure 2-9. INL and DNL Characterization Graphs



2.3 Bill of Materials

Table 2-1. Parts Lists

Item #	Qty	Designator	Manufacturer	Part Number	Description
1	1	C8	Panasonic	ECUV1H105JCH	1 µF, 1206 Multilayer ceramic capacitor
2	2	C9 C10	Panasonic	ECUV1H103KBM	Ceramic capacitor
3	5	C1 C2 C3 C7 C13	Panasonic	ECJ3VB1C104K	Ceramic capacitor
4	1	C12	Panasonic	ECUV1H102JCH	Ceramic capacitor
5	5	C4 C5 C6 C11 C14	Kemet	C1210C106K8PAC	10 µF, 1210 Multilayer ceramic X5R capacitor
6	1	R8	Panasonic	ERJ-8GEY0R00V	0 Ω, 1/4W 1206 chip resistor
7	2	R7 R10	Panasonic	ERJ-8ENF2002V	Chip resistor
8	5	R4 R5 R6 R12 R13	Panasonic	ERJ-8ENF1002V	Chip resistor
9	2	R1 R2	Bourns	3214W-103E	10 kΩ, Bourns_32X4W series 5T Pot
10	1	R11	Bourns	3214W-104E	100 kΩ, Bourns_32X4W series 5T Pot
11	1	R3	Panasonic	ERJ-8GEYJ104V	Chip resistor
12	1	J6	Samtec	TSM-105-01-T-DV	5X2X0.1 10-pin 3A isolated power socket
13	2	J2 J4	Samtec	TSM-110-01-S-DV-M	10X2X.1, 20 Pin .025”sq SMT socket
14	2	J1 J3	On-Shore Technology	ED555/3DS	3-Pin terminal connector
15	1	U1	Texas Instruments	DAC7731	16-bit, voltage output, serial input DAC, SSOP-24
16	1	U2	Texas Instruments	OPA627AU	8-SOP(D) precision op amp
17	1	U3	Texas Instruments	REF102AU	+10 V , 8-SOP(D) precision voltage reference
18	4	TP1 TP2 TP3 TP4	Mill-max	2348-2-01-00-00-07-0	Turret terminal test point
19	1	W13	Samtec	TSW-103-07-L-D	3X2X0.1, 6-Pin IDC header
20	2	P2 P4 (see Note)	Samtec	SSW-110-22-S-D-VS-P	20 pin 0.025”sq SMT terminal strips
21	1	P6 (see Note)	Samtec	SSW-105-F-D-VS-K	3A Isolated 10-pin power header
22	11	W6 W7 W8 W9 W10 W14 W15 W16 W17 W18 W19	Molex	22-03-2021	2 Position jumper_ 0.1” spacing
23	5	W1 W2 W3 W4 W5	Molex	22-03-2031	3 Position jumper_ 0.1” spacing
24	1	R9	Bourns	3214W-203E	20 kΩ, Bourns_32X4W series 5T Pot

Note: P2, P4 & P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.

Chapter 3

EVM Operation

This chapter covers the detailed operation of the EVM to provide guidance to the user in evaluating the onboard DAC. It describes how to interface the EVM to a specific host processor.

Refer to the DAC7731 data sheet SBAS249 for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

Topic **Page**

3.1 Factory Default Settings

Factory default jumper settings for the EVM board are shown in Table 3-1. These settings allow the EVM to operate in bipolar, ±10 V mode of operation using the internal voltage reference.

Table 3-1. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	OPEN	V_{REF} output pin is floated and not used for offset adjustment.
W2	2-3	REFEN pin is tied to AGND to enable 10 V internal reference.
W3	1-2	REF_{OUT} pin is strapped to REF_{IN} to provide 10 V internal voltage reference.
W4	OPEN	Onboard external reference through U3 is disconnected.
W5	1-2	Negative supply rail of U2 op amp is supplied with –15 V.
W6	OPEN	REFADJ pin is floated.
W7	CLOSE	RFB2 pin is strapped to V_{OUT} pin for DAC output feedback.
W8	CLOSE	TEST pin is tied to DGND.
W9	OPEN	SJ pin is floated.
W10	OPEN	RFB1 is floated.
W13	3-4	Buffered output of DAC is channeled through to J4-6.
W14	OPEN	Reset pin is pulled high.
W15	OPEN	Configure U2 op amp for unity gain.
W16	OPEN	RSTSEL pin is tied high to set DAC reset value to mid-scale.
W17	OPEN	Not applicable. For DSP FS receive line use only.
W18	OPEN	Not applicable. For DSP data receive line use only.
W19	OPEN	Not applicable. For DSP clock receive line use only.

3.2 Host Processor Operation

The host processor basically drives the DAC, so proper DAC operation depends on the successful configuration of the host processor and the EVM board. In addition, properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through the J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector. An interface adapter card is also available for specific DSP starter kit, as well as an MSP430 motherboard as mentioned in Chapter 1 of this manual.

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. This is set to a unity gain configuration by default. Regardless, the raw output of the DAC can be probed through W13 pin 2 so that it can be compared with the output of U2 if necessary. The output terminal, J4, is provided mainly for mechanical stability when stacking or plugging into an interface card or the MSP430 motherboard. But it is also used to monitor the different output configuration of the DAC through U2 easily by shorting the respective pins of W13. In addition, it provides easy access for monitoring up to three DAC7731 EVMs in daisy chain or cascading fashion with the option of using U2 for each of the EVMs stacked together.

The following sections describe the different configurations of the output amplifier, U2.

3.2.1 Unity Gain Output

The buffered output configuration is used to prevent loading the DAC7731 and closely matches the raw output of the DAC with possible slight distortion because of the feedback resistor and capacitor. You can tailor the feedback circuit to closely match the desired wave shape by desoldering R7 and C11 and replacing with desired values. You can also remove R7 and C11 altogether, and solder a zero-ohm resistor in place of R7 if desired.

Table 3-2 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 3-2. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W5	2-3	1-2	Supplies the voltage for the negative rail of op amp.
W13	3-4	3-4	DAC output is channeled to the output terminal J4-6.
W15	Open	Open	Disconnect negative input of op amp from GND.

3.2.2 Output Gain of Two

This configuration allows the DAC output with a gain of two, but is limited to the effective rails of the operational amplifier. When the DAC7731 is configured to operate in bipolar mode, the DAC output must be within the range of 12 V_{P-P} or less. Anywhere above the range of 12 V_{P-P} clips the output of the op amp. Likewise, when operating the DAC in unipolar mode, the DAC output must not exceed 6 V_{P-P}.

Table 3-3 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 3-3. Gain of Two Output Jumper Settings

Reference	Setting	Function
W5	1-2 (Bipolar) 2-3 (Unipolar)	Negative rail of the op amp tied to -15 V for bipolar operation or AGND for unipolar operation.
W13	3-4	Amplified output of DAC is channeled to the output terminal J4-6
W15	Close	Configures op amp for a 2× gain output

3.2.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all op-amps under certain conditions can become unstable depending on the op-amp configuration, gain, and load value. These are just a few factors that can affect op-amps stability performance and should be considered when implementing.

In unity gain, the OPA627 op-amp, U2, performs very well with very large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and adding a load resistor further improves the capacitive load drive capability.

Table 3-4 shows the jumper setting configuration for a capacitive load drive.

Table 3-4. Capacitive Load Drive Output Jumper Settings

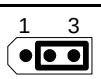
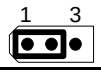
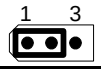
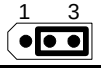
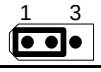
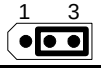
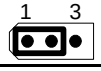
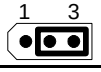
Reference	Setting	Function
W5	1-2 (Bipolar) 2-3 (Unipolar)	Negative rail of the op amp tied to -15 V for bipolar operation or AGND for unipolar operation.
W13	5-6	Capacitive load drive output of DAC is channeled to the output terminals
W15	Open	Disconnect R12 (see Note)

Note: If there is a need to incrementally adjust the capacitive load output, replace R12 with a capacitor having the desired capacitance value and close W15.

3.3 Jumper Setting

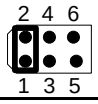
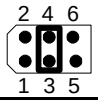
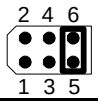
Table 3-5 shows the function of each jumper on the EVM.

Table 3-5. Jumper Setting Functions

Reference	Setting	Function
W1		R_{OFFSET} is strapped to V_{REF} to set V_{SJ} (summing junction) to $V_{REF}/2$. Refer to the data sheet for offset adjustment.
		R_{OFFSET} is not connected to set V_{SJ} (summing junction) to $V_{REF}/3$. Refer to the data sheet for offset adjustment.
		R_{OFFSET} is strapped to AGND to set V_{SJ} (summing junction) to $V_{REF}/6$. Refer to the data sheet for offset adjustment.
W2		Disables the internal reference voltage.
		Enables the internal reference voltage of 10 V.
W3		REFin is strapped to REFout to allow the internal 10 V to supply the DAC reference voltage.
		REFin is strapped to exREFin to allow either the onboard adjustable reference or user supplied reference to supply the DAC reference voltage.
W4		Routes the onboard 10 V reference through the adjustable pot to W3.
		Routes the user supplied reference from TP1 or J4-20 through the adjustable pot to W3.
W5		Negative supply rail of op amp is powered by V_{SS} for bipolar operation.
		Negative supply rail of op amp is tied to AGND for unipolar operation.
W6		REFadj pin is not connected.
		REFadj pin is connected to R1 pot for gain adjustment input when internal reference is used.
W7		RFB2 pin is not connected to the V_{OUT} pin.
		RFB2 pin is strapped to the V_{OUT} pin for feedback.
W8		TEST pin not connected to DGND.
		TEST pin connected to DGND (default mode).
W9		SJ (summing junction) pin of the DAC output amplifier is not connected.
		SJ (summing junction) pin of the DAC output amplifier is connected to R2 pot to allow small amount of current for offset adjustment.
W10		RFB1 pin is not connected.
		RFB1 pin is strapped to RFB2 pin for DAC V_{OUT} feedback.

Legend:  Indicates the corresponding pins that are shorted or closed.

Table 3-5. Jumper Setting Function(Continued)

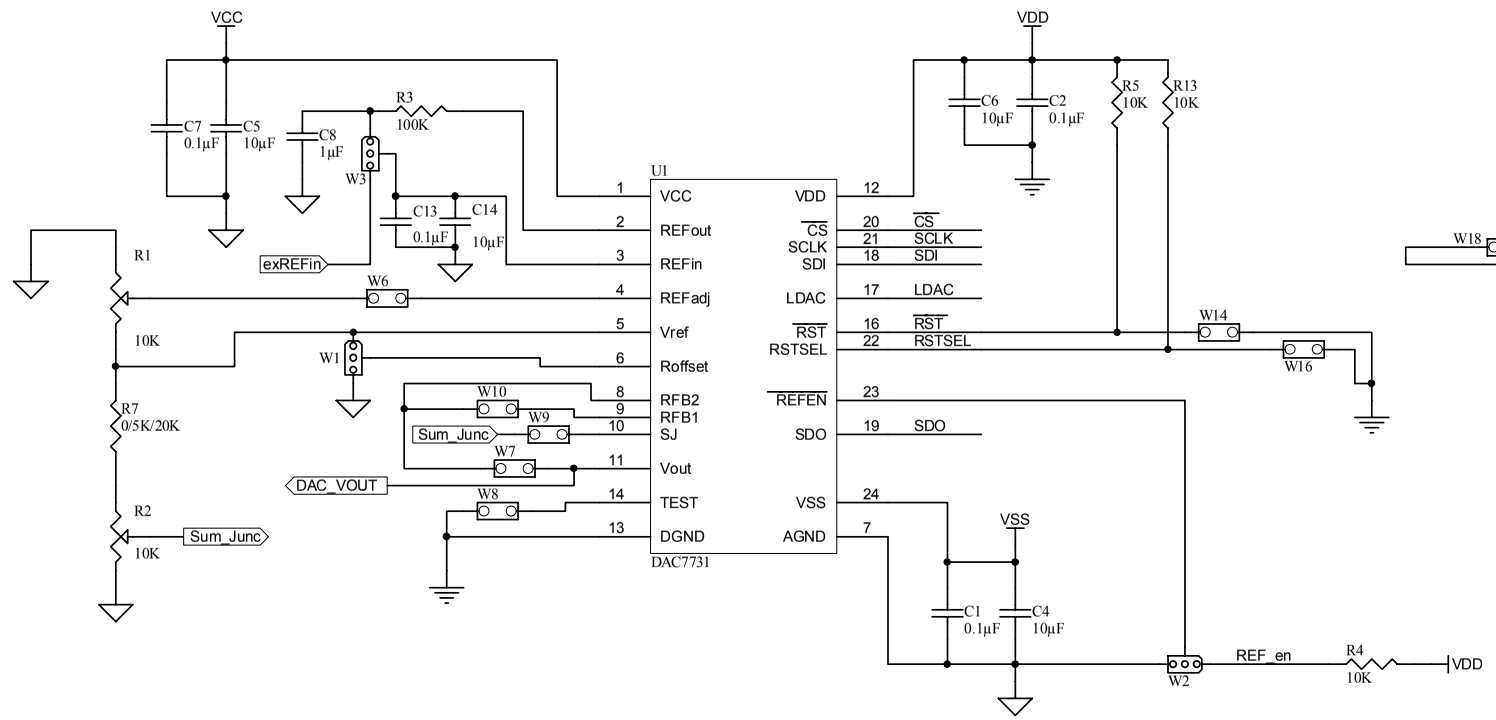
Reference	Setting	Function
W13		Routes the raw output of the DAC7731 to J4-2 output terminal.
		Routes the output of U2 to J4-6 output terminal. Used for unipolar and bipolar modes of operation.
		Routes the output of U2 to J4-10 output terminal. Used for capacitive load driving.
W14		Disconnects RST_ pin from DGND.
		Connects RST_ pin to DGND and forces a hard reset on the DAC7731.
W15		Disconnect the negative terminal of U2 to AGND and disable 2x gain.
		Configures U2 for a 2× gain output. Also used for capacitive driving configuration.
W16		RSTSEL pin is pulled high and configures the DAC to mid-scale when POR or reset is initiated.
		RSTSEL pin is pulled low and configures the DAC to min-scale when POR or reset is initiated.
W17		For use with DSP starter kit. Disconnects the FSX line from the FSR line (Default mode).
		For use with DSP starter kit. Loops the FSX line back to the FSR line.
W18		For use with DSP starter kit. Disconnects the DX line from the DR line (Default mode).
		For use with DSP starter kit. Loops the DX line to the DR line.
W19		For use with DSP starter kit. Disconnects the CLKX line from the CLKR line (Default mode).
		For use with DSP starter kit. Loops the CLKX line to the CLKR line.

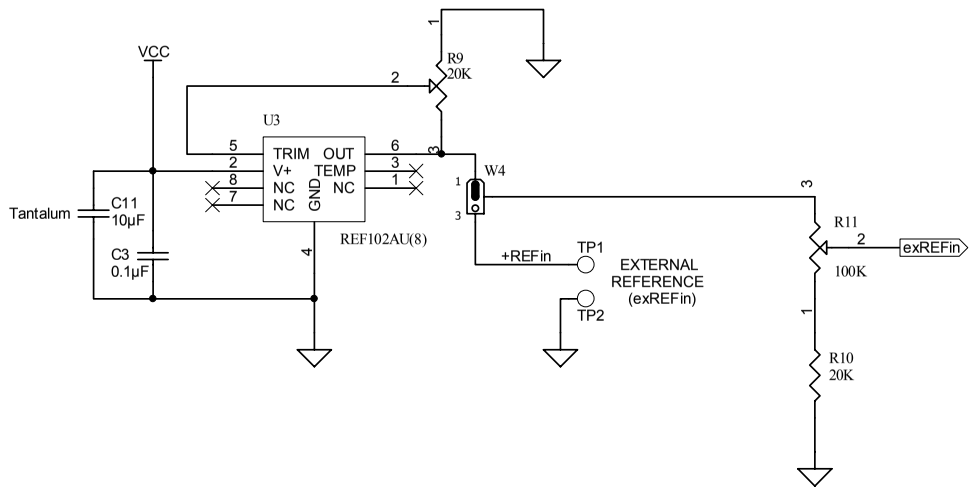
Legend:  Indicates the corresponding pins that are shorted or closed.

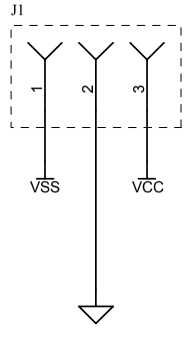
3.4 Schematics

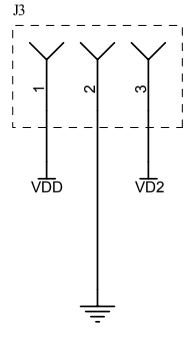
The B-size (11 in. X 17 in.) DAC7731EVM schematic is furnished as an attachment to this chapter.

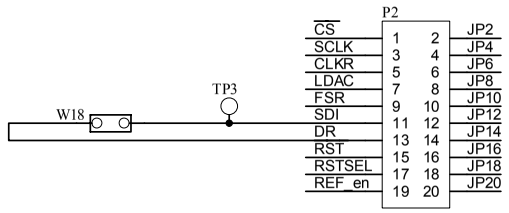
Revision History		
REV	ECN Number	Approved

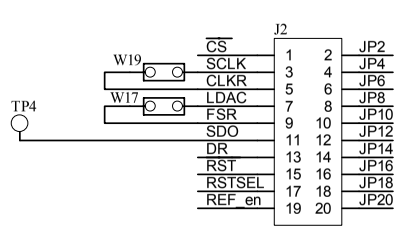


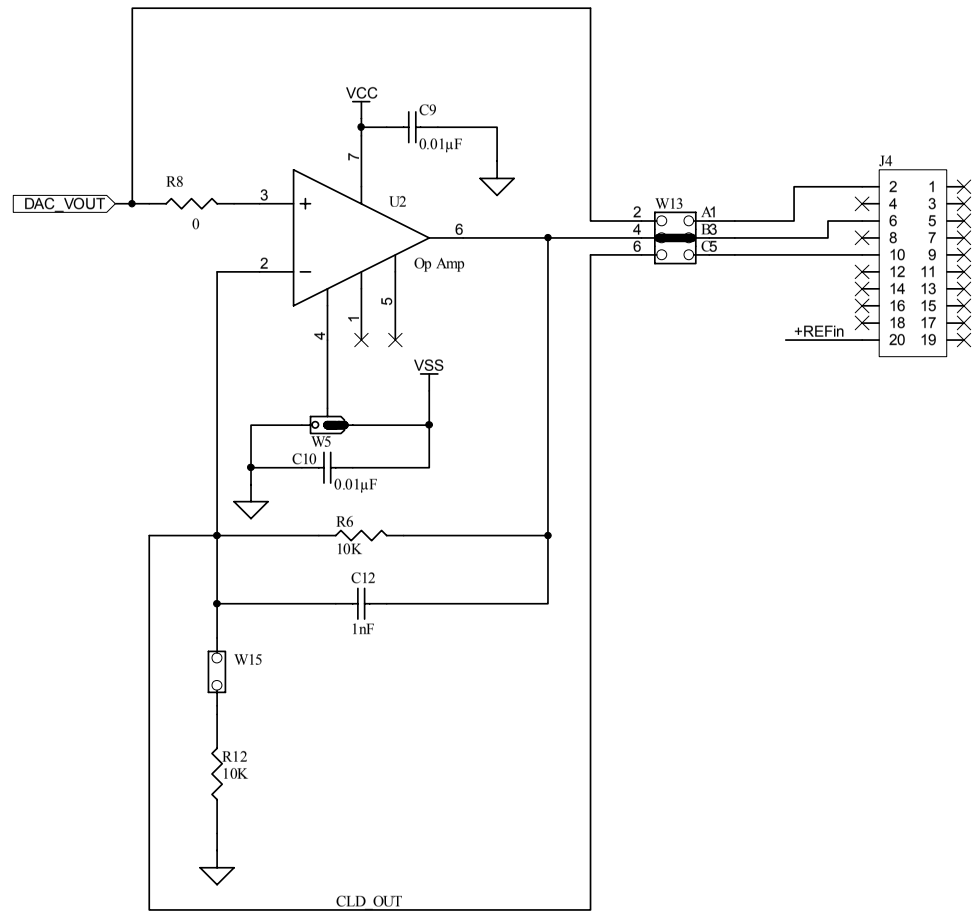












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