ADS1202 Modular EVM

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±125 mV and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 23°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS1202 Modular EVM. A complete circuit description as well as schematic diagram is included.

How to Use This Manual

This document contains the following chapters:

❑ Chapter 1—EVM Overview

❑ Chapter 2—Power Supply Options

❑ Chapter 3—EVM Operation

❑ Chapter 4—ADS1202 Modular EVM BOM and Schematic

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This book may contain cautions and warnings.

This is an example of a caution statement.

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Data Sheet:	**Literature Number:**
ADS1202	SBAS275

User's Guide:	**Literature Number:**
5‑6K Interface Board EVM	SLAU104

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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EVM Overview

The ADS1202 modular EVM provides direct modulator output to a host processor and allows all operating modes of the ADS1202. It provides various isolation options for a variety of applications.

The new modular EVM form factor allows for direct evaluation of the ADC's performance and operating characteristics. This EVM is compatible with the 5-6K Interface Board (SLAU104) from Texas Instruments.

❑ Direct modulator output

❑ Various isolation options

❑ Direct operation with a variety of DSK platforms from Texas Instruments

1.1 Analog Interface

The ADS1202 modular EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J1. Connector J1 provides access to the ADS1202 input pins. The modulator + input terminal is connected to pin 2, the - input terminal is connected to pin 4. Pins 1-19 are connected to analog ground.

1.2 Digital Interface

The ADS1202 modular EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J2. This header/socket combination provides access to the clock and data output pins of the ADS1202 Sigma Delta modulator.

Signal		Description
J2.1	Unused	
J2.3	SCLK	Serial clock input (for use with MODE 3 Operation)
J2.5	CLKR	Modulator clock output (for use with MODES 0, 1 and 2)
J2.7	Unused	
J2.9	Unused	
J2.11	Unused	
J2.13	SDO	Bit stream data output from ADS1202
J2.15	Unused	
J2.17	Unused	
J2.19	SPARE	

Power Supply Options

The ADS1202 modular EVM board requires 5-V dc for the ADS1202 circuit. When used in combination with the 5-6K interface boards, J5 (located on the bottom side of the PWB) provides connection to the common power bus described in document SLAU104. For isolated applications, J4 provides power to isolation components including optocouplers or LVDS drivers. For evaluation purposes, TP3 and TP4 can be shorted together to provide a common power source across the isolation boundary. Similarly, TP2 and TP6 can be shorted together to provide a common ground.

When used as a stand alone EVM, the ADS1202 power can be applied to J3. While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

EVM Operation

The analog input source can be applied directly to J1 pins 2 and 4. Series resistors R10 and R11 as well as capacitors C8, C9, and C10 provide filtering to the input of the ADS1202.

The digital control signals can be applied directly to J2 (top or bottom side). The ADS1202 modular EVM can also be connected directly to a DSP interface board.

Footprints are provided on the PWB which allow a variety of isolation options. Transformers, optoisolators or optocouplers may be installed for evaluation of different isolation techniques.
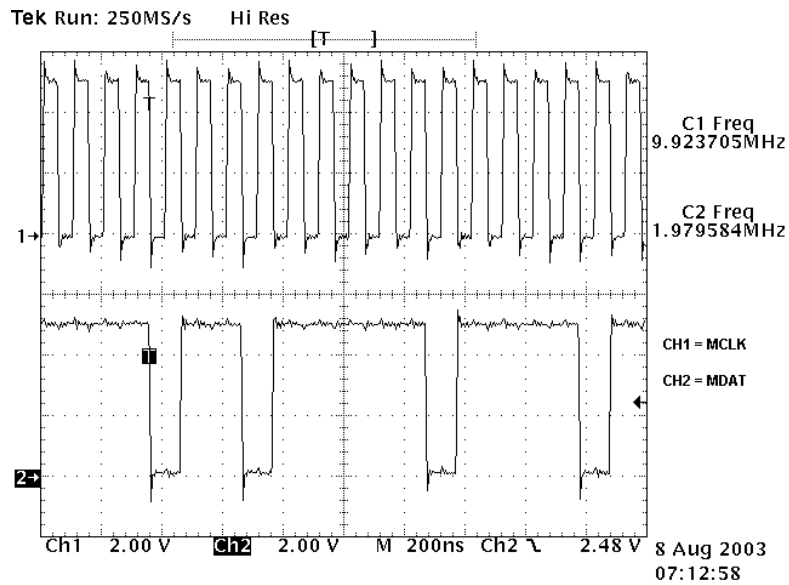
The EVM uses two *solder shorts* at position U3 to provide direct nonisolated operation of the ADS1202, for isolated operation, these shorts may be replaced with isolation devices such as the IL711 from NVE (close W3 pins 2‑3), HCPL‑2631 optocouplers (close W3 pins 1‑2) or transformer circuits such as those described in application note SLAA096.

The operating mode of the ADS1202 can be controlled by placing shunt jumpers on W1 and W2. When the jumper is open (not installed) logic 1 is applied to the mode pins. W1 controls M0, W2 controls M1. The EVM is configured with both W1 and W2 closed, providing Mode 0 operation.

Jumper		Description
W1	**W2**	
closed	closed	Mode 0 operation – processor reads MDAT on rising clock edge only
open	closed	Mode 1 operation – processor reads MDAT on *every* clock edge
closed	open	Mode 2 operation – Manchester decoding required
open	open	Mode 3 operation – requires external clock (optional - short TP1 to TP7)

To verify the ADS1202EVM is functional, arrange W1 and W2 for Mode 0 operation by ensuring the shunt jumpers are installed (factory default conditions). Apply 5-V power to the EVM through J3. Apply a 200-kHz sinusoidal wave (250 mV$_{PP}$) to J1.2 referenced to J1.4.

Using an oscilloscope view the MCLK and MDAT output signals on J2.5 and J2.13 respectively. The outputs should look similar to those in the following figure:

Tek Run: 250MS/s   Hi Res

C1 Freq
9.923705MHz

C2 Freq
1.979584MHz

CH1 = MCLK
CH2 = MDAT

Ch1 2.00 V   Ch2 2.00 V   M 200ns Ch2 ⌐ 2.48 V 8 Aug 2003
07:12:58

Slowly increase the time base of the oscilloscope. As the time base increases, the sine wave applied to the input terminals should begin to appear on the oscilloscope screen as shown below. These screen shots were taken using a Tektronics digital oscilloscope model TDS-754D set for *Hi Resolution* mode.

Tek Run: 50.0kS/s   Hi Res

C1 Freq
7.103825kHz
Low
resolution

C2 Freq
199.9265 Hz

CH1 = MCLK
CH2 = MDAT

Ch1 2.00 V   Ch2 2.00 V   M1.00ms Ch2 ⌐ 2.48 V 8 Aug 2003
07:14:07
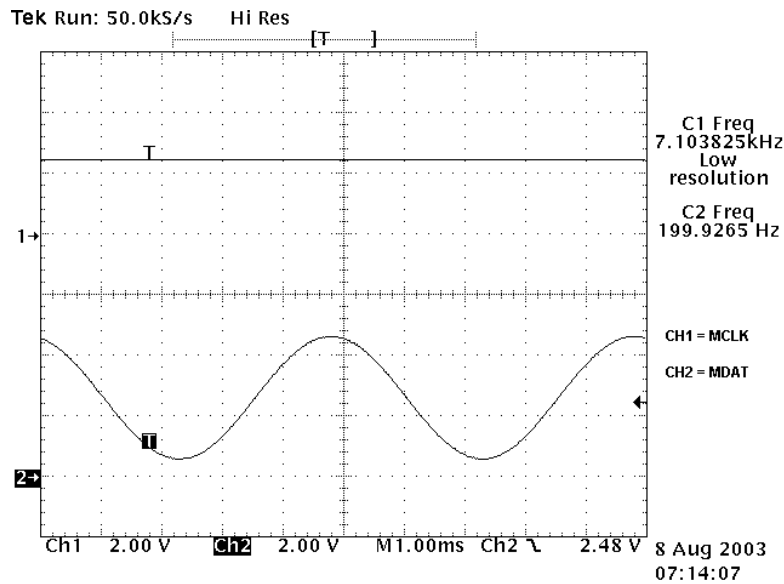
ADS1202 Modular EVM BOM and Schematic

This chapter contains the bill of materials and the schematic

4.1   ADS1202 Modular EVM BOM

The following table contains a complete bill of materials for the ADS1202 EVM.

Table 4‑1. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1, C8	1 nF, 0805, ceramic, NPO, 50 V, 5%	PhyComp	0805CG102J9B200
C2, C3, C4, C9, C10	0.1 µF, 0805, ceramic, X7R, 50 V, 10%	Panasonic	ECJ‑2YB1H104K
C5, C6	33 µF, 16V, Aluminum, Size C	Cornell Dubilier	AVS336M16C12T
C7, C8, C11‑C15	Not installed		
FB1, FB2	SMT, EMI beads, Z=47 Ω at 100 MHz	Fair‑Rite	2743019447
J1, J2 (top side)	10 Pin, dual row SMT header (20 positive)	Samtec	TSM‑110‑01‑T‑DV‑P
J1B, J2B (bottom side)	10 Pin, dual row, SMT socket (20 positive)	Samtec	SSW‑110‑22‑F‑D‑VS‑K
J3, J4	2 Terminal screw connector	OST	ED1514
J5 (bottom side)	4 Pin, dual row, TH header (8 positive.)	Samtec	SSW‑105‑22‑F‑D‑VS‑K
R1, R2	10 kΩ, 0805, 0.1 W resistor	Yageo America	9C08052A1002JLHFT
R3, R5, R10, R11	33 Ω, 0805, 5%, 0.1 W resistor	Yageo America	9C08052A33R0JLHFT
R4, R6‑R9, R12‑R16	Not installed		
TP1, TP3, TP4, TP5, TP7	Red test point loop	Keystone	5000
TP2, TP6	Black test point loop	Keystone	5001
U1	ADS1202	Texas Instruments	ADS1202
U2, U3	Not installed		
T1, T2	Not installed		
W1, W2	2 Pin header	Samtec	TSW‑102‑07‑L‑S
W3	3 Pin header (not installed)	Samtec	TSW‑103‑07‑L‑S

4.2 Schematic

The schematic diagrams are shown on the following pages.

+5Va

+Vd

J5
1 2
3 4
5 6
7 8
9 10

TP5

AVdd

C1 0.01uF   C2 0.1uF   R1 10K   R2 10K

W1   W2

ISO_Vd

R6 TBD   R7 TBD   C7 NI

ISO_GND

J1
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20

R10 33

R11 33

C8 1nF

C9 .1uF   C10 .1uF

U1
Vdd   8
M0   1
M1   4
MCLK   7
MDAT   6
GND   5
VIN+   2
VIN-   3
ADS1202

TP1 TP7

ISO_MCLK

R3 33   C11 0   MCLK   T1   R12 TBD
R4 SIT   R14 SIT

U2
Vcc   1
         8
         7
         3
         6
         5
GND   4
SN65LVDX34

ISO_MDAT

ISO_GND

R5 33   C12 0   MDAT   T2   R13 TBD

R8 TBD   R9 TBD

ISO_GND

J2
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20

ISO_GND

AVdd

TP4

J3
1
2
+5Va   FB1

C3 0.1uF   + C5 33uF

ISO_Vd

TP3

J4
1
2
FB2

C4 0.1uF   + C6 33uF

TP6   TP2

ISO_GND   ISO_GND

AVdd

C15 NI

U3
Vdd1   1
Vdd2   8
MCLK   2   7
MDAT   3   6
GND1   4
GND2   5
IL711

C16 NI

W3

AVdd

ISO_Vd

R15 TBD   R16 TBD

ISO_MCLK

ISO_MDAT

6

ISO_GND

TEXAS INSTRUMENTS

12500 TI Blvd. Dallas, Texas 75243

Title:
ADS1202 - miniEVM Schematic

Drawn By: Tom Hendrick
Engineer: Tom Hendrick
SIZE: B   DATE: 8-Aug-2003   REV: A
FILE: SHEET: 1 OF: 1