AD8509/8519 EVM User's Guide

Contents

List of Figures

List of Tables

1 Introduction

The AD8509 and AD8519 are complete 16-bit analog-to-digital (A/D) using state-of-the-art CMOS structures. They contain a complete 16-bit, capacitor-based, successive approximation register (SAR) A/D with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or can be synchronized to an external data clock. The AD8509 and AD8519 also provide an output synchronization pulse for ease of use with standard DSP processors. The EVM is available with either the AD8509 or AD8519 installed.

1.1 Features

- Full-Featured Evaluation Board for the AD8509 or AD8519, serial Analog to Digital Converters
- 4 V, 5 V, 10 V, ±3.3 V, ±5 V and ±10 V Analog Input Ranges
- Built in reference
- High-Speed Serial Interface
- Compatible with the 5-6K Interface Board for use with a variety of DSP Starter Kits as well as the HPA-MCU Interface

2 Analog Interface

For maximum flexibility, the AD8509/8519 EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 shows the pin out of the analog input connector, J1.

Table 1. Pinout of the Analog Input Connector, J1

Pin Number	Signal	Description
J1.2 thru J1.16 (even)	Analog Input	To accommodate EVM Stacking using the TAG feature of the data converter, jumper JP12 can be used in combination with J1 to choose one of eight analog input channels to the evaluation module.
J1.20	REF(+)J	External reference source input, accessible through JP6.
J1.15	REFOUT	Optional connection via JP6. Provides external AFE circuitry with REFOUT bias voltage.
J1.1- J1.19 (odd)	AGND	Analog ground connections. Note J1.15 is used for REFOUT connections to external AFE circuitry.

The analog front-end (AFE) circuitry found on the EVM consists of a simple RC filter. When used in combination with the 5-6K Interface Board, the circuits found on both DAP Signal Conditioning Boards (see SLAU105) provide the level shifting and amplifier configurations to realize single ended or bi-polar mode operation of the analog-to-digital converter installed on the EVM.

2.1 Analog Input Range Selection

Jumpers JP1 through JP5 provide a convenient way to choose the analog input range. JP1 controls the input connection to pin 1 (R1IN), JP2 controls the connection to pin 3 (R2IN) and JP3 controls the inputs on pins 4 and 5 (R3IN and CAP). Jumpers JP4 and JP5 provide connections to 33.2K resistors wired to the CAP pin and TRIM adjustment pot R6 (via JP5). Table 2 is representative of the input range selection.

Table 2. Input Range Selection(1)

Range	Without Trim					With Trim				
	JP1	JP2	JP3	JP4	JP5	JP1	JP2	JP3	JP4	JP5
0–10 V	5–6	1–2	5–6	1–2	2–3	5–6	1–2	5–6	1–2	1–2
0–5 V	5–6	5–6	1–2	1–2	2–3	5–6	5–6	1–2	1–2	1–2
0–4 V	1–2	5–6	1–2	2–3	2–3	1–2	5–6	1–2	2–3	1–2
±10 V	5–6	5–6	3–4	2–3	2–3	5–6	5–6	3–4	2–3	1–2
±5 V	1–2	1–2	3–4	1–2	2–3	1–2	1–2	3–4	1–2	1–2
±5 V	1–2	1–2	3–4	2–3	2–3	1–2	1–2	3–4	2–3	1–2

(1) For Offset Adjustment, close JP6 pins 5–6 and adjust R8 before trimming.

2.2 Optional Amplifier Input

Jumper JP7 provides access to an optional amplifier/buffer circuit on the front end of the data converter. Component U2 can be installed at the user's option with any standard 8 pin SOIC single amplifier component. The amplifier circuit is connected to the ±VA terminals for split supply operation. If single supply amplifiers are used, the –VA (J3 pin 2) can be tied to analog ground (J3 pin 6). The footprint for common 4mm trim pots (see component R11) is provided as an offset adjustment pot for single supply amplifiers. When used in conjunction with the 5-6K Interface Board, please be aware that the –VA supply is common to all power connectors (JP1 through JP6). Shorting the –VA supply to ground on the AD8509/8519 EVM is possible only if it is not used elsewhere on the interface board.

3 Digital Interface

The AD8509/8519 EVM is designed for easy interfacing to multiple control platforms. Jumper options are provided on the EVM to allow direct control over the serial clock source as well as the data output and TAG features.

The active low $\overline{CS0}$ pin is connected to J2 pin 1. This pin can be controlled through GPIO functions on the 5–6K Interface Board. For standalone operation, a shunt jumper can be placed between J2T pins 1 and 2 to tie $\overline{CS}$ to ground.

The DATA output from the EVM is applied to JP9. When the supplied shunt is on pins 1-2 (default state), the DATA output is fed to J2B (bottom side) pin 11. This is required when operating in the internal data clock mode, where the ADC supplies an SPI master clock to the host processor. Data is input to the SIMO pin of the host in this case. JP13 is provided as a means to return the ADC generated SPI clock to DSP host processors using the 5-6K Interface Board.

3.1 Using TAG Features via JP8, JP9, and JP10

JP8 controls the TAG function of the ADC. With the supplied shunt in position 1-2 (default state), TAG is grounded and the EVM is to be considered as either the only converter in the system, or the LAST converter in the data chain (see SBAA007 for additional details). When the shunt on JP8 is moved to position 2–3, data input to the TAG pin is fed from J2T (top side) pin 13. JP8 and JP9 must be in position 1-2 for the last converter in the chain and position 2–3 for all other devices when using the TAG feature. The TAG feature also requires the use of an external data clock. JP10 sets the EXT/INT pin high (external clock) when the pins are open (no shunt installed). The external data clock can be applied to J2 pin 3 (top or bottom side).

3.2 Additional Digital Control and Monitoring

As mentioned previously, JP10 controls the selection of the internal or external data clock. When JP10 is closed (default) the ADC generates a low dwelling burst mode clock that allows the user to read valid data on either the rising or falling edge. Removing the shunt from JP10 requires an external data clock applied to J2 pin 3 (top or bottom side) to produce a data output stream. JP11 controls the data format; when closed (default) the DATA output pin provides a Binary Twos Complement data stream. Opening JP11 provides a straight binary output of the conversion results. JP14 controls the device power down function. Opening JP14 applies a logic high to the PWRD pin, shutting down the ADC.

Test points TP4 and TP6 provide access to the SYNC and BUSY signals respectively. These can be monitored by referencing an oscilloscope to TP5, digital ground (labeled DGND). The applied digital voltage can be monitored at TP3. Analog signals and the applied VANA voltage can be monitored at TP2 (+5V) referenced to TP1 (AGND).

4 Power Supplies

The AD8509/8519 EVM board requires +5V DC for both the analog and digital sections of the ADC. Power to the ADC is sourced from J3 pin 3 and pin 10 (+5VA and +5VD - see Table 3).

NOTE: VDIG must be less than or equal to VANA.

Table 3 shows the pin out of J3.

Table 3. Pinout of J3

Signal	Pin Number		Signal
+VA	1	2	-VA
+5VA	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
Unused	9	10	+5VD

For stand alone operation, power sources can be applied via various test points located on the EVM (VANA to TP2 and VDIG to TP3). Refer to the schematic at the end of this document for details.

The option amplifier located at position U2 (user supplied) can be powered through J3 pins 1 and 2.

NOTE: While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

4.1 Reference Voltage control via JP6

The AD8509/8519 is normally configured to use its internal reference. Jumper JP6 provides various options to allow the EVM user to send the converter's reference voltage off board to external amplifier circuits (JP6 pins 3-4, default state). An external reference source applied to J1 pin 20 can be sent to the ADC by moving the shunt at JP6 to pins 1-2. An on board trim pot is provided at R8, and can be used with a shunt jumper placed on JP6 pins 5–6.

5 EVM Operation

The max analog input swing is ±10V_{PP}. The input range can be adjusted directly on the EVM by configuring jumpers JP1 through JP5, with offset trim capability using JP6. The EVM is set for the 0-10V input range by default with the serial data stream supplied by the internal clock. Offset trim can be accomplished on board via R8 or through an external input through J1. Single amplifier U2 in an industry standard SOIC 8 package can be installed to do on board signal conditioning if necessary. Refer to Section 12 of Op Amps for Everyone (Doc. No. SLOD006) for information on various circuit applications.

Once power is applied to the EVM, the analog input source can be connected directly to J1 (top or bottom side) or through optional amplifier and signal conditioning modules using the 5-6K Interface Board. Jumper JP12 allows the EVM user to choose which analog signal applied to J1 is directed to the input of the ADC, providing the ability to stack up to eight AD8509/8519 EVM's using the TAG features of the device. When using the TAG feature, be sure to set the jumpers according to section 2.1 of this Users Guide.

The digital control signals can be applied directly to J2 (top or bottom side). The AD8509/8519 EVM can also be connected directly to the 5-6K Interface Board for use with a variety of C5000 and C6000 series DSP Starter Kits (DSK). The analog and digital input connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon type cables on 0.1" centers.

No specific evaluation software is provided with this EVM, however, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments Incorporated. Check the product folders for a listing of available code examples. The EVM Gerber files are available on request.

Table 4 shows the factory default jumper locations for the AD8509/8519 EVM:

Table 4. Factory Default Jumper Locations

Jumper	Function	Default Condition
JP1	Controls application of the applied analog signal to R1IN	5–6
JP2	Controls application of the applied analog signal to R2IN	1–2
JP3	Controls application of the applied analog signal to R3IN	5–6
JP4	Controls connection of 33.2 kΩ resistors to the CAP pin and TRIM pot	1–2
JP5	Controls connection of 33.2 kΩ resistors to the CAP pin and TRIM pot	2–3
JP6	Controls the application of the reference voltage	3–4
JP7	Controls the application of optional signal conditioning circuitry	1–2
JP8	Controls the TAG feature	1–2
JP9	Controls the application of the DOUT data stream	1–2
JP10	Controls the EXT/INT clock pin	CLOSED
JP11	Controls the SB/BTC data format pin	CLOSED
JP12	Used to select an analog input channel when used with DAP Signal Conditioning Boards	1–2
JP13	Controls the application of clock return for DSP receiver operations	CLOSED
JP14	Controls the PWRD function	CLOSED

6 EVM Bill of Materials and Schematic

Table 5 contains a complete Bill of Materials for the AD8509/8519EVM. The schematic diagram is also provided for reference.

Table 5. Bill of Materials

Item	Qty.		Designators	Description	Manufacturer	Mfg. Part Number
	ADS8509	ADS8519				
1	1	1	N/A	Printed Wiring Board	Texas Instruments	6465120
2	1	1	C1	2200pF Ceramic, 0603,C0G, 50V, 5%	TDK	C1608C0G1H222J
3	2	2	C2 C9	2.2uF Ceramic, 0805, X5R, 10V, 10%	TDK	C2012X5R1A225K/0.85
4	3	3	C4 C5 C7	10uF Ceramic, 0805, X5R, 16V, 20%	TDK	C2012X5R1C106M
	1	0	C3	10uF Ceramic, 0805, X5R, 16V, 20%	TDK	C2012X5R1C106M
5	2	2	C6 C12	0.1uF Ceramic, 0603, X7R, 25V, 20%	TDK	C1608X7R1E104K
6	2	2	C8 C13	0.01uF Ceramic, X7R, 50V	TDK	C1608X7R1H103K
	0	0	C10 C11	Not Installed		
7	2	2	FB1 FB2	73 SM BEAD	Fair-Rite	2773044447L
8	2	2	J1 J2 (top side)	10 Pin, Dual Row, SMT Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
9	2	2	J1B J2B (bottom side)	10 Pin, Dual Row, SMT Socket (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
10	1	1	J3 (top side)	5 Pin, Dual Row, SMT Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
11	1	1	J3 (bottom side)	5 Pin, Dual Row, SMT Socket (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
12	4	4	JP1 JP2 JP3 JP6	3 Pin, dual row header (6 pos)	Samtec	TSW-103-07-L-D
13	2	0	JP4 JP5	3 Pin, single row header	Samtec	TSW-103-07-L-S
	3	3	JP7 JP8 JP9	3 Pin, single row header	Samtec	TSW-103-07-L-S
14	4	4	JP10 JP11 JP13 JP14	2 Pin header	Samtec	TSW-102-07-L-S
15	1	1	JP12	8 Pin, dual row, 2mm header (16 pos)	Samtec	TMM-108-02-L-D
16	2	2	R1 R4	100 Ohm, 0603, 1%, 1/10W	Yageo America	RC0603FR-07100RL
17	1	1	R2	576k Ohm, 0603, 1%, 1/10W	Yageo America	RC0603FR-07576KL
18	2	0	R3 R5	33.2k Ohm, 0603, 1%, 1/10W	Yageo America	RC0603FR-0733K2L
19	1	0	R6	50k, SMT Trim Pot, 4mm	Bourns	3214W-1-503E
	1	1	R8	50k, SMT Trim Pot, 4mm	Bourns	3214W-1-503E
20	1	0	R7	200 Ohm, 0603, 1%, 1/10W	Yageo America	RC0603FR-07200RL
21	1	1	R9	0 Ohm, 0603, 5%, 1/10W	Yageo America	RC0603JR-070RL
22	0	0	R10 R11 R16 R17	Not Installed		
23	3	3	R12 R13 R14	10K ohm, 0603, 1%, 1/10W	Yageo America	RC0603FR-0710KL
24	1	1	R15	33.0 ohm, 0603, 1%, 1/10W	Yageo America	RC0603FR-0733RL
25	4	4	TP2 TP3 TP4 TP6	Red Test Point Loop	Keystone	5000
26	2	2	TP1 TP5	Black Test Point Loop	Keystone	5001
27	1	0	U1	ADS8509 16BIT 250KSPS SRL 28-SSOP	Texas Instruments	ADS8509IBDBR
	0	1		ADS8519 16BIT 250KSPS SAMP 28-SSOP	Texas Instruments	ADS8519IBDBR
28	0	0	U2	Not Installed		
29	13	11	Shunt for items 12,13, 14	0.1" Econ. Shunt - Black	Samtec	SNT-100-BK-T
30	1	1	Shunt for item 15	2mm Econ. Shunt - Black	Samtec	2SN-BK-G

7 Related Documentation from Texas Instruments

Table 6. EVM Compatible Device Data Sheets, Users Guides and Additional Resources

Data Sheet	**Literature Number**
AD8519	SLAS462
AD8509	SLAS324
Users Guides	**Literature Number**
5-6K Interface Board	SLAU104
DAP Signal Conditioning Boards	SLAU105
Additional Resources	**Literature Number**
Op Amps for Everyone	SLOD006
AD8509 TAG Features	SBAA007

Revision History		
REV	ECN Number	Approved
1	Prototype	TH
A	Initial Release	TH
B	Update U1 footprint	TH

RANGE	W/O TRIM					W/TRIM				
	JP1	JP2	JP3	JP4	JP5	JP1	JP2	JP3	JP4	JP5
0-10V	5-6	1-2	5-6	1-2	2-3	5-6	1-2	5-6	1-2	1-2
0-5V	5-6	5-6	1-2	1-2	2-3	5-6	5-6	1-2	1-2	1-2
0-4V	1-2	5-6	1-2	2-3	2-3	1-2	5-6	1-2	2-3	1-2
+/-10V	1-2	5-6	3-4	2-3	2-3	1-2	5-6	3-4	2-3	1-2
+/-5V	5-6	1-2	3-4	1-2	2-3	5-6	1-2	3-4	1-2	1-2
+/-3V	1-2	1-2	3-4	2-3	2-3	1-2	1-2	3-4	2-3	1-2

FOR OFFSET ADJUST, MOVE JP6 to position 5-6

Operating Modes:
Internal Clock (SPI Master) - JP10 Closed, JP8 1-2, JP9 1-2
External Clock (No TAG) - JP10 Open, JP8 1-2, JP9 2-3
External Clock (W/ TAG) - JP10 Open, JP8 2-3 (1-2 Last Board), JP9 2-3

	ADS8509	ADS8519
R3	33.2k	NI
R4	100	0
R5	33.2k	NI
R6	50k	NI
R7	200	0
C3	10uF	NI
JP4	INSTALLED	NI
JP5	INSTALLED	NI

TEXAS INSTRUMENTS
12500 TI Blvd. Dallas, Texas 75243

Title: ADS8509/19 Evaluation Module Schematic			
Drawn By: Tom Hendrick			
Engineer: Tom Hendrick	SIZE: B	DATE: 26-Aug-2009	REV: B
FILE: EDGE #6465121			SHEET: 1 OF: 1

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It is important to operate this EVM within the input voltage range of –10 V to +10 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30 C. The EVM is designed to operate properly with certain components above 60 C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
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