DAC7558 Evaluation Module

This user's guide describes the characteristics, operation, and use of the DAC7558 Evaluation Module. It includes all pertinent information to properly use this EVM board and the devices supported by the EVM. The physical PCB layout, schematic diagram, and circuit descriptions are included.

Contents

List of Figures

List of Tables

1 EVM Overview

This chapter includes a general overview of the DAC7558 evaluation module (EVM) and describes some of the factors that must be considered in using this module.

1.1 Features

This EVM features the DAC7558 digital-to-analog converter. The DAC7558 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the 12-bit resolution, octal-channel and serial input DAC. This EVM features an ultra-low glitch, voltage output with superior linearity and monotonicity. The serial interface of this DAC can communicate with any host microprocessor or TI DSP based system.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The DC analog power supply requirement for the DAC7558 EVM (V_{DD} and IOV_{DD}) is selectable between +3.3 V and +5 V via jumper headers, W1 and W2 respectively. The +3.3 V is supplied from the J6-8 or J5-1 terminals (if installed), and the +5 V is supplied from the J6-3 or J5-3 terminals (if installed), when plugged in via a 5-6k adapter interface card or the HPA449. These power supply voltages are referenced to ground through the J6-6 terminal. V_{CC} and V_{SS} are only used by the U2 op-amp, which ranges from +15 V to –15 V maximum and connects through the J1-3 and J1-1 terminals respectively (if installed), or through the J6-1 and J6-2 terminals. All of the analog power supplies are referenced to analog ground through the J1-2 and J6-6 terminals.

The negative rail of the output op-amp, U2, can be selected between V_{SS} and AGND via the W5 jumper. The external op-amp is installed as an option to provide output signal conditioning or for other output mode requirements.

CAUTION

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The +4.096-V precision voltage reference is provided to supply the external voltage reference and sets the voltage output range of the DAC under test through REF3140, U3, via an 8-pin jumper, J7, by shorting pins 1-2, 3-4, 5-6, and 7-8. The test point TP4 as well as J4-20 are also provided to allow the user to connect to an external reference source if use of the onboard reference circuit is not desired. If different reference voltages are required for each DAC reference, then they must be connected directly to the even pins of J7. The external voltage reference should not exceed the applied power supply, V_{DD}, of the DAC under test.

The REF3140 precision reference is powered by +5 VA through the J6-3 or J5-3 terminal (if installed).

CAUTION

When applying an external voltage reference through TP4 or J4-20, make sure that it does not exceed the DAC7558 power supply (V_{DD}) maximum. Otherwise, this can permanently damage the DAC7558, U1, device under test.

1.3 EVM Basic Functions

The DAC7558 EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC7558 digital-to-analog converter. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TI DSP, or various waveform generator.

The headers J2 and P2 are connectors for the control signals and data required to interface a host processor or waveform generator to the DAC7558 EVM using a custom built cable.

An adapter interface card (5-6k adapter interface) is also available to fit and mate with the TI C5000 and C6000 DSP Starter Kit (DSK). This eliminates the problems associated with building a custom cable. In addition, there is also an MSP430 based platform (HPA449) that uses the MSP430F449 microprocessor, which this EVM can connect to and interface with as well. For more details or information regarding the 5-6k adapter interface card or the HPA449 platform, call Texas Instruments Incorporated or send email to dataconvapps@list.ti.com.

The DAC outputs can be monitored through selected pins of the J3 or J4 header connectors. The header connector, J3, is used for stacking. Stacking two EVMs allows for a total of sixteen DAC channels to be monitored when using the daisy-chain feature of the device. Refer to section 3.3 of this User's Guide for further information regarding EVM stacking.

In addition, the option of selecting one DAC output that can be connected to the noninverting side of the output op-amp, U2, is also possible by using a jumper across selected pins of J4. The first four channels (A through D) can be easily connected using a jumper shunt, but the last four channels (E through H) need to be wired (refer to the schematic in section 3.6).

A block diagram of the EVM is shown in Figure 1.

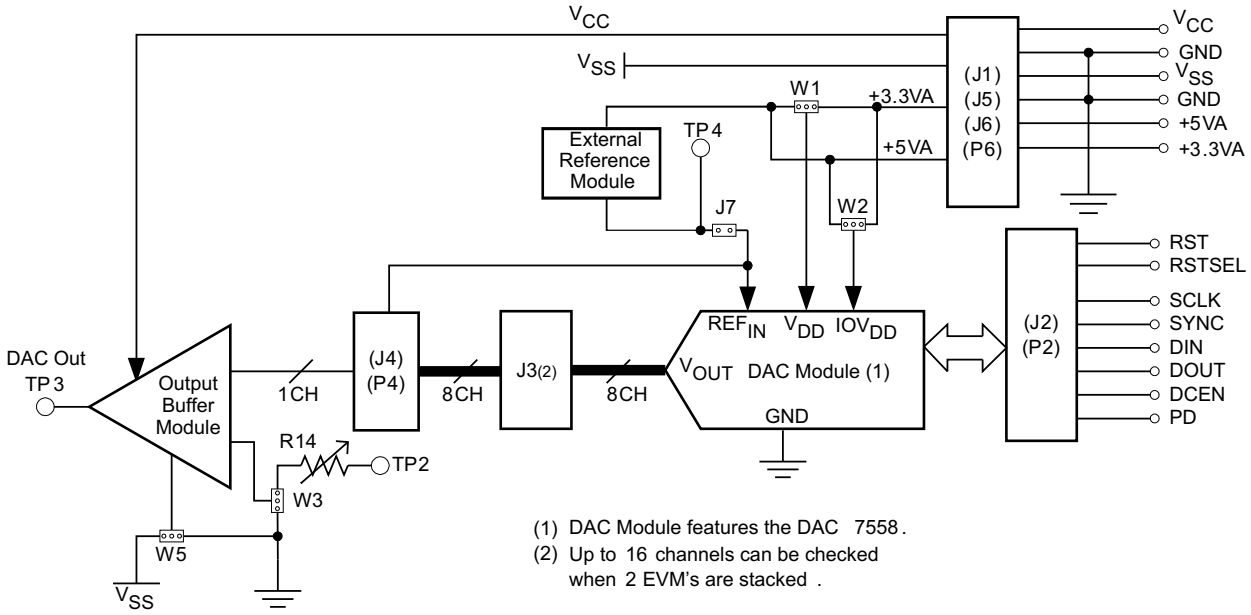


Figure 1. EVM Block Diagram

2 PCB Design and Performance

This chapter presents the layout design of the PCB and describes the physical and mechanical characteristics of the EVM. A list of the components used on the module is also included in this section.

2.1 PCB Layout

The DAC7558 EVM is designed to preserve the performance quality of the DAC, the device under test, as specified in the datasheet. Carefully analyzing the physical restrictions of the EVM and the given or known elements that contribute to performance degradation of the EVM is the key to a successful design implementation. These attributes that diminish the performance of the EVM can be eliminated during the schematic design phase by selecting the appropriate components and building the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and knowing or understanding the mechanical attributes of the components.

The obscure part of the design is the layout process where lack of knowledge and inexperience can easily present a problem. The main concern here is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane works just as well. When considering a split plane design, analyze component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling noise and other effects that otherwise contribute to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practices can be seen in the following figures.

The DAC7558 EVM board is constructed on a four-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board dimensions are 43,1800 mm (1.7000 inch) × 81,2800 mm (3.200 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2 through Figure 8 show the individual artwork layers.

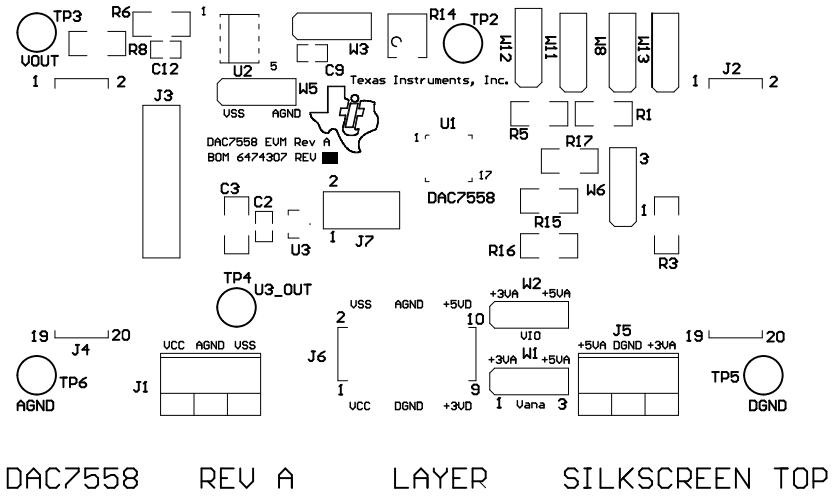


Figure 2. Top Silkscreen

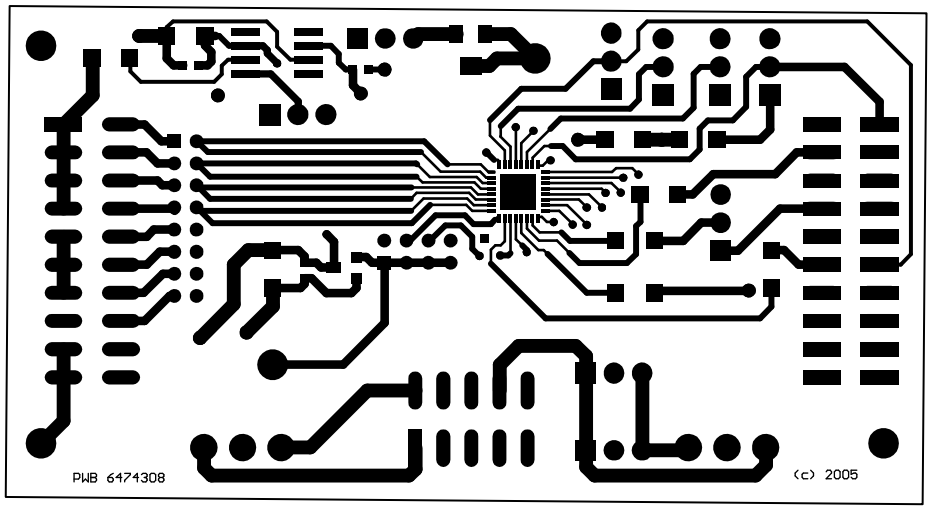


Figure 3. Top Layer (Signal Plane)

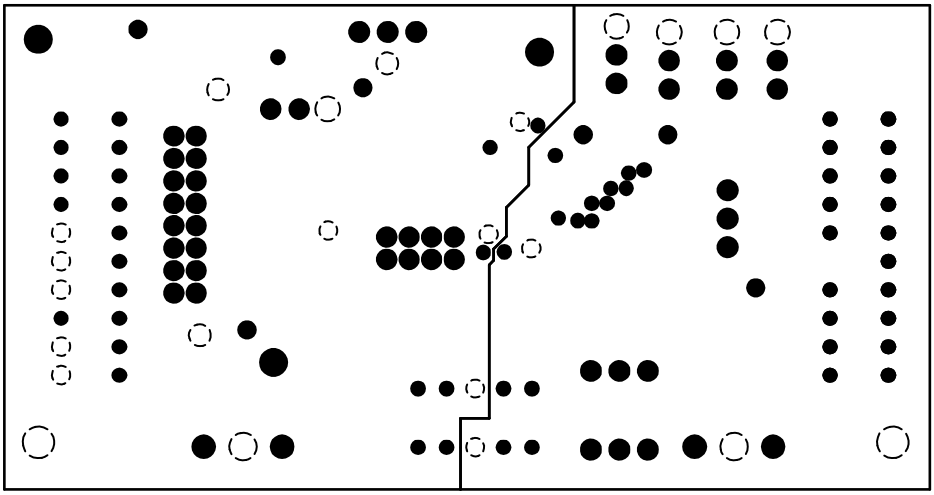


Figure 4. Internal Layer 1 (Split Ground Plane)

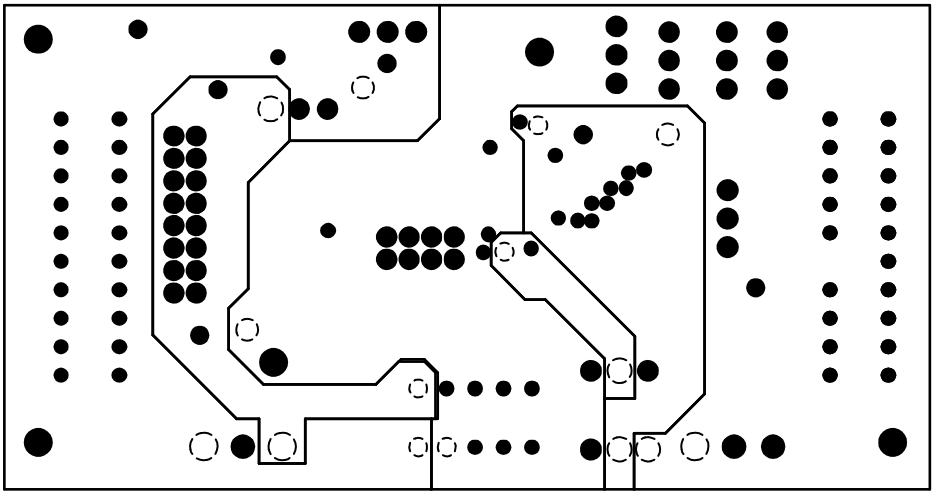


Figure 5. Internal Layer 2 (Split Power Plane)

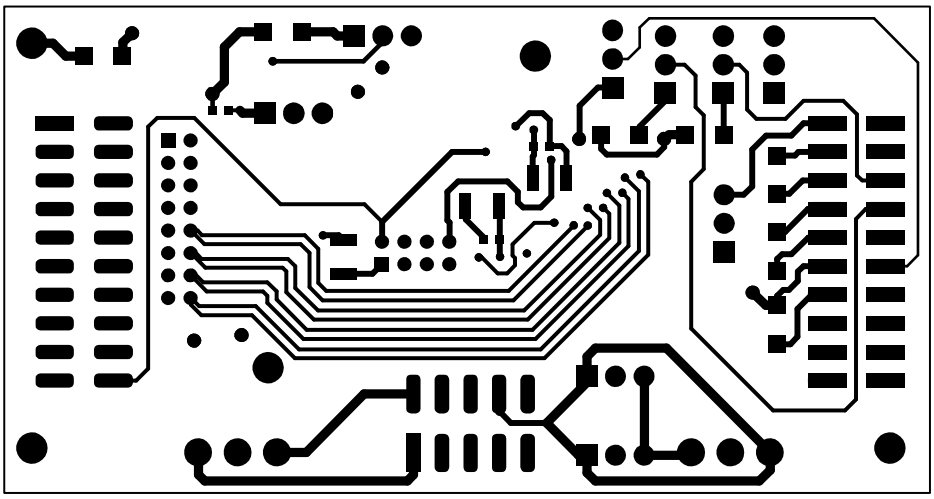


Figure 6. Bottom Layer (Signal Plane)

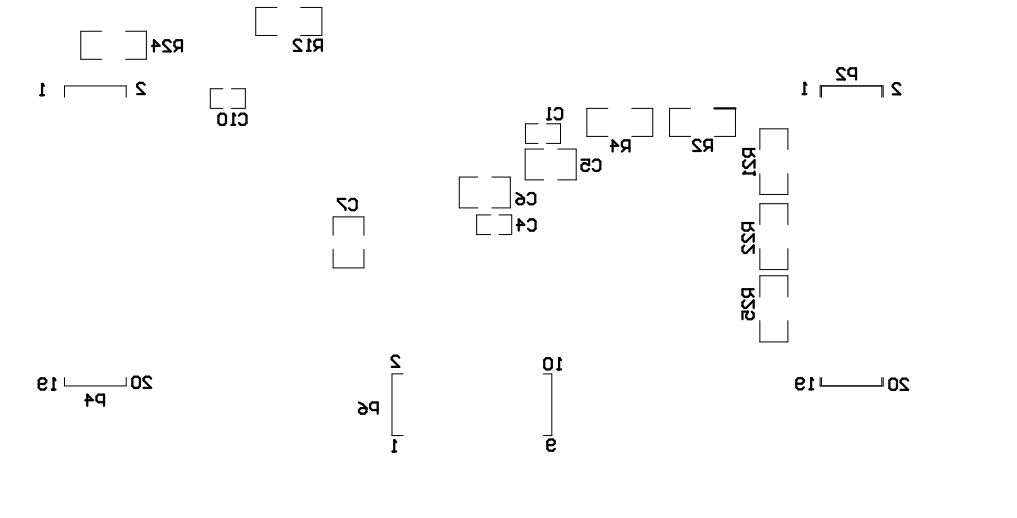


Figure 7. Bottom Silkscreen

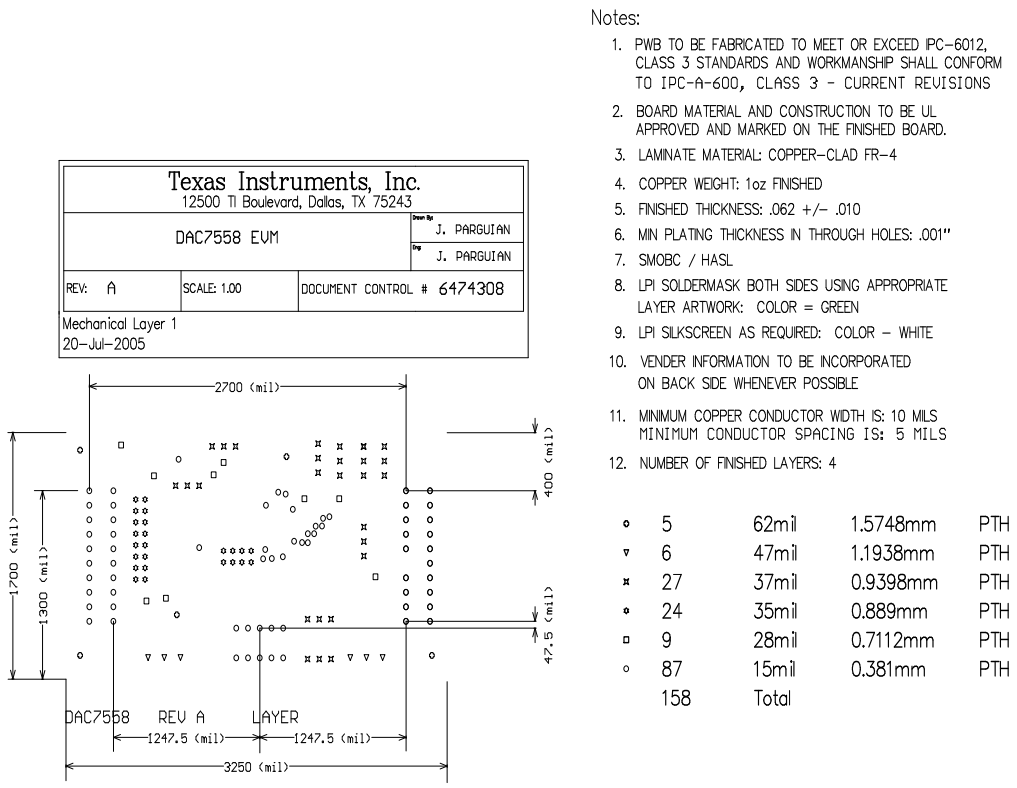


Figure 8. Drill Drawing

2.2 Bill of Materials

Table 1. Parts List

Item	Qty.	Designators	Description	MFG.	MFG. Part Number
1	3	C1, C2, C4	0.1-µF Cap	TDK	C1608X7R1E104KT
2	2	C9, C10	0.01-µF Cap	TDK	C1608COG1E103KT
3	1	C12	1-nF Cap	TDK	C1608COG1E102KT
4	1	C3	0.47-µF, Cap 50-V, ceramic chip, 1206 SMD	TDK	C3216X7R1H474KT
5	3	C5, C6, C7	10-µF Cap	TDK	C3225X7R1E106KT
6	6	R1, R2, R4, R5, R6, R12	10-kΩ Resistor	Panasonic	ERJ-8ENF1002V
7	1	R14	10-kΩ POT	Bourns	3214W-1-103E
8	8	R3, R8, R15, R16, R17, R21, R22, R25	0-Ω Resistor(1)	Panasonic	ERJ-8GEY0R00V
9	1	R24	100-Ω Resistor	Panasonic	ERJ-8GEYJ101V
10	2	J2, J4	20-Pin IDC	Samtec	TSM-110-01-S-DV-M
11	1	J6	10-Pin IDC	Samtec	TSM-105-01-T-DV
12	2	J1, J5	3-Pin terminal connector (1)	On-Shore Tech.	ED555/3DS
13	2	P2, P4	20-Pin IDC(2)	Samtec	SSW-110-22-S-DVS-P
14	1	P6	10-Pin isolated power socket, 0.100(2)	Samtec	SSW-105-22-F-DVS-K
15	5	TP2, TP3, TP4, TP5, TP6	Test point, TP_turrent	Mill-Max	2348-2-01-00-00-07-0
16	1	U2	8-SOP(D) High precision op-amp	Texas Instruments	OPA277UA
17	1	U1	QFN-32(RHB) DAC7558, 12-Bit, 8-CH, SPI™	Texas Instruments	DAC7558IRHB
18	1	U3	4.096-V Voltage reference SOT23-3	Texas Instruments	REF3140AIDBZT
19	1	J7	8-Pin terminal strip	Samtec	TMMH-108-01-T-D
20	1	J3	16-Pin terminal strip	Samtec	TMMH-116-01-T-D
21	9	W1, W2, W3, W5, W6, W8, W11, W12, W13	3 Circuit header, 0.100 straight	Molex	22-03-2031

(1) J1, J5, R21, R22, and R25 are not installed.
(2) P2, P4 and P6 parts are not shown in the schematic diagram. All of the P designated parts are installed on the bottom side of the PC board opposite the J designated counterpart. For example, J2 is installed on the topside while P2 is installed on the bottom side opposite of J2.

3 EVM Operation

This chapter describes in detail the operation of the EVM to assist the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

Refer to the DAC7558 data sheet, SLAS435, for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in unipolar output mode.

3.1 Factory Default Settings

The EVM board default configuration is set at the factory, as described in Table 2, to operate in unipolar mode. The jumper configuration is shown in Figure 9 for clarity.

Table 2. Factory Default Jumper Settings

Reference	Jumper Position	Function
W1	2-3	Analog supply, V_{DD}, for the DAC7558 is +5 VA.
W2	1-2	Digital logic supply, IOV_{DD}, for the DAC7558 is +3.3 VA. DAC output A ($V_{OUT}A$) is routed to J4-2.
W3	Open	External op-amp, U2, is in unity gain configuration.
W5	1-2	Negative supply rail of U2 op-amp is supplied with V_{SS}.
W6	1-2	FSX signal from J2 is routed through to drive the SYNC signal.
W8	1-2	PD pin is tied high.
W11	2-3	RSTSEL pin is tied low to reset DAC at zero scale upon power up.
W12	1-2	RST is tied high.
W13	2-3	DCEN is tied low and daisy-chain is disabled. SDO pin is Hi-Z.
J3	All pins closed	DAC outputs A through H are connected to the J4 output header terminal.
J4	1-2	DAC output A ($V_{OUT}A$) is connected to the noninverting input of the output op-amp, U2.
J7	1-2	Onboard external reference, U3, is routed to $V_{REF}1$.
	3-4	Onboard external reference, U3, is routed to $V_{REF}2$.
	5-6	Onboard external reference, U3, is routed to $V_{REF}3$.
	7-8	Onboard external reference, U3, is routed to $V_{REF}4$.

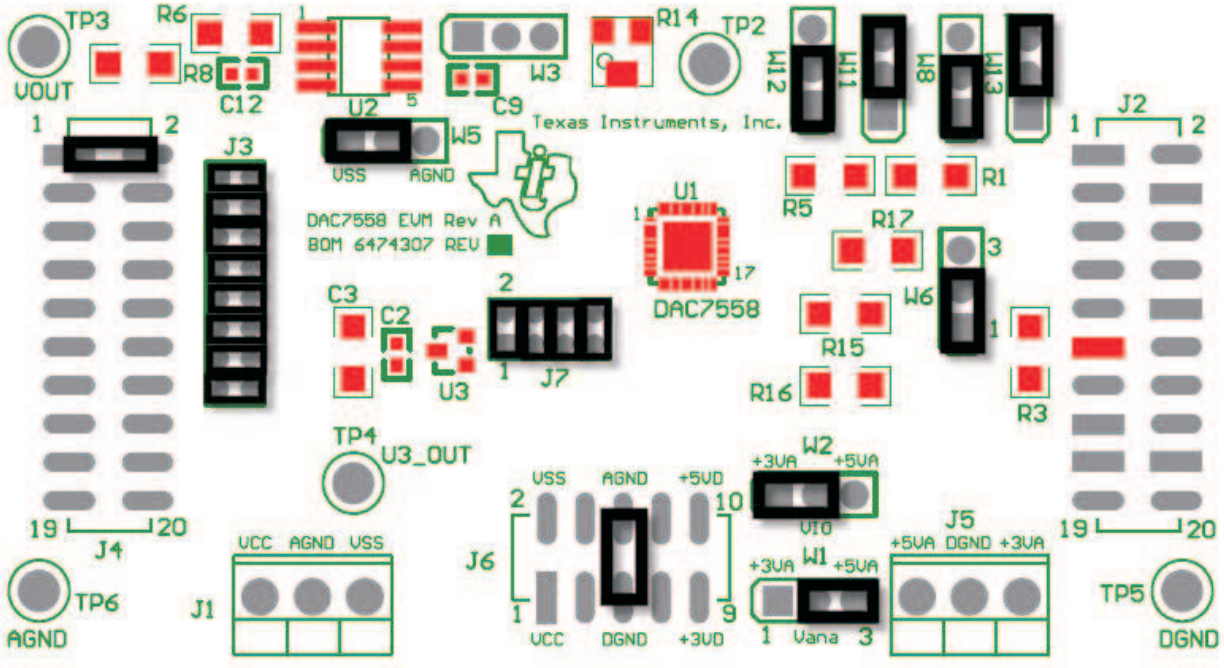


Figure 9. Factory Default Jumper Settings

3.2 Host Processor Interface

The host processor basically drives the DAC, so proper DAC operation depends on a successful configuration between the host processor and the EVM board. In addition, properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM provides an interface to the host processor through the J2 header connector for serial control signals and serial input data. The output can be monitored through the J4 header connector.

An interface adapter card is also available for a specific TI DSP starter kit as well as an MSP430 based microprocessor as mentioned in chapter 1 of this manual. The interface card can be used to alleviate the tedious task of building customized cables and allows easy configuration of a simple evaluation system.

The DAC7558 interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP. For more information regarding the DAC7558 data interface, refer to the data sheet, SLAS435.

3.3 EVM Stacking

The stacking of up to two EVMs is possible if there is a need to evaluate a total of sixteen output channels. The header where the outputs can be measured is through the J3 header connector of the EVM that sits on the top of the stack. The DAC channel outputs A through H of the EVM on top of the stack can be measured from pins 9 through 16 of the J3 header, while the DAC channel outputs A through H of the EVM on the bottom of the stack can be measured from pins 1 through 8 of the same header.

The bottom EVM should be configured as the default setting shown in Figure 9, except W13 should be shunted between pins 1 and 2 to enable the daisy chain feature of the device. A pull-down resistor of 10 kΩ to 20 kΩ on the SDO pin should be placed when in daisy chain operation to ensure that the state of the SDI pin on the the next device in the chain is known. This is because the SDO pin goes to high impedance when SYNC is high. The pull-down resistor also ensures that the devices in the chain do not consume alot of power. The pull-down resistor can be installed on R25, and J2–13 should be shunted to DGND. Shunting to DGND can be achieved through J2 pins 4, 10, or 18 if using a DSK or the HPA449 as these pins are grounded on these boards.

The EVM on top of the stack should also have the same configuration setup as the bottom EVM as described previously. The only difference is the top EVM should have all jumper shunts on J3 taken off so the output signals do not collide.

Table 3 shows how the DAC output channels are mapped into the output terminal, J3 (EVM on top of stack).

Table 3. DAC Output Channel Mapping with Two EVMs Stacked

DAC Output	J3 Header Pin (Top EVM)	
	Bottom DUT	Top DUT
DAC output A (V_{OUT}A)	1	16
DAC output B (V_{OUT}B)	2	15
DAC output C (V_{OUT}C)	3	14
DAC output D (V_{OUT}D)	4	13
DAC output E (V_{OUT}E)	5	12
DAC output F (V_{OUT}F)	6	11
DAC output G (V_{OUT}G)	7	10
DAC output H (V_{OUT}H)	8	9

3.4 The Output Op-Amp

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation since the odd numbered pins (J4-1 to J4-7) are tied together. When two EVM boards are stacked together and the output op-amp is to be used, only the first four output channels of the DUT in the bottom of the stack can be connected with ease using jumper shunts.

Nevertheless, the raw outputs of the DUT for both top and bottom EVMs can be measured through the header, J3. Refer to section 3.3.

The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The default configuration setting of the EVM from the factory is for a unity gain output. The buffered output configuration can be used to prevent loading the DAC7558 although it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R6 and C12 and replacing them with components with the desired values. The user can also remove R6 and C12 and solder a 0-Ω resistor in place of R6, if desired.

Table 4 shows the jumper settings for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 4. Unity Gain Output Jumper Settings

Reference	Jumper Settings		Function
	Unipolar	Bipolar	
W3	Open	Open	Disconnects R12 (gain resistor) or any signals connected to TP2 from the inverting input of the op-amp.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of the op-amp, U2, or ties V_{SS} to AGND.

3.4.2 Output Gain of Two

Table 5 shows the proper jumper settings of the EVM for the 2x gain output of the DAC.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Settings		Function
	Unipolar	Bipolar	
W3	1-2	1-2	Inverting input of the output op-amp, U2, is connected to the gain resistor, R12.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of the op-amp, U2, for bipolar mode, or ties V_{SS} to AGND for unipolar mode.

3.4.3 Adding an Offset to the Output Op-Amp

Another output configuration option is the capability to add an offset to the inverting input of the output op-amp, U2. This can be done by applying a voltage source to TP2 and adjusting the variable pot to the desired offset level. Table 6 shows the jumper setting configuration for adding an offset voltage.

Table 6. Jumper Settings to Add an Offset to the Output Op-Amp

Reference	Jumper Settings		Function
	Unipolar	Bipolar	
W3	2-3	2-3	Offset voltage source is connected to the inverting input of the output op-amp, U2.

Table 6. Jumper Settings to Add an Offset to the Output Op-Amp (continued)

Reference	Jumper Settings		Function
	Unipolar	Bipolar	
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of the op-amp, U2, for bipolar mode, or ties V_{SS} to AGND for unipolar mode.

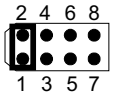
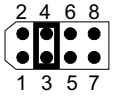
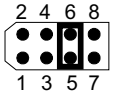
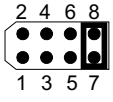
3.5 Jumper Settings

Table 7 shows the function of each specific jumper setting of the EVM.

Table 7. Jumper Setting Functions

Reference	Jumper Settings	Function
W1		+3.3-V Analog supply is selected for DUT V_{DD}.
		+5-V Analog supply is selected for DUT V_{DD}.
W2		+3.3-V Analog supply is selected for DUT IOV_{DD}.
		+5-V Analog supply is selected for DUT IOV_{DD}.
W3		Connects the gain resistor, R12, to the inverting input of the output op-amp, U2. Use for 2x gain configuration.
		Configures the output op-amp, U2, for unity gain.
		Connects any voltage source applied to TP2 to the inverting input of the output op-amp, U2 for offset functionality.
W5		Negative supply rail of the output op-amp, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output op-amp, U2, is tied to AGND for unipolar operation.
W6		FSX signal from J2-7 is routed through to control the SYNC function of the DAC7558. Normally used for DSP operation.
		CS signal from J2-1 is routed through to control the SYNC function of the DAC7558. Normally used for µC operation.

Table 7. Jumper Setting Functions (continued)

Reference	Jumper Settings	Function
W8		PD pin is tied high for normal operation.
		PD pin is tied low and device is put in hardware powerdown mode.
W11		RSTSEL pin is tied high and configures device to reset at mid-scale on power up or reset.
		RSTSEL pin is tied low and configures device to reset at zero-scale on power up or reset.
W12		RST pin is tied high.
		RST pin is tied low and device is put in hardware reset.
W13		DCEN pin is tied high and configures the device in daisy-chain mode.
		DCEN pin is tied low and disables daisy-chain mode of the device.
J7		Routes the onboard +4.096-V reference to the $V_{REF}1$ input of the DAC7558.
		Routes the onboard +4.096-V reference to the $V_{REF}2$ input of the DAC7558.
		Routes the onboard +4.096-V reference to the $V_{REF}3$ input of the DAC7558.
		Routes the onboard +4.096-V reference to the $V_{REF}4$ input of the DAC7558.
Legend: 	Indicates the corresponding pins that are shorted or closed.	

4 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477 – 8924 or the Product Information Center (PIC) at (972) 644 – 5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:	Literature Number:
DAC7588	SLAS435
REF3140	SBVS046A
OPA277	SBOS079

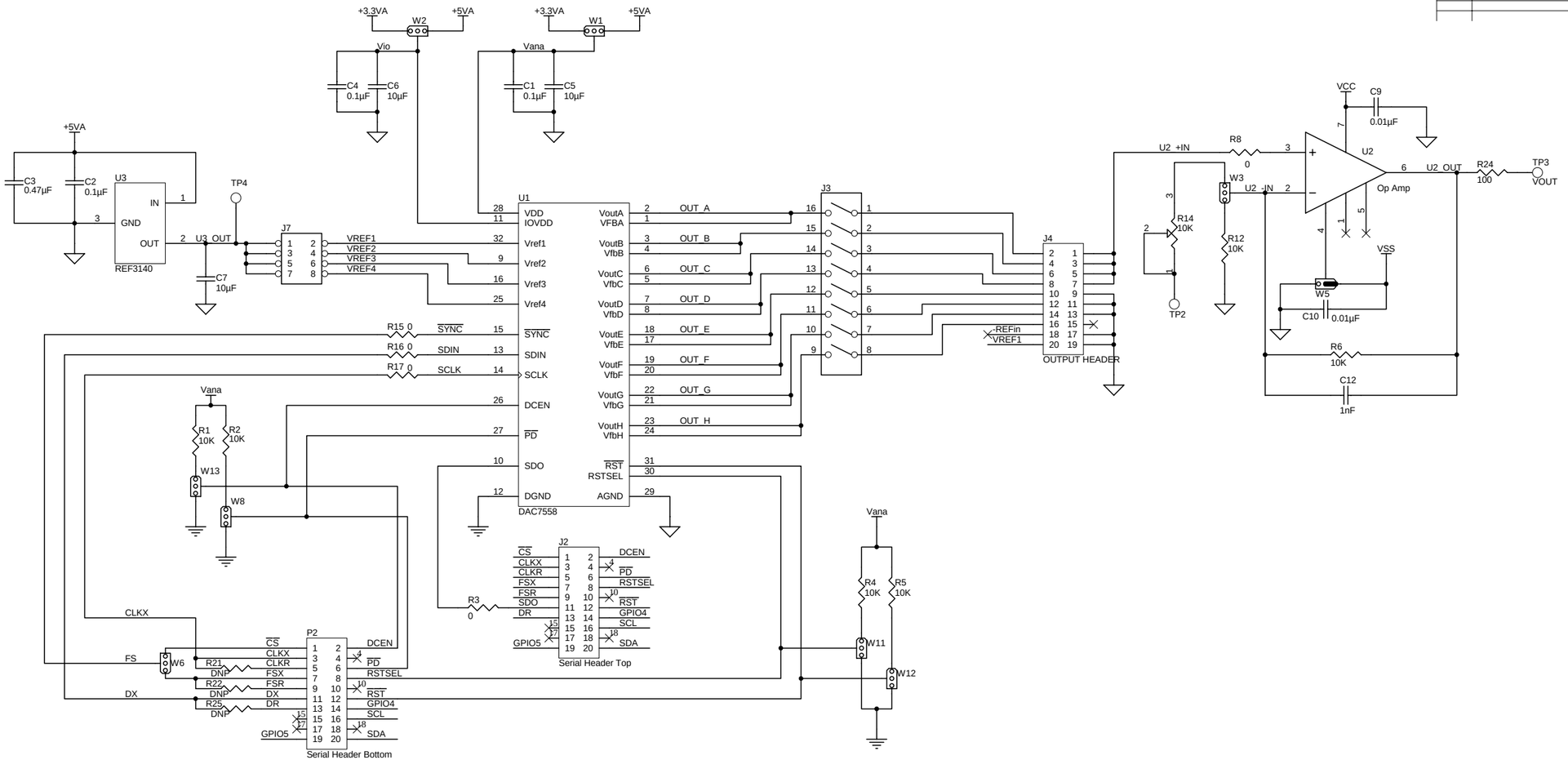
5 Questions about this or other Data Converter EVMs?

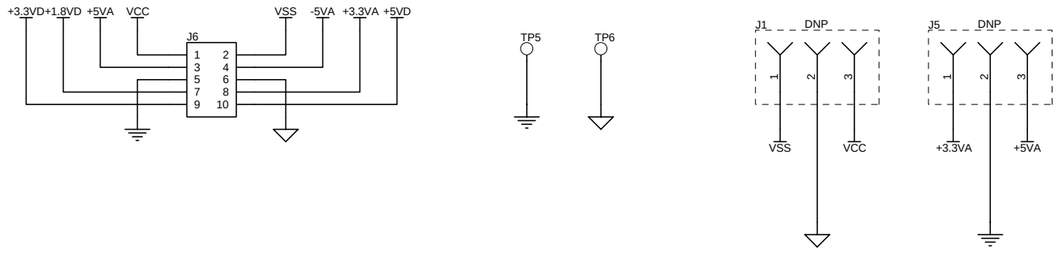
If you have questions about this or other Texas Instruments Data Converter evaluation modules, feel free to e-mail the Data Converter Application Team at dataconvapps@list.ti.com. In the subject heading, include the product you have questions or concerns with.

6 Schematic

Refer to the following page for the EVM schematic.

Revision History		
REV	ECN Number	Approved





Notes:

DNP = Do Not Populate
VCC = +15V Analog Max
VDD = +2.7V to +5.5V Digital Max
VSS = 0V to -15V Analog Max

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: DAC7558 EVM			
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6474309		REV: A
Drawn By:			
FILE: DAC7558 Rev A.Sch	DATE: 20-Jul-2005	SIZE:	SHEET: 1 OF: 1

FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 5 V and the output voltage range of 0 V to 10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265