

ADS5263EVM Evaluation Module

This user's guide gives an overview of the ADS5263EVM and describes how the evaluation module can be used to evaluate the performance, functions, and features of the ADS5263 device.

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1 Quick Look at the Evaluation Setup

Figure 1 shows an overview of the evaluation setup that includes the ADS5263EVM evaluation module (EVM), TSW1250 capture card, external equipment, and software requirements.



Figure 1. Evaluation Setup

TSW1250 Capture Card: The high-speed LVDS deserializer card is required for capturing data from the ADS5263EVM and its analysis using the TSW1250 graphical user interface (GUI).

For information pertaining to the TSW1250 card, see http://focus.ti.com/docs/toolsw/folders/print/tsw1250evm.html.

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, band-pass filters are required in both the signal and clock paths to attenuate the harmonics and noise from the generators.

Power Supply: A single 5-V supply powers the EVM . The supplies for the ADS5263 device are derived from the 5-V supply. The power supply must be able to source up to 1.5 A. A 6-V supply can power the TSW1250 card using a laptop-style adapter.

USB Interface to PC: The USB connection from the ADS5263EVM and TSW1250 card to the personal computer (PC) must be set up; Step 3 in Section 3.1 explains the USB driver installation.

ADS5263EVM GUI: Section 3.1 explains the GUI installation procedure and its operation.



2 EVM Circuit Description

The complete schematic of the EVM can be found at the end of this user guide. Critical portions of the EVM are explained in the following text.

2.1 Power

The EVM requires a single 5-V supply for operation that can be supplied through banana jacks. Separate LDOs convert the 5-V input to generate the 3.3-V AVDD supply and the 1.8-V LVDD supply required for the ADS5263 operation.

2.2 Clock Input

The clock can be supplied to the analog-to-digital converter (ADC) in one of two ways. The default factory-configured option supplies a single-ended sine wave clock directly to the SMA connecter J31. This clock is converted to differential by the TC4-1W transformer from MiniCircuits and is ac coupled to the ADC. This transformer has an impedance ratio of 4, so the voltage applied on J31 is stepped up by a factor of 2.

The clock input must be from a clean, low-jitter source (such as SMA100A or 8644B) and filtered by a narrow band-pass filter. Taking into account the attenuation of the filter, the clock amplitude must be set appropriately to get about 1.5-V peak-to-peak at the clock pins of the ADS5263.

The clock source is commonly synchronized with the signal generator of the input frequency to keep the clock and input coherent for meaningful FFT analysis.



Figure 2. AD5263 Sine Wave Clocking Using Transformer

LVPECL Clock Option

Alternately, the clock may be supplied by an onboard LVPECL clock buffer (TI's CDCLVP1102). To use this option,

- Remove the coupling capacitors C59, C61.
- Replace the $0-\Omega$ resistors with $0.1-\mu F$ capacitors.
- Apply a single-ended, square-wave clock signal on SMA connector J33.





Figure 3. ADS5263 Clocking Using a LVPECL Buffer

2.3 Analog Input

The ADS5263 can be used as a quad-channel, 16-bit ADC or as a quad-channel, 14-bit ADC. Each channel can be configured to use either a transformer-coupled input or a TH77006 amplifier input, from a single-ended source. As a result, two input configurations exist detailed in Table 1.



Figure 4. Input Drive Circuit – Using Transformers

EVM Circuit Description





EVM Config	Transformer Drive	THS770006 Drive	Description			
1	On channels 1, 2, 3, 4	On channel 3	• All components in the transformer drive path for all four channels are available in the EVM.			
			• All components in the THS path for only channel 3 is available in the EVM.			
2	On channels 1, 2, 3, 4	On channels 1, 2, 3, 4	 All components in the transformer and THS paths for all four channels are available in the EVM. 			

Table 1. Two-Input Configurations

Note that the 16-bit ADC and the 14-bit ADC have different analog input pins. Analog input pins 1A, 2A, 3A, 4A correspond to the 16-bit ADC inputs while 1B, 2B, 3B, 4B correspond to the 14-bit ADC inputs. Each of the four transformer paths can be configured to drive either the 16-bit or 14-bit ADC inputs. Similarly, each of the four THS paths can be configured to drive either the 16-bit or 14-bit ADC inputs. This configuration is achieved using pairs of 0 Ω SMT resistors, as listed in Table 2.

Table 2. SMT Resistors

Drive Type	Chan 1A 16-Bit ADC	Chan 1B 14-Bit ADC	Chan 2A 16-Bit ADC	Chan 2B 14-Bit ADC
Transformer	R80,R81 = Open R169,R170 = 0 Ω R35, R153 =Open	R169, R170 = Open R35, R153 = 0 Ω	R98, R99 = Open R171, R172 = 0 Ω R154, R155 = Open	R171, R172 = Open R154, R155 = 0 Ω
THS770006	R80, R81 = 0 Ω R169, R170 = Open	This option is not supported	R98, R99 = 0 Ω R171, R172 = Open	This option is not supported
1	Chan 2A	Chan 3D	Chan 44	Chan 4D
Drive Type	Chan 3A 16-Bit ADC	Chan 3B 14-Bit ADC	Chan 4A 16-Bit ADC	Chan 4B 14-Bit ADC
Drive Type Transformer	Chan 3A 16-Bit ADC R138,R139 = Open R173, R174 = 0 Ω R165, R166 = Open	Chan 3B 14-Bit ADC R173, R174 = Open R165, R166 = 0 Ω	Chan 4A 16-Bit ADC R125, R126 = Open R175, R176 = 0 Ω R167, R168 = Open	Chan 4B 14-Bit ADC R175, R176 = Open R167, R168 = 0 Ω

2.4 Onboard Band-Pass Filter in THS Path

A provision exists in the EVM to include a band-pass filter in the analog input between the THS770006 amplifier and the ADS5263 input pins. Component placeholders are provided to support up to sixth-order LC band-pass filter on each of the four channels. This allows users to design their own filters, populate the EVM with the corresponding components, and verify the performance on the EVM itself.



ADS5263EVM GUI

www.ti.com



Figure 6. Band-Pass Filter

3 ADS5263EVM GUI

This section describes the software features accompanying the EVM kit. The ADS5263EVM control software allows users to write to the ADC registers found in the data sheet.

3.1 Installing the EVM GUI

The EVM comes with a software installation CD that includes an installer zip file for the GUI and associated USB driver.

Step 1 – Install the software before plugging in the USB cable for the first time.

• Unzip the installer file, and run the setup.exe file

Step 2 – Connect the USB cable from the PC to the EVM.

- If the USB driver has not been previously installed in the PC, then a Windows™ message *Found New Hardware* appears. Proceed to Step 3 to complete the installation.
- If the message does not appear, then skip Step 3

Step 3 – Completing the USB Driver Installation

• In the Found New Hardware message, select *No, not this time* from the options, and press the Next button





• Select Install from a list or specific location (Advanced) as shown in the following illustration, and then click Next.



 Select Search for the best driver in these locations., and enter the file path C:\Program Files\Texas Instruments\CDM 2.04.06 WHQL Certified in the combo-box, or browse to it by clicking the Browse button. Once the file path has been entered in the box, click Next to proceed.

nd New Hardware Wizard		
Please choose your search and insta	Illation options.	
Search for the best driver in these lo	ocations.	
Use the check boxes below to limit of paths and removable media. The be	or expand the default se st driver found will be in	earch, which includes local hstalled.
🔲 Search removable media (flop	ppy, CD-ROM)	
Include this location in the se	arch:	
C:\Program Files\Texas Instru	uments\CDM 2.04.06 \	V ▼ Browse
C. Don't search I will choose the drive	r to install	
Choose this option to select the devi the driver you choose will be the bes	ce driver from a list. W It match for your hardw	'indows does not guarantee tha are.

• Windows XP can be configured to warn when unsigned (non-WHQL certified) drivers are about to be installed. In that case, the following screen is displayed. Click on *Continue Anyway* to continue with the installation.

Hardwa	re Installation
1	The software you are installing for this hardware: USB Serial Converter has not passed Windows Logo testing to verify its compatibility with Windows XP. (Tell me why this testing is important.) Continuing your installation of this software may impair or destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware vendor for software that has passed Windows Logo testing.
	Continue Anyway STOP Installation

• If Windows XP is configured to ignore file signature warnings, no message appears.

3.2 GUI Features

Once it is launched, the ADS5263 GUI comes up in the state shown in the following illustration. The ADS5263 has many programmable registers to control various modes. In the GUI, registers with similar functions are grouped into separate tabs such as:

- Top-level
- Interface

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Dig Sig Proc



TEAS INSTRUMENTS	ADS 5263 GUI	
Read Me vel/Pin Ctl Interface/Test Pattern Dig Sig Proc	Dig Sig Proc FILTER 1/0 Mapping Debug	AD55263 Features
Self-Reset Off Reg_Read Disable STAND_BY Normal ADC Operation GLOBAL_PDN Normal ADC operation CONFIG PD PIN FON pin works as standby Select 140R ADC Mode Disable 168_148 ADC Operation Enable 16-bit ADC operation	ENABLE SERALIZATION 16x Serialization 14x Serialization Disable PAD two 0s Disable MSB_LSB LSB First DATA_FORMAT Ceffset Binary 2-WIRE 0.SX FRAME	Save saving let to a file COMPLAND SEQUENCE PLAY BACK Commands play back Saving List Endex Addr Data
LVDS Current for Data Buff 3.5mA LVDS Current for ADCLK Buff 3.5mA LVDS Current for LCLK Buff 3.5mA DEVICE PIN CONTROL ADC_RESCI PDN	Internal LVDS Termination for Data Buff No Termination Internal LVDS Termination for ADCLK Buff No Termination Internal LVDS Termination for LCLK Buff No Termination	address Data Last Data x 0 x 1 x 1 Digital Waveform Graph - Write SCIX - SDATA - SDN -

Figure 7. ADS5263 GUI

Additionally, the GUI has a couple of interesting features – debug mode and command sequence. The debug mode is an alternate way of controlling the registers in the device by directly specifying the hexadecimal values for the register address and register data.

The command sequence can be used to record and store a sequence of register writes into a text file. The next time, after a device reset, the text file can be simply played back. The GUI configures the device with the registers stored in the text file.



TEXAS INSTRUMENTS	ADS 5263 G	UI
Read Me vel/Pin Ctl Interface/Test Pattern Dig Sig Proc	Dig Sig Proc FILTER 1/0 Mapping Debug	AD55263 Features
Self-Reset Off Reg_Read Disable STAND_EV Normal ADC Operation GLOBAL_PON Normal ADC operation CONFIG PD PIN FON pin works as standby Select 1488 ADC Mode Disable 168_148 ADC Operation Enable 16-bit ADC operation	C ENABLE SERALIZATI 16x Serialization Disable 14x Serialization Disable PAD two 0s Disable MSB_LSB LSB First DATA_FORMAT Offset Binary 2-WIRE 0.SX FRAME 1x frame dock	COMPAND SEQUENCE PLAY BACK Commands play back Commands play back Saving List Endex Addr Data
LVDS Current for Data Buff 3.5mA LVDS Current for ADCLK Buff 3.5mA LVDS Current for LCLK Buff 3.5mA DEVICE PIN CONTROL ADC_RESET	ENABLE LVDS Internal LVDS Termination for Data Buff 140 Termination Internal LVDS Termination for ADCLK Buff 140 Termination Internal LVDS Termination for LCLK Buff 140 Termination	address Data Last Data x 0 x 1 x 1
		SEN -

Figure 8. ADS5263 GUI

4 TSW1250 GUI

The TSW1250 GUI is required to transfer ADC data from the TSW1250 card. The data can be viewed in the time-domain. The spectrum of the captured data can be viewed in the Single Tone FFT tab.

For installation of the TSW GUI, see *TSW1250EVM: High-Speed LVDS Deserializer and Analysis System* user's guide (SLOU260).

If the PC is already pre-installed with TSW1250, it may be an earlier revision that does not support the ADS5263 device. Follow the steps outlined in the relevant section of the TSW1250EVM user's guide to *first uninstall* and then re-install the latest TSW1250 version.

4.1 Verify the Setup

Perform the following steps before launching the TSW1250 GUI:

- Connect the TSW1250 card to the ADS5263EVM.
- · Connect the power supplies to both cards and power up.
- Connect the USB cables from the PC to the ADS EVM and TSW card.





Figure 9. EVM and TSW Card Connections

- · Launch the ADS5263GUI, and initialize the device
 - First, reset the device by clicking the *Self-reset* button (this is a self-clearing bit that resets the device and clears itself to zero)
 - Put device in 2-wire, ...modes



dit <u>O</u> perate <u>I</u> ools <u>W</u> indow <u>H</u> elp		
TEXAS INSTRUMENTS	ADS 5263 GUI	
Read Me		AD55263 Features
Level/Pin Cti Interface/Test Pattern Dig Sig Proc	Dig Sig Proc FILTER I/O Mapping Debug	SAVE COMMAND SEQUENCE
Self-Reset Off Reg_Read Disable STAND_BY Normal ADC Operation GLOBAL_PDN Normal ADC operation CONFIG PD PIN PDN pin works as standby Select 14Bit ADC Mode Disable	Enable SeralIZATION 16x Serialization 14x Serialization Disable PAD two 0s Disable MSB_LSB MSB First DATA_FORMAT Offset Binary 2-WIRE 0.5X FRAME 0.5x frame dock	Save saving list to a file COMMAND SEQUENCE PLAY BACK Commands play back Saving List Index Add Data
LVDS Current for Data Buff 3.5mA v LVDS Current for ADCLK Buff 3.5mA v LVDS Current for ADCLK Buff 3.5mA v	ENABLE LVDS TERM Internal LVDS Termination for Data Buff No Termination Internal LVDS Termination for ADCLK Buff No Termination Internal LVDS Termination for LCLK Buff No Termination	address Data Last Data × 46 × 8809 × 8808
DEVICE PIN CONTROL		Digital Waveform Graph - Write SCLK - SDATA - SEN -

Figure 10. Initializing the ADS5263GUI

- Apply input clock signal to SMA connector J31.
- The device is now ready for data capture by the TSW card.
 - Check the DCM LED on the TSW card it must be flashing. This indicates that the TSW card is able to correctly detect the bit clock output from the ADS EVM.
- Launch the TSW GUI; at this point, the TSW GUI communicates with the EVM and once proper communication is established, a message is displayed at the bottom left of the GUI.
- This completes the setup verification.





Figure 11. Successful Interface Between TSW Card and Computer

4.2 Verify the Ramp Test Pattern

- Initialize the TSW GUI with the following settings.
 - Select the device.
 - Choose the channel.
 - Enter the ADC sample rate. For example, *100M* for 100-MSPS sample rate.
- Using the ADS5263 GUI, enable the Ramp Test Pattern mode

TEXAS INSTRUMENTS	ADS 526	3 GUI
Read	1e	AD55263 Features
vel/Pin Ctl Interface/Test Pattern Dig	Sig Proc Dig Sig Proc FILTER I/O Mapping Debug	SAVE COMMAND SEQUENCE
F ENABLE WORD WISE CONTROL		Add addr/data to saving list Save saving list to a file
WORD WISE CH1 BYTE-WISE	DUAL CUSTOM PATTERN Disabl	ed COMMAND SEQUENCE PLAY BACK Commands play back
WORD WISE CH2 BYTE-WISE	SINGLE CUSTOM PATTERN Disabl	ed Clear Saving List
WORD WISE CH3 BYTE-WISE		Index Addr Data
	CUSTOM PATTERN A DATA 1 CUSTOM PATTERN A DATA 2 CUSTOM PATTERN A DATA 2 CUSTOM PATTERN A DATA 3 CUSTOM PATTERN A DATA 3 CUSTOM PATTERN A DATA 4 CUSTOM PATTERN A DATA 5 CUSTOM PATTERN A DATA 5 CUSTOM PATTERN A DATA 6 CUSTOM PATTERN A DATA 7 CUSTOM PATTERN A DATA 8 CUSTOM PATTERN A DATA 10 CUSTOM PATTERN A DATA 10 CUSTOM PATTERN A DATA 11 CUSTOM PATTERN A DATA 12 CUSTOM PATTERN A DATA 12 CUSTOM PATTERN A DATA 14 CUSTOM PATTERN A DATA 14	PATTERN B DATA 1 PATTERN B DATA 2 PATTERN B DATA 3 PATTERN B DATA 3 PATTERN B DATA 5 PATTERN B DATA 5 PATTERN B DATA 5 PATTERN B DATA 6 PATTERN B DATA 13 PATTERN B DATA 13 PATTERN B DATA 13 PATTERN B DATA 13 PATTERN B DATA 14 PATTERN B DATA 13 PATTERN B DATA 14 PATTERN B DATA 14 PATTERN B DATA 13 PATTERN B DATA 14 PATTERN B DATA 15 PA
	CUSTOM PATTERN A DATA 15	Digital Waveform Graph - Write SCLK - SDATA - SEN -

Figure 12. Enabling Ramp Test Pattern in the ADS5263 GUI

- Press the Capture button in the TSW GUI.
- Time Domain:
 - Select the Time Domain tab in the GUI.
 - Uncheck the overlay unwrap waveform button.
 - Graph shows the captured time domain data.
 - It Must be a clean digital ramp that increases from code 0 to code 65535 from one sample to the next. Note that the starting code in the capture graph is not fixed and can be anywhere from 0 to 65535.





Figure 13. Verifying With Ramp Test Pattern

- Now, disable the Ramp Test Pattern in the ADS5263 GUI.
- This completes the verification of the ramp test pattern.

4.3 Verify With a Sine Wave Analog Input

- Note that for all performance evaluation, low-phase noise signal generators are required (see Figure 1) for both analog signal and sampling clock inputs.
- In the TSW GUI,
 - Enter the ADC input frequency being applied. For example, 3M for 3-MHz input frequency.
 - choose the desired channel
- Set the frequency in the signal generator to the value displayed in the field ADC Input Coherent frequency and connect the generator output to the desired channel.
 This makes the input signal coherent with respect to the sampling clock, which is required for FFT analysis.
- Now, press the Capture button, and check the overlay unwrap waveform button.
- The time domain graph shows the captured sine wave data.



TSW1250 GUI



Figure 14. Sine Wave Data Capture

- Frequency Domain:
 - Select the Single tone FFT tab in the GUI.
 - The fft graph shows the spectrum of the captured sine wave data



ADS5263EVM Schematics and Test Points



Figure 15. Spectrum of Captured Data

5 ADS5263EVM Schematics and Test Points

The schematics for the ADS5263EVM evaluation module are attached at the end of this document.

5.1 List of Test Points

Test Points	Name	Description
TP1	SDOUT	Serial register output
TP2	Ground	Board ground
TP9	VCM	1.5V common-mode output
TP12	SDATA	Serial interface data input
TP13	SCLK	Serial interface clock input
TP14	CSZ	Serial interface enable input
TP15	ADCRESETZ	Reset input
TP16	PD	Power down control input

Table 3. Test Points on the EVM

6 ADS5263EVM PCB Layout

The following figures (Figure 16 through Figure 21) show the design of the ADS5263EVM printed-circuit board. PCB dimensions: L x W = 5 x 6 inches, four layers and 0.5-oz copper on outer layers and 1oz copper on inner layers.



Figure 16. ADS5263EVM Top Layer Assembly Drawing – Top View

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Figure 17. ADS5263EVM Bottom Layer Assembly Drawing – Bottom View







Figure 18. ADS5263EVM Top Layer Copper – Top View





Figure 19. ADS5263EVM Internal Layer 1, Ground – Top View



Figure 20. ADS5263EVM Internal Layer 2, Power – Top View





Figure 21. ADS5263EVM Bottom Layer Copper – Top View

7 Bill of Materials

Table 4. EVM Components List

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
6	C1,C3,C5,C25,C29,C42	10 µF	AVX	1206YC106MAT2A	CAP CER 10UF 16V X7R 20% 1206
4	C2,C4,C6,C40	1 µF	AVX	0603YC105KAT2A	CAP CER 1.0UF 16V X7R 10% 0603
	C10,C11,C12,C18,C19,C20,				
	C21,C26,C27,C30,C43,C44,				
00	C45,C46,C59,C60,C61,C94,	0.4.5	A) ()(50140/04044/	
32	C99,C115,C116,C118,C119,	0.1 µF	AVX	ECJ-1VB1C104K	CAP CER .100F 50V X7R 10% 0603
	C124,C125,C126,C152,C154				
	C28,C41,C95,C96				
8	C51,C52,C53,C54,C55,C56, C57,C58	220 pF	AVX	06035A221FAT2A	CAP CERM 220PF 1% 50V NP0 0603
1	C149	10 nF	Panasonic	ECJ-1VB1C103K	CAP 10000PF 16V CERM X7R 0603
2	C150,C153	47 pF	Panasonic	ECJ-1VC1H470J	CAP CERAMIC 47PF 50V 0603 SMD
1	C151	4.7 μF	AVX	TAJA475K020R	
1	D2	MBRB2515L	MBRB2515LT4GOSCT-ND	MBRB2515LT4GOSCT-ND	DIODE SCHOTTKY 15V 25A D2PAK
2	JP2,JP3	HEADER 3POS 0.1 CTR	ANY	JUMPER,3P,.100CC	JUMPER,3P,.1CC
2	JP12,JP13	HEADER_1x2_100_430L	ANY		
1	J1	RED	ALLIED ELECTRONICS	ST-351A	Banana Female Red
1	J2	BLK	ALLIED ELECTRONICS	ST-351B	Banana Female Black
1	J8	QTH-060-02-F-D-A	SAMTEC	QTH-060-02-F-D-A	High speed connector
1	J13	USB_MINI_AB	JAE	DX3R005HN2E700	USB_MINI_AB
8	J14,J16,J17,J18,J19,J30,J31,J33	SMA	SAMTEC	SMA-J-P-H-ST-TH1	JACK PANEL MOUNT SMA
1	L7	1K at 100 MHz			
2	L18,L19	0 Ω	Panasonic	ERJ-3GEY0R00	RESISTOR,SMT,0603,0 OHM,5%,
					ZERO OHM JUMPER
8	L30,L31,L32,L33,L34,L35,L36,L37	56 nH	Panasonic	EXC-ML32A680U	Inductor
23	R3,R5,R7,R9,R10,R132,	0 Ω	Panasonic	ERJ-3GEY0R00	RESISTOR,SMT,0603,0 OHM,5%,
	R133,R138,R139,R141,R165,				
	R166,R169,R170,R171,R172,				
	R175,R176,R188,R189,R190,				
	R191,R192				
2	R4,R78	56.2K	Panasonic - ECG	ERJ-3EKF5622V	RES 56.2K OHM 1/10W 1% 0603 SMD
1	R6	50 Ω	Panasonic	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
8	R36,R37,R38,R39,R40,R41,R42,R43	25 Ω	Panasonic	ERJ-3EKF24R9V	RES 24.9 OHM 1/10W 1% 0603 SMD
2	R45,R48	100	Panasonic	ERJ-3EKF1000V	RES 100 OHM 1/10W 1% 0603 SMD
1	R46	10 Ω	Panasonic	ERJ-3EKF10R0V	RES 10.0 OHM 1/10W 1% 0603 SMD
2	R53,R56	10K	Panasonic	ERJ-3EKF1002V	RES 10.0K OHM 1/10W 1% 0603 SMD
8	R59,R60,R61,R62,R63,R64,R65,R67	12.4 Ω	Panasonic	ERJ-3EKF12R4V	RES 12.4 OHM 1/10W 1% 0603 SMD
2	R77,R152	56K	Panasonic	ERJ-3EKF5602V	RES 56.0K OHM 1/10W 1% 0603 SMD
2	R107,R108	250 Ω	Vishay	PLT0603Z2500AST5	RES 250 OHM 0.05% 5PPM 0603 SMD
2	R134,R135	200 Ω	Panasonic	ERJ-3EKF2000V	RES 200 OHM 1/10W 1% 0603 SMD
2	R136,R137	15 Ω	Vishay	CRCW06035R10FNEA	RES 15 OHM 1/10W 1% 0603 SMD
1	R142	50 Ω	Panasonic	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
2	R186,R187	0 Ω	Vishay/Dale	CRCW04023K00FKED	RESISTOR,SMT,0603,0 OHM,5%,
44					
11	TP14 TP15 TP46 TP17 TP18 TP40	TPOINTR			
1	T15	TC4 1W		TC4 1WC21	Transformar
0		104-1W		104-1WG2+	Transformer
0	120,127,120,129,130,131,132,133			WDGI-IILD	
		AD00203_QFN04		ET345DI	
1		F 1245KL		F1245KL	
1		TPS/3201-SO123	Texas Instruments	TPS/320IDBV1	IC LDO REG 250MA ADJ-V SO123-5
2	011,012	THO770000	Texas Instruments	TP077000010050	
1	019	THS770006	Texas Instruments	IPS770006IRGER	IC AMP DIFF ADC DVR 16BIT 24VQFN
1			rexas Instruments	CDCLVP1102RGIT	IC CLK BUFF 1:2 LVPECL SGL 16QFN
2	2_SH-H3,2_SH-H4	SHUNI-HEADER			
2	Z_SH-J1,Z_SH-J2	SHUNI-JUMPER-0402			



Qty	Reference Designator	Value	Manufacturer	Part Number	Description
4	STANDOFF HEX M3 THR ALUM 18MM		Digi-Key	24436K-ND	STANDOFF HEX M3 THR ALUM 18MM
4	SCREW STEEL M3 THR 6MM		Digi-Key	29311K-ND	SCREW STEEL M3 THR 6MM

Table 4. EVM Components List (continued)

EVM CONFIGURATION MODES

DEFAULT (SINGLE AMP) CONFIGURATION

Default Config (with transformer drive on 3 channels &

THS770006 on one channel (IN3A)

OPTIONAL (4 CHANNEL AMP) CONFIGURATION

THS7700 Config - THS770006-based drive on all 4 channels

Channel (IN1A, IN2A, IN3A IN4A)































* Denotes components uninstalled in default configuration









Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of -0.3 V to 5.3 V and the output voltage range of -0.3 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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