MSP430F123 Device Erratasheet

1 Revision History

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
BCL5	✓
CPU4	✓
EEM20	✓
JTAG11	✓
PORT3	✓
RES4	✓
TA12	✓
TA16	✓
TA21	✓
TAB22	✓
US13	✓
US15	✓
WDG2	✓

2 Package Markings

DW28

SOP (DW), 28 Pin

YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

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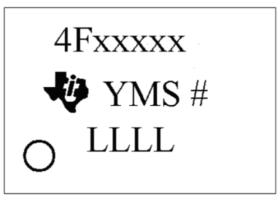
PW28

TSSOP (PW), 28 Pin



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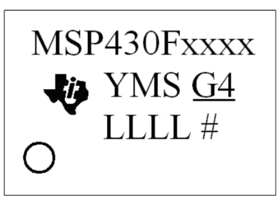

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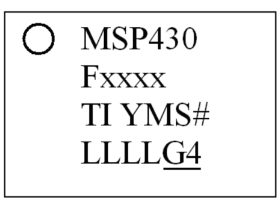
RHB32

QFN (RHB), 32 Pin



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3 Detailed Bug Description

BCL5 — *BCS Module*

Function

RSELx bit modifications can generate high frequency spikes on MCLK

Description

When DIVMx = 00 or 01 the RSELx bits of the Basic Clock Module are incremented or decremented in steps of 2 or greater, the DCO output may momentarily generate high frequency spikes on MCLK, which may corrupt CPU operation. This is not an issue when DIVMx = 10 or 11.

Workaround

Set DIVMx = 10 or 11 to divide the MCLK input prior to modifying RSELx. After the RSELx bits are configured as desired, the DIVMx setting can be changed back to the original selection.

CPU4 — *CPU Module*

Function

PUSH #4, PUSH #8

Description

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround

Workaround implemented in assembler.

EEM20 — *EEM Module*

Function

Debugger might clear interrupt flags

Description

During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

Workaround

None.

JTAG11 — *JTAG Module*

Function

Debug with JTAG interface

Description

The debug operation using the JTAG interface of a program executed in the RAM is not possible. The RAM content gets corrupted.

Workaround

None

PORT3 — *PORT Module*

Function

Port interrupts can get lost

Description

Port interrupts can get lost if they occur during CPU

access of the P1IFG and P2IFG registers.

Workaround

None

RES4 — *RESET Module*

Function

No reset if external resistor exceeds certain value

Description

No reset of the device is performed if the external pull down resistor on RST/NMI pin is above a certain limit. The limits are:

Vcc = 1.8V: maximum pull down resistor = 12 kohm

Vcc = 3.0V: maximum pull down resistor = 5 kohm

Vcc = 3.6V: maximum pull down resistor = 2.5 kohm

In addition, a higher current consumption occurs during high/low RST/NMI signal transition when using improper resistors.

Workaround

Use external pulldown resistors below the listed values or directly drive RST/NMI low to generate a reset.

TA12 — *TIMER_A Module*

Function

Interrupt is lost (slow ACLK)

Description

Timer_A counter is running with slow clock (external TACLK or ACLK)compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 — *TIMER_A Module*

Function

First increment of TAR erroneous when IDx > 00

Description

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround

None

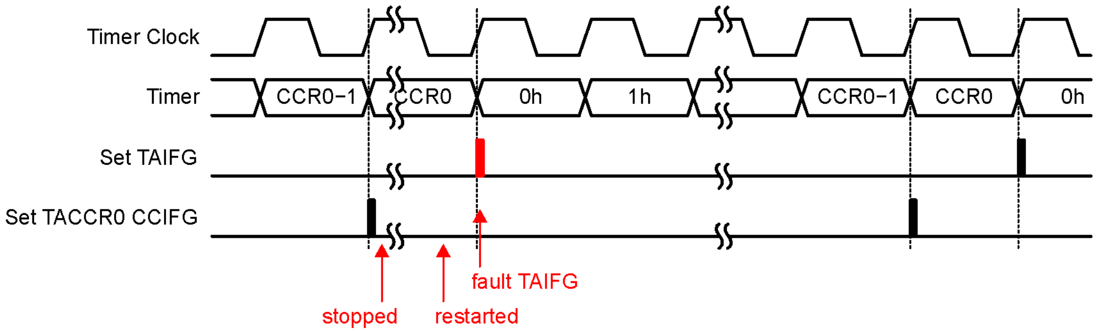
TA21 — *TIMER_A Module*

Function

TAIFG Flag is erroneously set after Timer A restarts in Up Mode

Description

In Up Mode, the TAIFG flag should only be set when the timer resets from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



Workaround None.

TAB22 *TIMER_A/TIMER_B Module*

Function Timer_A/Timer_B register modification after Watchdog Timer PUC

Description Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer_A/Timer_B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/Timer_B does not need to be running).

Workaround Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

MOV.W #VAL, &TACTL

or

MOV.W #VAL, &TBCTL

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

US13 *USART Module*

Function Unpredictable program execution

Description USART interrupts requested by URXS can result in unpredictable program execution if this request is not served within two bit times of the received data.

Workaround Ensure that the interrupt service routine is entered within two bit times of the received data.

US15 *USART Module*

Function UART receive with two stop bits

Description USART hardware does not detect a missing second stop bit when SPB = 1.

The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround None (Configure USART for a single stop bit, SPB = 0)

WDG2 — *WDT Module*

Function Incorrectly accessing a flash control register

Description If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to the expected PUC.

Workaround None

4 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Errata TA22 was renamed to TAB22
2. Description for TAB22 was updated

Changes from device specific erratasheet to document Revision A.

1. Errata EEM20 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata TA21 was added to the errata documentation.

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