TEXAS INSTRUMENTS

MSP430F5219 Device Erratasheet

1 Revision History

✓ The check mark indicates that the issue is present in the specified revision.

The revision of the device can be identified by the revision letter on the Package Markings or by the HW_ID located inside the TLV structure of the device

Errata Number	Rev B
BSL7	✓
BSL11	✓
CPU40	✓
DMA4	✓
DMA10	✓
EEM17	✓
EEM19	✓
EEM21	✓
EEM23	✓
PMAP1	✓
PMM9	✓
PMM11	✓
PMM12	✓
PMM14	✓
PMM18	✓
PMM20	✓
PORT15	✓
PORT19	✓
RTC3	✓
RTC6	✓
SYS12	✓
SYS16	✓
UCS7	✓
UCS9	✓
UCS11	✓
USCI26	✓
USCI35	✓

2   Package Markings

RGC64   *QFN (RGC), 64 pin*

M430Fxxx

TI YMS
LLLL #

TI   = TI
YM   = Year and Month Date Code
LLLL = LOT Trace Code
S   = Assembly Site Code
= DIE Revision
o   = PIN 1

M430Fxxxx

TI YMS #
LLLL G4

TI   = TI
YM   = Year and Month Date Code
LLLL = LOT Trace Code
S   = Assembly Site Code
= DIE Revision
o   = PIN 1

MSP430™
Fxxx
TI YMS #
LLLL G4

YM   = Year and Month Date Code
S   = Assembly Site Code
#   = Die Revision
LLLL = Lot Trace Code
○   = Pin 1

Note: Package marking with "TM" applies only to devices released after 2011.

ZQE80   *BGA (ZQE), 80 pin*

M430Fxxxxx
YMLLLLS #
G1

YM   = Year and Month Date Code
LLLL = LOT Trace Code
S   = Assembly Site Code
= DIE Revision
o   = PIN 1

MSP430™
Fxxx
YMLLLLS #
TI   G1

YM   = Year and Month Date Code
LLLL = Lot Trace Code
S   = Assembly Site Code
= Die Revision
○   = Pin 1

Note: Package marking with "TM" applies only to devices released after 2011.

3   TLV Hardware Revision

Die Revision	TLV Hardware Revision
Rev B	11h

Further guidance on how to locate the TLV structure and read out the HW_ID can be found in the device User's Guide.

4   Detailed Bug Description

BSL7	***BSL Module***

Function	BSL does not start after waking up from LPMx.5
Description	When waking up from LPMx.5 mode, the BSL does not start as it does not clear the Lock I/O bit (LOCKLPM5 bit in PM5CTL0 register) on start-up.
Workaround	1. Upgrade the device BSL to the latest version (see Creating a Custom Flash-Based Bootstrap Loader (BSL) Application Note - SLAA450 for more details)
	OR
	2. Do not use LOCKLPM5 bit (LPMx.5) if the BSL is used but cannot be upgraded.

BSL11	***BSL Module***

Function	P1.0 is set to output high after BSL starts.
Description	When the BSL is invoked, P1.0 is set to output driven high.
Workaround	Do not ground P1.0 if the BSL is used.

> **NOTE:** A high P1.0 during BSL invoke should not pose any risk to the circuit design.
>
> An updated version of the BSL can be programmed to circumvent this issue.

CPU40	***CPUXv2 Module***

Function	PC is corrupted when executing jump/conditional jump instruction that is followed by instruction with PC as destination register or a data section
Description	If the value at the memory location immediately following a jump/conditional jump instruction is 0X40h or 0X50h (where X = don't care), which could either be an instruction opcode (for instructions like RRCM, RRAM, RLAM, RRUM) with PC as destination register or a data section (const data in flash memory or data variable in
	RAM), then the PC value is auto-incremented by 2 after the jump instruction is executed; therefore, branching to a wrong address location in code and leading to wrong program execution.
	For example, a conditional jump instruction followed by data section (0140h).
	@0x8012 Loop DEC.W R6
	@0x8014 DEC.W R7
	@0x8016 JNZ Loop
	@0x8018 Value1 DW 0140h
Workaround	In assembly, insert a NOP between the jump/conditional jump instruction and program code with instruction that contains PC as destination register or the data section.

DMA4	***DMA Module***

Function	Corrupted write access to 20-bit DMA registers

Description	When a 20-bit wide write to a DMA address register (DMAxSA or DMAxDA) is interrupted by a DMA transfer, the register contents may be unpredictable.
Workaround	1. Design the application to guarantee that no DMA access interrupts 20-bit wide accesses to the DMA address registers.
	OR
	2. When accessing the DMA address registers, enable the Read Modify Write disable bit (DMARMWDIS = 1) or temporarily disable all active DMA channels (DMAEN = 0).
	OR
	3. Use word access for accessing the DMA address registers. Note that this limits the values that can be written to the address registers to 16-bit values (lower 64K of Flash).

DMA10　　　　*DMA Module*

Function	DMA interrupting CPU wait state might cause peripheral module into unknown state.
Description	When the CPU accesses a module that is capable of stalling the CPU with a wait mechanism, if a DMA interrupts the instruction during the CPU stall, the module might be caused into an unknown state.
	The affected modules (if present on the device) that can stall CPU are: FRAM controller in manual timing mode, MPY, CRC, USB, and RF1A.
	As an example a wrong result can be read by DMA from MPY result register because the DMA does not wait until MPY operation is finished.
Workaround	Disable DMA when using affected modules.

EEM17　　　　*EEM Module*

Function	Wrong Breakpoint halt after executing Flash Erase/Write instructions
Description	Hardware breakpoints or Conditional Address triggered breakpoints on instructions that follow Flash Erase/Write instructions, stops the debugger at the actual Flash Erase/Write instruction even though the flash erase/write operation has already been executed. The hardware/conditional address triggered breakpoints that are placed on either the next two single opcode instructions OR the next double opcode instruction that follows the Flash Erase/Write instruction are affected by this erratum.
Workaround	None. Use other conditional/advanced triggered breakpoints to halt the debugger right after Flash erase/write instructions.

> **NOTE:**　This erratum affects debug mode only.

EEM19　　　　*EEM Module*

Function	DMA may corrupt data in debug mode
Description	When the DMA is enabled and the device is in debug mode, the data transferred by the DMA may be corrupted when a breakpoint is hit or when the debug session is halted.
Workaround	None. Do not set a breakpoint during a DMA transfer.

> **NOTE:**   This erratum applies to debug mode only.

EEM21   *EEM Module*

Function   LPMx.5 debug limitations

Description   Debugging the device in LPMx.5 mode might wake the device up from LPMx.5 mode inadvertently, and it is possible that the device enters a lock-up condition; that is, the device cannot be accessed by the debugger any more.

Workaround   Follow the debugging steps in Debugging MSP430 LPM4.5 SLAA424 .

EEM23   *EEM Module*

Function   EEM functions do not work reliably when modules using wait cycles are enabled

Description   When modules using wait states (USB, MPY,CRC and FRAM controller in manual mode) are enabled the EEM may not perform profile counter and state storage functions reliably.

Workaround   Do not enable profile counter and state storage functions when modules using wait states are enabled.

> **NOTE:**   This erratum affects debug mode only.

PMAP1   *PMAP Module*

Function   Port Mapping Controller does not clear unselected inputs to mapped module.

Description   The Port Mapping Controller provides the logical OR of all port mapped inputs to a module (Timer, USCI, etc). If the PSEL bit (PxSEL.y) of a port mapped input is cleared, then the logic level of that port mapped input is latched to the current logic level of the input. If the input is in a logical high state, then this high state is latched into the input of the logical OR. In this case, the input to the module is always a logical 1 regardless of the state of the selected input.

Workaround   1. Drive input to the low state before clearing the PSEL bit of that input and switching to another input source.

or

2. Use the Port Mapping Controller reconfiguration feature, PMAPRECFG, to select inputs to a module and map only one input at a time.

PMM9   *PMM Module*

Function   False SVSxIFG events

Description   The comparators of the SVS require a certain amount of time to stabilize and output a correct result once re-enabled; this time is different for the Full Performance versus the Normal mode. The time to stabilize the SVS comparators is intended to be accounted for by a built-in event-masking delay of 2 us when Full Performance mode is enabled.

However, the comparators of the SVS in Full Performance mode take longer than 2 us to

stabilize so the possibility exists that a false positive will be triggered on the SVSH or SVSL. This results in the SVSxIFG flags being set and depending on the configuration of SVSxPE bit a POR can also be triggered.

Additionally when the SVSxIFGs are set, all GPIOs are tri-stated i.e. floating until the SVSx comparators are settled.

The SVS IFG's are falsely set under the following conditions:

1. Wakeup from LPM2/3/4 when SVSxMD = 0 (default setting) && SVSxFP=1. The SVSx comparators are disabled automatically in LPM2/3/4 and are then re-enabled on return to active mode.

2. SVSx is turned on in full performance mode (SVSxFP=1).

3. A PUC/POR occurs after SVSx is disabled. After a PUC or POR the SVSx are enabled automatically but the settling delay does not get triggered. Based on SVSxPE bit this may lead to POR events until the SVS comparator is fully settled.

Workaround   For each of the above listed conditions the following workarounds apply:

1. If the Full Performance mode is to be enabled for either the high- or low-side SVS comparators, the respective SVSxMD bits must be set (SVSxMD = 1) such that the SVS comparators are not temporarily shut off in LPM2/3/4. Note that this is equivalent to a 2 uA (typical) adder to the low power mode current, per the device-specific datasheet, for each SVSx that remains enabled.

2. The SVSx must be turned on in normal mode (SVSxFP=0). It can be reconfigured to use full performance mode once the SVSx/SVMx delay has expired.

3. Ensure that SVSH and SVSL are always enabled.

PMM11   *PMM Module*

Function   MCLK comes up fast on exit from LPM3 and LPM4

Description   The DCO exceeds the programmed frequency of operation on exit from LPM3 and LPM4 for up to 6 us. This behavior is masked from affecting code execution by default: SVSL and SVML run in normal-performance mode and mask CPU execution for 150 us on wakeup from LPM3 and LPM4. However, when the low-side SVS and the SVM are disabled or are operating in full-performance mode (SVMLE = 0 and SVSLE = 0, or SVMLFP = 1 and SVSLFP = 1) AND MCLK is sourced from the internal DCO running over 4 MHz, 7 MHz, 11 MHz, or 14 MHz at core voltage levels 0, 1, 2, and 3, respectively, the mask lasts only 2 us. MCLK is, therefore, susceptible to run out of spec for 4 us.

Workaround   Set the MCLK divide bits in the Unified Clock System Control 5 Register (UCSCTL5) to divide MCLK by two prior to entering LPM3 or LPM4 (set DIVMx = 001). This prevents MCLK from running out of spec when the CPU wakes from the low-power mode. Following the wakeup from the low-power mode, wait 32, 48, 80, or 100 cycles for core voltage levels 0, 1, 2, and 3, respectively, before resetting DIVMx to zero and running MCLK at full speed [for example, __delay_cycles(100)].

PMM12   *PMM Module*

Function   SMCLK comes up fast on exit from LPM3 and LPM4

Description   The DCO exceeds the programmed frequency of operation on exit from LPM3 and LPM4 for up to 6 us. When SMCLK is sourced by the DCO, it is not masked on exit from LPM3 or LPM4. Therefore, SMCLK exceeds the programmed frequency of operation on exit from LPM3 and LPM4 for up to 6 us. The increased frequency has the potential to

change the expected timing behavior of peripherals that select SMCLK as the clock source.

Workaround   - Use XT2 as the SMCLK oscillator source instead of the DCO.

or

- Do not disable the clock request bit for SMCLKREQEN in the Unified Clock System Control 8 Register (UCSCTL8). This means that all modules that depend on SMCLK to operate successfully should be halted or disabled before entering LPM3 or LPM4. If the increased frequency prevents the proper function of an affected module, wait 32, 48, 80, or 100 cycles for core voltage levels 0, 1, 2, or 3, respectively, before re-enabling the module [for example, __delay_cycles(100)].

PMM14   *PMM Module*

Function   Increasing the core level when SVS/SVM low side is configured in full-performance mode causes device reset

Description   When the SVS/SVM low side is configured in full performance mode (SVSMLCTL.SVSLFP = 1), the setting time delay for the SVS comparators is ~2us. When increasing the core level in full-performance mode; the core voltage does not settle to the new level before the settling time delay of the SVS/SVM comparator expires. This results in a device reset.

Workaround   When increasing the core level; enable the SVS/SVM low side in normal mode (SVSMLCTL.SVSLFP=0). This provides a settling time delay of approximately 150us allowing the core sufficient time to increase to the expected voltage before the delay expires.

PMM18   *PMM Module*

Function   PMM supply overvoltage protection falsely triggers POR

Description   The PMM Supply Voltage Monitor (SVM) high side can be configured as overvoltage protection (OVP) using the SVMHOVPE bit of SVSMHCTL register. In this mode a POR should typically be triggered when DVCC reaches ~3.75V.

If the OVP feature of SVM high side is enabled going into LPM234, the SVM might trigger at DVCC voltages below 3.6V (~3.5V) within a few ns after wake-up. This can falsely cause an OVP-triggered POR. The OVP level is temperature sensitive during fail scenario and decreases with higher temperature (85 degC ~3.2V).

Workaround   Use Adaptive mode (SVMACE=1). The SVM high side is inactive in LPM234.

PMM20   *PMM Module*

Function   Unexpected SVSL/SVML event during wakeup from LPM2/3/4 in fast wakeup mode

Description   If PMM low side is configured to operate in fast wakeup mode, during wakeup from LPM2/3/4 the internal VCORE voltage can experience voltage drop below the corresponding SVSL and SVML threshold (recommendation according to User's Guide) leading to an unexpected SVSL/SVML event. Depending on PMM configuration, this event triggers a POR or an interrupt.

NOTE: As soon the SVSL or the SVML is enabled in Normal performance mode the device is in slow wakeup mode and this erratum does not apply.

In addition, this erratum has sporadic characteristic due to an internal asynchronous circuit. The drop of Vcore does not have an impact on specified device performance.

Workaround   If SVSL or SVML is required for application (to observe external disruptive events at Vcore pin) the slow wakeup mode has to be used to avoid unexpected SVSL/SVML events. This is achieved if the SVSL or the SVML is configured in "Normal" performance mode (not disabled and not in "Full" Performance Mode).

PORT15   *PORT Module*

Function   In-system debugging causes the PMALOCKED bit to be always set

Description   The port mapping controller registers cannot be modified when single-stepping or halting at break points between a valid password write to the PMAPWD register and the expected lock of the port mapping (PMAP) registers. This causes the PMAPLOCKED bit to remain set and not clear as expected.

Note: This erratum only applies to in-system debugging and is not applicable when operating in free-running mode.

Workaround   Do not single step through or place break points in the port mapping configuration section of code.

PORT19   *PORT Module*

Function   Port interrupt may be missed on entry to LPMx.5

Description   If a port interrupt occurs within a small timing window (~1MCLK cycle) of the device entry into LPM3.5 or LPM4.5, it is possible that the interrupt is lost. Hence this interrupt will not trigger a wakeup from LPMx.5.

Workaround   None

RTC3   *RTC Module*

Function   Unreliable write to RTC register

Description   A write access to the RTC registers (SEC, MIN, HOUR, DATE, MON, YEAR, DOW) may result in unexpected results. As a consequence the addressed register might not contain the written data, or some data can be accidentally written to other RTC registers.

Workaround   Use the RTC library routines, available as F541x/F543x code examples on the MSP430 Code Examples page (www.ti.com/msp430 > Software > Code Examples), which use carefully aligned MOV instructions. Library is listed as RTC_Workaround.zip and includes both CCE and IAR example projects that show proper usage. Using this library, full access to RTC registers is possible.

RTC6   *RTC Module*

Function   the step size of the RTC frequency adjustment is twice the specified size.

Description   The step size of the RTC frequency adjustment is =4ppm/-8ppm. This is twice the size specified in the User's Guide.

For up calibration this results in a step size per step of 8ppm (1024 cycles) instead of 4ppm (512 cycles). For down calibration this results in a step size per step of 4ppm (512 cycles) instead of 2ppm (256 cycles).

Workaround   Half the calibration value written into RTCCAL register to compensate the doubled step size.

SYS12   *SYS Module*

Function   Invalid ACCVIFG when DVcc in the range of 2.4 to 2.6V

Description   A Flash Access Violation Interrupt Flag (ACCVIFG) may be triggered by the Voltage Changed During Program Error bit (VPE) when DVcc is in the range of 2.4 to 2.6V. Although this behavior is expected according to the user's guide, the VPE does not signify an invalid flash operation has occured.

If the ACCVIE bit is set and a flash operation is executed in the affected voltage range, an unnecessary interrupt is requested. The bootstrap loader also cannot be used to execute write/erase flash operations in this voltage range, because it exits the flash operation and returns an error on an ACCVIFG event.

Workaround   None

SYS16   *SYS Module*

Function   Fast Vcc ramp after device power up may cause a reset

Description   At initial power-up, after Vcc crosses the brownout threshold and reaches a constant level, an abrupt ramp of Vcc at a rate dV/dT > 1V/100us can cause a brownout condition to be incorrectly detected even though Vcc does not fall below the brownout threshold. This causes the device to undergo a reset.

Workaround   Use a controlled Vcc ramp to power up the device.

UCS7   *UCS Module*

Function   DCO drifts when servicing short ISRs when in LPM0 or exiting active from ISRs for short periods of time

Description   The FLL uses two rising edges of the reference clock to compare against the DCO frequency and decide on the required modifications to the DCOx and MODx bits. If the device is in a low power mode with FLL disabled (LPM0 with DCO not sourcing ACLK/SMCLK or LPM2, LPM3, LPM4 where SCG1 bit is set) and enters a state which enables FLL (enter ISR from LPM0/LPM2 or exit active from ISRs) for a period less than 3x reference clock cycles, then the FLL will cause the DCO to drift.

This occurs because the FLL immediately begins comparing an active DCO with its reference clock and making the respective modifications to the DCOx and MODx bits. If the FLL is not given sufficient time to capture a full reference clock cycle (2 x reference clock periods) and adjust accordingly (1 x reference clock period), then the DCO will keep drifting each time the FLL is enabled.

Workaround   (1) If DCO is not sourcing ACLK or SMCLK in the application, use LPM1 instead of LPM0 to make sure FLL is disabled when interrupt service routine is serviced.

(2) When exiting active from ISRs, insert a delay of at least 3 x reference clock periods. To save on power budget, the 3 x reference clock periods could also be spent in LPM0 with TimerA or TimerB using ACLK/SMCLK sourced from DCO. This way, the FLL and DCO are still active in LPM0.

UCS9   *UCS Module*

Function   Digital Bypass mode prevents entry into LPM4

Description   When entering LPM4, if an external digital input applied to XT1 in HF mode or XT2 is not turned off, the PMM does not switch to low-current mode causing higher than expected power consumption.

Workaround   Before entering LPM4:

(1) Switch to a clock source other than external bypass digital input.

OR

(2) Turn off external bypass mode (UCSCTL6.XT1BYPASS = 0).

UCS11   *UCS Module*

Function   Modifying UCSCTL4 clock control register triggers an erroneous clock source request

Description   Changing the SELM/SELS/SELA bits in the UCSCTL4 register might trigger the respective clocks to select an incorrect clock source which requests the XT1/XT2 clock. If the crystals are not present at XT1/XT2 or present but not yet configured in the application firmware, then the respective XT1/XT2 fault flag is falsely set.

Workaround   Clear all the fault flags in UCSCTL7 register once after changing any of the SELM/SELS/SELA bits in the UCSCTL4 register.

USCI26   *USCI Module*

Function   Tbuf parameter violation in I2C multi-master mode

Description   In multi-master I2C systems the timing parameter Tbuf (bus free time between a stop condition and the following start) is not guaranteed to match the I2C specification of 4.7us in standard mode and 1.3us in fast mode. If the UCTXSTT bit is set during a running I2C transaction, the USCI module waits and issues the start condition on bus release causing the violation to occur.

Note: It is recommended to check if UCBBUSY bit is cleared before setting UCTXSTT=1.

Workaround   None

USCI35   *USCI Module*

Function   Violation of setup and hold times for (repeated) start in I2C master mode

Description   In I2C master mode, the setup and hold times for a (repeated) START, $t_{SU,STA}$ and $t_{HD,STA}$ respectively, can be violated if SCL clock frequency is greater than 50kHz in standard mode (100kbps). As a result, a slave can receive incorrect data or the I2C bus can be stalled due to clock stretching by the slave.

Workaround   If using repeated start, ensure SCL clock frequencies is < 50kHz in I2C standard mode
                        (100 kbps).

5   Document Revision History

Changes from device specific erratasheet to document Revision A.

1. Errata PMM15 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata DMA10 was added to the errata documentation.
2. Errata BSL7 was added to the errata documentation.
3. Errata RTC3 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. DMA10 Description was updated.
2. DMA10 Function was updated.

Changes from document Revision C to Revision D.

1. DMA10 Description was updated.
2. Errata EEM23 was added to the errata documentation.

Changes from document Revision D to Revision E.

1. SYS16 Description was updated.
2. Errata PMM15 was removed from the errata documentation.
3. Device TLV Hardware Revision information added to erratasheet.

Changes from document Revision E to Revision F.

1. Errata PMM20 was added to the errata documentation.
2. Errata USCI35 was added to the errata documentation.

Changes from document Revision F to Revision G.

1. BSL7 Workaround was updated.
2. BSL7 Function was updated.
3. Errata SYS12 was added to the errata documentation.

Changes from document Revision G to Revision H.

1. EEM19 Workaround was updated.
2. EEM17 Workaround was updated.
3. EEM23 Workaround was updated.
4. EEM17 Description was updated.
5. Errata BSL11 was added to the errata documentation.
6. EEM23 Description was updated.
7. EEM19 Description was updated.

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