MSP430FR5723 Device Erratasheet

1 Revision History

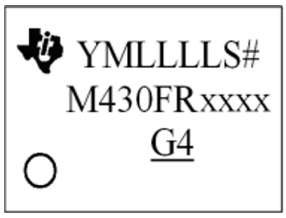
✓ The check mark indicates that the issue is present in the specified revision.

The revision of the device can be identified by the revision letter on the Package Markings or by the HW_ID located inside the TLV structure of the device

Errata Number	Rev H
CPU40	✓
DMA9	✓
DMA10	✓
EEM19	✓
EEM23	✓
MPY1	✓
PORT16	✓
PORT19	✓
USCI36	✓
USCI37	✓
WDG6	✓
XOSC13	✓

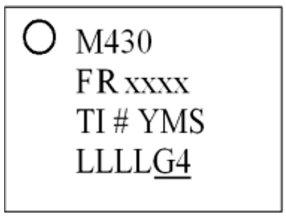
2 Package Markings

DA38 *TSSOP (DA), 38 Pin*



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RHA40 *QFN (RHA), 40 Pin*



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
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o = PIN 1

3 TLV Hardware Revision

Die Revision	TLV Hardware Revision
Rev H	24h

Further guidance on how to locate the TLV structure and read out the HW_ID can be found in the device User's Guide.

4 Detailed Bug Description

CPU40 *CPUXv2 Module*

Function

PC is corrupted when executing jump/conditional jump instruction that is followed by instruction with PC as destination register or a data section

Description

If the value at the memory location immediately following a jump/conditional jump instruction is 0X40h or 0X50h (where X = don't care), which could either be an instruction opcode (for instructions like RRCM, RRAM, RLAM, RRUM) with PC as destination register or a data section (const data in flash memory or data variable in

RAM), then the PC value is auto-incremented by 2 after the jump instruction is executed; therefore, branching to a wrong address location in code and leading to wrong program execution.

For example, a conditional jump instruction followed by data section (0140h).

@0x8012 Loop DEC.W R6

@0x8014 DEC.W R7

@0x8016 JNZ Loop

@0x8018 Value1 DW 0140h

Workaround

In assembly, insert a NOP between the jump/conditional jump instruction and program code with instruction that contains PC as destination register or the data section.

DMA9 *DMA Module*

Function

DMA stops transferring bytes unexpectedly

Description

When the DMA is configured to transfer bytes from the eUSCI_A transmit or receive buffers, the transmit or receive triggers (TXIFG and RXIFG) may not be seen by the DMA module and the transfer of the bytes is missed. Once the first byte in a transfer sequence is missed, all the following bytes are missed as well. All eUSCI_A modes, including UART, SPI, and IrDA, are affected. DMA transfers from eUSCI_B modes, including SPI and I2C, are not affected.

Workaround

None. Use Interrupt Service Routines to transfer data to and from the eUSCI_A.

DMA10 *DMA Module*

Function

DMA interrupting CPU wait state might cause peripheral module into unknown state.

Description

When the CPU accesses a module that is capable of stalling the CPU with a wait mechanism, if a DMA interrupts the instruction during the CPU stall, the module might be caused into an unknown state.

The affected modules (if present on the device) that can stall CPU are: FRAM controller in manual timing mode, MPY, CRC, USB, and RF1A.

As an example a wrong result can be read by DMA from MPY result register because the DMA does not wait until MPY operation is finished.

Workaround

Disable DMA when using affected modules.

EEM19 *EEM Module*

Function

DMA may corrupt data in debug mode

Description When the DMA is enabled and the device is in debug mode, the data transferred by the DMA may be corrupted when a breakpoint is hit or when the debug session is halted.

Workaround None. Do not set a breakpoint during a DMA transfer.

NOTE: This erratum applies to debug mode only.

EEM23 *EEM Module*

Function EEM functions do not work reliably when modules using wait cycles are enabled

Description When modules using wait states (USB, MPY,CRC and FRAM controller in manual mode) are enabled the EEM may not perform profile counter and state storage functions reliably.

Workaround Do not enable profile counter and state storage functions when modules using wait states are enabled.

NOTE: This erratum affects debug mode only.

MPY1 *MPY32 Module*

Function Save and Restore feature on MPY32 not functional

Description The MPY32 module uses the Save and Restore method which involves saving the multiplier state by pushing the MPY configuration/operand values to the stack before using the multiplier inside an Interrupt Service Routine (ISR) and then restoring the state by popping the configuration/operand values back to the MPY registers at the end of the ISR. However due to the erratum the Save and Restore operation fails causing the write operation to the OP2H register right after the restore operation to be ignored as it is not preceded by a write to OP2L register resulting in an invalid multiply operation.

Workaround None. Disable interrupts when writing to OP2L and OP2H registers.

Note: When using the C-compiler, the interrupts are automatically disabled while using the MPY32

PORT16 *PORT Module*

Function GPIO pins are driven low during device start-up

Description During device start-up, all of the GPIO pins are expected to be in the floating input state. Due to this erratum, some of the GPIO pins are driven low for the duration of boot code execution during device start-up, if an external reset event (via the RST pin) interrupted the previous boot code execution. Boot code is always executed after a BOR, and the duration of this boot code execution is approximately 500us.

For a given device family, this erratum affects only the GPIO pins that are not available in the smallest package device family member, but that are present on its larger package variants.

NOTE: This erratum does not affect the smallest package device variants in a particular device family.

Workaround Ensure that no external reset is applied via the RST pin during boot code execution of the device, which occurs 1us after device start-up.

NOTE: System application needs to account for this erratum in to ensure there is no increased current draw by the external components or damage to the external components in the system during device start-up.

PORT19 *PORT Module*

Function Port interrupt may be missed on entry to LPMx.5

Description If a port interrupt occurs within a small timing window (~1MCLK cycle) of the device entry into LPM3.5 or LPM4.5, it is possible that the interrupt is lost. Hence this interrupt will not trigger a wakeup from LPMx.5.

Workaround None

USCI36 *eUSCI Module*

Function UCLKI not usable in I2C master mode

Description When EUSCIB is configured as I2C Master with the external UCLKI as clock source, the UCLKI signal is not available and cannot be used to source I2C clock.

Workaround Use LFXTCLK via ACLK or HFXTCLK via SMCLK as clock source (BRCLK) for I2C in master mode with external clock source.

USCI37 *eUSCI Module*

Function Reading RXBUF during an active I2C communication might result in unintended bus stalls.

Description The falling edge of SCL bus line is used to set an internal RXBUF-written flag register, which is used to detect a potential RXBUF overflow. If this flag is cleared with a read access from the RXBUF register during a falling edge of SCL, the clear condition might be missed. This could result in an I2C bus stall at the next received byte.

Workaround (1) Execute two consecutive reads of RXBUF, if $t_{SCL} > 4 \times t_{IFCLK}$.

or

(2) Provoke an I2C bus stall before reading RXBUF. A bus stall can be verified by checking if the clock line low status indicator bit UCSCLLOW is set for at least three USCI bit clock cycles i.e. $3 \times t_{BitClock}$.

WDG6 *WDT_A Module*

Function Clock Fail-Safe feature in LPMx.5

Description The watchdog clock fail-safe feature does not prevent the device from going into LPMx.5. As a result, the device enters LPMx.5 state independently of running the watchdog. Note that the watchdog is off in LPMx.5.

Workaround None.

XOSC13 *XOSC Module*

Function XT1 in bypass mode does not work with RTC enabled

Description When the RTC module is enabled and XT1 is configured in bypass mode to be sourced by an external digital signal, the XT1OFFG flag is set indefinitely, resulting in ACLK defaulting its clock source to VLO instead of XT1.

Workaround Do not use RTC module with XT1 in bypass mode with external digital clock source.

5 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Revision F was removed
2. Revision G was removed

Changes from device specific erratasheet to document Revision A.

1. Errata PORT19 was added to the errata documentation.
2. Module name for MPY1 was modified.
3. Errata DMA9 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata XOSC13 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Errata DMA10 was added to the errata documentation.

Changes from document Revision C to Revision D.

1. DMA10 Description was updated.
2. DMA10 Function was updated.

Changes from document Revision D to Revision E.

1. DMA10 Description was updated.
2. Errata WDG6 was added to the errata documentation.
3. MPY1 Description was updated.
4. Errata EEM23 was added to the errata documentation.

Changes from document Revision E to Revision F.

1. DMA9 Description was updated.
2. DMA9 Workaround was updated.
3. Device TLV Hardware Revision information added to erratasheet.

Changes from document Revision F to Revision G.

1. Errata USCI37 was added to the errata documentation.

Changes from document Revision G to Revision H.

1. EEM19 Workaround was updated.
2. PORT16 Workaround was updated.
3. EEM23 Workaround was updated.
4. EEM23 Description was updated.
5. Errata USCI36 was added to the errata documentation.
6. PORT16 Description was updated.
7. EEM19 Description was updated.

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