PGA400-Q1 EVM User Guide

Mixed Signal Automotive

Car Information Systems

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the PGA400-Q1EVM. An EVM overview, GUI description, interface requirements, and complete schematic are included.

How to Use This Manual

This document contains the following chapters:

- Section 1 – Power Supply Requirements and Connections
- Section 2 – Jumper Settings
- Section 3 – PGA400-Q1 Sensor Inputs and Simulators
- Section 4 – PGA400-Q1 VOUT1/VOUT2 Circuitry
- Section 5 – PGA400-Q1 Communication Interfaces
- Section 6 – Controlling the PGA400-Q1 Memory Spaces with the GUI
- Section 7 – Controlling the PGA400-Q1 Functions with the GUI
- Section 8 – Controlling the EVM peripherals with the GUI
- Section 9 – PGA400-Q1 EVM Schematics and Layout

EVM Overview

Features

- Single +12VDC power-supply input for basic operation
- Resistive and Capacitive Sensor Simulators
- PC Control with a Graphical User Interface and USB Communications Board
- One-Wire-Interface (OWI) Activation and Communication Circuitry
- RS-232 transceiver for UART testing and debug

Introduction

The PGA400-Q1 is a generic sensor interface IC for resistive and capacitive sensors. It features a configurable Analog Front-End (AFE) with diagnostics, Sigma-Delta ADC, 8051 microcontroller, DACs, SPI, I2C, and a One-Wire Interface (OWI).

1 Power Supply Requirements and Connections

There is only one main +9VDC - +12VDC power connector on the PGA400-Q1EVM that supplies power to the entire board. The user is required to connect a power supply to the banana jacks, P1 “VPWR” and P3 “GND” or use the screw terminal P2. An example using the banana jack connections can be seen in the figure below.

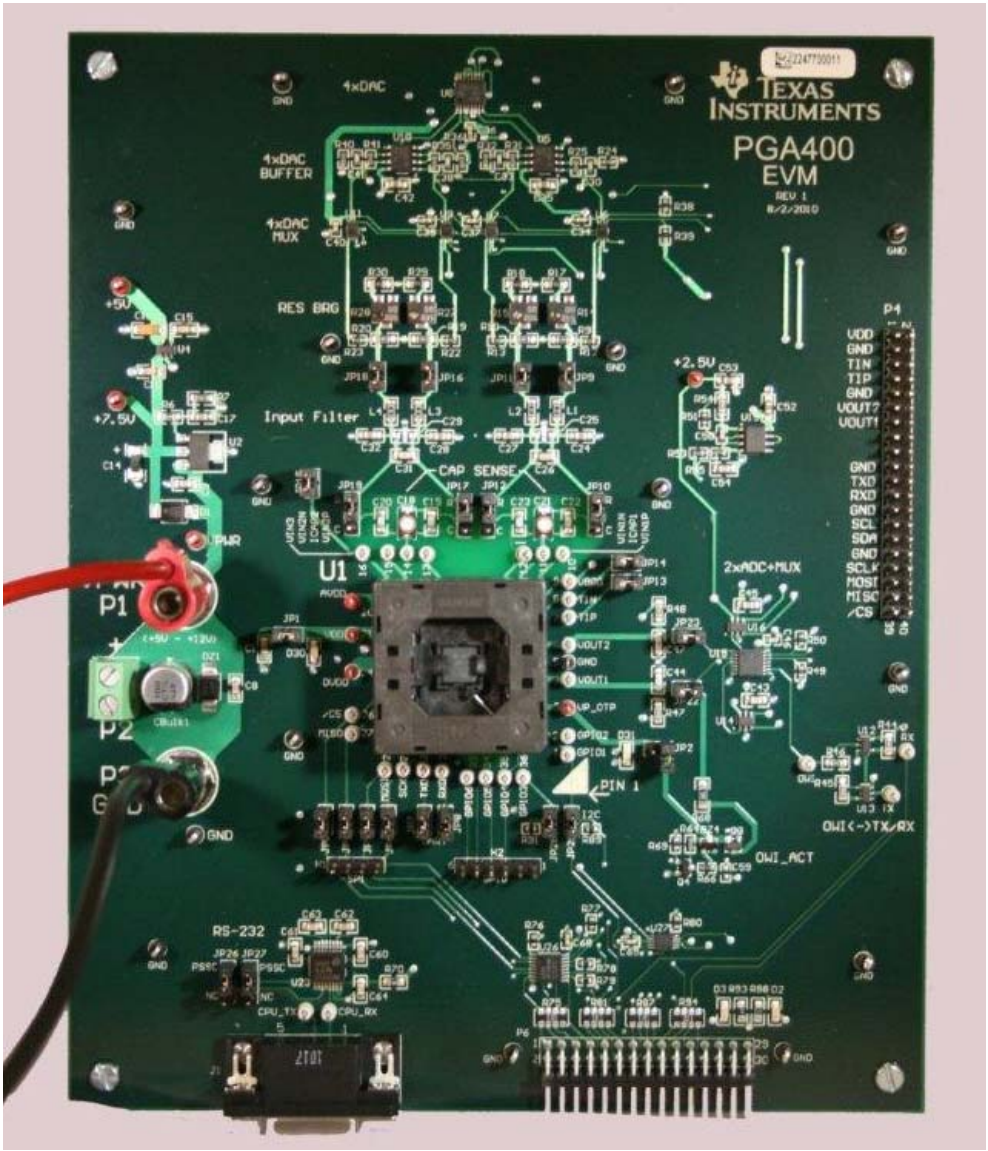


Figure 1. Minimum Power Connections to the PGA400-Q1 EVM

Configure the power supply based on the table below:

Connection	Voltage	Current Limit
VPWR	+9 – +12VDC	100mA

When powered, the “D30” LED should illuminate and the EVM should draw between 30 and 55mA depending on what state of operation it is in.

Figure 2. Minimum Power Supply Connections to Operate the R2D2 EVM

1.1 Controlling and Powering the R2D2 EVM via TI-GER USB board

The PGA400-Q1 EVM is shipped with a TI-GER USB communication board that provides a link from the PC controlled GUI (described later) to the EVM. The user must connect the TI-GER board to the PGA400-Q1 by connecting the 15x2 100mil female header on the TI-GER board to P6, the male 15x2 header on the PGA400-Q1 EVM. The TI logo on the TI-GER board should face up when it is plugged in. The figure below shows the TI-GER board connected to the PGA400-Q1 EVM.

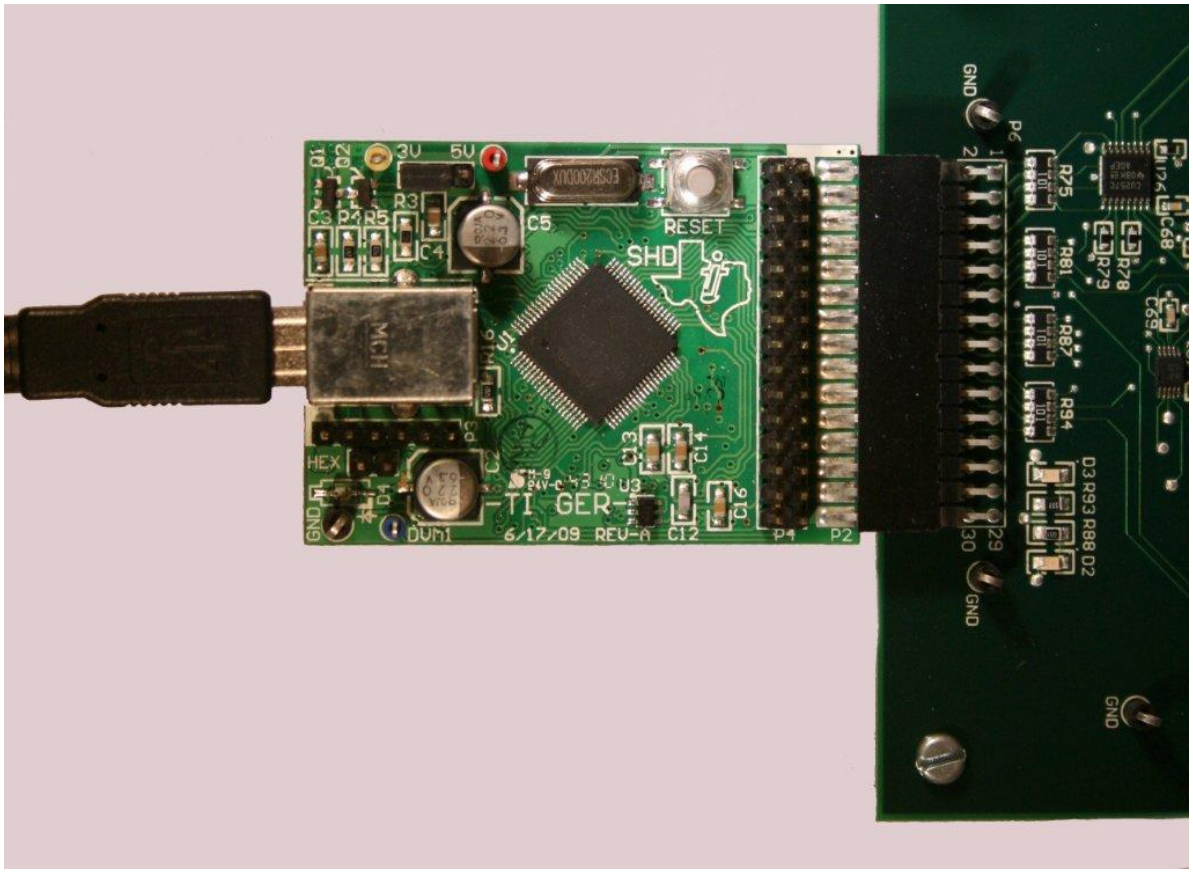


Figure 3. Connecting the TI-GER USB Communication Board to the PGA400-Q1 EVM

1.2 Power Supply LEDs

LEDs are installed in several places on the EVM to provide the user indication that power-supplies are connected correctly. The VDD and VP_OTP connections on the PGA400-Q1 have LEDs to indicate that power is applied. Also, there are two LEDS that indicate that the USB power supplies on the TI-GER boards are present.

LED	Supply
D2	TI-GER 3.3V
D3	TI-GER 5V
D30	PGA400-Q1 VDD
D31	PGA400-Q1 VP_OTP

Table 1. Power Supply LED Connections

2 Jumper Settings

There are several jumpers located on the board used to configure the connections to the PGA400-Q1 and the rest of the EVM. Although they are installed to default settings in the factory it is recommended that the user verify that the shunts are installed to their default settings before powering on the EVM. The default settings and their effects are listed below.

2.1 Default Jumper Settings:

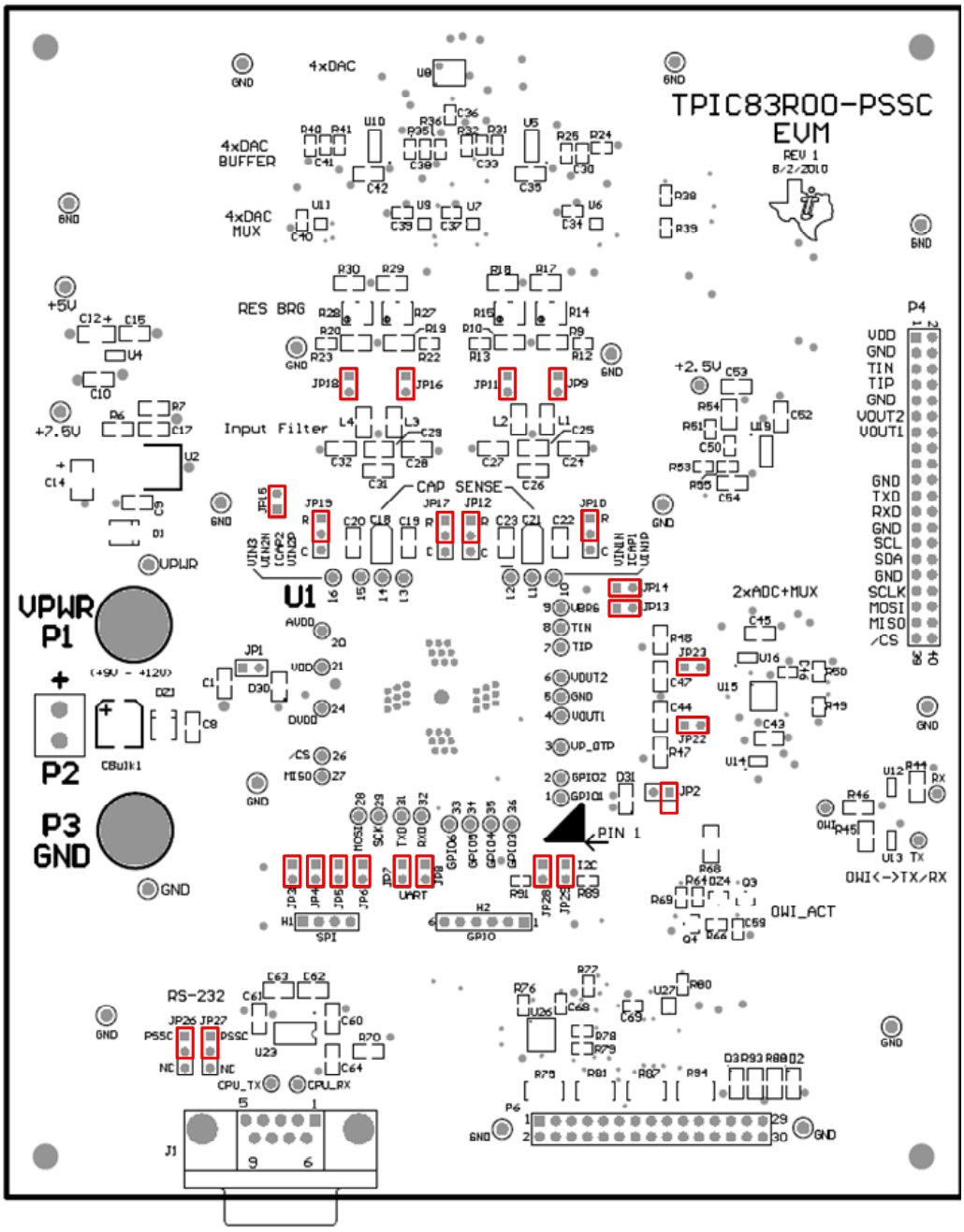


Figure 4. Default Jumper Settings

Reference	Jumper Position(s)	Function
JP1	Closed	The VDD power supply input on the PGA400-Q1 will be supplied from the +5V regulator on the EVM
JP2	Open	The VP_OTP power supply input on the PGA400-Q1 is not connected to the +7.5V regulator on the EVM
JP3	Closed	The /CS signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
JP4	Closed	The MISO signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
JP5	Closed	The MOSI signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
JP6	Closed	The SCLK signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
JP7	Closed	The TXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver
JP8	Closed	The RXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver
JP9	Closed	The VIN1P input filter is connected to the DAC MUX and variable resistive bridge.
JP10	Closed	The VIN1P signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
JP11	Closed	The VIN1N input filter is connected to the DAC MUX and variable resistive bridge.
JP12	1-2	The VIN1N signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
JP13	Closed	The TIP signal on the PGA400-Q1 is connected to the DAC MUX
JP14	Closed	The TIN signal on the PGA400-Q1 is connected to the DAC MUX
JP15	Closed	The VIN3 signal on the PGA400-Q1 is connected to the DAC MUX
JP16	Closed	The VIN2P input filter is connected to the DAC MUX and variable resistive bridge.
JP17	Closed	The VIN2P signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
JP18	Closed	The VIN2N input filter is connected to the DAC MUX and variable resistive bridge.
JP19	Closed	The VIN2N signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
JP22	Closed	The VOUT1 signal on the PGA400-Q1 is connected to the DAC Output MUX and to the P4 header
JP23	Closed	The VOUT2 signal on the PGA400-Q1 is connected to the DAC Output MUX and to the P4 header
JP26	1-2	The U23 RS-232 Transceiver TX signal is connected to the PGA400-Q1
JP27	1-2	The U23 RS-232 Transceiver RX signal is connected to the PGA400-Q1
JP28	Closed	The SCL signal from the TI-GER is connected to the GPIO_3 signal on the PGA400-Q1
JP29	Closed	The SDA signal from the TI-GER is connected to the GPIO_1 signal on the PGA400-Q1

Table 2. Default Jumper Settings

2.1.1 Jumper Setting Options

Table 3 below shows the function of each specific jumper setting on the EVM.

Reference	Jumper Setting	Function
JP1		The VDD power supply input on the PGA400-Q1 will be supplied from the +5V regulator on the EVM
		The VDD power supply input on the PGA400-Q1 will not be supplied from the +5V regulator on the EVM and can be connected to an external +5V power supply
JP2		The VP_OTP power supply input on the PGA400-Q1 is connected to the +7.5V regulator on the EVM
		The VP_OTP power supply input on the PGA400-Q1 is not connected to the +7.5V regulator on the EVM
JP3		The /CS signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
		The /CS signal from the TI-GER is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header
JP4		The MISO signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
		The MISO signal from the TI-GER is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header
JP5		The MOSI signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
		The MOSI signal from the TI-GER is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header
JP6		The SCLK signal from the TI-GER is connected to the PGA400-Q1 device in the U1 socket and to the P4 header
		The SCLK signal from the TI-GER is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header
JP7		The TXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver
		The TXD signal from the PGA400-Q1 device is not connected to the U23 RS-232 transceiver
JP8		The RXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver
		The RXD signal from the PGA400-Q1 device is not connected to the U23 RS-232 transceiver
JP9		The VIN1P input filter is connected to the DAC MUX and variable resistive bridge
		The VIN1P input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that will go through the input filter to the PGA400-Q1
JP10		The VIN1P signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
		The VIN1P signal on the PGA400-Q1 is connected to the capacitive sensor simulator on the EVM
		The VIN1P signal on the PGA400-Q1 is not connected to anything on the EVM

JP11		The VIN1N input filter is connected to the DAC MUX and variable resistive bridge
		The VIN1N input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that will go through the input filter to the PGA400-Q1
JP12		The VIN1N signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
		The VIN1N signal on the PGA400-Q1 is connected to the capacitive sensor simulator on the EVM
		The VIN1P signal on the PGA400-Q1 is not connected to anything on the EVM
JP13		The TIP signal on the PGA400-Q1 is connected to the DAC MUX and the P4 header.
		The TIP signal on the PGA400-Q1 is not connected to anything on the EVM. The TIP signal on the P4 header is still connected to the DAC MUX
JP14		The TIN signal on the PGA400-Q1 is connected to the DAC MUX
		The TIN signal on the PGA400-Q1 is not connected to anything on the EVM. The TIN signal on the P4 header is still connected to the DAC MUX
JP15		The VIN3 signal on the PGA400-Q1 is connected to the DAC MUX
		The VIN3 signal on the PGA400-Q1 is not connected to anything on the EVM
JP16		The VIN2P input filter is connected to the DAC MUX and variable resistive bridge
		The VIN2P input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that will go through the input filter to the PGA400-Q1
JP17		The VIN2P signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
		The VIN2P signal on the PGA400-Q1 is connected to the capacitive sensor simulator on the EVM
		The VIN2P signal on the PGA400-Q1 is not connected to anything on the EVM
JP18		The VIN2N input filter is connected to the DAC MUX and variable resistive bridge
		The VIN2N input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that will go through the input filter to the PGA400-Q1
JP19		The VIN2N signal on the PGA400-Q1 is connected to the resistive bridge sensor simulators and input filters on the EVM
		The VIN2N signal on the PGA400-Q1 is connected to the capacitive sensor simulator on the EVM
		The VIN2N signal on the PGA400-Q1 is not connected to anything on the EVM
JP22		The VOUT1 signal on the PGA400-Q1 is connected to the DAC Output MUX , the OWI activation circuit, and the P4 header
		The VOUT1 signal on the PGA400-Q1 is not connected to the DAC Output MUX and the OWI activation circuit. The VOUT1 signal on the P4 header is still connected to the DAC Output MUX
JP23		The VOUT2 signal on the PGA400-Q1 is connected to the DAC Output MUX , and the P4 header

		The VOUT2 signal on the PGA400-Q1 is not connected to the DAC Output MUX. The VOUT2 signal on the P4 header is still connected to the DAC Output MUX
JP26		The TXD signal on the PGA400-Q1 is connected to the RS-232 transceiver
		The TXD input of the RS-232 transceiver is not connected to the PGA400-Q1 and is open so an external signal can be connected
JP27		The RXD signal on the PGA400-Q1 is connected to the RS-232 transceiver
		The RXD input of the RS-232 transceiver is not connected to the PGA400-Q1 and is open so an external signal can be connected
JP28		The GPIO_3 signal on the PGA400-Q1 is connected to the SCL signal on the TI-GER and also to the P4 header
		The GPIO_3 signal on the PGA400-Q1 is not connected to the SCL signal on the TI-GER. The SCL signal from the TI-GER is still connected to the P4 header.
JP29		The GPIO_1 signal on the PGA400-Q1 is connected to the SDA signal on the TI-GER and also to the P4 header
		The GPIO_1 signal on the PGA400-Q1 is not connected to the SDA signal on the TI-GER. The SDA signal from the TI-GER is still connected to the P4 header.

Legend:  Indicates the corresponding pins that are shorted or closed.

Table 3. Jumper Setting Options

3 Sensor Inputs and Simulators

There are two main sensor Analog Front Ends (AFE) in the PGA400-Q1 sensor signal conditions, one targeted towards resistive or voltage based sensors and one targeted for capacitive sensors. The PGA400-Q1 EVM is equipped with simple circuits to simulate the basic functionality of these different sensors. Below is a simplified block diagram of the sensor simulators on the PGA400-Q1 EVM.

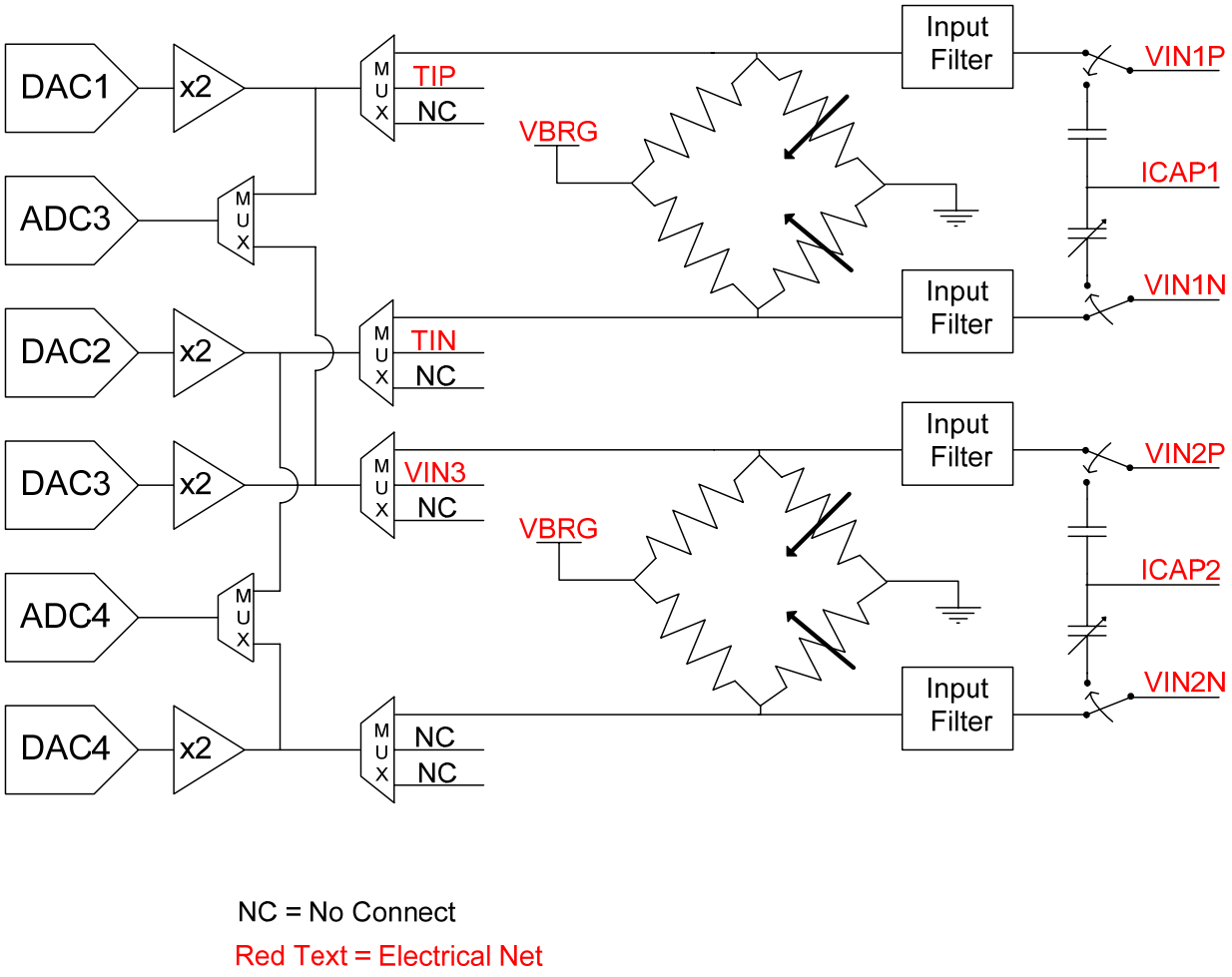


Figure 5. Simplified Block Diagram of PGA400-Q1 Input Circuitry

3.1 Resistive Bridge Sensors

There are two main ways to simulate a resistive bridge sensor on the PGA400-Q1 EVM. The first is a simple resistive bridge with two variable legs that can be used to adjust the voltage to the VIN1P/VIN1N and VIN2P/VIN2N inputs. The second uses 16-bit DACs and ADCs to set and measure the voltage at the inputs. Either one of these simulators can be fed through an input filter and then into the PGA400-Q1 inputs.

3.1.1 Variable Resistive Bridge

The EVM is equipped with a variable resistive bridge that can be used to adjust the voltage at the inputs of the PGA400-Q1. The bridge is biased with the VBRG regulator from the PGA400-Q1. The resistance of each leg of the bridge varies from 17.5k to 22.k. The figure below shows the channel 1 resistive bridge that is used to vary the voltage to the VIN1P/VIN1N inputs. The channel 2 resistive bridge is identical.

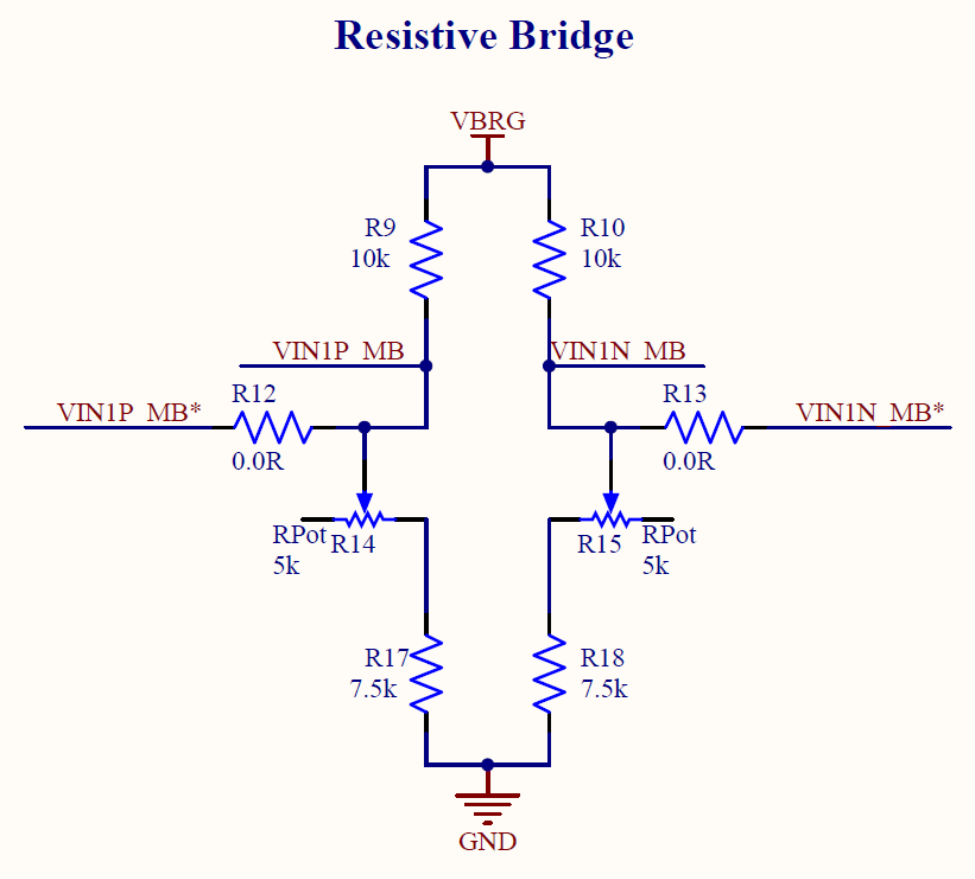


Figure 6. Channel 1 Resistive Bridge Sensor Simulator

3.1.2 Buffered DAC Outputs

The second way to excite the voltage inputs to the PGA400-Q1 is to use the buffered DAC outputs on the EVM. The DAC8574, a four-channel 16-bit DAC, is used to generate voltage signals that can be used to excite the VIN1P/VIN1N and VIN2P/VIN2N inputs. When the DAC MUX is set to the VIN1P/VIN1N and VIN2P/VIN2N sensor inputs, the DAC buffers over-drive the voltage that the resistive bridge was previously producing. The buffered DAC voltage is measured with the ADS1100, 16-bit ADCs, and then adjusted to servo out errors. The DACs are controlled with the GUI which will be described later in this guide. The figure below shows the DACs and the DAC buffers.

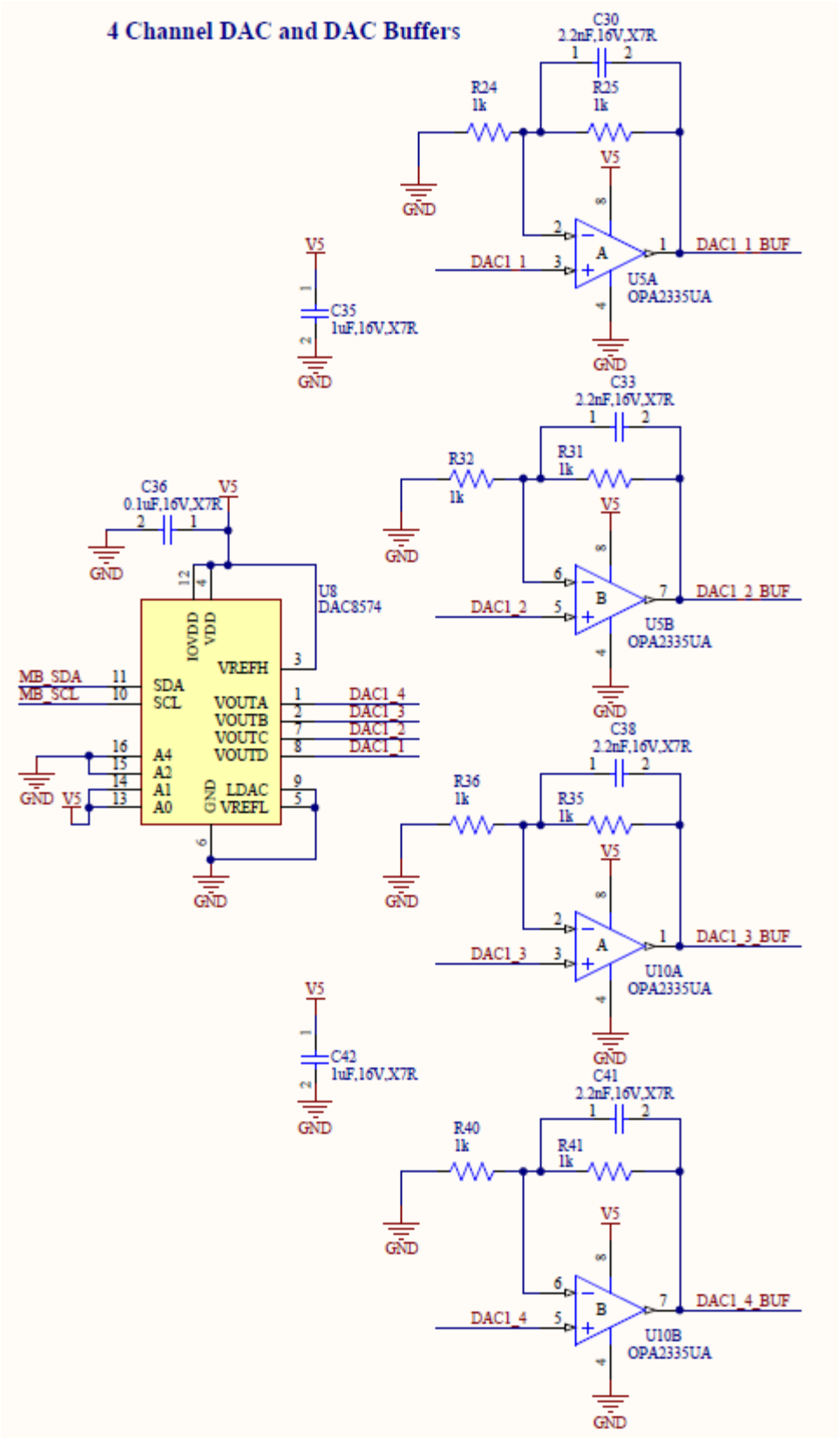

4 Channel DAC and DAC Buffers
C30
2.2nF,16V,X7R
R24
1k
R25
1k
V5
GND
DAC1_1
DAC1_1_BUF
U5A
OPA2335UA
C35
1uF,16V,X7R
C33
2.2nF,16V,X7R
R31
1k
R32
1k
C36
0.1uF,16V,X7R
U8
DAC8574
IOVDD
VDD
VREFH
SDA
SCL
VOUTA
VOUTB
VOUTC
VOUTD
LDAC
VREFL
A4
A2
A1
A0
MB_SDA
MB_SCL
DAC1_4
DAC1_3
DAC1_2
DAC1_1
DAC1_2
DAC1_2_BUF
U5B
OPA2335UA
C38
2.2nF,16V,X7R
R35
1k
R36
1k
DAC1_3
DAC1_3_BUF
U10A
OPA2335UA
C42
1uF,16V,X7R
C41
2.2nF,16V,X7R
R41
1k
R40
1k
DAC1_4
DAC1_4_BUF
U10B
OPA2335UA

Figure 7. DAC8574 and OPA2335 Buffers

3.1.3 Input Filters

Both the buffered DAC outputs and the Resistive Bridge outputs feed through the input filter on the EVM before they connect to the inputs to the PGA400-Q1. The input filter is comprised of a common-mode and differential filter made from ferrite beads and capacitors. When the EVM is delivered to the customer, the ferrite beads L1-L4 are populated with 49Ohm resistors so that the filters work as simple RC low-pass filters. If desired, the resistors can be replaced with ferrite beads that meet the requirements of the final customer system. Similarly, the EVM comes with an unpopulated footprint for an X2Y capacitor to replace the two common-mode and single differential cap. To use the X2Y, uninstall the three populated filter caps on the desired channels and install a single X2Y capacitor. The figure below shows the input filters on the EVM.

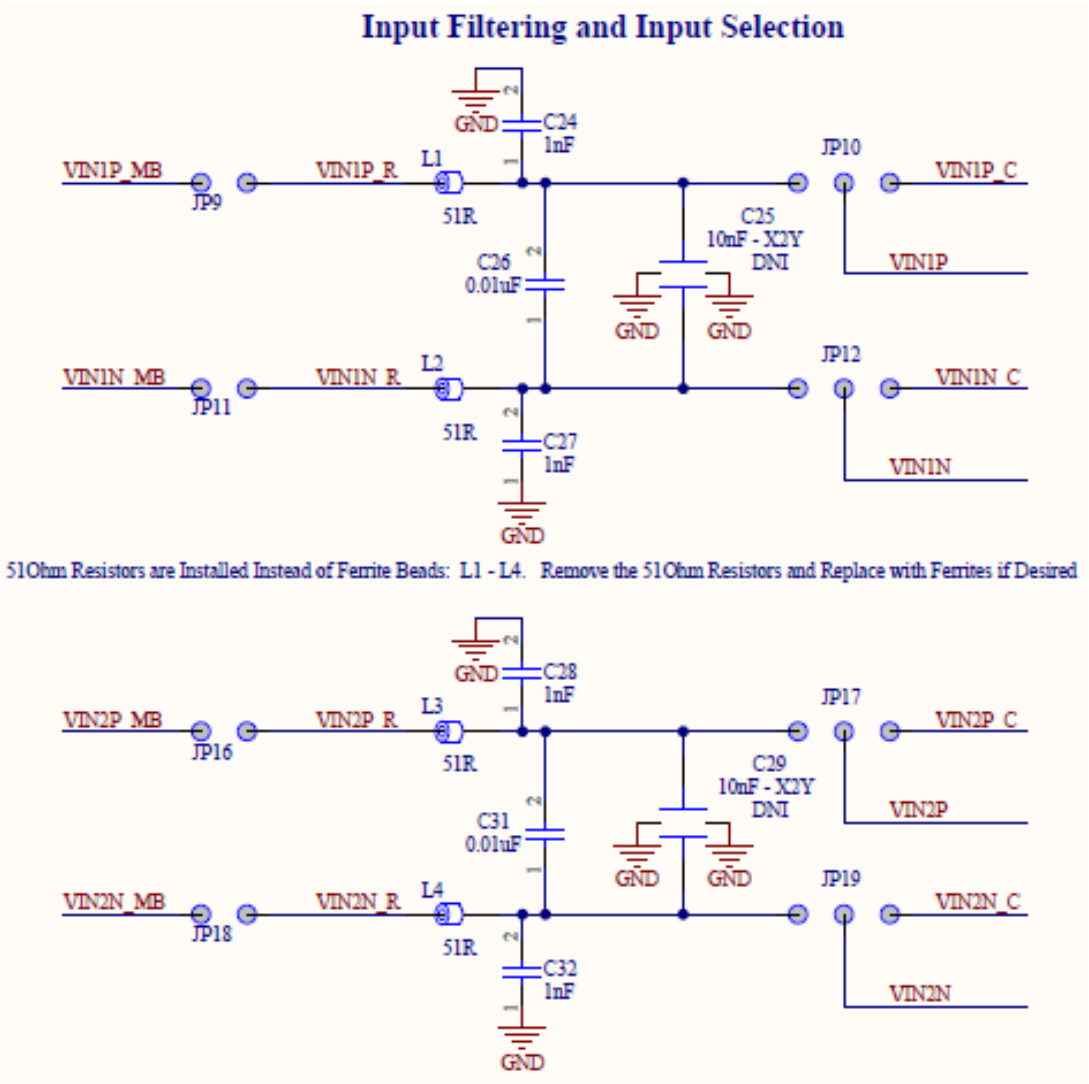


Figure 8. Input Filtering on the PGA400-Q1 EVM

3.2 Capacitive Sensors

There is only one way to easily simulate capacitive sensors on the PGA400-Q1 EVM. This method uses a fixed reference cap on one leg, and then a fixed cap in parallel with a variable trim cap on the other leg. The reference leg capacitance is set to 56pF, and the variable leg is adjustable from 35 – 80pF. The figure below shows the circuit for the capacitive sensor simulator.

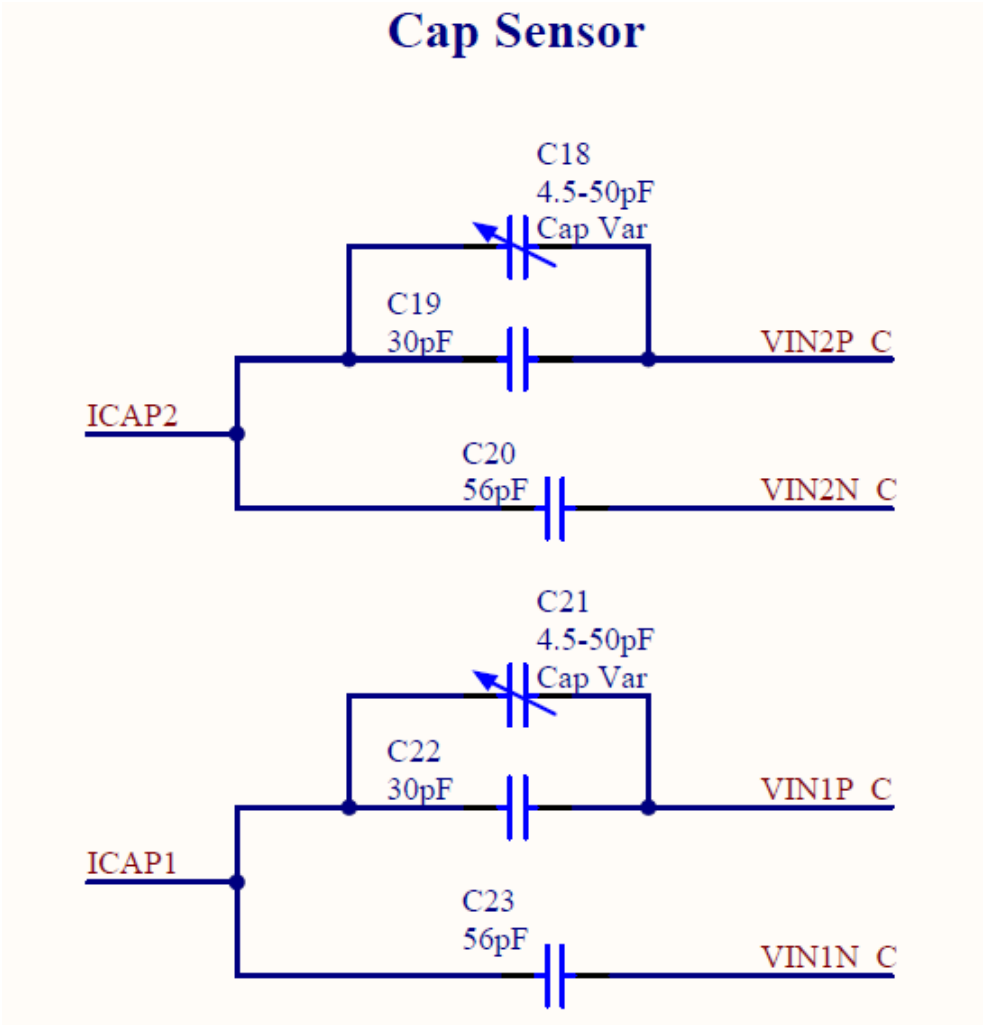


Figure 9. Capacitive Sensor Simulator

4 PGA400-Q1 VOUT1/VOUT2 Output Circuitry

There are two DAC outputs on the PGA400-Q1, VOUT1 and VOUT2, which serve as the main output for the PGA400-Q1 device. Simple circuitry including output filtering and ADC monitoring of the DAC outputs are present on the EVM. The VOUT1 output also has circuitry that is used for the OWI activation as well as the OWI communication.

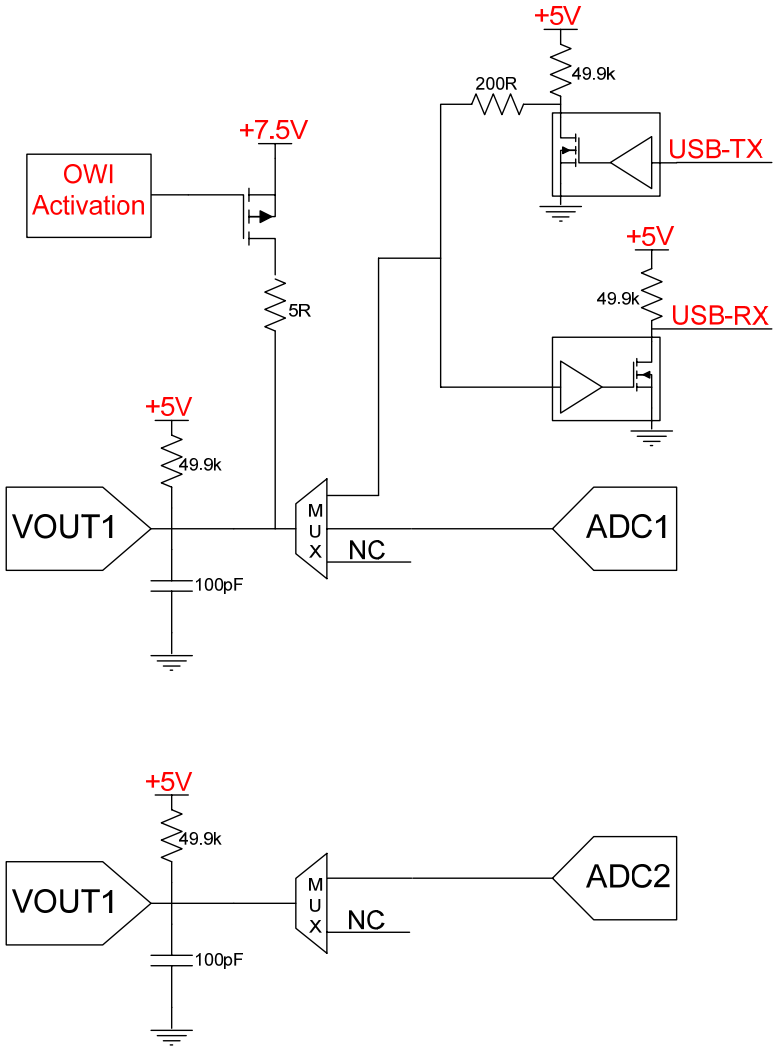


Figure 10. Simplified Block Diagram of PGA400-Q1 Output Circuitry

4.1 Output Filtering for VOUT1 and VOUT2

Both the VOUT1 and VOUT2 outputs on the PGA400-Q1 have simple output filtering comprised of a resistive pull-up and a capacitor to GND. The capacitor is used to form a low-pass filter with the output impedance of the VOUT1/VOUT2 DACs. The resistive pull-up is primarily used to fill the requirements for an external pull-up in OWI mode. Shown below are the output filters on the VOUT1/VOUT2 pins.

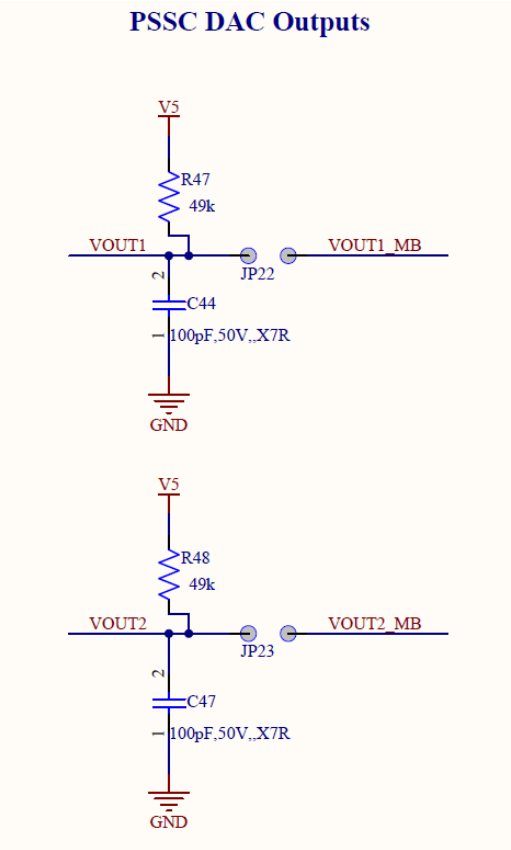


Figure 11. VOUT1/VOUT2 Output Filtering

4.2 ADC Measurement of VOUT1/VOUT2 DAC Outputs

The EVM comes equipped with two ADCs that are used to monitor and report the voltage at the VOUT1/VOUT2 outputs back to the GUI. The EVM uses two ADS1100, 16-bit ADCs, to monitor the two outputs. The ADCs are enabled by configuring the PGA400-Q1 DAC Output MUX to route the VOUT1/VOUT2 outputs into the ADCs. The PGA400-Q1 DAC Output MUX and the ADCs are all configurable with the GUI.

4.3 OWI Activation Circuitry – VOUT1

The VOUT1 pin on the PGA400-Q1 is shared between the DAC output and the OWI transceiver. When the PGA400-Q1 is running in MCU mode, the only way to signal to the IC that it needs to enter OWI mode is to use a pull-up to bring the VOUT1 pin of the device to 7.5V for at least 10ms before it is released back to its previous value. The OWI activation circuitry is comprised of a simple PMOS pull-up to 7.5V that is activated with a GPIO from the TI-GER USB Communication Board. The GUI ensures that the PGA400-Q1 DAC Output MUX is open while the OWI activation pulse occurs so that the 5V tolerant circuitry for the ADCs and the OWI transceiver are not damaged with the 7.5V pulse. The figure below shows the OWI Activation Circuit.

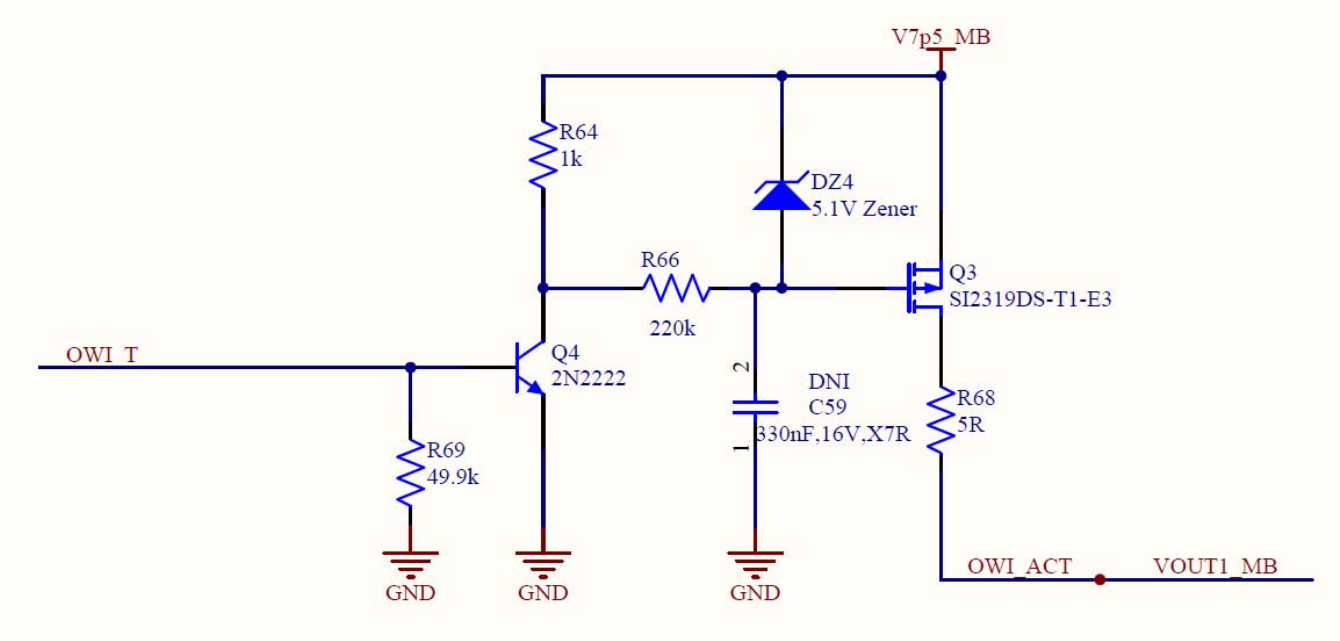


Figure 12. OWI Activation Circuit

4.4 OWI Transceiver – VOUT1

Once the OWI transceiver in the PGA400-Q1 has been activated either by the OWI activation pulse, or by a direct SPI write the TI-GER needs to communicate with the PGA400-Q1 with the proper OWI signals. A simple circuit is used to convert the two-signal TI-GER USART (TX/RX) into the single wire OWI signal. The circuit operates in a way that the receiver is always listening even while transmitting so there is always a loop-back feature that the GUI uses to ensure the correct information was transmitted out of the TI-GER. When a read is requested from the PGA400-Q1, the VOUT1 signal drives the OWI signal and the TI-GER receives it. There are no issues of possible bus contention and the OWI transceiver circuit ensures that only the RX line is affected by the data transmitted out of the PGA400-Q1. The OWI transceiver circuit is shown below.

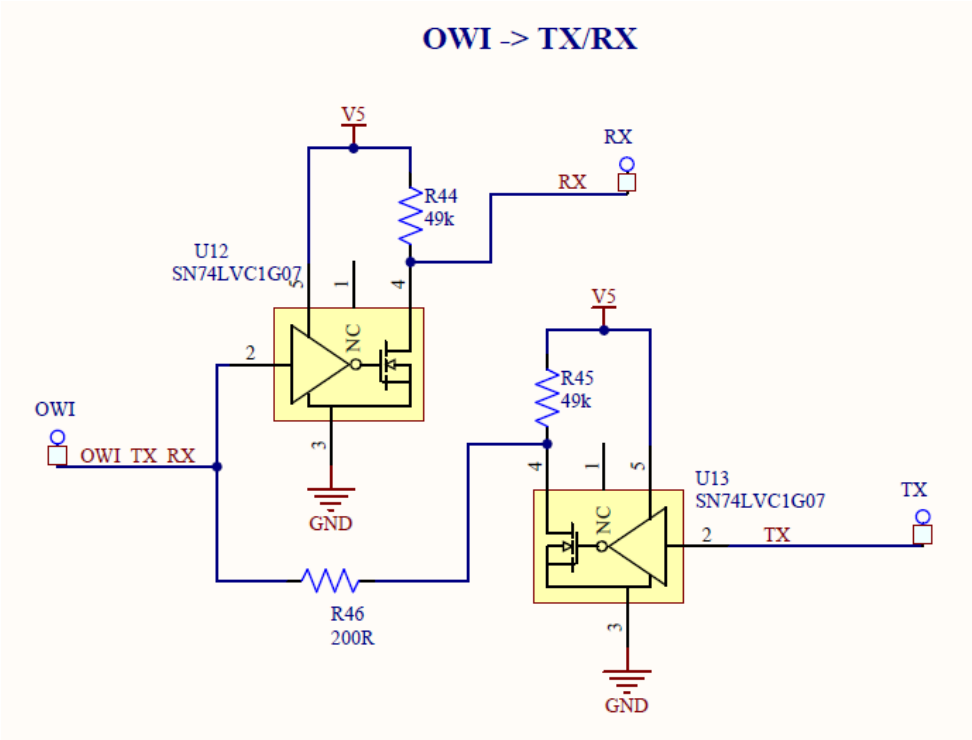


Figure 13. OWI Transceiver

5 PGA400-Q1 Communication Interfaces

The PGA400-Q1 has several communication options including: SPI, I2C, OWI, and UART. All of these communication interfaces and related circuitry are present on the PGA400-Q1 EVM.

5.1 SPI

SPI is the main communication method on the PGA400-Q1 and must be used to initially select one of the other communication methods (with the exception of the OWI activation pulse). Since the SPI and I2C pins are shared on the TI-GER communication board, a communication MUX is used to differentiate between the SPI and I2C functions on the EVM. By default the EVM powers up with the SPI communication interface selected and the user must change the setting on the communication MUX to change to I2C. The SPI signals can be monitored on the “H1” header on the EVM. Shown below is the SPI/I2C communication MUX.

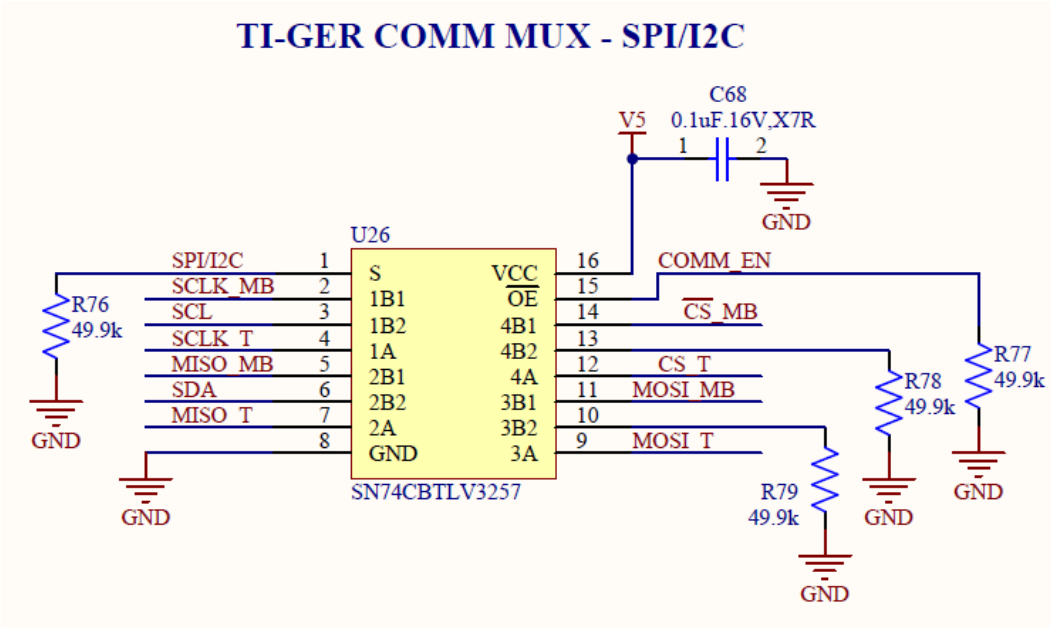


Figure 14. SPI/I2C Communication MUX

5.2 I2C

I2C is the second most common protocol for communicating with the PGA400-Q1 device. The I2C communication method must be selected in the PGA400-Q1 by sending the appropriate SPI commands before the communication will work. If the GUI is used to change from SPI to I2C mode, the GUI will configure the SPI/I2C MUX to send the I2C signals to the PGA400-Q1. I2C is also used as the main communication method for the DAC and ADC peripherals on the EVM. To avoid any conflicts between I2C signals meant for the PGA400-Q1 and I2C signals meant for the EVM peripherals, there is a second MUX installed that splits the I2C signals between the PGA400-Q1 and the rest of the EVM. The circuit of this MUX is shown below.

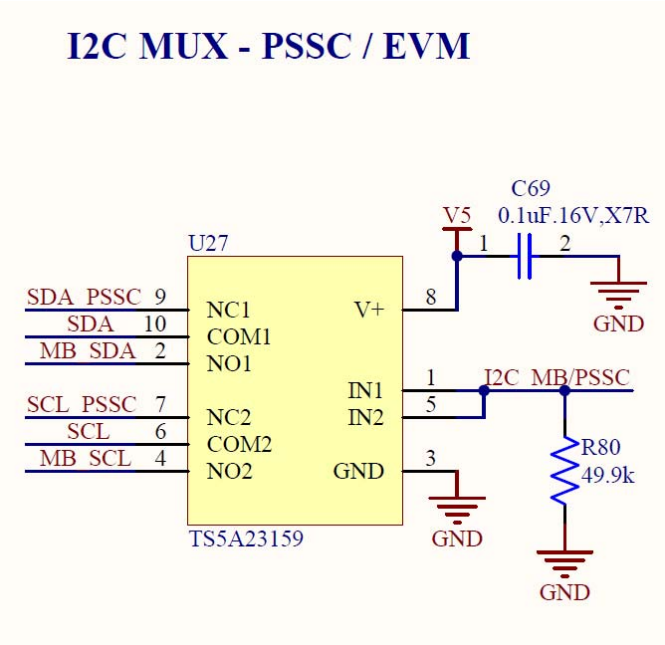


Figure 15. PGA400-Q1 / EVM I2C MUX

5.3 OWI

During final system calibration, the OWI communication method is preferred because it allows for a three-pin sensor module (Power, GND, VOUT/OWI). The OWI communication method can be selected in the PGA400-Q1 by either sending the appropriate SPI commands to place the device in OWI mode, or by issuing the OWI activation pulse and writing software in the 8051 to switch to OWI mode when the OWI activation pulse is detected. The GUI can be used to create the OWI activation signal as well as performing the direct SPI writes to place the EVM into OWI mode. If the GUI is used to send the signals to enter OWI mode, then the EVM will automatically be configured to route the TX/RX lines from the TI-GER through the OWI transceiver to the VOUT1 pin.

5.4 UART

An RS-232 transceiver (MAX3221) is present on the EVM that can be used as a debugging interface from the 8051 MCU to a host PC. The circuit connects the TXD and RXD pins on the PGA400-Q1 to the MAX3221. The +/-15V RS-232 signals are routed to a standard DB-9 connector on the EVM. The RS-232 circuit is shown below:

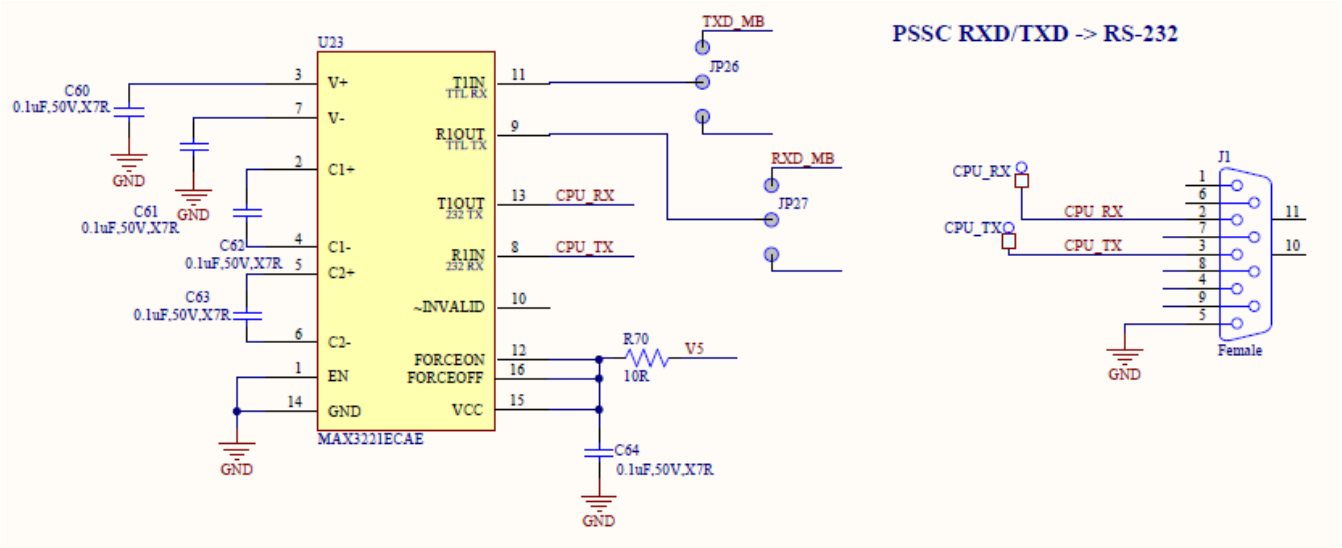


Figure 16. RS-232 Transceiver

6 Controlling the PGA400-Q1 Memory Spaces with the GUI

The PGA400-Q1 EVM is controlled by the user through a PC with the TI-GER USB communication board and associated GUI. The PGA400-Q1 EVM GUI provides ways to manipulate all of the register spaces present inside the PGA400-Q1 (TEST, ESFR, EEPROM, IRAM, OTP). The following sections describe how to manipulate the register spaces.

6.1 Using the Register Grids to Manipulate the Register Spaces

Most of the register spaces have register grids associated with them that provide a simple way to read/write the registers in the grid. There are eight buttons that are associated with the grid operations: “ZERO GRID”, “DESELECT GRID”, “SAVE GRID”, RECALL GRID”, “READ SELECTED”, “WRITE SELECTED”, “READ ALL”, and “WRITE ALL”. These buttons perform operations on whichever register grid is currently displayed. For example, when the GUI first loads the “TEST” register tab is displayed, if any of the previously listed buttons are pressed they will perform operations on the “TEST” register space. Each of the GRID functions are described below.

6.1.1 ZERO GRID

The “ZERO GRID” button will replace the contents of the entire grid with “0”.

6.1.2 DESELECT GRID

The “DESELECT GRID” button will remove any selections that have been made in the grid without performing any operations on the registers that were selected.

6.1.3 SAVE GRID

The “SAVE GRID” button will take the contents of the register grid and save them to a .TXT file. The data is saved in comma-separated-values format.

6.1.4 RECALL GRID

The “RECALL GRID” button will open a prompt that will allow the user to select a .TXT file that was produced during the “SAVE GRID” operation and will then load the grid with the contents from the .TXT file.

6.1.5 READ SELECTED

The “READ SELECTED” button will perform a read operation on any registers in the grid that have been selected by clicking the desired register number. Any selected registers will be displayed blue.

6.1.6 WRITE SELECTED

The “WRITE SELECTED” button will perform a write operation on any registers in the grid that have been selected by clicking the register number or modifying the register contents. Any selected registers will be displayed blue and any modified registers will be highlighted in yellow. Any blue or yellow registers will be written to when the “WRITE SELECTED” button is pressed.

6.1.7 READ ALL

The “READ ALL” button will perform a read operation on every register in the grid.

6.1.8 WRITE ALL

The “WRITE ALL” button will perform a write operation on every register in the grid.

6.2 Test Registers

By default, the GUI opens with the “TEST” register grid displayed. Besides the functions associated directly with the grid, the “TEST” tab includes two buttons related to the “TEST” registers.

6.2.1 IFSEL/uC_RST

The “IFSEL/uC_RST” button toggles bit0 and bit1 of register 0x0E. It is required to press this button to select SPI and shutdown the 8051 uC before most other commands on the GUI will take affect.

6.2.2 Restricted Access

As described in the PGA400-Q1 datasheet, to access some of the features in the TEST register map, a special unlock sequence must be sent to register 0xFF. The Restricted Access button sends this sequence to the PGA400-Q1 device.

6.3 ESFR Registers

The “ESFR” register tab only contains a grid that can be used with the functions described before to directly manipulate the “ESFR” register space. Most of the buttons on the right half of the GUI control bits in the ESFR register tab. These buttons will be described later.

6.4 EEPROM Registers

The EEPROM in the PGA400-Q1 is comprised of six banks of EEPROM (BANK_0 – BANK_5) and a shared cache. In the PGA400-Q1 GUI, each EEPROM BANK is given its own grid even though all operations are performed on the shared cache. As before, whichever BANK tab is displayed is the EEPROM bank that will be operated on. This is achieved by updating the EEPROM bank select bits in the TEST register space when the user selects a different EEPROM tab. By default, BANK_0 is selected. There are also four buttons on the EEPROM tab that will described below.

6.4.1 Auto Program EEPROM

The Auto Program EEPROM button uses the internal EEPROM charge pump and timer to enable and then disable the EEPROM charge pump after the programming time has been met. This button should be used if the user desires to burn the current EEPROM cache contents to the EEPROM bank.

6.4.2 PROG_ON

The PROG_ON button is used for a manual method of programming/testing the EEPROM. The PROG_ON button turns on the EEPROM charge pump. Since there is no timer to automatically turn the EEPROM charge pump back off, the user must press the “PROG_OFF” button to disable the charge-pump

6.4.3 PROG_OFF

The PROG_OFF button is used to complete a manual EEPROM programming by disabling the EEPROM charge pump.

6.4.4 Reload CACHE

The Reload CACHE button uses TEST register 0x0D to reload the CACHE with the contents of the selected EEPROM bank and then performs a “READ ALL” to update the grid with the refreshed contents of the EEPROM bank.

6.5 IRAM

The IRAM tab is setup only for individual register read/writes without the use of the grid. When this tab is displayed, the “READ SELECTED / READ ALL” and “WRITE SELECTED / WRITE ALL” buttons perform the same operations respectively.

6.6 OTP

The OTP tab is setup only for individual register read/writes without the use of the grid. When this tab is displayed, the “READ SELECTED / READ ALL” and “WRITE SELECTED / WRITE ALL” buttons perform the same operations respectively. The OTP tab also contains buttons used to load a .HEX 8051 program file into the 8051 MCU in the PGA400-Q1.

6.6.1 Load .HEX File into GUI

The “Load .HEX File into GUI” button is used to load the contents of a .HEX file into the GUI RAM for use with other operations. When the button is pressed, a second window will open that will allow the user to locate and open the desired .HEX file on the PC. See the figure below to see an example of this operation.

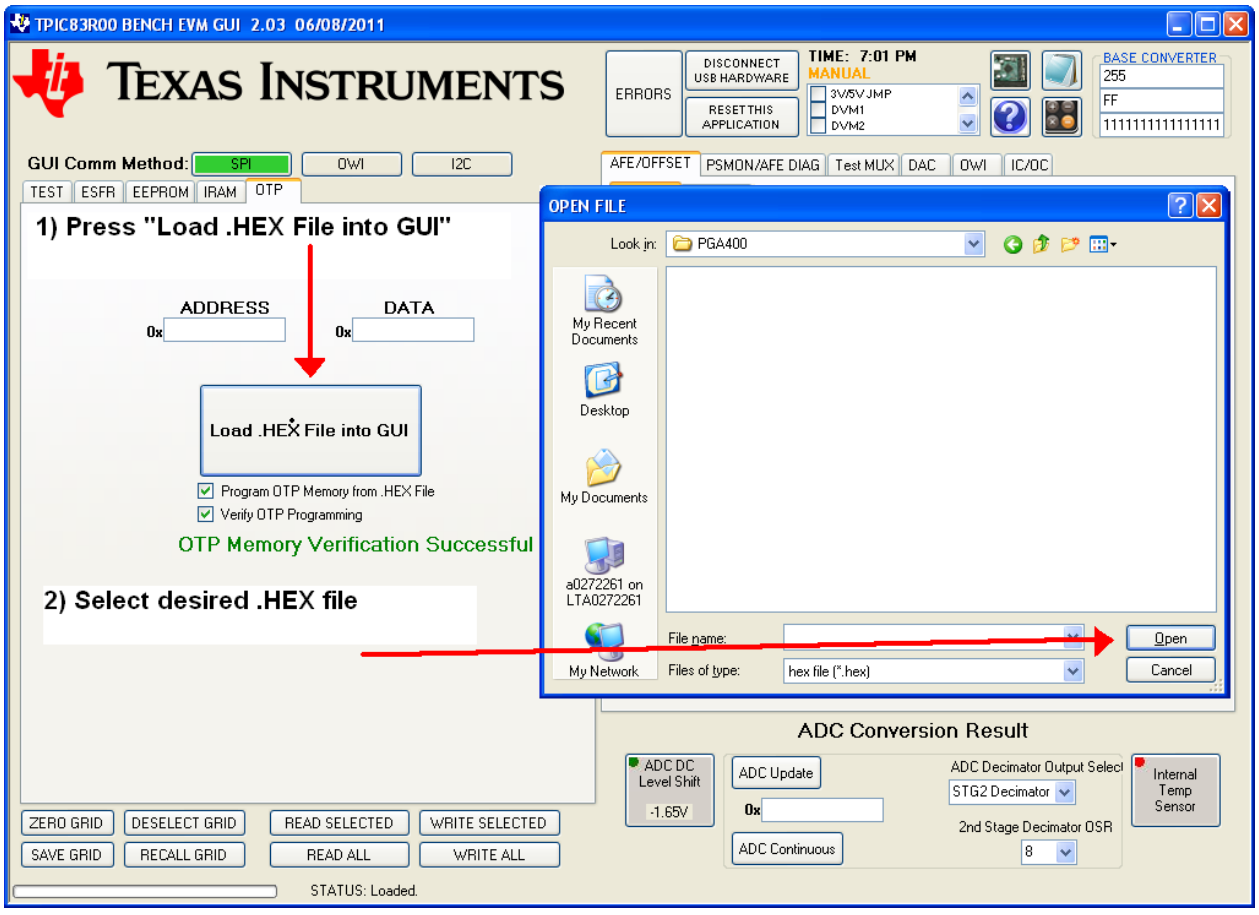


Figure 17. Loading a .HEX File into the GUI

6.6.2 Program OTP Memory from .HEX File

If the “Program OTP Memory from .HEX File” check box was checked (default) when the .HEX file was loaded into the GUI, the OTP memory will be programmed with the contents of the .HEX file.

6.6.3 Verify OTP Programming

If the “Verify OTP Programming” button was also checked (default) then after the OTP memory is finished programming, the GUI will reset the MCU and then verify that the contents of the OTP memory match the .HEX file. If the OTP memory matches the contents of the .HEX file, the GUI will display the message “OTP Memory Verification Successful” as seen in the figure below.

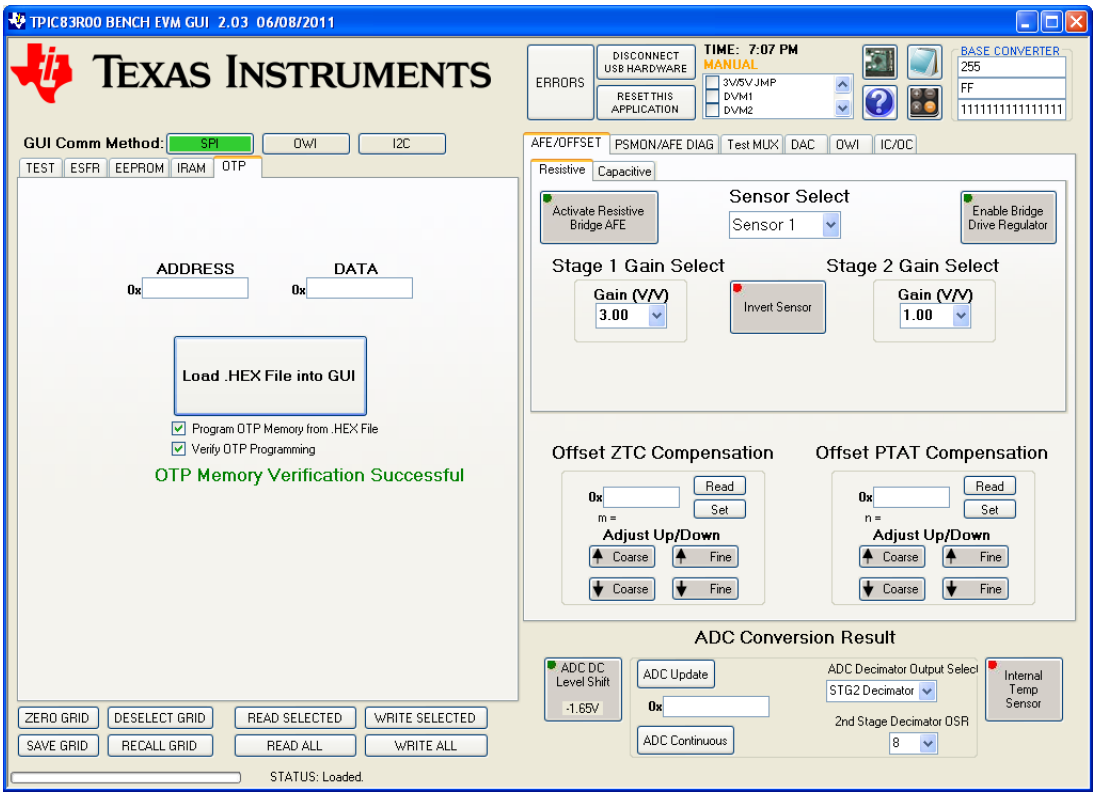


Figure 18. OTP Memory Successful Programming Verification

7 Controlling the PGA400-Q1 Functions with the GUI

The previous section focuses on the left side of the GUI which is primarily setup for direct register manipulation. The right side of the GUI is focused much more on providing a graphical method for controlling the PGA400-Q1.

7.1 ADC Conversion Result Section of the GUI

In the bottom right corner of the GUI is dedicated for functions that support or directly read from the internal ADC inside the PGA400-Q1. These buttons were not put inside a tab like the rest of the buttons because it is useful to be able to read the ADC registers which modifying the AFE settings without having to switch tabs. An image along with a description of the buttons can be found below.

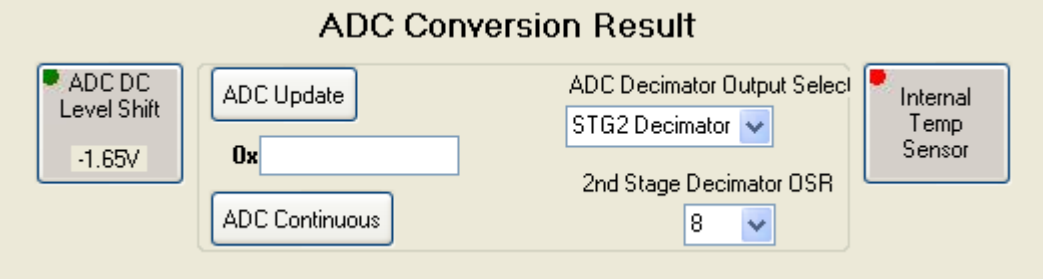


Figure 19. ADC Conversion Result Section of GUI

7.1.1 ADC Update

The “ADC Update” button is used to load the contents of the ADC into the shadow register and then read them into the GUI. The ADC Update button will load the output from the decimator that is selected with the “ADC Decimator Output Select” combo-box. Results are displayed in both two’s complement and signed decimal.

7.1.2 ADC Decimator Output Select

The “ADC Decimator Output Select” combo-box is used to control with ADC decimator output is loaded when the “ADC Update” button is pressed. The combo-box controls bits 0-2 in ESFR 0xB3.

7.1.3 ADC DC Level Shift

The “ADC DC Level Shift” button controls bit 5 in ESFR 0xA9.

7.1.4 Internal Temp Sensor

The “Internal Temp Sensor” button controls bit 4 in ESFR 0xA9.

7.2 AFE/Offset Tab

By default, the AFE/Offset tab is displayed in the right side of the GUI. This tab is divided into two parts. The first enables and controls either the resistive or capacitive AFEs, the second manipulates the shared “Offset DACs” in the PGA400-Q1. The buttons on these tabs are described in the following sections

7.2.1 Resistive AFE Tab

The resistive AFE tab is selected by default when the GUI loads. This corresponds to the default setting to have the resistive AFE selected on power-up. An image of the resistive AFE tab along with a description of the buttons can be found below.

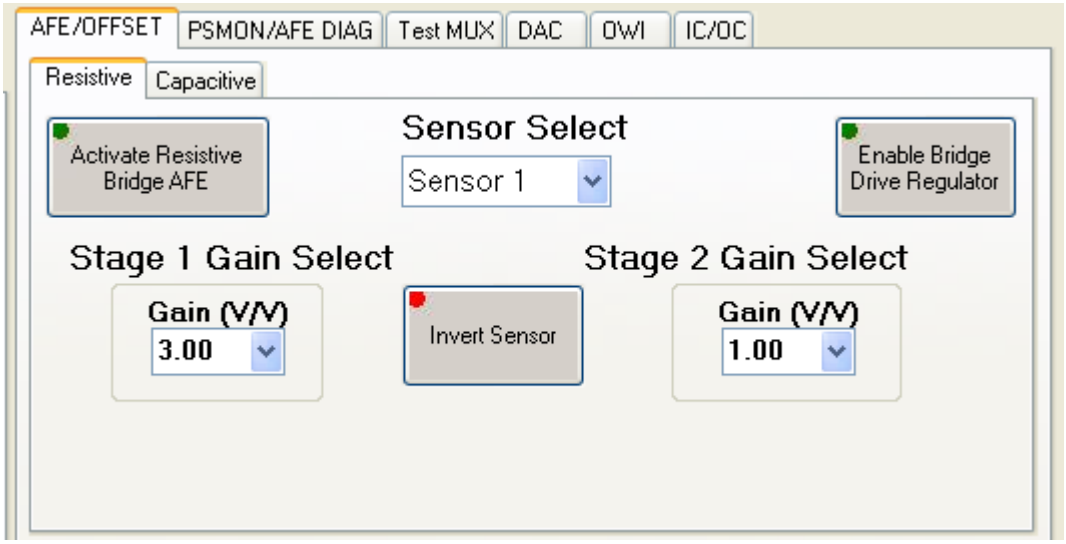


Figure 20. Resistive AFE Tab

7.2.1.1 Activate Resistive Bridge AFE

The “Activate Resistive Bride AFE” button configures the PGA400-Q1 for the Resistive AFE by controlling bit 7 in ESFR 0xA7.

7.2.1.2 Enable Bridge Drive Regulator

The “Enable Bridge Drive Regulator” button enables/disables the VBRG regulator by controlling bit 2 in ESFR 0xA9.

7.2.1.3 Sensor Select

The “Sensor Select” combo-box controls which input signals are routed through the AFE by controlling bit 7 of ESFR 0xA9. The combo-box also controls which set of registers the rest of the resistive AFE GUI controls. By default “Sensor 1” is selected so all of the sensor specific buttons on the resistive tab as well as the Offset section are set to control the “Sensor 1” registers. If the combo-box is changed, the buttons will control the registers associated with the “Sensor 2” inputs.

7.2.1.4 Invert Sensor

The “Invert Sensor” button controls the sign-bit MUX in the PGA400-Q1 by controlling either bit 5 or bit 6 in register 0xA9 depending on the state of the “Sensor Select” combo-box.

7.2.1.5 Stage 1 Gain Select

The “Stage 1 Gain Select” combo-box controls bits 5-7 of either register 0xA1 or 0xA2 depending on the state of the “Sensor Select” combo-box

7.2.1.6 Stage 2 Gain Select

The “Stage 2 Gain Select” combo-box controls bits 0-4 of either register 0xA1 or 0xA2 depending on the state of the “Sensor Select” combo-box

7.2.2 Capacitive AFE Tab

The capacitive AFE tab is not activated by default when the GUI loads. The user can select the capacitive tab and then enable the capacitive AFE to begin evaluating the capacitive signal chain on the PGA400-Q1. An image of the capacitive AFE tab along with a description of the buttons can be found below.

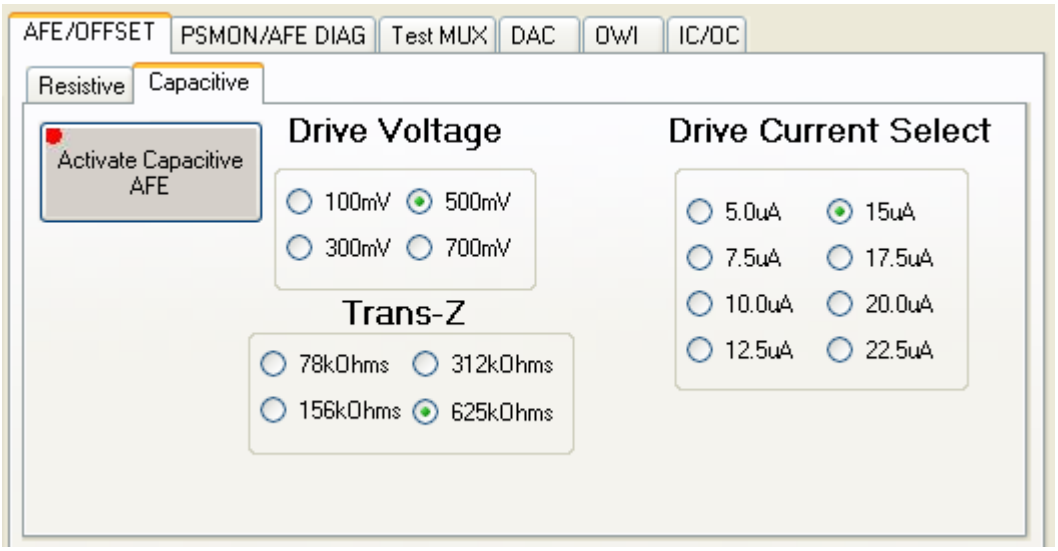


Figure 21. Capacitive AFE Tab

7.2.2.1 Activate Capacitive AFE

The “Activate Capacitive AFE” button configures the PGA400-Q1 for the Resistive AFE by controlling bit 7 in ESFR 0xA7.

7.2.2.2 Drive Voltage

The “Drive Voltage” selection boxes control the voltage on the clock generator comparator in the PGA400-Q1 by controlling bits 2 and 3 in ESFR 0xA7.

7.2.2.3 Drive Current Select

The “Drive Current Select” selection boxes control the current that is switched in and out of the ICAP pins by controlling bits 4-6 in ESFR 0xA7.

7.2.2.4 Trans-Z

The “Trans-Z” selection boxes control the transimpedance resistance by controlling bits 0 and 1 in ESFR 0xA7.

7.2.3 ZTC and PTAT Offset Control

The ZTC and PTAT Offset circuits are shared whether the user is using the PGA400-Q1 in resistive or capacitive mode, therefore they are displayed while either AFE tab is selected. An image and description of the buttons on the offset control region of the GUI are described below.

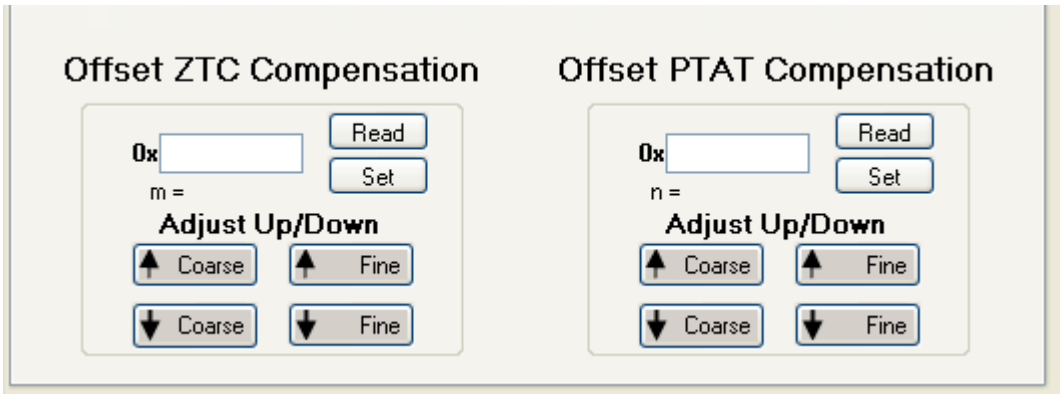


Figure 22. ZTC and PTAT Offset Control

7.2.3.1 Offset ZTC Compenstation Read/Set

The “Read” and “Set” buttons in the Offset ZTC Compensation region can be used to directly enter in the desired offset values. The buttons either read to or write from the ZTC offset bits in ESFRs 0xA3/0xA4 or 0xA5/0xA6 depending on the state of the “Sensor Select” combo-box.

7.2.3.2 Offset ZTC Compenstation Adjust Up/Down

The “Coarse” Up/Down and “Fine” Up/Down buttons are used to adjust the value of the ZTC offset register up or down in set increments. The buttons write to the ZTC offset bits in ESFRs 0xA3/0xA4 or 0xA5/0xA6 depending on the state of the “Sensor Select” combo-box. The “Fine” adjustments move the ZTC offset value by one, while the “Coarse” buttons move the ZTC offset value by 50.

7.2.3.3 Offset PTAT Compenstation Read/Set

The “Read” and “Set” buttons in the Offset PTAT Compensation region can be used to directly enter in the desired offset values. The buttons either read to or write from the PTAT offset bits in ESFRs 0xA4 or 0xA6 depending on the state of the “Sensor Select” combo-box.

7.2.3.4 Offset PTAT Compenstation Adjust Up/Down

The “Coarse” Up/Down and “Fine” Up/Down buttons are used to adjust the value of the PTAT offset register up or down in set increments. The buttons write to the PTAT offset bits in ESFRs 0xA4 or 0xA6 depending on the state of the “Sensor Select” combo-box. The “Fine” adjustments move the PTAT offset value by one, while the “Coarse” buttons move the PTAT offset value by 50.

7.3 PSMON/AFE Diagnostics Tab

The PSMON/AFE Diagnostics tab is the second tab in the right half tab control. The tab is setup so that when activated, any flags that are currently set are displayed in red, while all of the bits that don’t have flags set are green. In the image below of the PSMON/AFE Diagnostics tab the “ADC Input Over-Voltage” flag is set showing that the input to the ADC is out of range. All of the power supply’s are in the correct range so none of the flags are set. A description of the buttons on the tab can be found below.

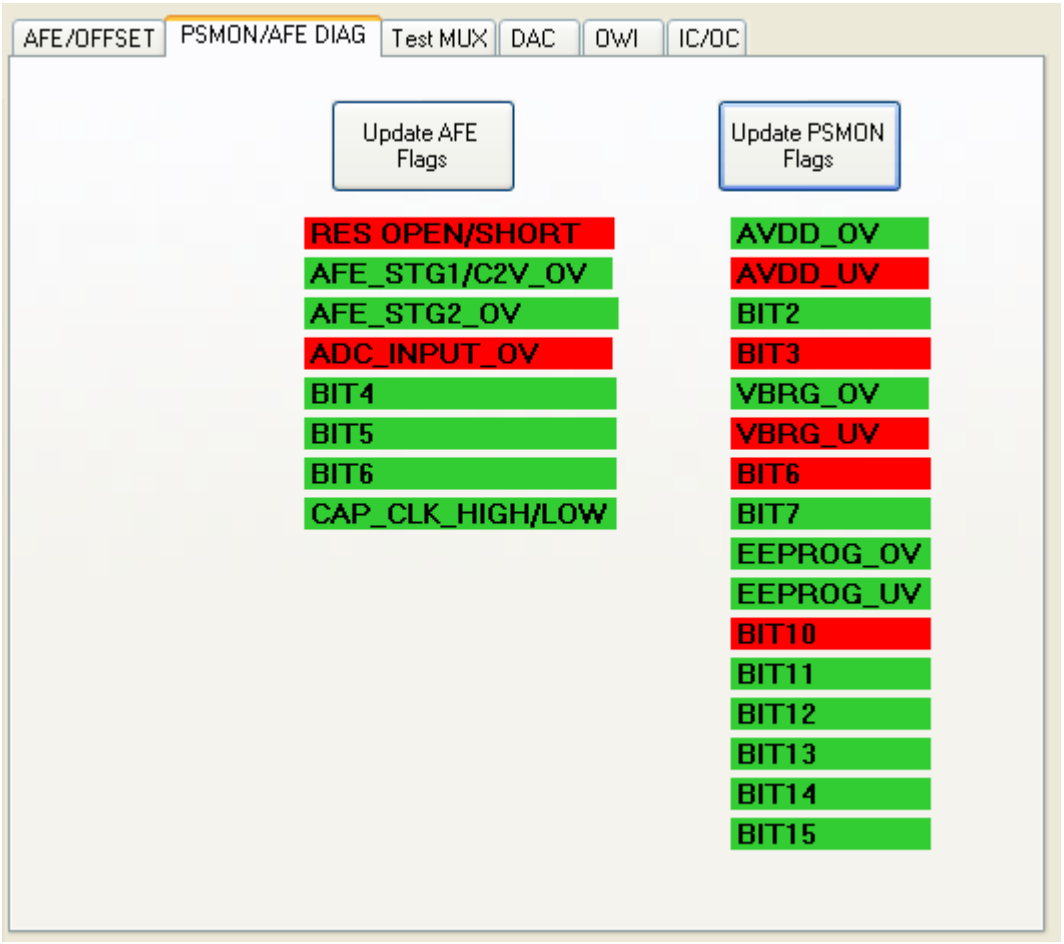


Figure 23. PSMON/ AFE Diagnostics Tab

7.3.1 Update AFE Flags

The “Update AFE Flags” button reads from ESFR 0x93 and then updates the color of the flags in the GUI accordingly.

7.3.2 Update PSMON Flags

The “Update PSMON Flags” button reads from ESFRs 0x91 and 0x92 and then updates the color of the flags in the GUI accordingly.

7.4 Test MUX

The Test MUX tab can be used to activate and control the settings on the analog and digital test in/out MUXes that are present inside the PGA400-Q1. The tab is divided into two tabs, one for the analog test MUXes and the other for the digital test MUXes.

7.4.1 Analog Test MUX Tab

The Analog Test MUX tab is used to control the settings for the analog test MUXes inside the PGA400-Q1. Before any changes on the Analog Test MUX tab will take effect, the user must activate “Restricted Access” mode from the “TEST” tab. An image along with a description of the controls on this tab can be found below.

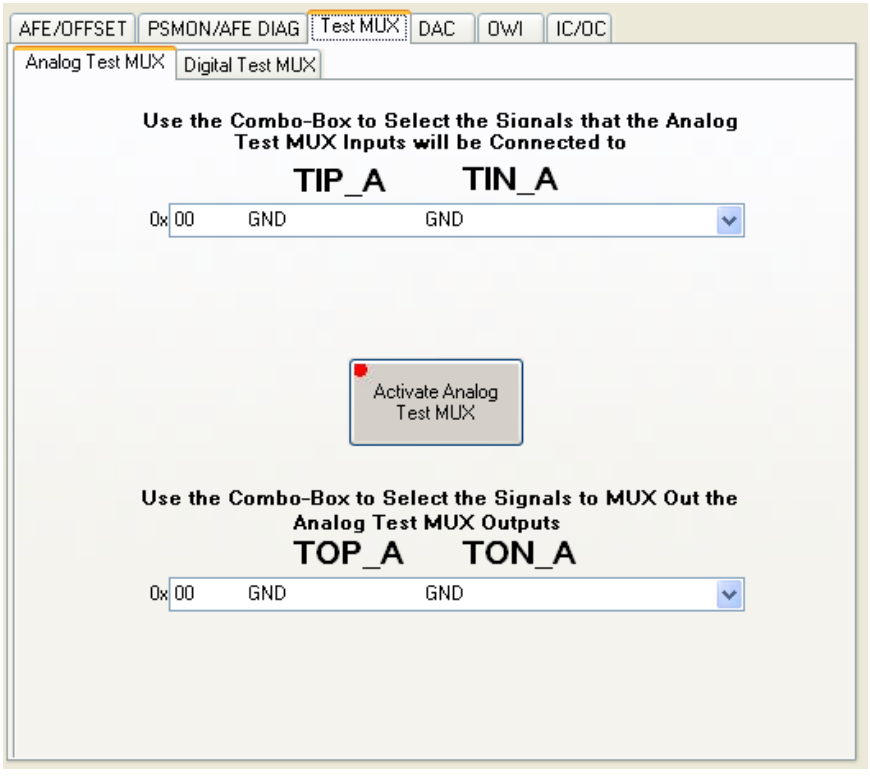


Figure 24. Analog Test MUX Tab

7.4.1.1 Activate Analog Test MUX

The “Activate Analog Test MUX” button disables the VOUT1/VOUT2 DACs and activates the Analog Test MUXes by controlling bits 3 and 4 of TEST register 0x10.

7.4.1.2 TIP_A / TIN_A Combo-Box

The “TIP_A / TIN_A” combo-box is used to select where the TIN and TIP signals get routed inside the PGA400-Q1 by controlling TEST register 0x08.

7.4.1.3 TOP_A / TON_A Combo-Box

The “TOP_A / TON_A” combo-box is used to select where the VOUT1/VOUT2 signals get routed inside the PGA400-Q1 by controlling TEST register 0x06.

7.4.2 Digital Test MUX Tab

The Digital Test MUX tab is used to control the settings for the digital test MUXes inside the PGA400-Q1. Before any changes on the Digital Test MUX tab will take effect, the user must activate “Restricted Access” mode from the “TEST” tab. An image along with a description of the controls on this tab can be found below.

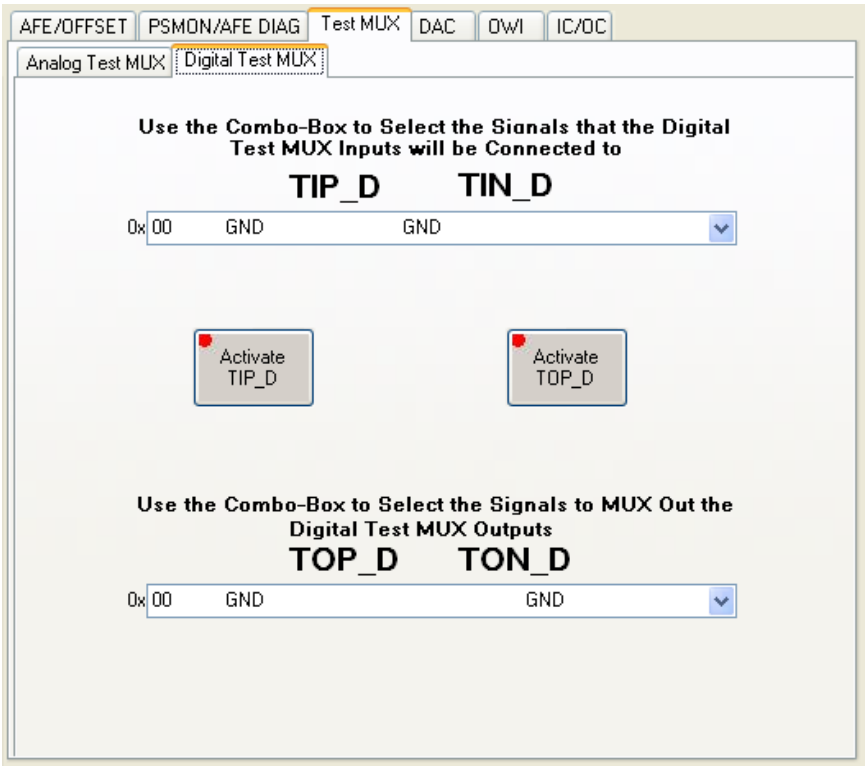


Figure 25. Analog Test MUX Tab

7.4.2.1 Activate TIP_D

The “Activate TIP_D” button disables the digital test input signal by controlling bit 1 of TEST register 0x03.

7.4.2.2 Activate TOP_D

The “Activate TOP_D” button disables the activates the digital test output signal by controlling bits 2 and 3 of TEST register 0x03.

7.4.2.3 TIP_D / TIN_D Combo-Box

The “TIP_D / TIN_D” combo-box is used to select where the digital test input signals get routed inside the PGA400-Q1 by controlling TEST register 0x07.

7.4.2.4 TOP_D / TON_D Combo-Box

The “TOP_A / TON_A” combo-box is used to select where the VOUT1/VOUT2 signals get routed inside the PGA400-Q1 by controlling TEST register 0x06.

7.5 DAC Output Tab

The DAC Output tab can be used to directly control the output of the VOUT1/VOUT2 DACs on the PGA400-Q1. An image of the tab along with a description of the buttons can be found below.

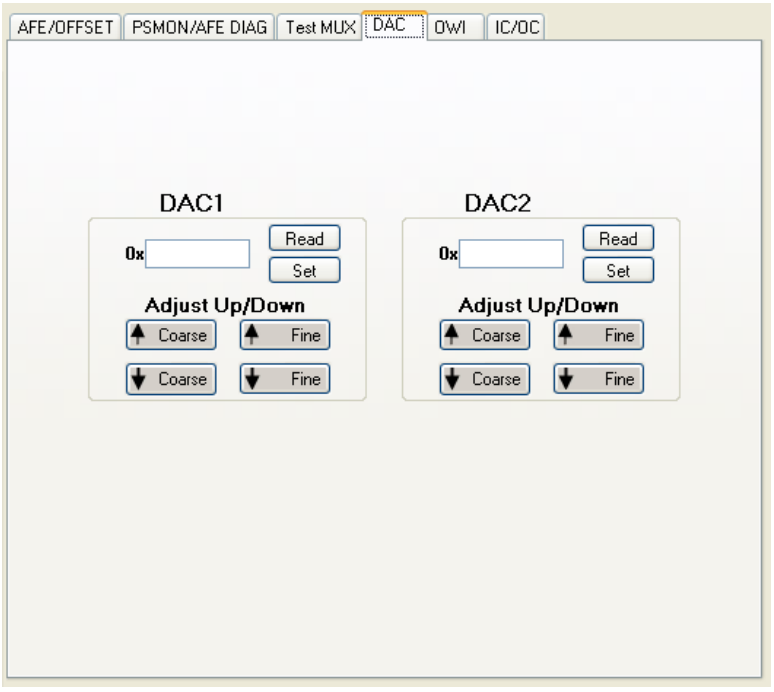


Figure 26. DAC Output Tab

7.5.1.1 DAC1 Output Read/Set

The “Read” and “Set” buttons in the DAC1 region can be used to directly enter in the desired DAC1 values. The buttons either read to or write from the DAC1 ESFRs 0xB7/0xB9.

7.5.1.2 DAC1 Output Adjust Up/Down

The “Coarse” Up/Down and “Fine” Up/Down buttons are used to adjust the value of the DAC1 output register up or down in set increments. The buttons write to the DAC1 output bits in ESFRs 0xB7/0xB9. The “Fine” adjustments move the DAC1 output value by one, while the “Coarse” buttons move the DAC1 output value by 50.

7.5.1.3 DAC2 Output Read/Set

The “Read” and “Set” buttons in the DAC2 region can be used to directly enter in the desired DAC2 values. The buttons either read to or write from the DAC2 ESFRs 0xBA/0xBB.

7.5.1.4 DAC2 Output Adjust Up/Down

The “Coarse” Up/Down and “Fine” Up/Down buttons are used to adjust the value of the DAC2 output register up or down in set increments. The buttons write to the DAC2 output bits in ESFRs 0xBA/0xBB. The “Fine” adjustments move the DAC2 output value by one, while the “Coarse” buttons move the DAC2 output value by 50.

7.6 OWI Tab

The OWI tab in the GUI is used to initialize the OWI communication interface in the PGA400-Q1 along with perform direct OWI write/reads. A thorough walk-through of the OWI communication is described in the “OWI Quick Start Guide” document. An image of the OWI tab and description of the buttons can be found below.

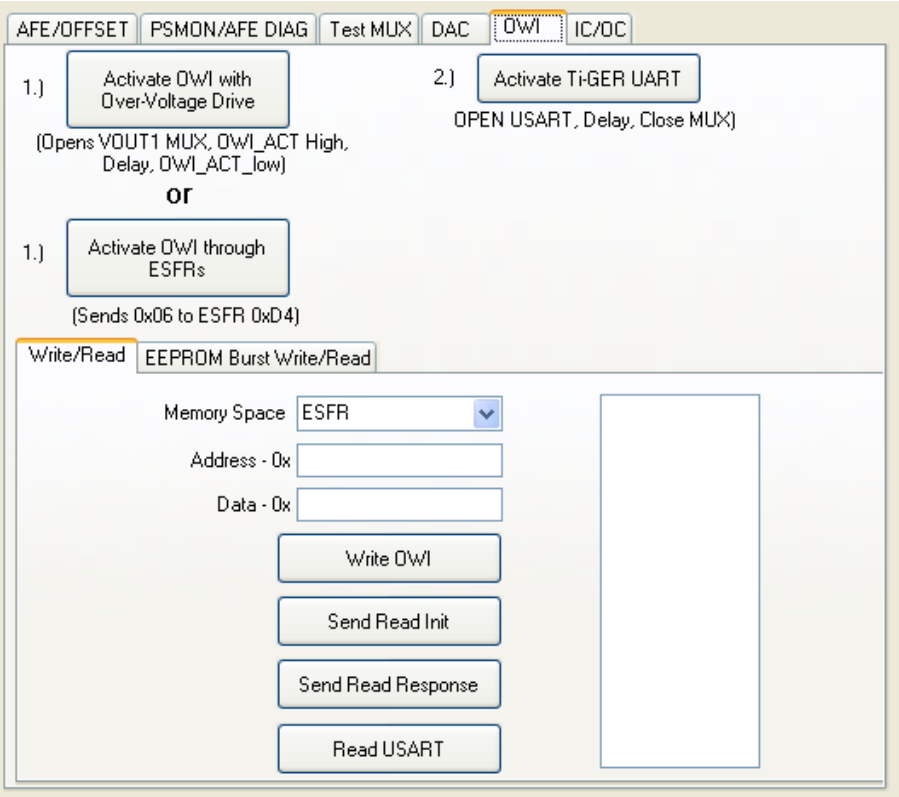


Figure 27. OWI GUI Tab

7.6.1 Activate OWI with Over-Voltage Drive

The “Activate OWI with Over-Voltage Drive” button on the GUI initializes the OWI activation circuit by controlling the signal that drives the “Q4” BJT. Pressing the button will disable the PGA400-Q1 Output MUX, activate the +7.5V pull-up, wait roughly 200ms, then release the OWI pull-up. The 8051 must be running have code loaded into it that will send the signals to activate the OWI transceiver.

7.6.2 Activate OWI with ESFRs

The “Activate OWI with ESFRs” button will activate the OWI transceiver by directly writing to ESFR 0xD4. After this button is pressed, the PGA400-Q1 will be in “OWI” mode and SPI commands will no longer work.

7.6.3 Activate TI-GER UART

The “Activate TI-GER UART” button will initialize the UART hardware module in the TI-GER in preparation for OWI communication.

7.6.4 Send Sync

The “Send Sync” button will send the required preliminary “Sync” pulse to flush the contents of the OWI transceiver shift buffer.

7.6.5 Write/Read Tab

The bottom portion of the main OWI tab is divided between performing simple OWI writes and reads and performing OWI burst write/reads. An image of the “Write/Read” tab can be seen in the previous figure and a description of the buttons can be found below.

7.6.5.1 Memory Space Selection Box

The currently selected Memory Space in the “Memory Space Selection Box” will be used to form the correct packet when an OWI write or read is performed using the Write/Read buttons on the “Write/Read” tab.

7.6.5.2 Address Text Box

The “Address Text Box” is used to enter the address that the user desires to write/read from when using the Write/Read buttons.

7.6.5.3 Data Text Box

The “Data Text Box” is used to enter the data that the user desires to write/read from when using the Write/Read buttons.

7.6.5.4 Write OWI

The “Write OWI” button will collect information from the “Memory Space Selection Box,” the “Address Text Box,” and the “Data Text Box” and then form the appropriate packet to write the data into the selected address in the correct memory space.

7.6.5.5 Send Read Init

The “Send Read Init” button will collect information from the “Memory Space Selection Box,” and the “Address Text Box,” and then form the appropriate packet to send in the “Read Init” command when reading from a selected address in the correct memory space.

7.6.5.6 Send Read Response

The “Send Read Response” button will send the “Read Response” command to the PGA400-Q1 that will be followed by the data that was requested in the “Read Init” command.

7.6.5.7 Read USART

The “Read USART” button will read out the contents of the TI-GER USART buffer. Data is shifted out of the FIFO buffer when the button is pressed and then displayed in the textbox on the right side of the “Write/Read” tab. Since the OWI always works in loop-back mode, the results of any OWI writes can be seen by reading the USART after a write is performed.

7.6.6 EEPROM Burst Write/Read Tab

The second tab on the bottom portion of the OWI tab is the “EEPROM Burst Write/Read” tab. This tab is used to perform the EEPROM “Burst” write/read commands that the PGA400-Q1 supports. An image of the tab along with a description of the buttons can be found below.

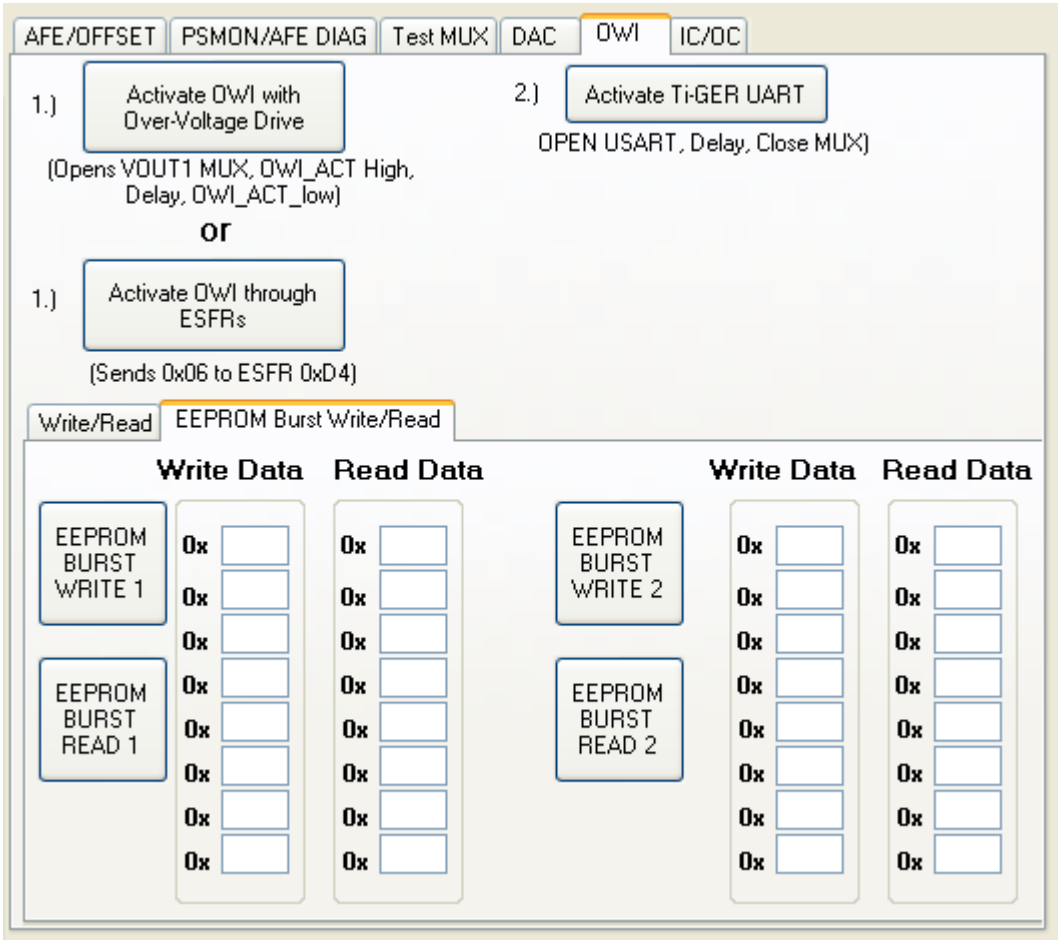


Figure 28. EEPROM Burst Write/Read Tab

7.6.6.1 EEPROM Burst Write 1

The “EEPROM BURST WRITE 1” button will perform a burst write with the data that has been entered into the textboxes under the “Write Data” label on the left side of the tab.

7.6.6.2 EEPROM Burst Read 1

The “EEPROM BURST READ 1” button will perform a burst read and then populate the data into the textboxes under the “Read Data” with the data that has been entered into the textboxes under the “Read Data” label on the left side of the tab.

7.6.6.3 EEPROM Burst Write 2

The “EEPROM BURST WRITE 2” button will perform a burst write with the data that has been entered into the textboxes under the “Write Data” label on the right side of the tab.

7.6.6.4 EEPROM Burst Read 2

The “EEPROM BURST READ 2” button will perform a burst read and then populate the data into the textboxes under the “Read Data” with the data that has been entered into the textboxes under the “Read Data” label on the right side of the tab.

7.7 IC/OC Tab

The “IC/OC” (Input Compare/Output Compare) tab on the GUI is used to read from and configure the input and output compare registers on the PGA400-Q1. The tab is broken into five main regions: Input Compare 1, Input Compare 2, Output Compare 1, Output Compare 2, and Free Running Timer. An image of the tab along with a description of the buttons can be found below.

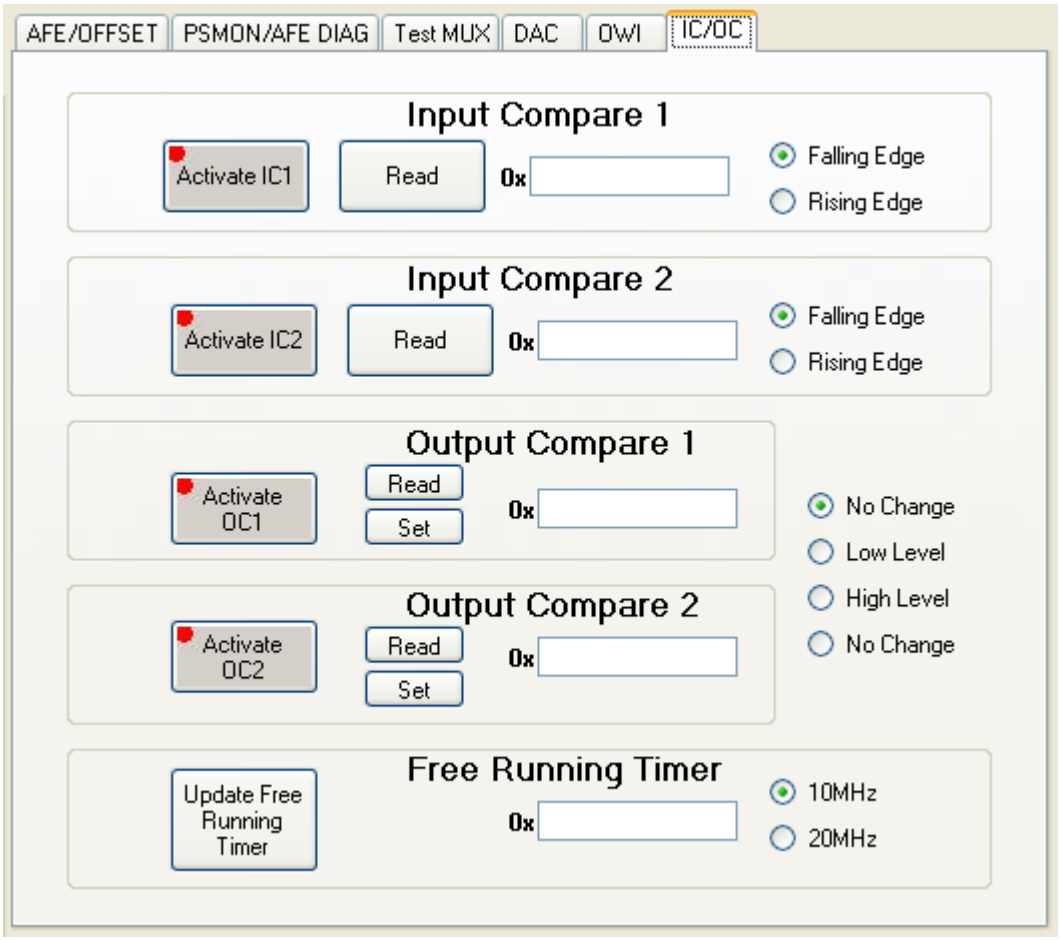


Figure 29. IC/OC GUI Tab

7.7.1 Input Compare 1 Region

The “Input Compare 1 Region” is used to activate and read from the Input Compare 1 peripheral in the PGA400-Q1.

7.7.1.1 Activate IC1

The “Activate IC1” button activates the Input Compare 1 function in the PGA400-Q1 by controlling bit 0 of ESFR 0xC7.

7.7.1.2 Read IC1

The “Read” button in the IC1 region is used to update the text box with the contents of the input compare registers by reading ESFRs 0xC1 and 0xC2.

7.7.1.3 Falling/Rising Edge Selection Box

The “Falling/Rising Edge” selection box is used to change the polarity that the input compare peripheral uses by controlling bit 1 of ESFR 0xC0.

7.7.2 Input Compare 2 Region

The “Input Compare 2 Region” is used to activate and read from the Input Compare 2 peripheral in the PGA400-Q1.

7.7.2.1 Activate IC2

The “Activate IC2” button activates the Input Compare 2 function in the PGA400-Q1 by controlling bit 1 of ESFR 0xC7.

7.7.2.2 Read IC2

The “Read” button in the IC2 region is used to update the text box with the contents of the input compare registers by reading ESFRs 0xC3 and 0xC4.

7.7.2.3 Falling/Rising Edge Selection Box

The “Falling/Rising Edge” selection box is used to change the polarity that the input compare peripheral uses by controlling bit 2 of ESFR 0xC0.

7.7.3 Output Compare 1 Region

The “Output Compare 1 Region” is used to activate and set/read the Output Compare 1 peripheral in the PGA400-Q1.

7.7.3.1 Activate OC1

The “Activate OC1” button activates the Output Compare 1 function in the PGA400-Q1 by controlling bit 2 of ESFR 0xC7.

7.7.3.2 Read OC1

The “Read” button in the OC1 region is used to update the text box with the contents of the output compare registers by reading ESFRs 0xC5 and 0xC6.

7.7.3.3 Set OC1

The “Set” button in the OC1 region is used to set the value in the Output Compare 1 register by writing to ESFR 0xC5 and 0xC6.

7.7.4 Output Compare 2 Region

The “Output Compare 2 Region” is used to activate and set/read the Output Compare 2 peripheral in the PGA400-Q1.

7.7.4.1 Activate OC2

The “Activate OC2” button activates the Output Compare 2 function in the PGA400-Q1 by controlling bit 3 of ESFR 0xC7.

7.7.4.2 Read OC2

The “Read” button in the OC2 region is used to update the text box with the contents of the output compare registers by reading ESFRs 0xC9 and 0xCA.

7.7.4.3 Set OC2

The “Set” button in the OC2 region is used to set the value in the Output Compare 2 register by writing to ESFR 0xC9 and 0xCA.

7.7.5 No Change / Low Level / High Level Selection Box

The “No Change / Low Level / High Level” selection box is used to control the level that both the OC1 and OC2 peripherals use for the output compare functions. This is achieved by controlling bits 3 and 4 of ESFR 0xC0.

7.7.6 Free Running Timer Region

The “Free Running Timer” region of the IC/OC tab is used to monitor the Free Running Timer in the PGA400-Q1.

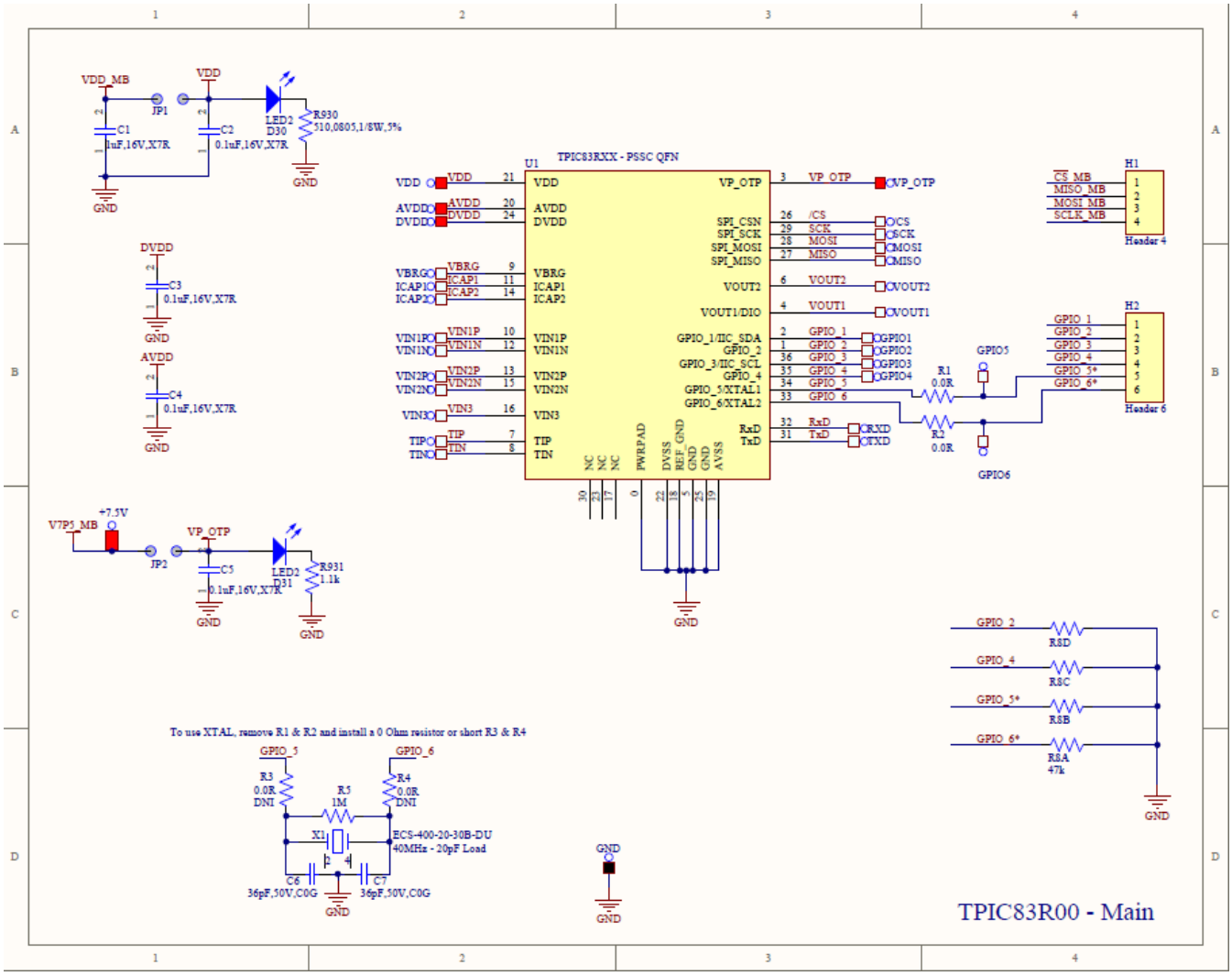
7.7.6.1 Update Free Running Timer

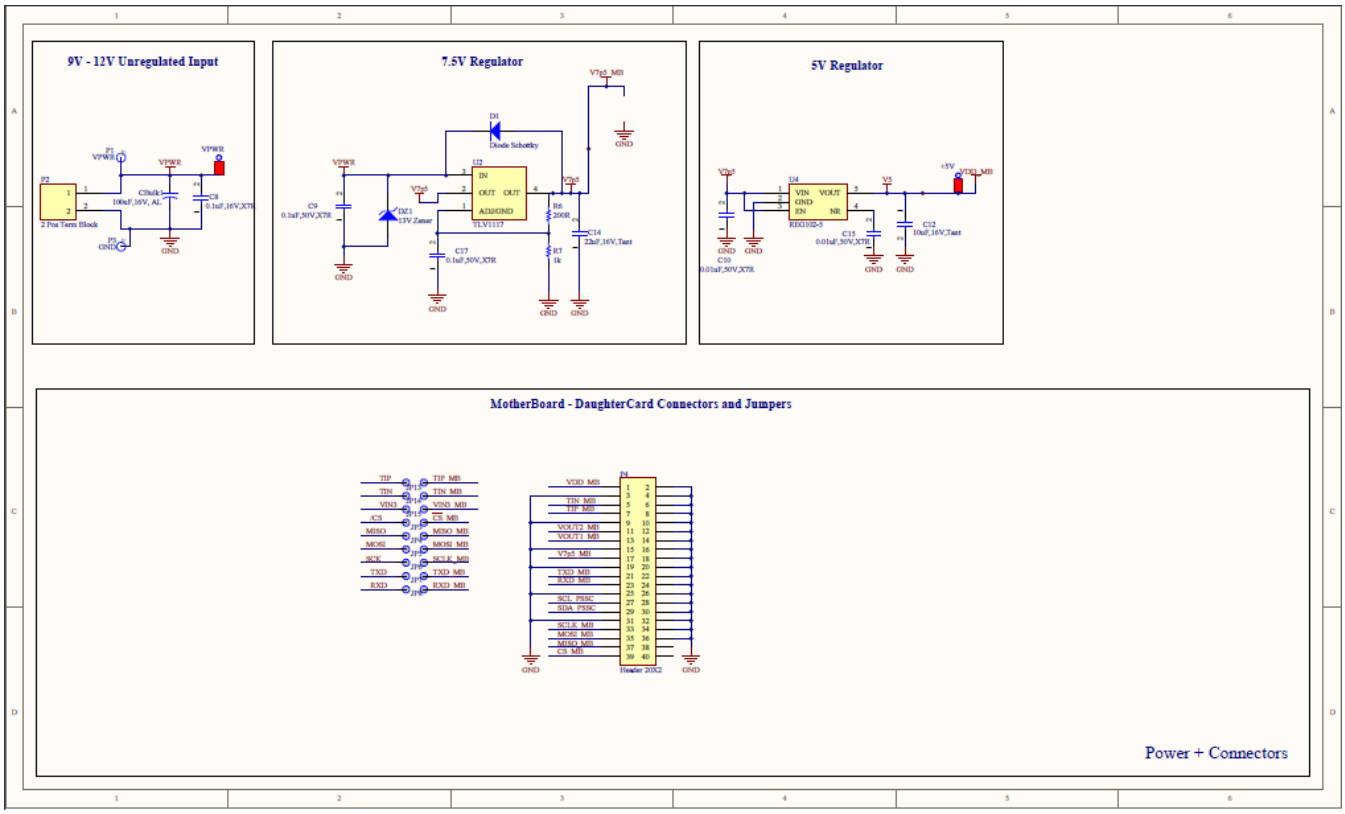
The “Update Free Running Timer” button is used to populate the textbox in the “Free Running Timer” region with the contents of the PGA400-Q1 Free Running Timer.

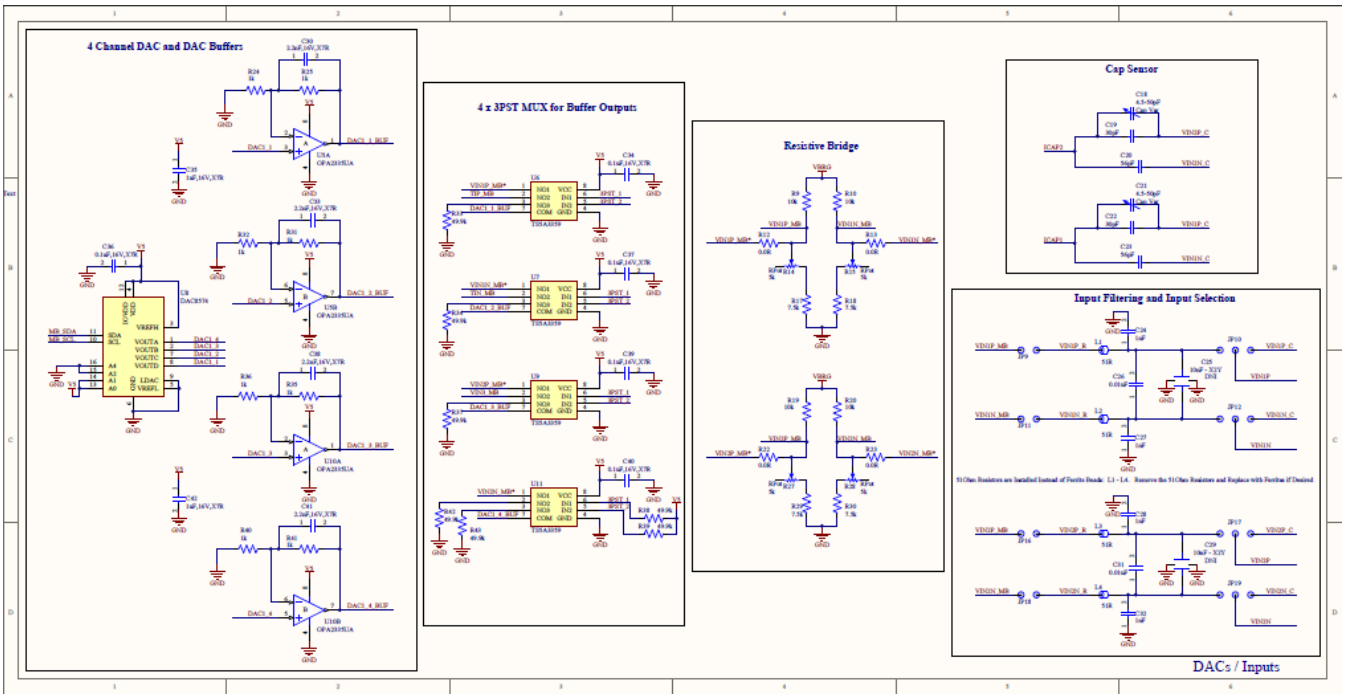
7.7.6.2 10MHz / 20MHz Selection Box

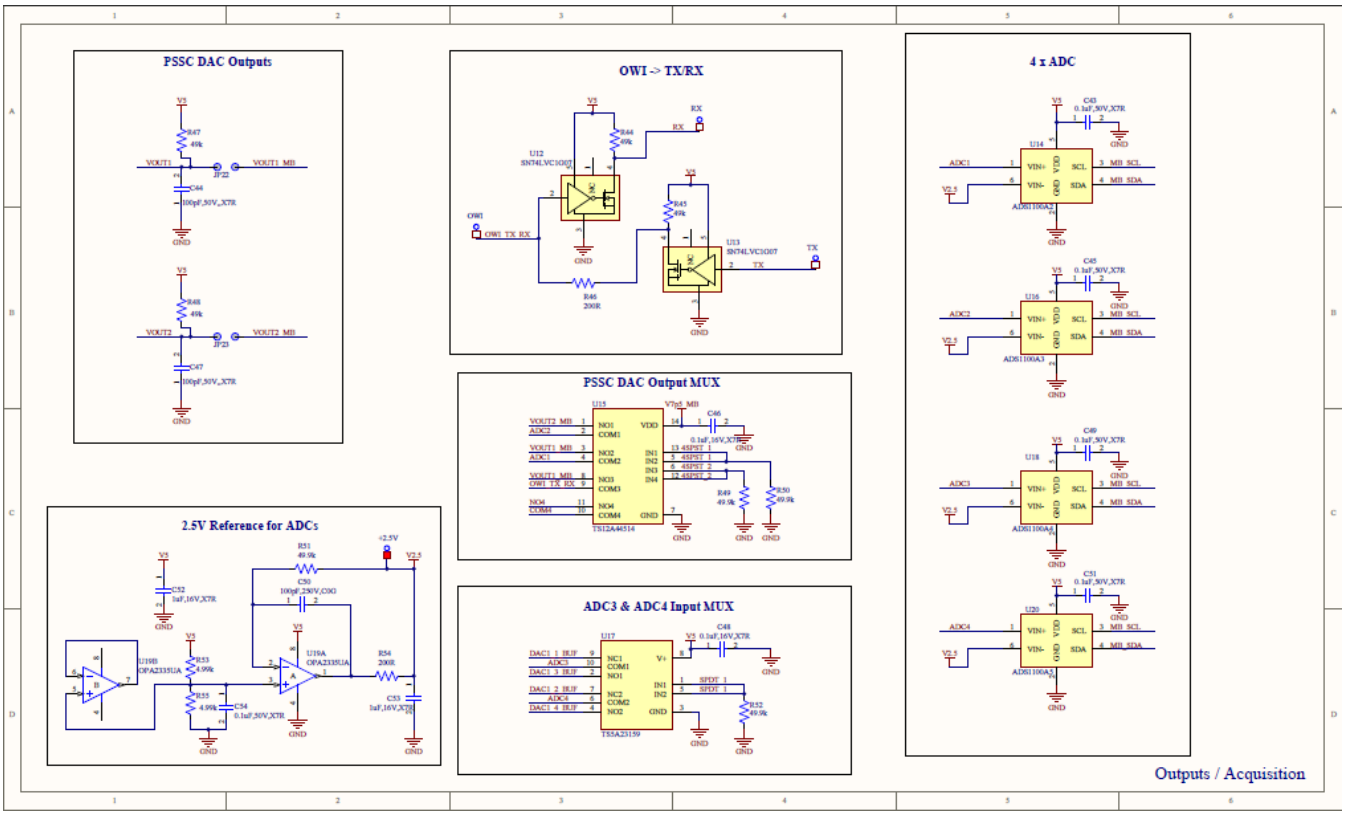
The “10MHz / 20MHz” selection box is used to select between a 10MHz and 20MHz Free Running Timer inside the PGA400-Q1 by controlling bit 0 of ESFR 0xC0.

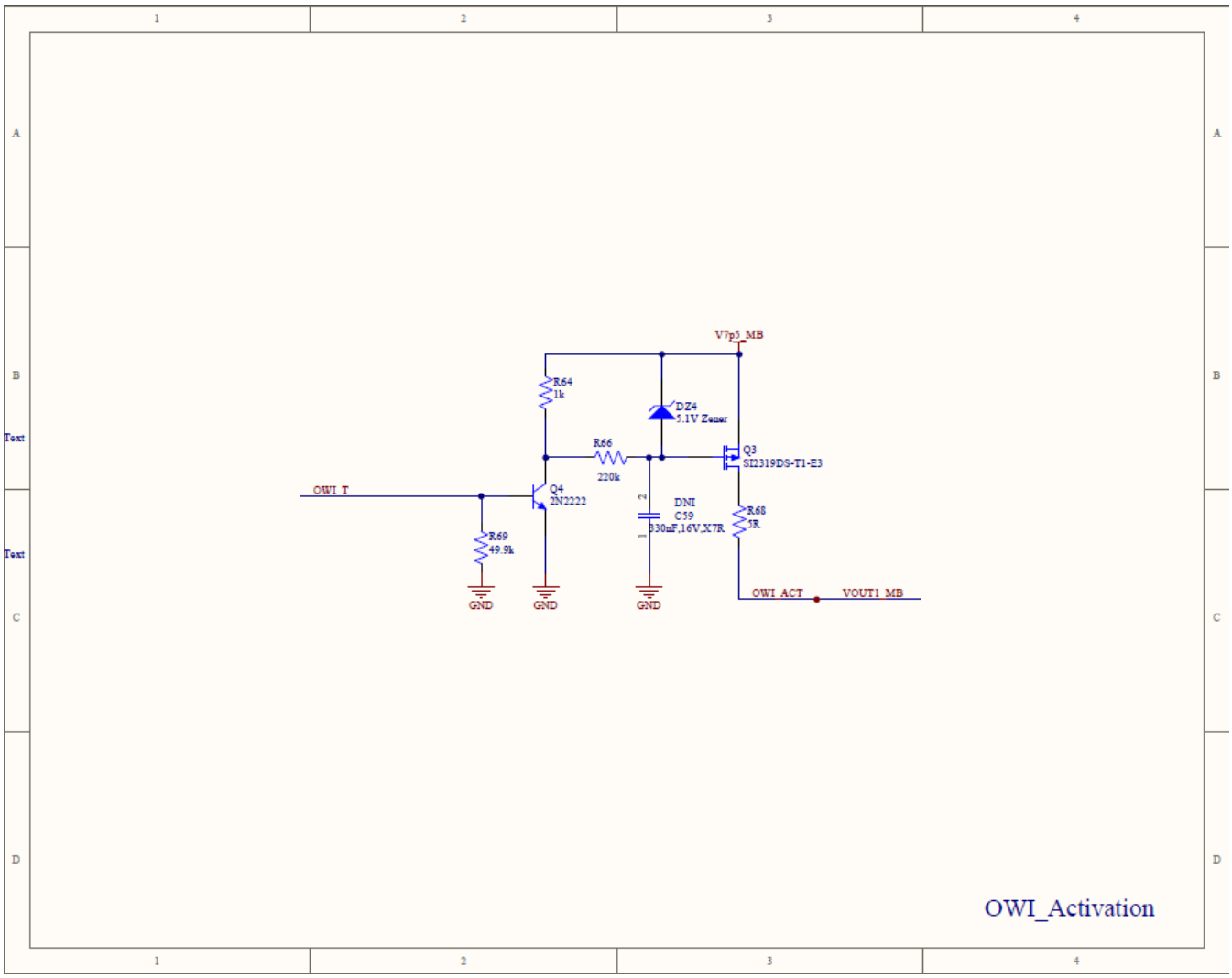
8 PGA400-Q1 EVM Schematics and Layout Drawings

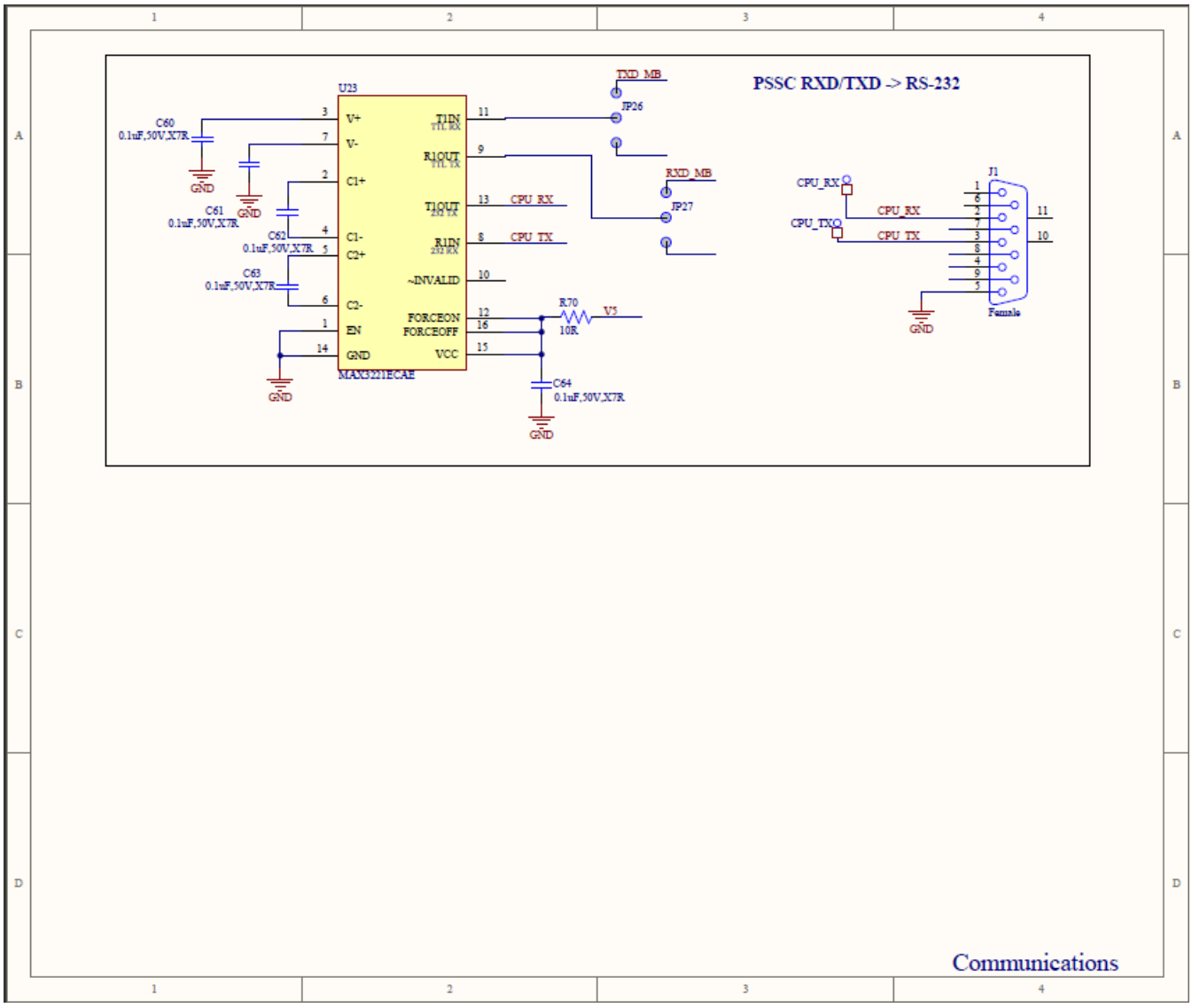


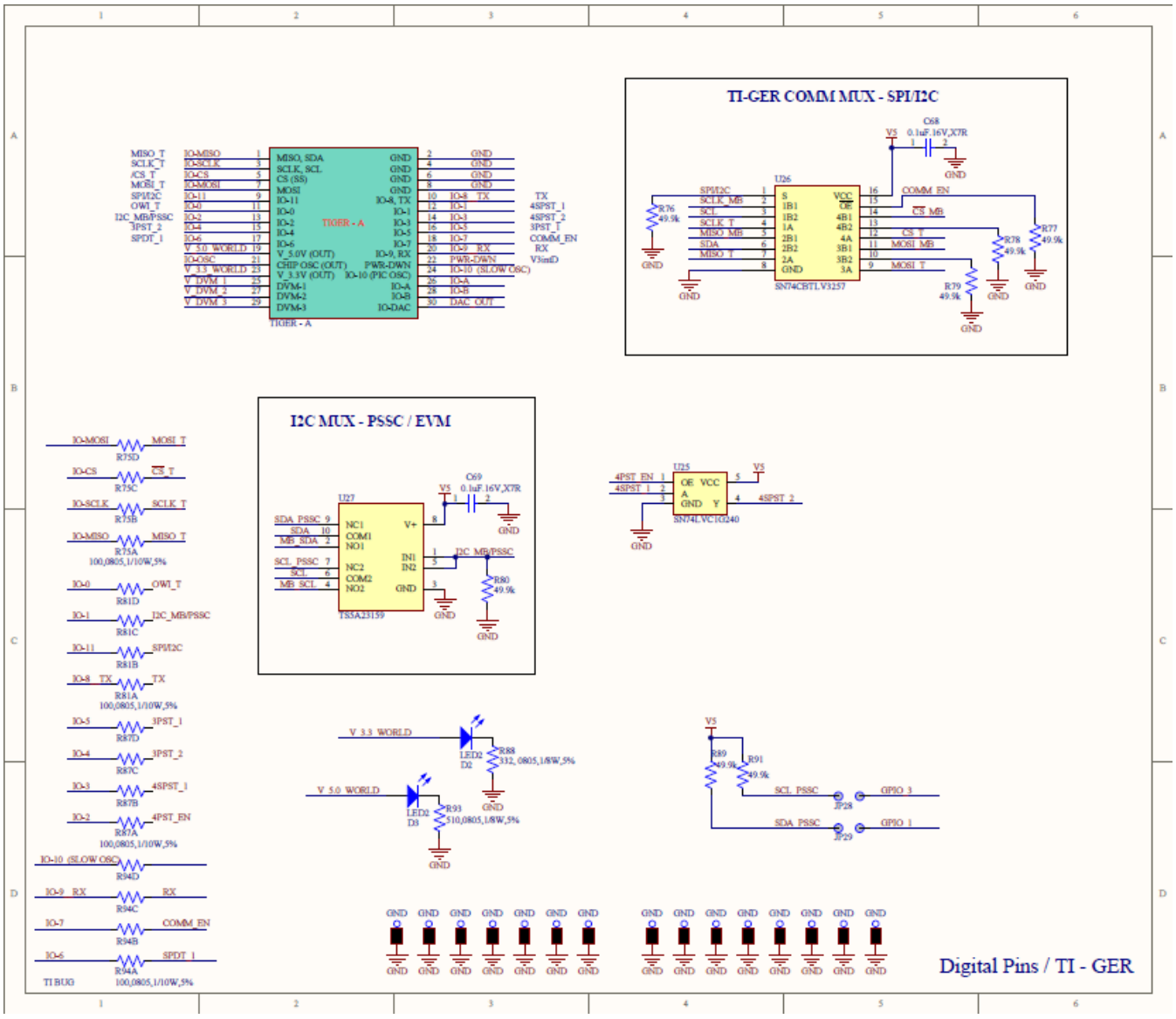

9V - 12V Unregulated Input
7.5V Regulator
5V Regulator
MotherBoard - DaughterCard Connectors and Jumpers
Power + Connectors


4 Channel DAC and DAC Buffers
4 x SPST MUX for Buffer Outputs
Resistive Bridge
Cap Sensor
Input Filtering and Input Selection
DACs / Inputs


PSSC DAC Outputs
OWI -> TX/RX
4 x ADC
PSSC DAC Output MUX
2.5V Reference for ADCs
ADC3 & ADC4 Input MUX
Outputs / Acquisition


V7p5_MB
R64
1k
DZ4
5.1V Zener
R66
220k
Q3
SI2319DS-T1-E3
OWI_T
Q4
2N2222
DNI
C59
330nF,16V,X7R
R68
5R
R69
49.9k
GND
GND
GND
OWI_ACT
VOUT1_MB
OWI_Activation


PSSC RXD/TXD -> RS-232
U23
MAX3221ECAE
V+
V-
C1+
C1-
C2+
C2-
EN
GND
VCC
T1IN
R1OUT
T1OUT
R1IN
~INVALID
FORCEON
FORCEOFF
C60
C61
C62
C63
C64
0.1uF,50V,X7R
R70
10R
V5
TXD_MB
RXD_MB
JP26
JP27
CPU_RX
CPU_TX
J1
Female
Communications


TI-GER COMM MUX - SPI/I2C
I2C MUX - PSSC / EVM
TIGER - A
TS5A23159
SN74CBTLV3257
SN74LVC1G240
Digital Pins / TI - GER

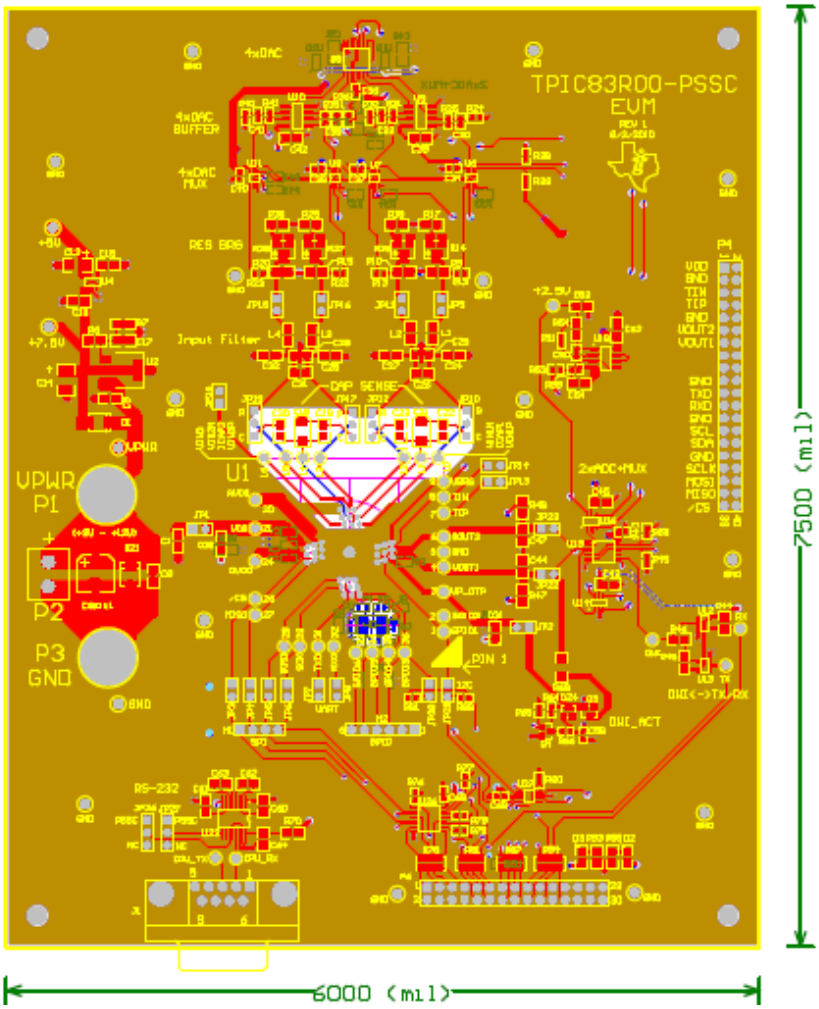
FABRICATION CHART				
FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT	
			EXTERNAL	INTERNAL
☐ 0.031 ■ 0.062 ☐ 0.093 ☐ 0.125	■ LAYER 1 ■ LAYER 2 ☐ NONE	■ LAYER 1 ■ LAYER 2 ☐ NONE	■ 1 OZ. ☐ 2 OZ. ☐ OTHER ____	■ 1 OZ. ☐ 2 OZ. ☐ OTHER ____

DESIGN	TRACE/GAP SPACING	LAYER COUNT	
☐ SMD ☐ THRU-HOLE ■ MIX	☐ 0.010/0.010 ☐ 0.008/0.007 ■ 0.006/0.006	☐ SINGLE SIDED ■ 4 LAYER ☐ 8 LAYER ☐ OTHER ____	☐ 2 LAYER ☐ 6 LAYER ☐ 10 LAYER

TEXAS INSTRUMENTS		
Board No. TPIC83R00 PSSC - EVM	Rev. E-0	
Date 5/18/2010	Filename	

Layer Stack Up Detail for: PCB2.PcbDoc

Layer Name
Top Layer
MidLayer1
MidLayer2
Bottom Layer



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Interface interface.ti.com	Military www.ti.com/military
Logic logic.ti.com	Optical Networking www.ti.com/opticalnetwork
Power Mgmt power.ti.com	Security www.ti.com/security
Microcontrollers microcontroller.ti.com	Telephony www.ti.com/telephony
RFID www.ti-rfid.com	Video & Imaging www.ti.com/video
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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
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日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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