

DEM-DAI3008 PCM3008 Evaluation Board

ABSTRACT

This document describes the primary features of the DEM-DAI3008 evaluation board. The description covers the motherboard and daughterboard and includes switches, jumpers and their settings, and schematic diagrams. In addition, for the daughterboard, the copper layout and silkscreen of the board are provided.

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WARNING:

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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1 Introduction

The DEM-DAI3008 is an evaluation fixture for stereo codec PCM3008. The DEM-DAI3008 consists of a daughterboard connected to a digital audio interface (DAI) motherboard (see Figure 1). The DEM-DAI3008 operates from +5-V and ± 15 -V power supplies. It has both optical and coax digital audio inputs and outputs. The input/output interface is in S/PDIF format. A block diagram of the DEM-DAI3008 is shown in Figure 2.

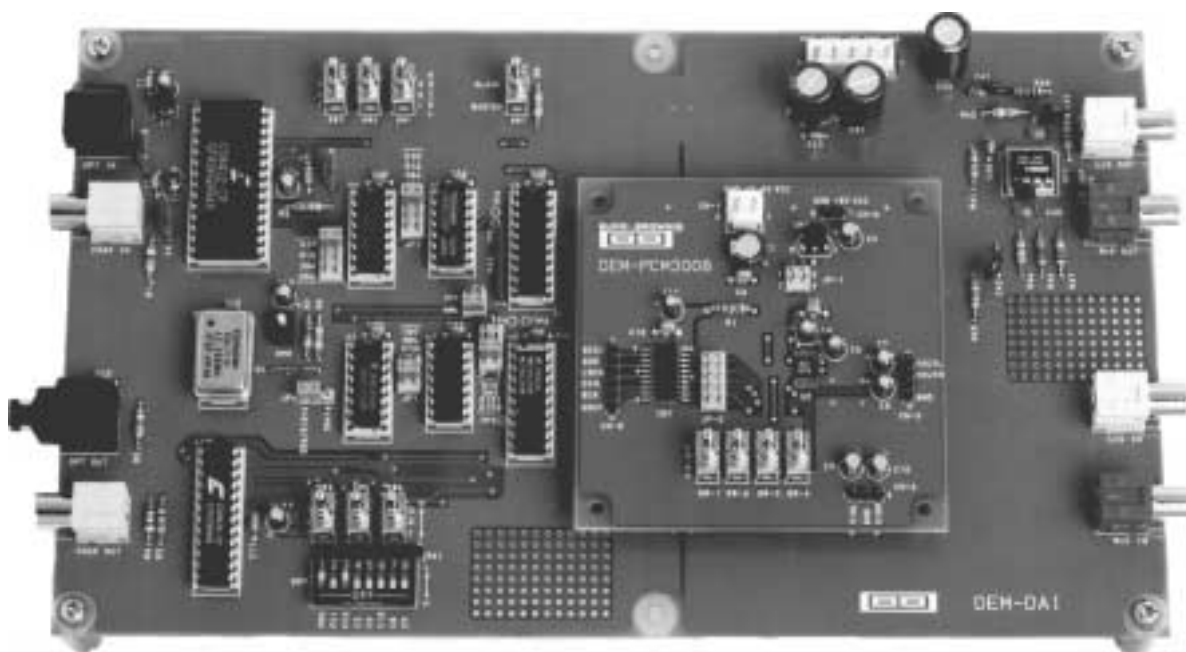


Figure 1. DEM-DAI3008

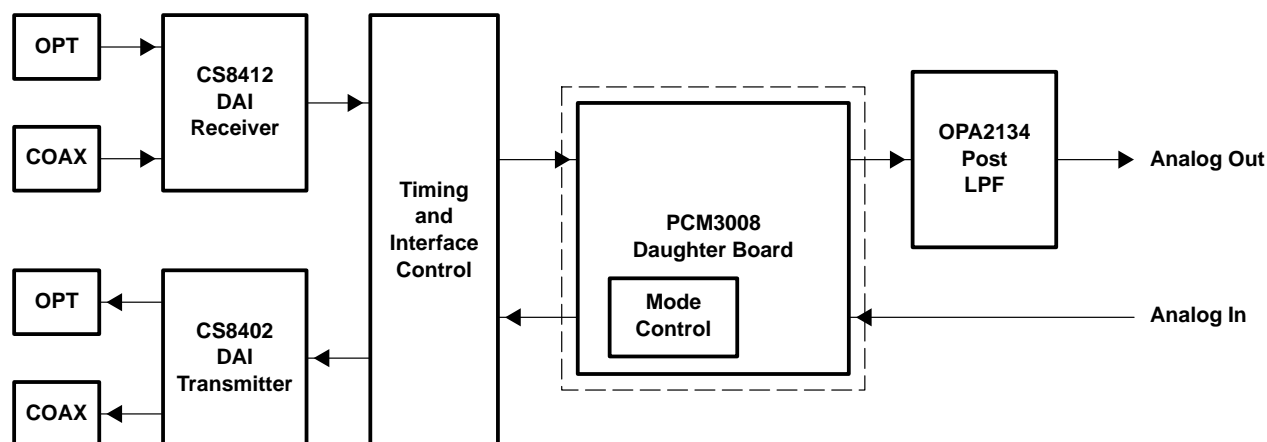


Figure 2. DEM-DAI3008 Block Diagram

2 Ordering Information

Model	Construction
DEM-DAI3008	PCM3008 daughterboard and DAI motherboard

3 Operating Controls and Connections

3.1 Daughterboard Controls

3.1.1 Switch Settings

The operation of de-emphasis on the PCM3008 is controlled by SW1 and SW2.

SW1 (DEM0)	SW2 (DEM1)	De-emphasis
L	L	44.1 kHz
H	L	OFF
L	H	48 kHz
H	H	32 kHz

The operation of the power-down mode for the DAC is controlled by SW3, and for the ADC by SW4.

SW3 (PDDA)	DAC Operation
L	Power-down mode
H	Normal operation

SW4 (PDAD)	ADC Operation
L	Power-down mode
H	Normal operation

3.1.2 Power Supply Connections

The PCM3008 daughterboard can accept power from either of two sources. Either 2.4 V supplied via CN-1 powers the board directly, or an onboard 2.5-V regulator powers the PCM3008 using a 5-V source. The 5-V power comes from the 5-V supply on the DAI motherboard via connector CN-2. Power source selection is accomplished by the use of jumper JP1.

JP-1 Setting	Power Supply Selected
1-2	5 V at CN-2
3-4	2.4 V at CN-1

3.2 DAI Motherboard Controls

3.2.1 Switch Settings

Selection of the audio output interface format for the DAI receiver is controlled by SW3, SW2, and SW1.

SW3(M2)	SW2(M1)	SW1(M0)	Audio Format
L	L	L	16–24-bit, MSB-first, left-justified
L	H	L	IIS
H	L	H	16-bit, MSB-first, right-justified
H	H	L	18-bit, MSB-first, right-justified

NOTE: JP6 must be connected INV when 16–24-bit, left-justified is selected.

Selection of the audio input interface format for the DAI transmitter is controlled by SW4, SW5, and SW6.

SW4(M2)	SW5(M1)	SW6(M0)	Audio Format
L	L	H	16–24-bit, MSB-first, left-justified
H	L	L	IIS
H	L	H	16-bit, MSB-first, right-justified
H	H	L	18-bit, MSB-first, right-justified

The operating mode and sampling frequency of the DAI transmitter are selected using PRO, FC1, and FC0 on SW9.

PRO: H = Consumer mode, L = Professional mode

FC1: Channel status bit 24 in consumer mode

FC0: Channel status bit 25 in consumer mode

FC1	FC0	Sampling Frequency
L	L	44.1 kHz
L	H	48 kHz
H	L	32 kHz

The remaining switches on SW9 are labelled C2, C3, C8, C9, and C15. They are used for the selection of channel status bits from the CS8404, and correspond to channel status bits 2, 3, 8, 9, and 15, respectively.

SW7 is the master/slave selection switch. It must be set to slave for proper operation the DAC and codec of the PCM3008.

3.2.2 Jumper Selections

JP1 selects the system clock source.

XTAL: System clock generated by onboard XTAL oscillator module

NML: System clock generated by DAI receiver

INV: Inverted system clock generated by DAI receiver

JP2 selects the BCK clock source.

DIR: BCK clock generated by DAI receiver
256/384/512: BCK clock generated by XTAL oscillator

JP3 selects the LRCK (f_s) clock source.

DIR: LRCK clock generated by DAI receiver
256/384/512: LRCK clock generated by XTAL oscillator

JP4 selects the clock frequency of the XTAL oscillator clock.

256/512fs: for 256 f_s or 512 f_s operation
384fs: for 384 f_s operation

JP5 selects the DAI transmitter clock source.

512,384 : 384 f_s or 512 f_s XTAL clock
DIR1: 256 f_s clock from XTAL clock or clock generated by DAI receiver
DIR2: Transparent operating mode for DAI transmitter

NOTE: In certain applications it is desirable to receive digital audio data with the CS8412 and retransmit it with the CS8402. In these situations, user and validity information and channel status must pass through unaltered. Details of transparent operation are described in Crystal's CS8402 data sheet.

3.2.3 Typical Board Settings

Jumper settings that are considered appropriate for some typical operating conditions are listed in the following tables.

Typical settings for DAC operation

JP1	JP2	JP3	JP4	JP5	JP6
NML	DIR	DIR	–	–	NML

Typical settings for ADC operation by DAI receiver clock

JP1	JP2	JP3	JP4	JP5	JP6
NML	DIR	DIR	–	DIR1	NML

Typical settings for ADC operation by XTAL clock

JP1	JP2	JP3	JP4	JP5	JP6
XTAL	256 to 512	256 to 512	256 to 512	512/DIR1	NML

4 Physical and Electrical

The silkscreen of the PCM3008 daughterboard is shown in Figure 3, and the top and bottom copper layers are shown in Figure 4 and Figure 5, respectively. Figure 6 is the schematic of the daughterboard, and the schematic of the motherboard is in Appendix A.

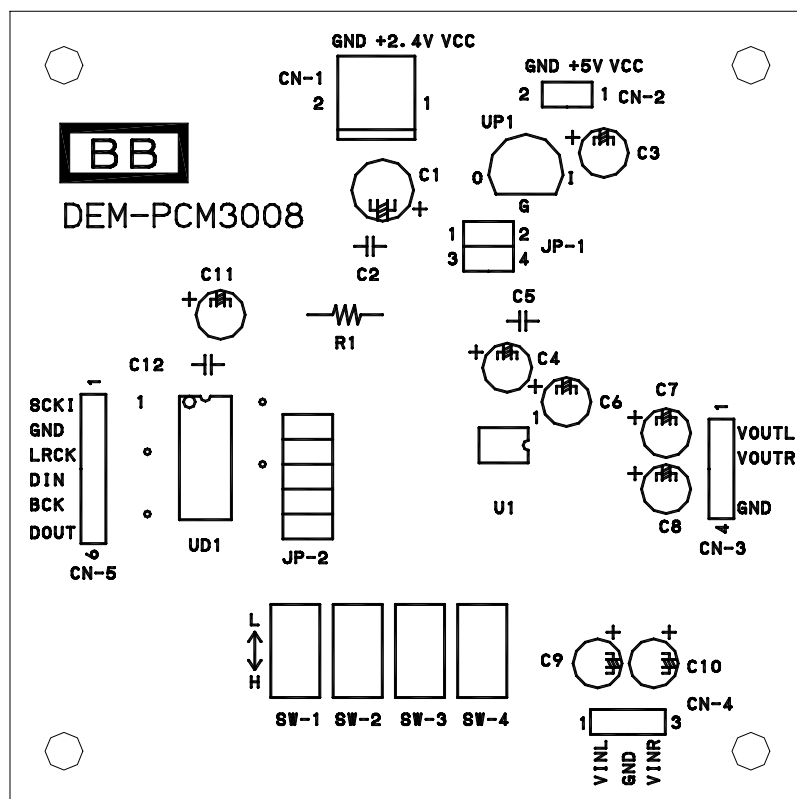


Figure 3. DEM-DAI3008 Board Silkscreen

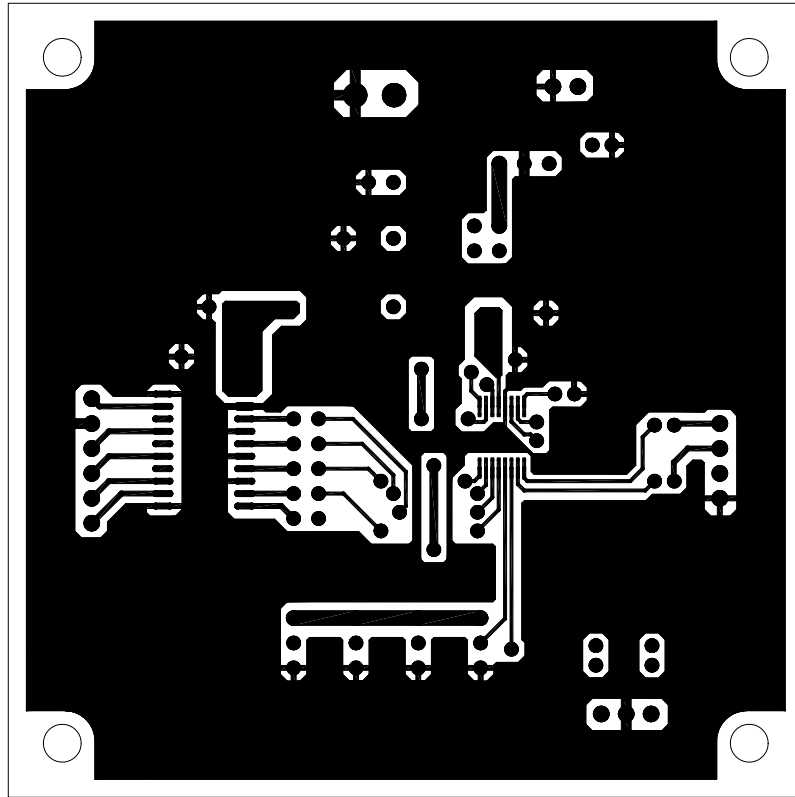


Figure 4. DEM-DAI3008 Board Top Copper Layer

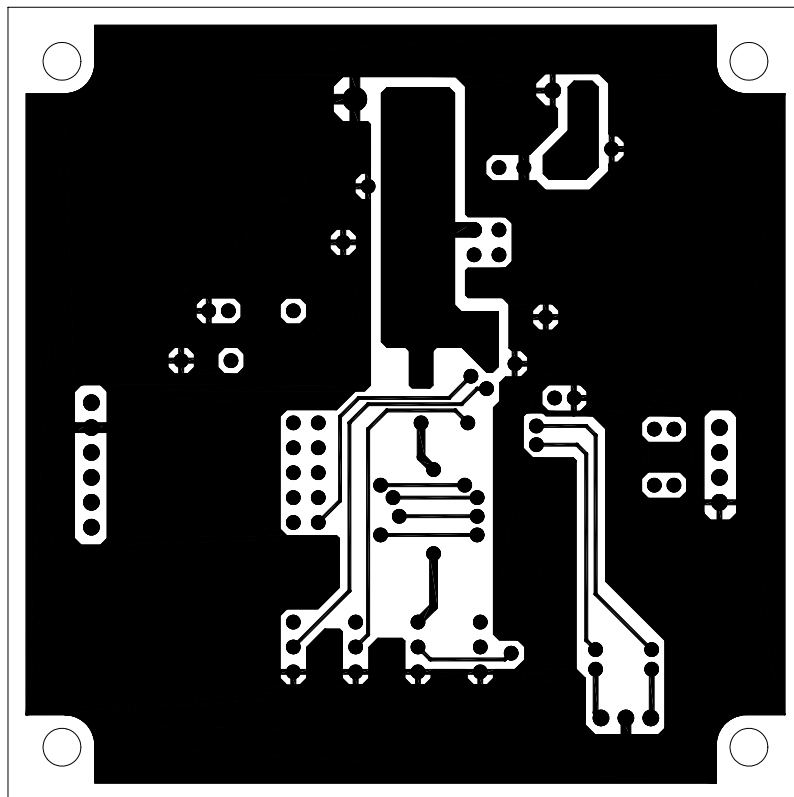


Figure 5. DEM-DAI3008 Board Bottom Copper Layer

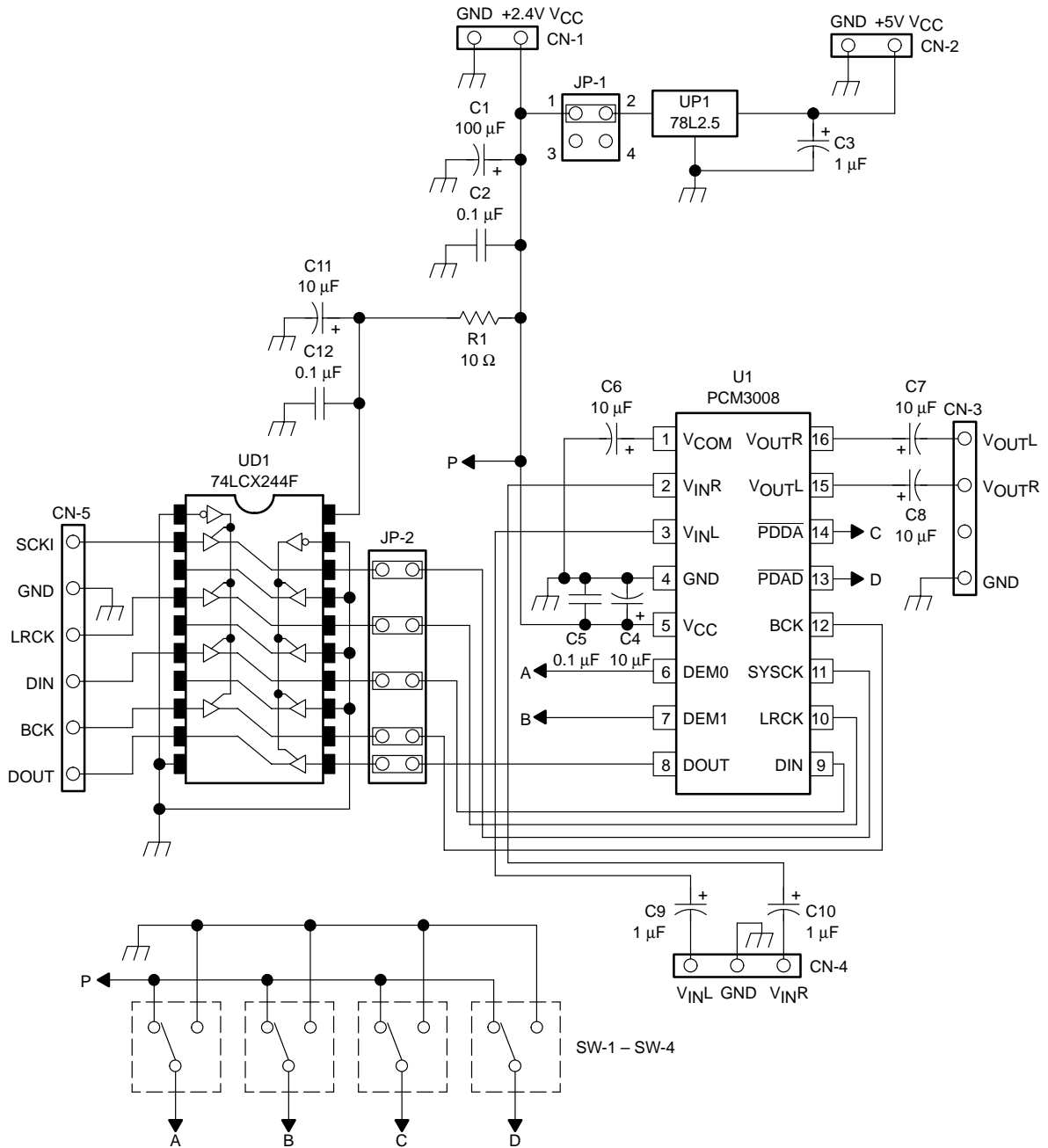
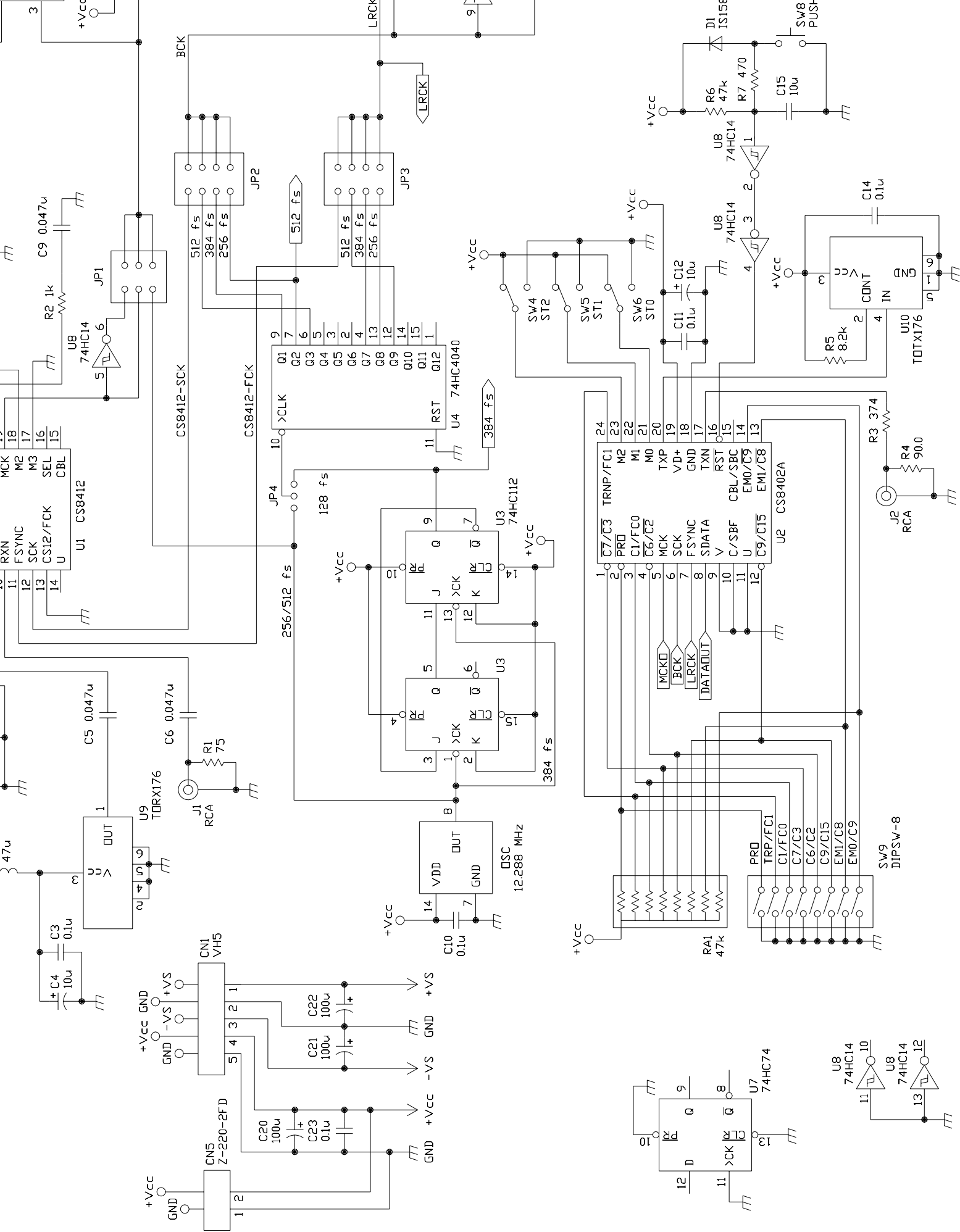


Figure 6. DEM-DAI3008 Schematic Diagram

Appendix A DEM-DAI Motherboard Schematic Diagram



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