TEXAS INSTRUMENTS

DEM-DAI1804

PCM1804 Evaluation Board

User's Guide

March 2002

DAV Digital Audio/Imaging Japan (DAL)

SLEU015

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Preface

Read This First

About This Manual

This user's guide provides a description of the DEM-DAI1804 evaluation module, including product specifications, board layout and silkscreening, and schematic diagrams.

How to Use This Manual

This document contains the following chapters:

Chapter 1 – *Description*
Chapter 2 – *Schematics and Printed-Circuit Board*

Related Documentation From Texas Instruments

PCM1804 Full Differential Analog Input 24-Bit, 192-kHz Stereo A/D Converter – Literature No. SLES022A

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Chapter 1

Description

The DEM-DAI1804 is an evaluation board for the PCM1804 192-kHz, 24-bit PCM/DSD-compatible audio A/D converter, which has digital audio transmitter, mode controls switch, on-board oscillator, LPF and single-end/differential converter.

The DEM-DAI1804 operates from 5-V and ±15-V analog power supplies, and with a balanced or unbalanced analog signal input.

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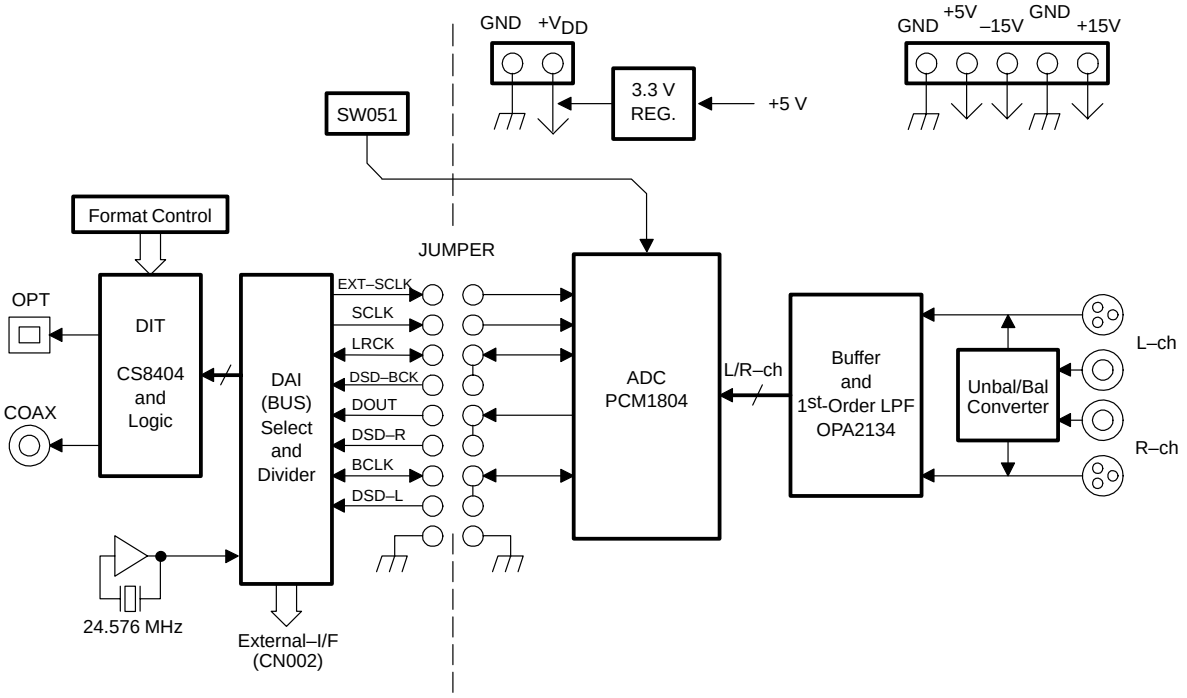
1.1 Block Diagram

Figure 1–1. DEM-DAI1804 Block Diagram



1.2 DEM-DAI1804 Basic Connection and Operation

- ❏ Connect the 5-V and ±15-V power supplies to V_{CC}, AV_{CC}, $–AV_{CC}$, and GND on connectors CN051–CN055.
- ❏ Connect the S/PDIF output signal via CN003 (coax) or U001 (optical).
- ❏ Select the system clock from the onboard oscillator or external input clock (CN001) using switch/jumper to PCM1804.
- ❏ Set the data format using SW001, JP003, and SW051.
- ❏ Select master or slave mode using SW002, JP002, and JP004.

1.2.1 Configuration Controls

Table 1–1. Analog Input Selection (CN103/107 for L Channel, CN104/108 for R Channel) Balanced Input: CN111/112, Unbalanced Input: CN113/114

Input	Jumper-Pin Position
Balanced (default)	BAL
Unbalanced	UNBAL

Table 1–2. Output Impedance Selection for Pre-LPF/Buffers (CN101/105 for L-Channel, CN102/106 for R-Channel)

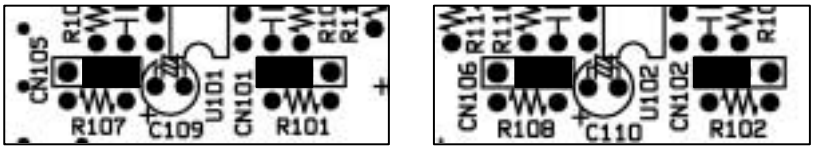
Output Impedance	Jumper-Pin Position
0-Ω (default)	
51-Ω	

Table 1–3. Biasing Selection of Pre-LPF/Buffers (CN109/110)

Biasing	Jumper-Pin Position
Op amp	OP AMP
PCM1804 (default)	PCM1804

Table 1–4. PCM1804: HPF Bypass Control (SW051)

HPF Bypass	BYPASS (SW051)
Disable	High
Enable (default)	Low

Table 1–5. PCM1804: Master/Slave and Oversampling Rate Selection (JP002/004 and SW002/051)

MODE	OVERSAMPLING RATIO	SYSCLK	OSR2 (SW051)	OSR1 (SW051)	OSR0 (SW051)	M/S Select (SW002)	BCK Select (JP002)	LRCK Select (JP004)
† Master mode	Single rate (× 128 f_S)	768 f_S	LOW	LOW	LOW	Master	Remove jumper pin	Remove jumper pin
	† Single rate (× 128 f_S)	512 f_S	LOW	LOW	HIGH			
	Single rate (× 128 f_S)	384 f_S	LOW	HIGH	LOW			
	Single rate (× 128 f_S)	256 f_S	LOW	HIGH	HIGH			
	Dual rate (× 64 f_S)	384 f_S	HIGH	LOW	LOW			
	Dual rate (× 64 f_S)	256 f_S	HIGH	LOW	HIGH			
	Quad rate (× 32 f_S)	192 f_S	HIGH	HIGH	LOW			
	Quad rate (× 32 f_S)	128 f_S	HIGH	HIGH	HIGH			
Slave mode	Single rate (× 128 f_S)	Auto-detect	LOW	LOW	LOW	Slave	Select /2, /4, or /8 (See Table 1–7)	Select /128, /256, or /512 (See Table 1–8)
	Dual rate (× 64 f_S)		LOW	LOW	HIGH			
	Quad rate (× 32 f_S)		LOW	HIGH	LOW			

† Default settings

Table 1–6. System Clock Dividing-Ratio for MCK: 128 f_S-CS8404 (JP001)

Dividing-Ratio	Jumper-Pin Position	BCK Value (24.576 MHz oscillator: default)
1/1	/1	—
1/2	/2	12.288 MHz (128 f_S for f_S = 96 kHz)
1/4	/4	6.144 MHz (128 f_S for f_S = 48 kHz)

Table 1–7. Bit Clock Dividing-Ratio (JP002)

Dividing-Ratio	Jumper-Pin Position	BCK Value (24.576 MHz oscillator: default)
1/2 (Slave)	/2	12.288 MHz (64 f_S for f_S = 192 kHz)
1/4 (Slave)	/4	6.144 MHz (64 f_S for f_S = 96 kHz)
1/8 (Slave)	/8	3.072 MHz (64 f_S for f_S = 48 kHz)
— (Master)	Remove	—

Table 1–8. LR Clock Dividing-Ratio (JP004)

Dividing-Ratio	Jumper-Pin Position	MCK Value (24.576 MHz oscillator: default)
1/128 (Slave)	/128	192 MHz
1/256 (Slave)	/256	96 MHz
1/512 (Slave)	/512	48 MHz
— (Master)	Remove	—

Table 1–9. Data Format Selection (JP003 and SW051)

DATA FORMAT	JP003	FMT1	FMT0
PCM, Left justified, 24-bit	L/J24	LOW	LOW
PCM, I^2S, 24-bit (default)	I^2S	LOW	HIGH
DSD	—	HIGH	HIGH

Note: FMT0 and FMT1 must be stable when RESET changes from LOW to HIGH.

Table 1–10. System Clock Source Selection (JP005)—Internal clock: X001/24.576 MHz, External Clock Input: CN001

Clock Source	Jumper-Pin Position
Internal (default)	INT
External	EXT

1.2.2 Manual Reset (SW003)

SW003 is the reset switch for the PCM1804 and CS8404.

1.2.3 Digital Signal I/F to PCM1804 (JP052)

Digital signals are generated by an internal oscillator, divider, and the PCM1804. For each pair of pins shorted, the corresponding digital signal (see Figure 1–2) is input to the PCM1804 and CS8404.

Figure 1–2. Digital Signal Selection (JP052)

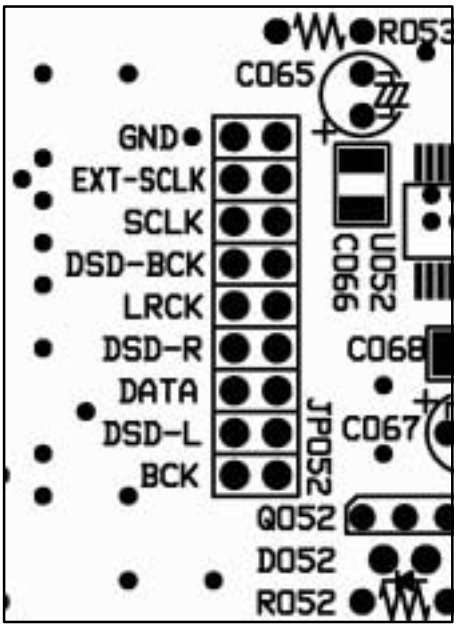


Table 1–11. S/PDIF Transmitter Format: CS8404 Configuration (SW004)

Professional Mode			**Consumer Mode**		
Switch	**L=0, H=1**		**Switch**	**L=0, H=1**	
PRO	0	Professional mode	PRO	1	Consumer mode
C9		C8,C9,C10,C11 – Channel mode (1 of 4)	C15		Generation status
	1	0000 – Not indicated (default: 2-ch)		1	0 – (see the S/PDIF standard)
	0	0100 – Stereophonic		0	1 – (see the S/PDIF standard)
EM1,EM0		C2,C3,C4 – Emphasis (2 of 3)	C8,C9		C8–C14 – Category code (2 of 7)
	1 1	Not indicated (default: none)		1 1	0000 0000 – General
	1 0	No emphasis		1 0	0100 0000 – PCM encoder/decoder
	0 1	50/15Us		0 1	1000 0000 – CD
	0 0	CCITT J.17		0 0	1100 0000 – DAT
C6,C7		C6,C7 – Sample frequency	C3		C3,C4,C5 – Emphasis (1 of 3)
	1 1	Not indicated (default: 48 kHz)		1	000 – None
	1 0	48 kHz		0	100 – 50/15Us
	0 1	44.1 kHz	C2		C2 – Copy/copyright
	0 0	32 kHz		1	0 – Copy inhibited/copyright asserted
C1		C1 – Audio		0	1 – Copy permitted/copyright not asserted
	1	0 – Normal audio	FC1, FC0		C24,C25,C26,C27 – Sample frequency
	0	1 – Nonaudio		1 1	44.1 kHz
TRNPT		Transparent mode		1 0	48 kHz
	0	0 – Normal operation		0 1	32 kHz
	1	1 – Transparent mode		0 0	44.1 kHz, CD mode

Chapter 2

Schematics and Printed-Circuit Board

This chapter presents the DEM-DAI1804 printed-circuit board and schematics.

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2.1 DEM-DAI1804 Printed-Circuit Board

Figure 2–1. DEM-DAI1804 Silkscreen

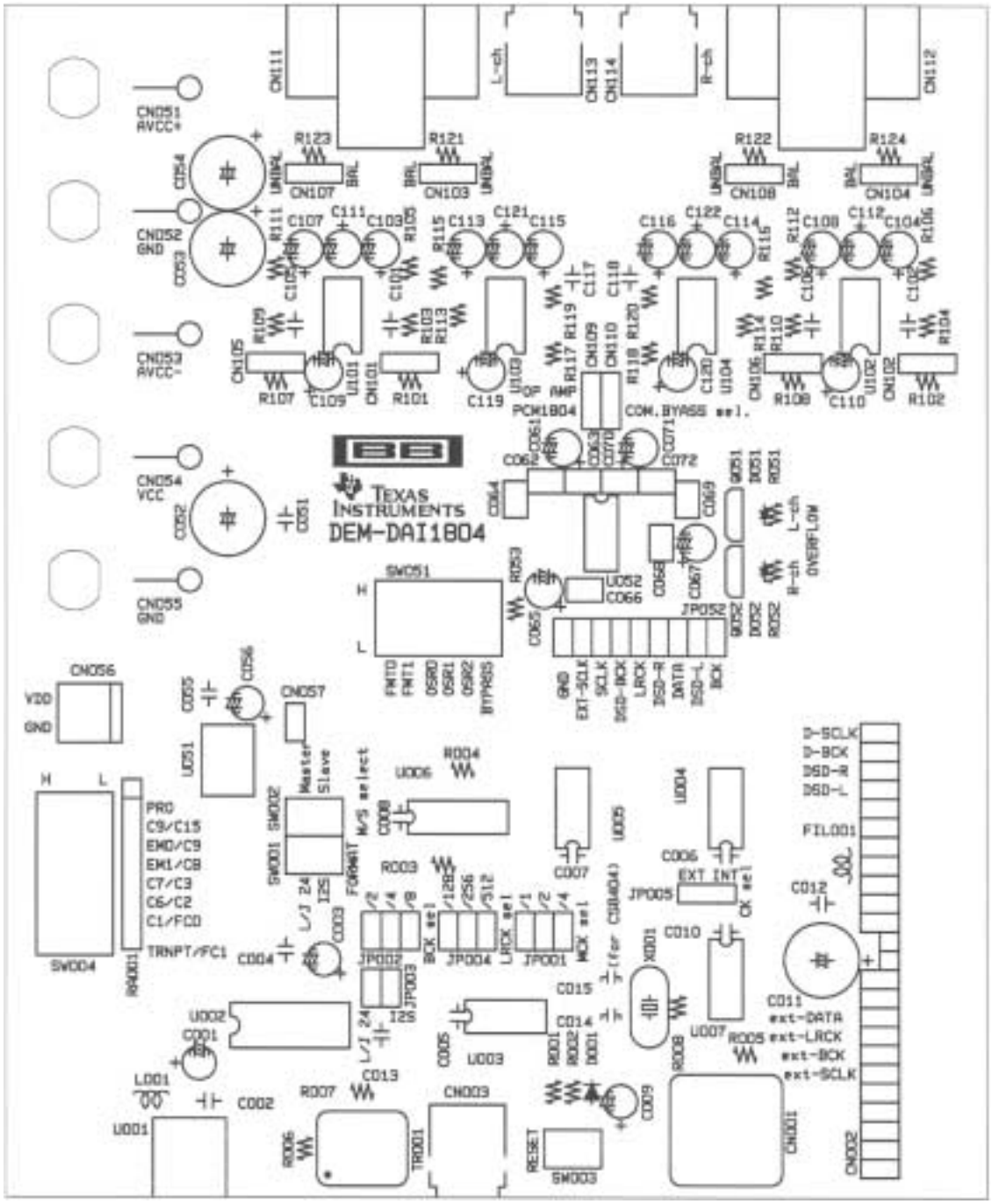


Figure 2–2. DEM-DAI1804—Top View

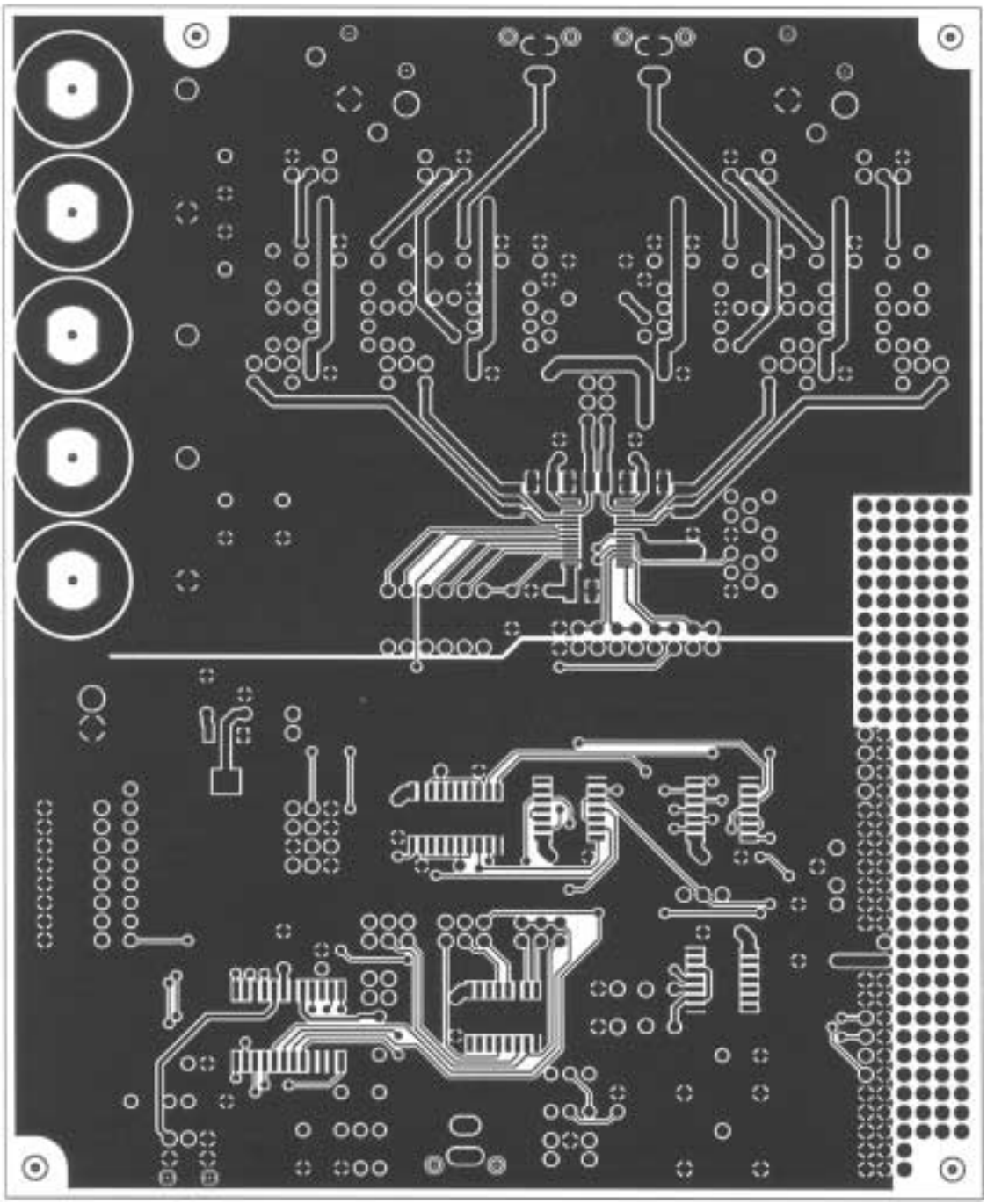
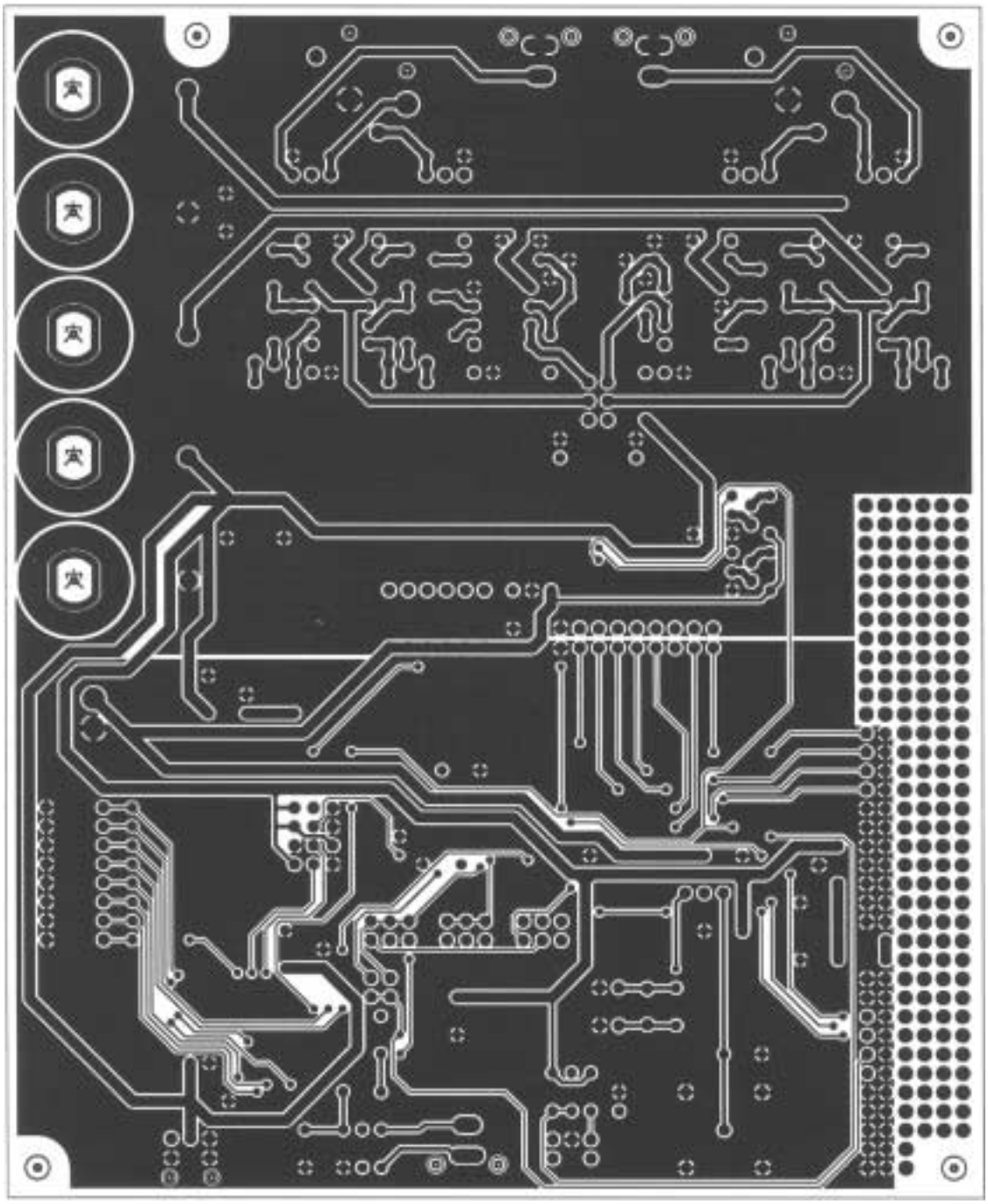
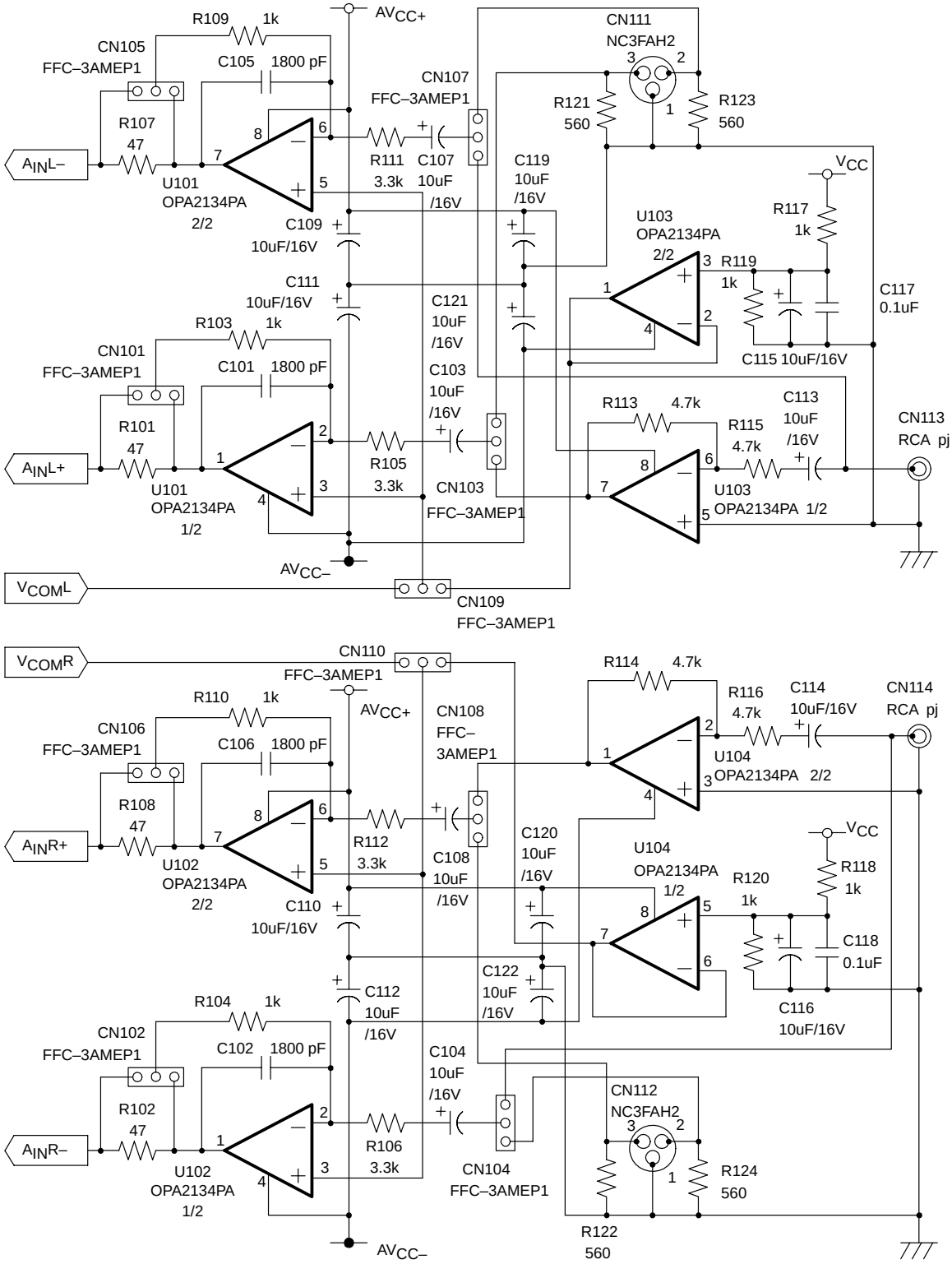


Figure 2–3. DEM-DAI1804—Bottom View



2.2 DEM-DAI1804 Schematics

Figure 2–4. DEM-DAI1804 Analog Section (Low-Pass Filter and Amplifier)



Note: Recommended value of capacitors C101/102/105/106 is 1800 pF for normal conditions. If an input signal level more than –6 dB of full scale at 100 kHz is applied in DSD mode, use 3300 pF instead.

Figure 2–5. DEM-DAI1804 A/D Converter Section

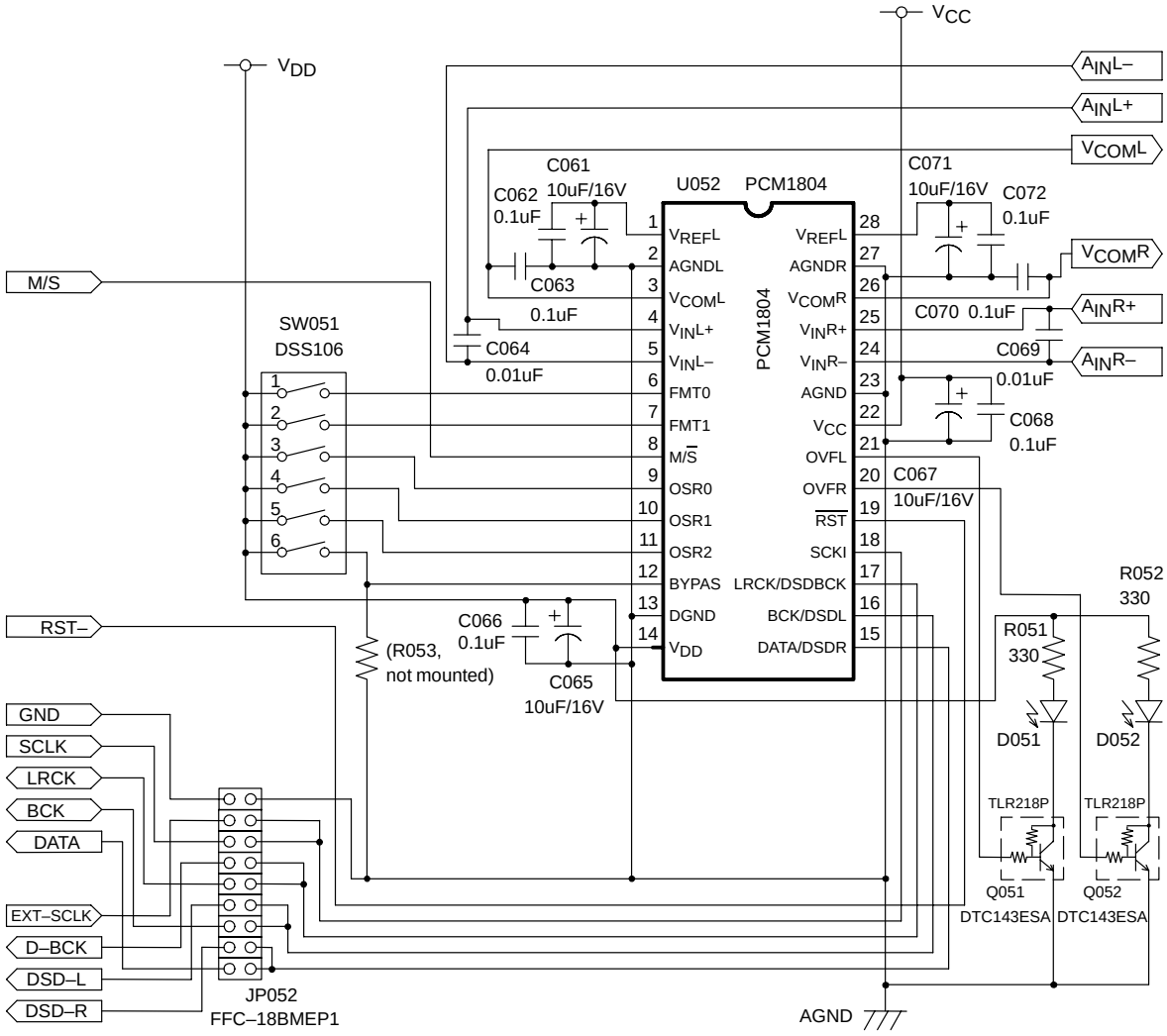


Figure 2–6. DEM-DAI1804 Regulator and Connector

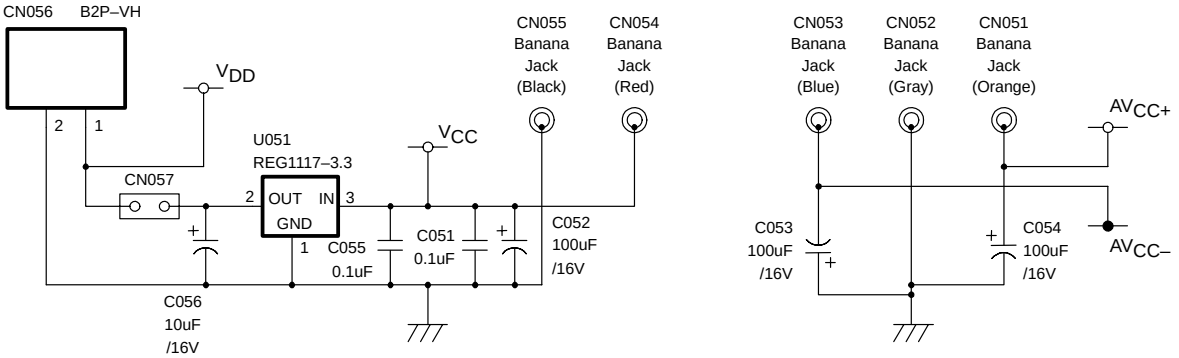


Figure 2–7. DEM-DAI1804 Digital Section (Digital Audio Interface)