

UCC2977EVM

**High Efficiency CCFL Backlight Push-Pull
Converter (1.8 W)**

User's Guide

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the UCC2977 CCFL backlight converter evaluation module (EVM). The users guide includes a schematic diagram, bill of materials and test results.

How to Use This Manual

This document contains the following chapters:

- ☐ Chapter 1—Hardware
- ☐ Chapter 2—Design Procedure
- ☐ Chapter 3—Test Results

Related Documentation From Texas Instruments

- ☐ Texas Instruments Users Manual, *UCC3976/7 Users Manual*, TI Literature Number SLUU108
- ☐ Texas Instruments Data Sheet, *UCC2977*, TI Literature Number SLUS499A

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Contents

1	Hardware	1-1
1.1	Introduction	1-2
1.2	Operating Specifications	1-2
1.3	Schematic	1-3
1.4	Bill of Materials	1-4
1.5	Board Layout	1-5
2	Design Procedure	2-1
2.1	Push-Pull Inductor Selection	2-2
2.2	Frequency Range Setting	2-2
2.3	Analog Dimming of the Lamp	2-2
2.4	Open-Lamp Voltage Programming	2-3
2.5	Shutdown	2-3
2.6	No Lock	2-3
2.7	Burst Dimming	2-4
2.8	Clamp Circuit (Optional)	2-4
3	Test Results	3-1
3.1	Test Setup	3-2
3.1.1	Lighting CCFL	3-2
3.1.2	Analog Dimming Test	3-3
3.1.3	Burst Dimming Test	3-4
3.2	Test Results	3-5

Figures

1-1	UCC2977EVM Schematic	1-3
1-2	Top Silk Screen With Top Copper Layer	1-5
1-3	Top Layer Copper	1-5
1-4	Bottom Layer Copper	1-5
3-1	Test Setup	3-2
3-2	Test Setup for Analog Dimming	3-3
3-3	Test Setup for Burst Dimming	3-4
3-4	Efficiency With a Low Profile Sumida Inductor	3-5
3-5	Efficiency With a High Profile Toko Inductor	3-5
3-6	Transformer Input/Output Voltages at $V_I = 3\text{ V}$	3-6
3-7	Transformer Input/Output Voltages at $V_I = 6\text{ V}$	3-6
3-8	Burst Dimming With 50% Duty Cycle	3-6
3-9	Burst Dimming With 80% Duty Cycle	3-7
3-10	Open Lamp Protection	3-7

Tables

1-1	Operating Specifications	1-2
1-2	Bill of Materials Required for the UCC2977 (SLUP178)	1-4

Hardware

The UCC2977 evaluation module (SLUP178) provides a reference design for evaluating the performance of a high efficiency CCFL backlight converter using the UCC2977 (push-pull backlight controller). The device contains all of the circuitry necessary to control a backlight converter. This chapter contains the schematic, board layout, and the bill of materials. The evaluation module (EVM) performance specifications are also given.

Topic	Page
1.1 Introduction	1-2
1.2 Operating Specifications	1-2
1.3 Schematic	1-3
1.4 Bill of Materials	1-4
1.5 Board Layout	1-5

1.1 Introduction

The UCC2977 EVM (SLUP178) is a 1.8-W dc/ac inverter module used to drive a cold cathode fluorescent lamp (CCFL) with a piezoelectric transformer (PZT). This EVM consists of a push-pull circuit using the UCC2977 controller.

The principle of operation for the inverter is explained in the application section of the UCC2977 data sheet.

1.2 Operating Specifications

This section summarizes the performance specifications of the SLUP178 converter. Table 1–1 lists the operating specifications for the SLUP178.

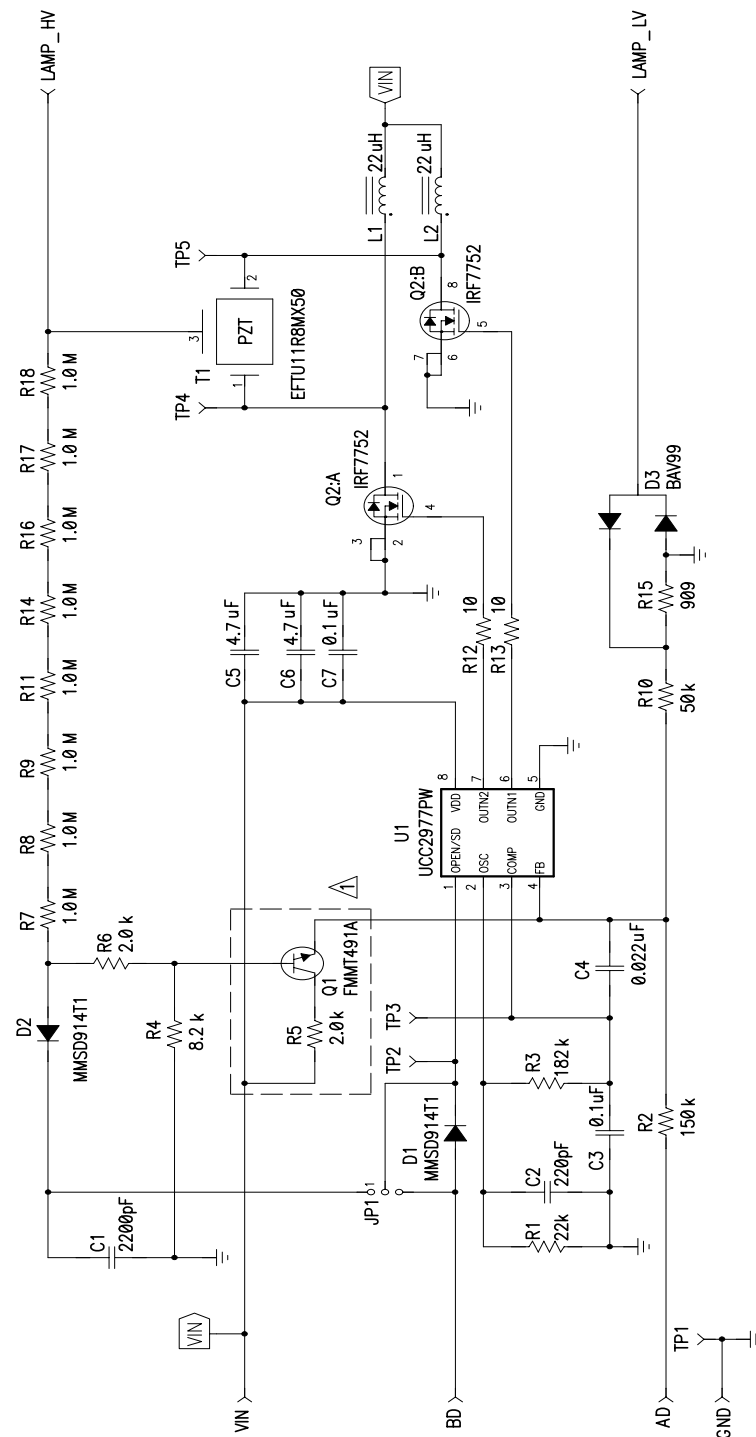
Table 1–1. Operating Specifications

Input voltage (V_{IN})	3–6 Vdc
Output voltage (Lamp_HV, Lamp LV)	300 Vac, rms
Output current (lamp current)	4.7 mA, rms
Operating frequency (kHz)	100 kHz
Burst dimming (BD) [†]	Square wave, 120 Hz, 0 to 3 V
Analog dimming (AD)	0–3 Vdc
CCFL lamp	JKL BF3100–20B (100 mm, 270 V _{RMS})

[†] Use a function generator.

1.3 Schematic

Figure 1–1. UCC2977EVM Schematic



 Optional max operating voltage clamp

1.4 Bill of Materials

Table 1–2. Bill of Materials Required for the UCC2977 (SLUP178)

Count	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 2200 pF, 50 V, X7R, 20%	603	Murata	GRM188R71H222KA01
1	C2	Capacitor, ceramic, 220 pF, 50 V, X7R, 20%	603	Murata	GRM188R7H221KD01
2	C3, C7	Capacitor, ceramic, 0.1 μ F, 25 V, X7R, 20%	805	Murata	GRM21BR71E104KA01
1	C4	Capacitor, ceramic, 0.022 μ F, 25 V, X7R, 20%	603	Murata	GRM188R71E223KA01
2	C5, C6	Capacitor, ceramic, 4.7 μ F, 10 V, X5R, 20%	1206	Murata	GRM31CR61A475KA01
2	D1, D2	Diode, switching, 1.0 mA, 75 V	SOD123	Motorola	MMSD914T1
1	D3	Diode, dual ultra fast, series, 200 mA, 70 V	SOT23	Fairchild	BAV99
1	JP1	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 $\times$ 3"	Sullins	PTC36SAAN
2	L1, L2	Inductor, SMT, 22 μ H, 1.2 A, 128 m Ω	6.7 $\times$ 6.7 $\times$ 3 mm	Sumida	CDRH6D28-220NC
		(or Toko inductor, 22 μ H, 115 m Ω)	7.6 $\times$ 7.6 $\times$ 5.1 mm	Toko	646CY-220M
1	Q1	Transistor, NPN, high performance, 500 mA	SOT23	ZeTek	FMMT491A
1	Q2	XSTR, MOSFET, N-channel, 30 V, 4.6 A, Rds 35 m Ω	TSSOP8	IR	IRF7752
1	R1	Resistor, chip, 22 k Ω , 1/16 W, 1%	603	Std	Std
1	R10	Resistor, chip, 50 k Ω , 1/16 W, 1%	603	Std	Std
2	R12, R13	Resistor, chip, 10 Ω , 1/16 W, 1%	603	Std	Std
1	R15	Resistor, chip, 909 Ω , 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 150 k Ω , 1/16 W, 1%	603	Std	Std
1	R3	Resistor, chip, 182 k Ω , 1/16 W, 1%	603	Std	Std
1	R4	Resistor, chip, 8.2 k Ω , 1/16 W, 1%	603	Std	Std
2	R5, R6	Resistor, chip, 2.0 k Ω , 1/16 W, 1%	603	Std	Std
8	R7, R8, R9, R11, R14, R16, R17, R18	Resistor, chip, 1.0 M Ω , 1/10 W, 1%	805	Std	Std
1	T1	Transformer, custom, Piezoelectric, SMT	0.760 $\times$ 0.244	Panasonic	EFTU11R8MX50
2	TP1, GND	Test point, black, 1 mm	0.038	Farnell	240-333
9	TP2–TP5, VIN, BD, AD, LAMP_HV, LAMP_LV	Test point, red, 1 mm	0.038	Farnell	240-345
1	U1	IC, CCFL push-pull driver	TSSOP-08	TI	UCC2977PW
1	—	PCB, 3.55" $\times$ 0.905" $\times$ 0.62"		Any	SLUP178

1.5 Board Layout

Figure 1–2. Top Silk Screen With Top Copper Layer

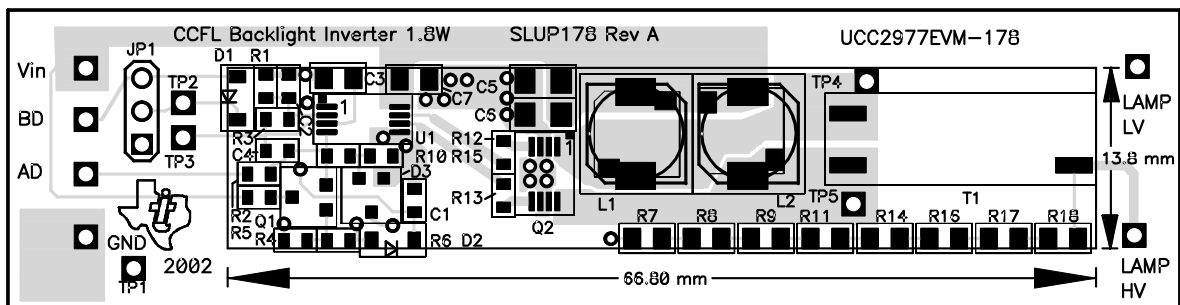


Figure 1–3. Top Layer Copper

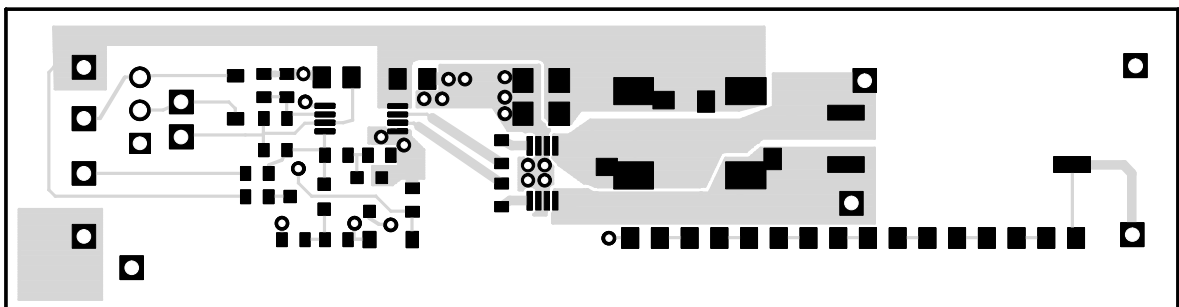
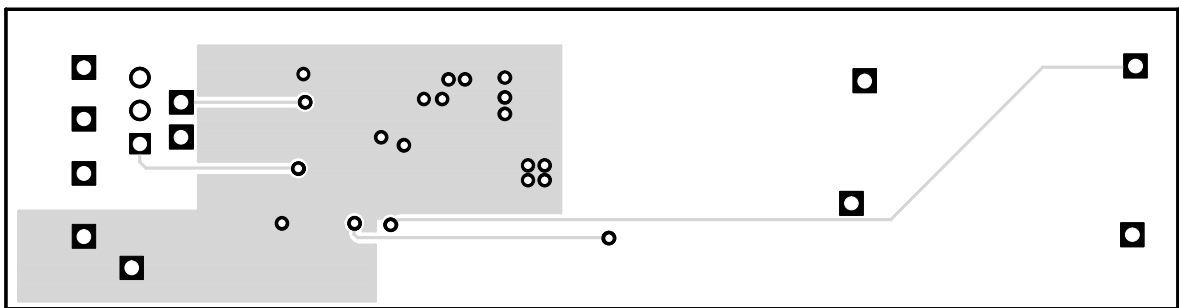


Figure 1–4. Bottom Layer Copper



Design Procedure

This chapter describes how to design the UCC2977EVM.

Topic	Page
2.1 Push-Pull Inductor Selection	2-2
2.2 Frequency Range Setting	2-2
2.3 Analog Dimming of the Lamp	2-2
2.4 Open-Lamp Voltage Programming	2-3
2.5 Shutdown	2-3
2.6 No Lock	2-3
2.7 Burst Dimming	2-4
2.8 Clamp Circuit (Optional)	2-4

2.1 Push-Pull Inductor Selection

The push-pull topology requires a different approach for calculating the external inductor values. Referring to Figure 1–1, Q2A and Q2B are driven out of phase at 50% duty cycle. When Q2A is on, current is ramped up in L1. During the next switch cycle Q2B is turned on, Q2A is turned off, and the energy stored in L1 is transferred through the piezoelectric transformer. L1 resonates with the piezoelectric primary capacitance forming a half sinusoid at Q2A's drain. In order to achieve zero-voltage switching, the drain voltage must return to ground before the next switching cycle. This dictates that the LC resonant frequency must be greater than the switching frequency.

$$L < \frac{1}{4 \times \pi^2 \times f^2 \times C_p} \quad (1)$$

In the EVM with a 100 kHz switching frequency and 61.6 nF piezoelectric transformer, L1 and L2 must be less than 41 μ H for zero-voltage switching, so 22- μ H inductors are used.

A suitable capacitor must be chosen so that the peak-to-peak output ripple is within the limits allowable for the application.

2.2 Frequency Range Setting

The VCO frequency range is programmed with external components R1, R3 and C2. The frequency is determined by the voltage decay from 1.7 V to 0.6 V at the OSC pin. When the voltage reaches 0.6 V, an internal current source charges OSC back to 1.7 V. The decay time is determined by the value of C2 and the discharge currents generated in R1 and R3. An accurate NPO capacitor is recommended for C2 and 1% resistors are recommended for R1 and R3. The output frequency range can be calculated by equation 2:

$$f(V_{COMP}) = \frac{\left[\frac{R1 + R3}{R1 \times R3 \times C2} \right]}{2 \times \ln \left[\frac{1.7 \text{ V} \times (R1 + R3) - V_{COMP} \times R1}{(0.6 \text{ V} - V_{COMP}) \times R1 + 0.6 \text{ V} \times R3} \right]} \quad (2)$$

With C2 set at 220 pF, R1 at 22 k Ω and R3 at 182 k Ω , the frequency is 100 kHz.

2.3 Analog Dimming of the Lamp

For analog dimming, enable the open-lamp detection by connecting pin 1 to pin 2 of jumper JP1 and ground BD. Lamp intensity is controlled with the signal AD.

The RMS lamp current becomes:

$$I_{LAMP} = \frac{\left[1.5 \text{ V} \times (R2 + R10) - V_{AD} \times R10 \right] \pi}{\sqrt{2} \times R2 \times R15} \quad (3)$$

Zero volts on V_{AD} commands full current while 3 V commands minimum current. For the initially configured EVM, maximum current is 4.8 mA. R15 is selected to be 909 Ω setting V_{AD} to 0 V and lamp current to 4.8 mA. With R2 set to 150 K, R10 is calculated to be 50 K. The control-voltage to lamp-current equation for the EVM is:

$$I_{LAMP}(mA) = 4.89 - 1.22 \times V_{AD} \quad (4)$$

2.4 Open-Lamp Voltage Programming

It is necessary to suspend the power-stage operation if an open lamp occurs because the piezoelectric transformer has a high gain. The open-lamp detection circuit is composed of voltage divider R7, R8, R9, R11, R14, R16, R17, R18, R4, R6, D2, and C1. A 1.5 V comparator at the OPEN pin shuts down the inverter if an open lamp is triggered. The RMS secondary voltage at which an open lamp shutdown occurs can be calculated by equation (5).

$$V_{OPEN} = \frac{(1.5 \text{ V} + V_{diode}) \times \left(\sum_{i=7}^9 R_i + R11 + R14 + \sum_{j=16}^{18} R_j + R4 + R6 \right)}{\sqrt{2} \times (R4 + R6)} \text{ RMS} \quad (5)$$

With R7~R9, R11, R14, R16~R18 at 1 Meg each, R6 at 2 k and R4 at 8.2 k, the RMS value of open lamp threshold voltage at the secondary is 1220 V_{RMS} .

The value of capacitor C1 should be large enough to filter the sinusoid waveform into dc. For this board, 2200 pF was chosen. If C5 is too large, it takes extra time for OPEN/SD to climb to 1.5 V when the output voltage hits the open-lamp threshold, resulting in a higher output voltage than the set value.

The open-lamp level should be set high enough to avoid tripping during normal operation. Open-lamp detection is disabled for the burst-dimming mode by connecting pin 3 to pin 2 of JP1. Connect pin 1 to pin 2 of JP1 to enable open lamp protection.

2.5 Shutdown

The OPEN/SD pin is used for both open-lamp detection and commanded shutdown. When a voltage higher than 2.5 V is applied to OPEN/SD through D1, the part enters the shutdown or sleep mode where the oscillator is inactive and both outputs are high. In this mode, the part draws little current at the V_{DD} pin and the OPEN/SD pin.

2.6 No Lock

If the part fails to achieve regulation before reaching minimum frequency (comp > 2.2 V), it causes an internal retry counter to increment and then attempt another start up. If the application does not operate normally after 7 attempts, the controller enters an error-induced shutdown state removing power to the load.

2.7 Burst Dimming

Burst dimming can be implemented at the OPEN/SD pin at the cost of open-lamp detection.

Connect pin 2 to pin 3 of JP1 to disable the open-lamp detection circuit during burst dimming mode.

Since the feedback loop does not need to operate with minimum lamp current (as with analog dimming), the feedback capacitor, C4, can be reduced to 22 nF to improve the response time when the lamp restrikes.

To implement burst dimming on the EVM, AD should be grounded to set maximum lamp brightness. A low-frequency 0 V – 4 V square wave applied to BD will modulate the lamp current between zero and full intensity at the desired frequency. A low-frequency repetition rate greater than 120 Hz is recommended to avoid visible flicker. Applying 5 V at BD forces the lamp current to zero, where 0 V at BD will force maximum lamp current. The duty cycle of the square wave determines the lamp brightness as a percent of rated lamp current.

2.8 Clamp Circuit (Optional)

There is also a clamp circuit to limit the maximum secondary voltage.

This circuit is typically not needed since the CCFL strikes or the open-lamp circuit triggers before destructive levels are reached.

If R5 and Q1 are added to the board, the peak clamp voltage for the EVM is given by equation (6):

Since the feedback loop does not need to operate with minimum lamp current (as with analog dimming), the feedback capacitor, C4, can be reduced to 22 nF to improve the response time when the lamp restrikes.

$$V_{\text{CLAMP}} = \left(1.5 \text{ V} + V_{\text{be}}\right) \times \frac{(R7 + R8 + R9 + R11 + R14 + R16 + R17 + R18 + R6 + R4)}{R4} \text{ PEAK} \quad (6)$$

The peak clamped voltage for the evaluation board is 2200V.

The evaluation board components can be modified depending on the application requirements. A supply between 3 Vdc and 6 Vdc is required for this board to operate a 270~450 V cold-cathode fluorescent lamp (CCFL) from 1 mA to 4.8 mA. The input voltage range changes with different voltage lamp.

Test Results

This chapter describes how to properly connect and setup the UCC2977EVM. It also presents the test results, which cover efficiency, burst dimming, and open-lamp protection.

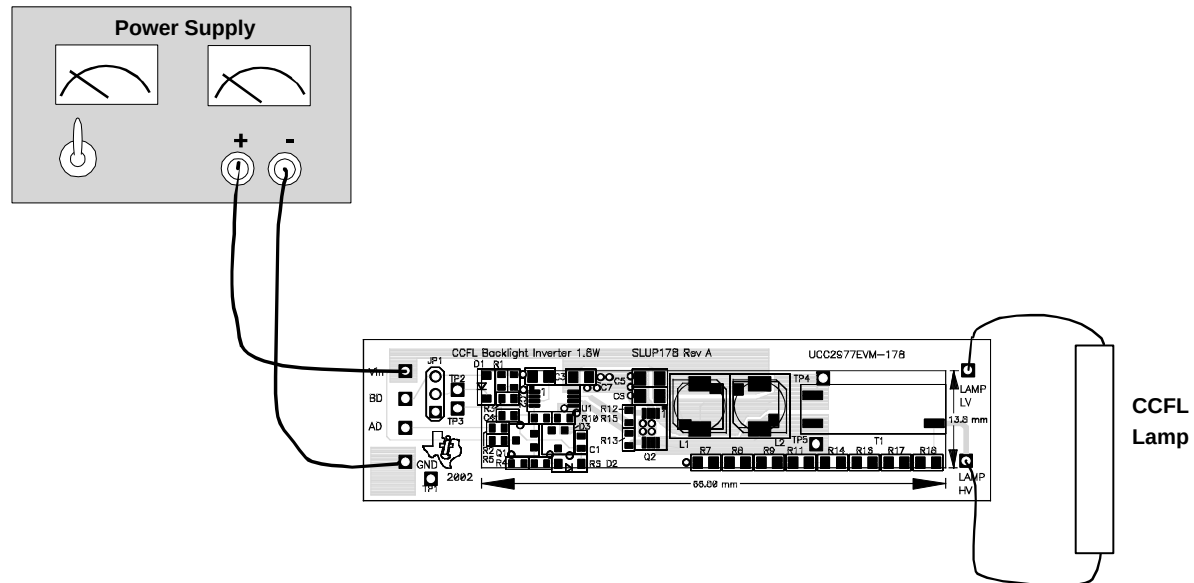
Topic	Page
3.1 Test Setup	3-2
3.2 Test Results	3-5

3.1 Test Setup

3.1.1 Lighting CCFL

A power supply with a power capability of 6 V/0.5 A is required for this test. Figure 3–1 shows the input/output connections to the SLUP178. Connect a 270-V lamp (BF3100–20B). Connect pin 1 to pin 2 of jumper JP1.

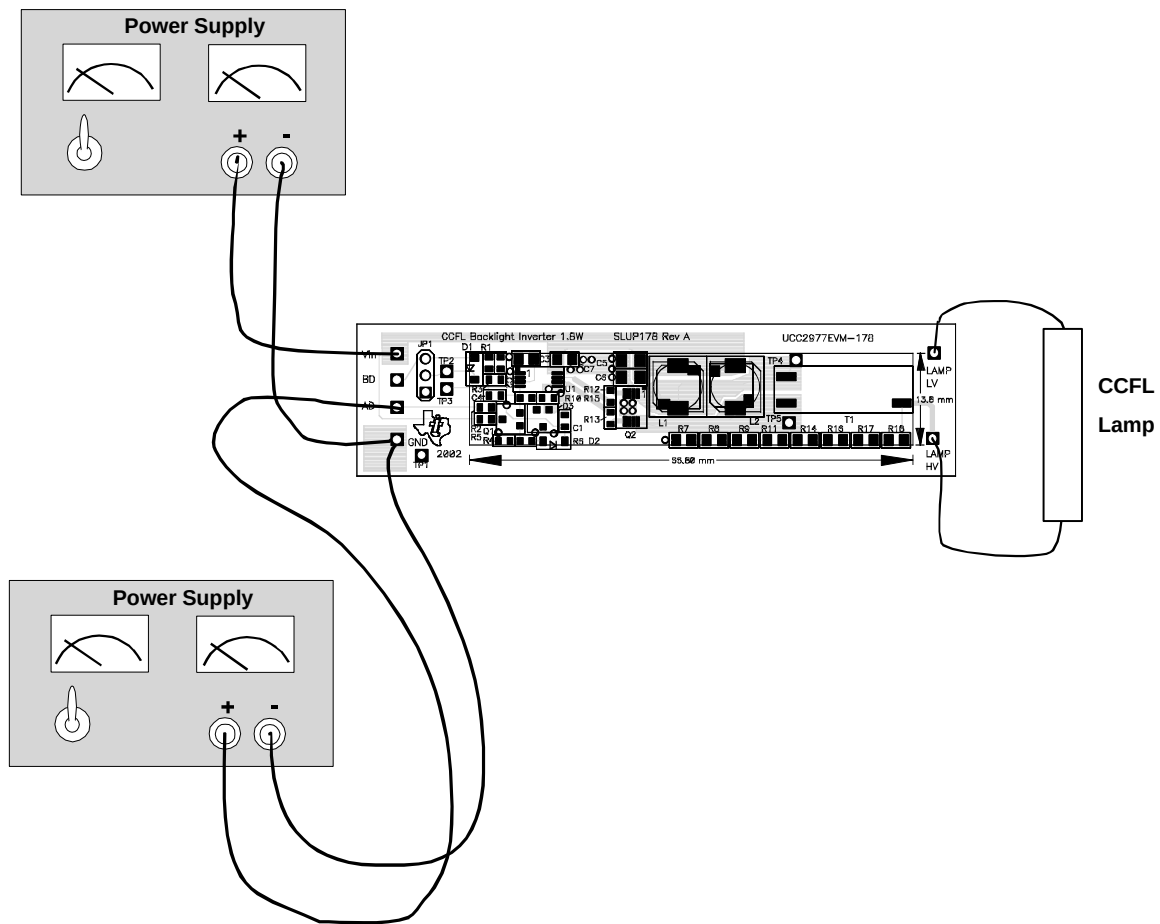
Figure 3–1. Test Setup



3.1.2 Analog Dimming Test

For analog dimming, enable the open-lamp detection by connecting pin 1 to pin 2 of jumper JP1. A power supply that has a power capability of 6 V/0.5 A is required for this test. Figure 3–2 shows the input/output connections to the SLUP178. The lamp intensity is controlled by V_{AD} (0–3 Vdc). Make sure the wire of the lamp is as short as possible and the lamp reflector (if there is one) is grounded to board ground. Do not let the high voltage wire cross any part of the board.

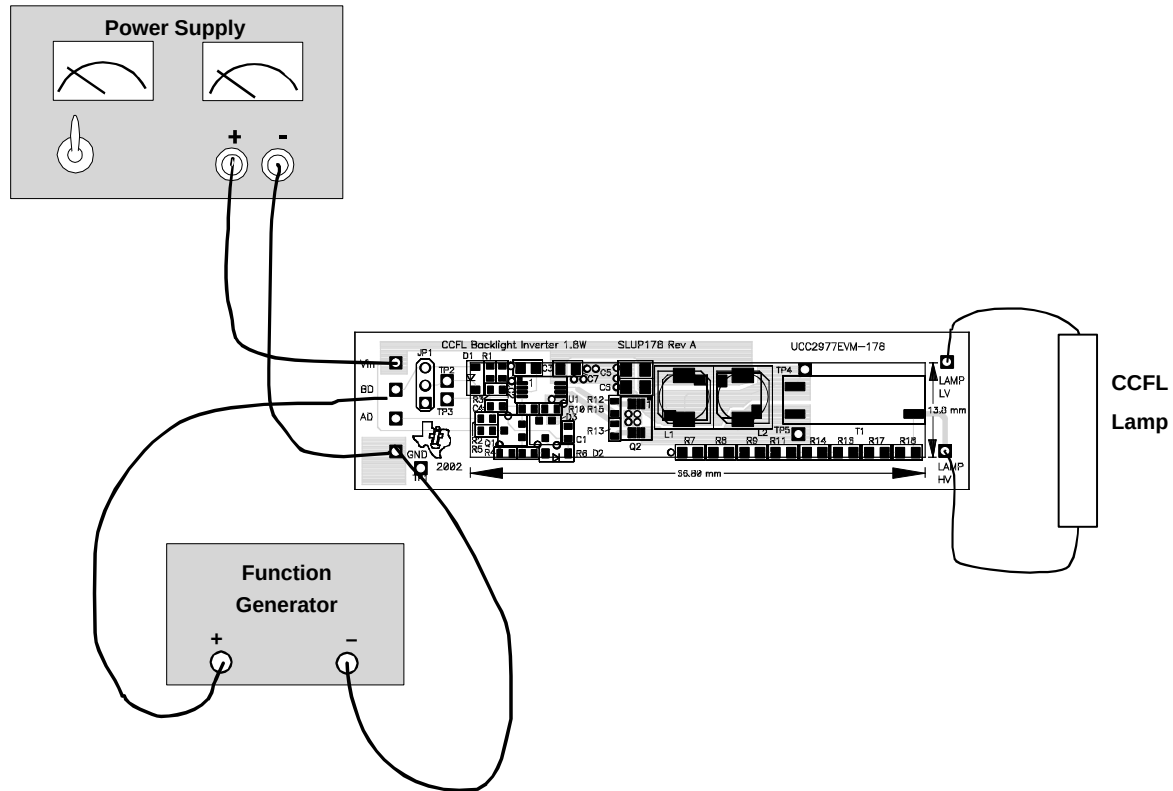
Figure 3–2. Test Setup for Analog Dimming



3.1.3 Burst Dimming Test

Connect pin 2 to pin 3 of JP1 to disable the open-lamp detection circuit during burst dimming. A low frequency (>100 Hz) 0~4 V square wave applied to BD modulates the lamp current.

Figure 3–3. Test Setup for Burst Dimming



3.2 Test Results

The test results for the SLUP178 are shown in this section.

Figure 3–4. Efficiency With a Low Profile Sumida Inductor (CDRH6D28; 22 μ H, 128 m Ω , 6.7 $\times$ 6.7 $\times$ 3 mm)

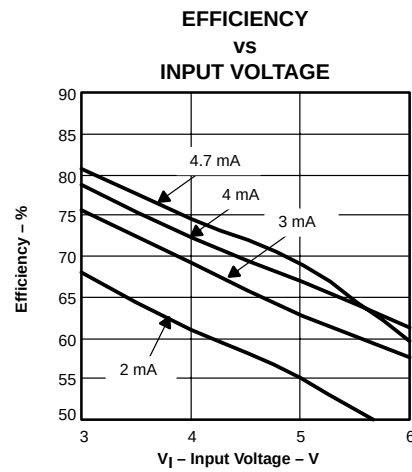


Figure 3–5. Efficiency With a High Profile Toko Inductor (646CY–220M; 22 μ H, 115 m Ω , 7.6 $\times$ 7.6 $\times$ 5.1 mm)

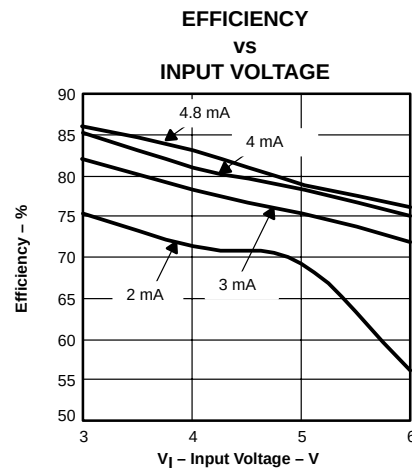


Figure 3–6. Transformer Input/Output Voltages at $V_I = 3\text{ V}$ (CH1=Primary 1, CH4=Primary 2, M1=Transformer Primary Voltage, CH3=Lamp Voltage)

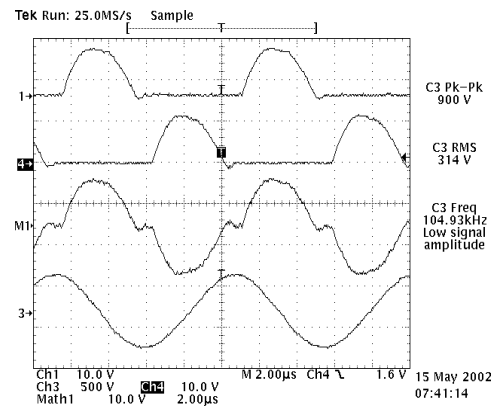


Figure 3–7. Transformer Input/Output Voltages at $V_I = 6\text{ V}$ (CH1=Primary 1, CH4=Primary 2, M1=Transformer Primary Voltage, CH3=Lamp Voltage)

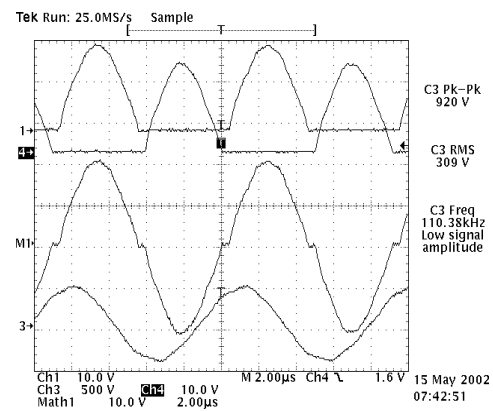


Figure 3–8. Burst Dimming With 50% Duty Cycle (CH1=Burst Dimming Control Signal, CH3=Lamp Voltage)

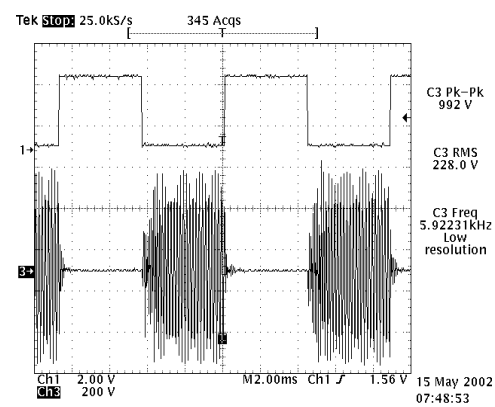


Figure 3–9. Burst Dimming With 80% Duty Cycle (CH1=Burst Dimming Control Signal, CH3=Lamp Voltage)

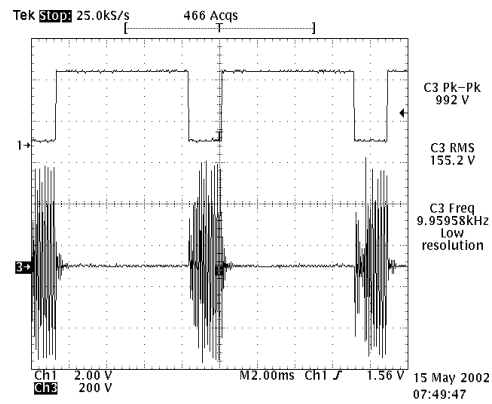


Figure 3–10. Open Lamp Protection (CH1=Comp, C2=Open/SD)

