AFE5805EVM

The AFE5805EVM is an evaluation tool designed for the ultrasound analog front-end (AFE) device AFE5805. In order to deserialize the outputs of the AFE5805, an ADSDeSer-50EVM or TSW1250EVM is needed during the evaluation.

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1 Introduction

The AFE5805 includes an 8-channel, voltage-controlled amplifier (VCA) and an 8-channel, 50-MSPS analog-to-digital converter (ADC). The outputs of the ADC are 8-channel LVDS outputs, which can be deserialized by the ADSDeSer-50EVM or TSW1250EVM. The AFE5805 evaluation module (EVM) provides an easy way to examine the performance and functionalities of AFE5805.

1.1 AFE5805EVM Kit Contents

The AFE5805EVM kit contains the following:

- AFE5805 EVM board
- USB cable
- CD-ROM containing
  - AFE5805 EVM User's Guide (this document)
  - GUI software

1.2 Features

- Characterizes the AFE5805
- Supports CW functionalities test
- Provides 8-channel low-voltage differential signal (LVDS) outputs from the ADC
- Compatible with the standard TI LVDS deserializer ADSDeSer-50EVM or TSW1250EVM
- Communicates with a personal computer (PC) through a USB interface
- RS-232 interface also can be configured in case users wish to control the AFE5805 with a microcontroller. MSP430 programming is required.
- Includes multiple power management solutions for the AFE5805 and other devices.
- Onboard Vcntl generator (0 V - 1.2 V).

1.3 Power Supplies

The AFE5805EVM requires only ±5-V power supplies for operation.

1.4 Indicators

The AFE5805EVM has four LEDs onboard as shown in Figure 1. The states of these LEDs demonstrate the normal operation of the AFE5805EVM.

- LED1, LED2: +3.3-VA and +3.3-VD power supply indicators. They show the normal operation of 3.3-V power regulators.
- LED 3: MCU operation indicator. Flashing state can indicate the normal operation of the MSP430 when the MSP430 is appropriately programmed.
- LED 4: 1.8-V power indicators

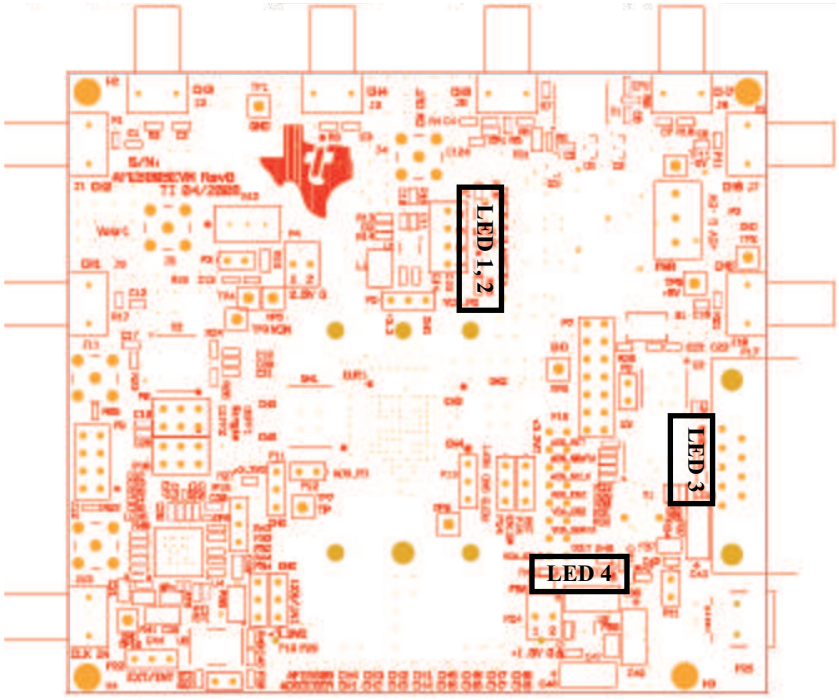


Figure 1. AFE5805EVM LED Locations

2 Board Configuration

This section describes in detail the locations and functionalities of inputs, outputs, jumpers, and test points of the AFE5805EVM.

2.1 I/O and Power Connectors

Pin A1 of the AFE5805 is marked by a white dot on its package as well as a white dot on the board. The positions and functions of the AFE5805EVM connectors are discussed in this section.

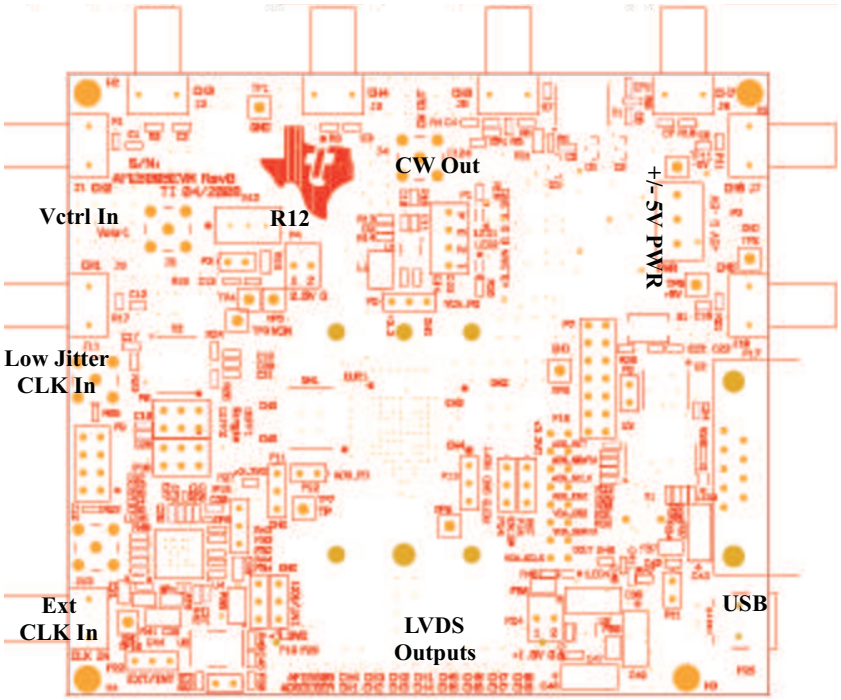


Figure 2. AFE5805EVM I/O Connectors and Locations

- Analog Inputs Ch1-Ch8 (J1-J3, J5-J7, J9, J10): Single-ended analog signal inputs with 50-Ω termination and AC-coupling
- CW Output (J4): CW output after I/V translator
- Vcntl Input (J8 optional): VCA gain control voltage of AFE5805, 0 V to 1.2 V, when this SMA connector is used, shunt P3 must be removed. .
- Low-Jitter CLK Source Input (J11): This input accepts clocks with low-jitter noise, such as HP8644 output. 20- to 50-MHz, 50% duty-cycle clock with 1- to 2-Vrms amplitude can be used. When J11 is used, ensure that shunts P18, P23, and P22 are removed.
- External CLK Input (J13): ADC Clock input, such as FPGA outputs. However, the AFE5805 does not achieve satisfactory performances due to the high-jitter noise of the clock.
- ±5-V PWR connector (P2): Power supply input
- Regulated power supply outputs (P1, P4, and P24): 3.3-VA, 3.3-VD, 2.5-VA, 1.8-VD outputs. Connectors need to be installed.
- RS-232 Input (P17): PC serial port interface for setting AFE5805
- USB input (P25): USB interface to control the AFE5805 (default)
- LVDS Outputs Ch1-Ch8 (P26): Differential LVDS data outputs
- R12 is used to adjust the onboard Vcntl from 0 V to 1.2 V. P3 must be shorted when onboard Vcntl is used.

2.2 Jumpers and Setup

In the following detailed description, the board has been set to default mode (see Figure 3).

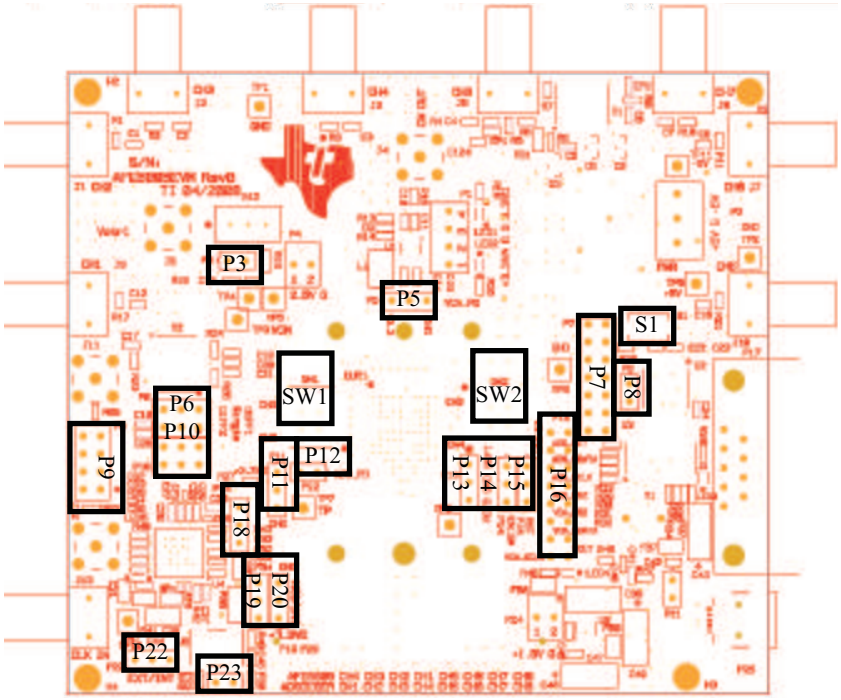


Figure 3. Locations of Jumpers, JTAG, and Switches on the AFE5805EVM

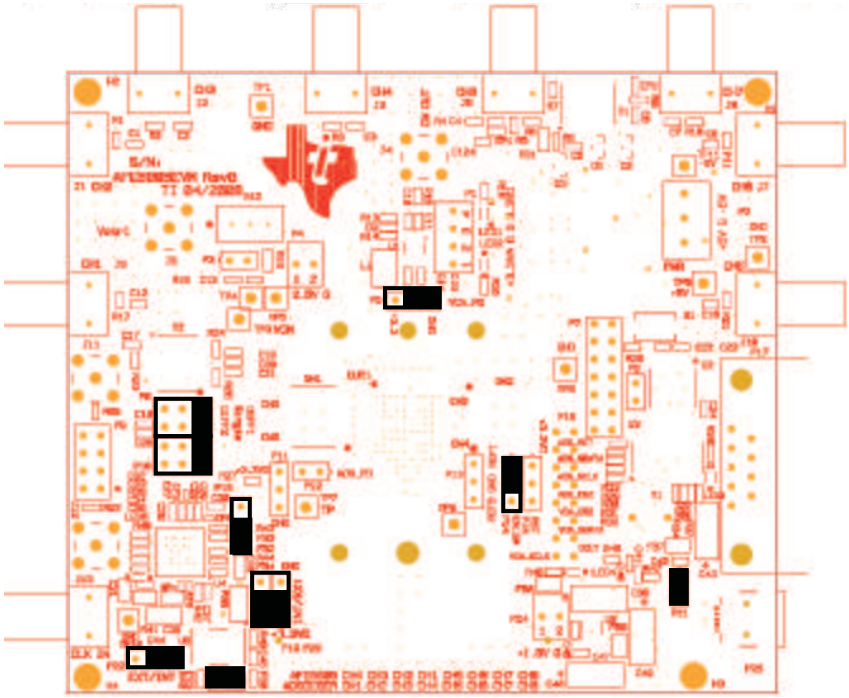


Figure 4. Default Setup for Jumpers

- P5: Power-down pin for the VCA section of the AFE5805. Grounded (default mode) or High (+3.3 VD) for power-down mode.
- P6, P10: AFE5805 ADC clock input selection: Transformer-based differential clock, single-ended LVCMOS clock, or future clock option (needs U4 for support). The default mode uses the transformer-based differential clock.
- P7: MSP430 microcontroller JTAG interface
- P8: MAX3221 (RS-232) power-off jumper. When the jumper is removed, MAX3221 is completely powered off. In the default mode, the jumper is uninstalled because the USB interface is used.
- P9: SPI™ interface for U4.
- P11: TI internal use. Default is floating.
- P12: Power-down pin for ADS. Active High (+3.3 VD). Floating for default mode.
- P13: External ADS reference voltage inputs. Floating in the internal reference mode.
- P14: EN_SM: In the default mode, P14 connects to +3.3 VD, and the state machine is enabled. The AFE5805 is operated using only one SPI port (ADS SPI port).
- P15: RST pin; connects to H4 in the default mode through 0-Ω resistors.
- P16: Debug port for monitoring VCA and ADS SPI signals.
- P19: TI internal use. Connects to 3.3 VD.
- P20: INT/EXT reference mode selection. +3.3 VD for the internal reference mode (default); GND for the external reference mode.
- P22: Uses onboard 40-MHz clock or external clock through J13. The default mode uses the onboard clock
- P23: Power-on onboard 40-MHz clock generator. Default is on.
- P18: Because U4 is uninstalled, this jumper must be set as Figure 4 shows
- S1: MSP430 reset button
- SW1, SW2: CW outputs summation switch. Individual CW output current can be summed through the I/V translator U1 when its corresponding switch is set to ON.

2.3 Test Points

Multiple test points are provided on the EVM. Detail descriptions follow. Under normal operation mode, it is unnecessary to measure voltages at most of these test points.

- TP1: GND
- TP2: GND
- TP3: VCM
- TP4: Vcntl test point
- TP5: GND
- TP6: GND
- TP7: Test point, TI internal only
- TP8: +5 V
- TP9: CM
- TP10:GND
- TP11: -5 V

3 Board Operation

This section describes how to operate the AFE5805EVM for evaluation purposes. Both software and hardware installation and operation are discussed.

3.1 Software Installation and Operation

The AFE5805EVM ships with the AFE5805EVM USB SPI Ver1 software and AFE5805EVM driver. Run the AFE5805EVM driver install.exe and the setup.exe to install the driver and software, respectively. The personal computer (PC) should recognize the EVM after software installation.

To launch the software after successful installation, click:
Start Menu → All Programs → Texas Instruments → AFE5805EVM USB SPI → AFE5805EVM USB SPI

Three different modes are shown in Figure 5, Figure 6, and Figure 7.

The software updates the AFE5805 registers as soon as users change any current setup (i.e., the program sends out new register values due to any value change). It is recommended that users change at least one register value before measurement. Therefore, the register values in a device can be synchronized to the displayed values on the software interface.

In most cases, users only need to change the VCA setup. The ADC setup can remain the same as the IC is powered up.

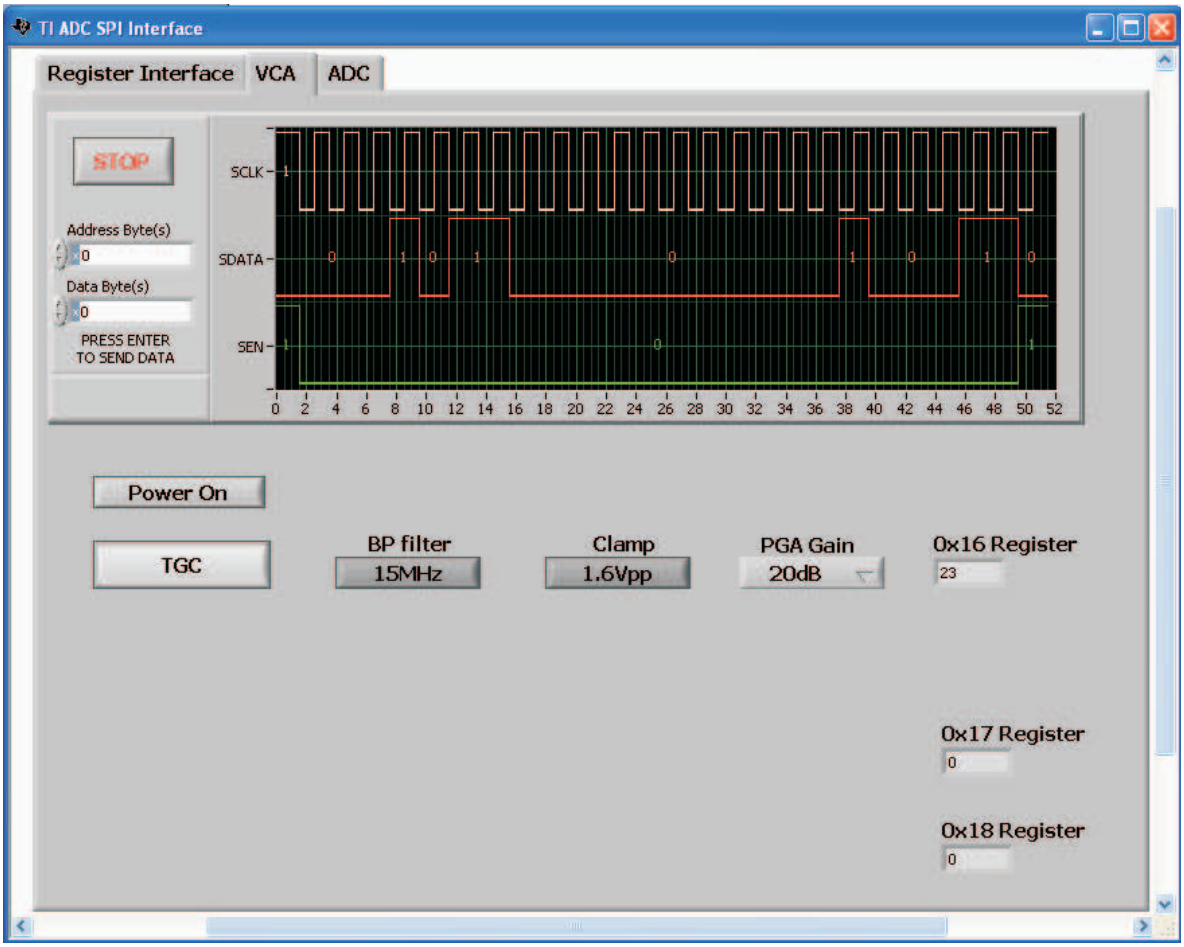


Figure 5. AFE5805EVM USB SPI Interface for TGC Mode

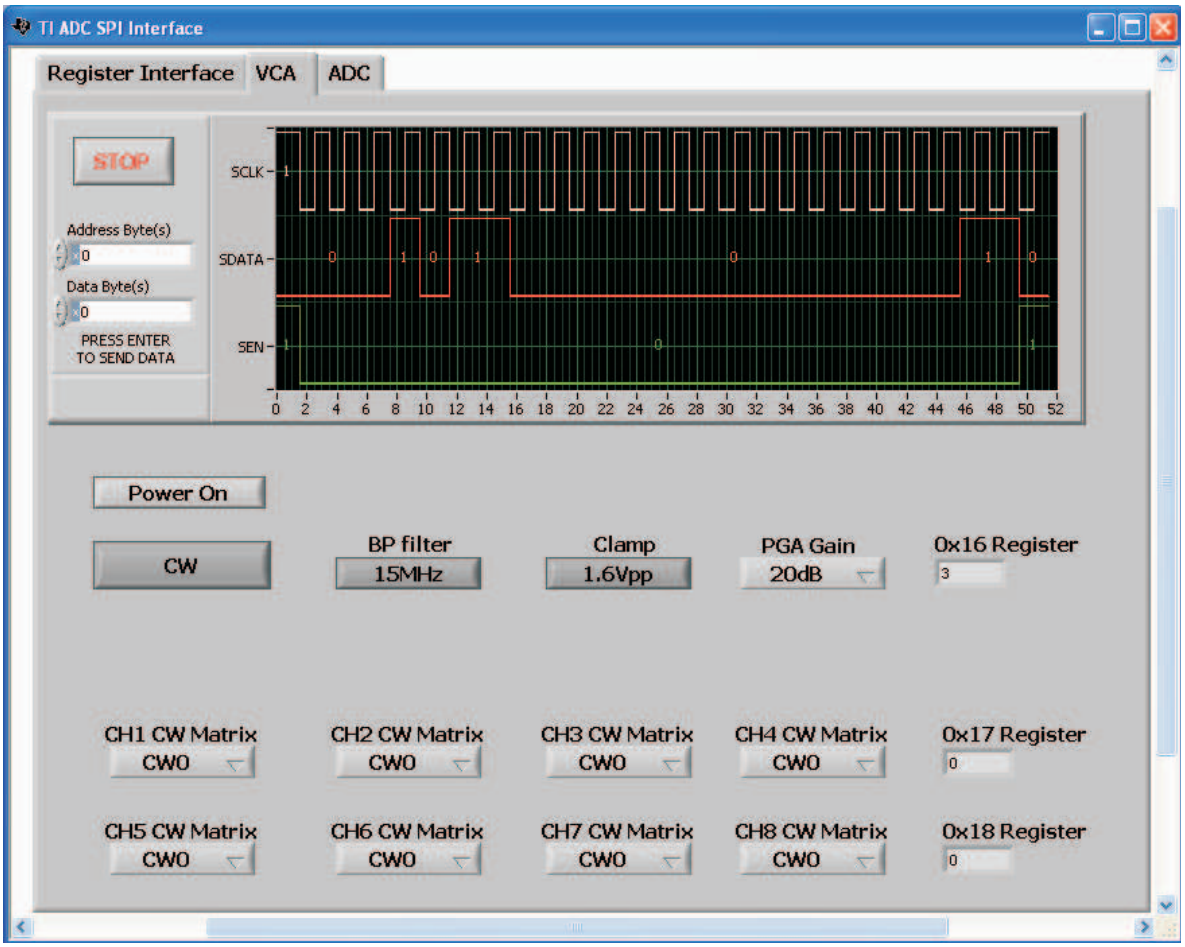


Figure 6. AFE5805EVM USB SPI Interface for CW Mode

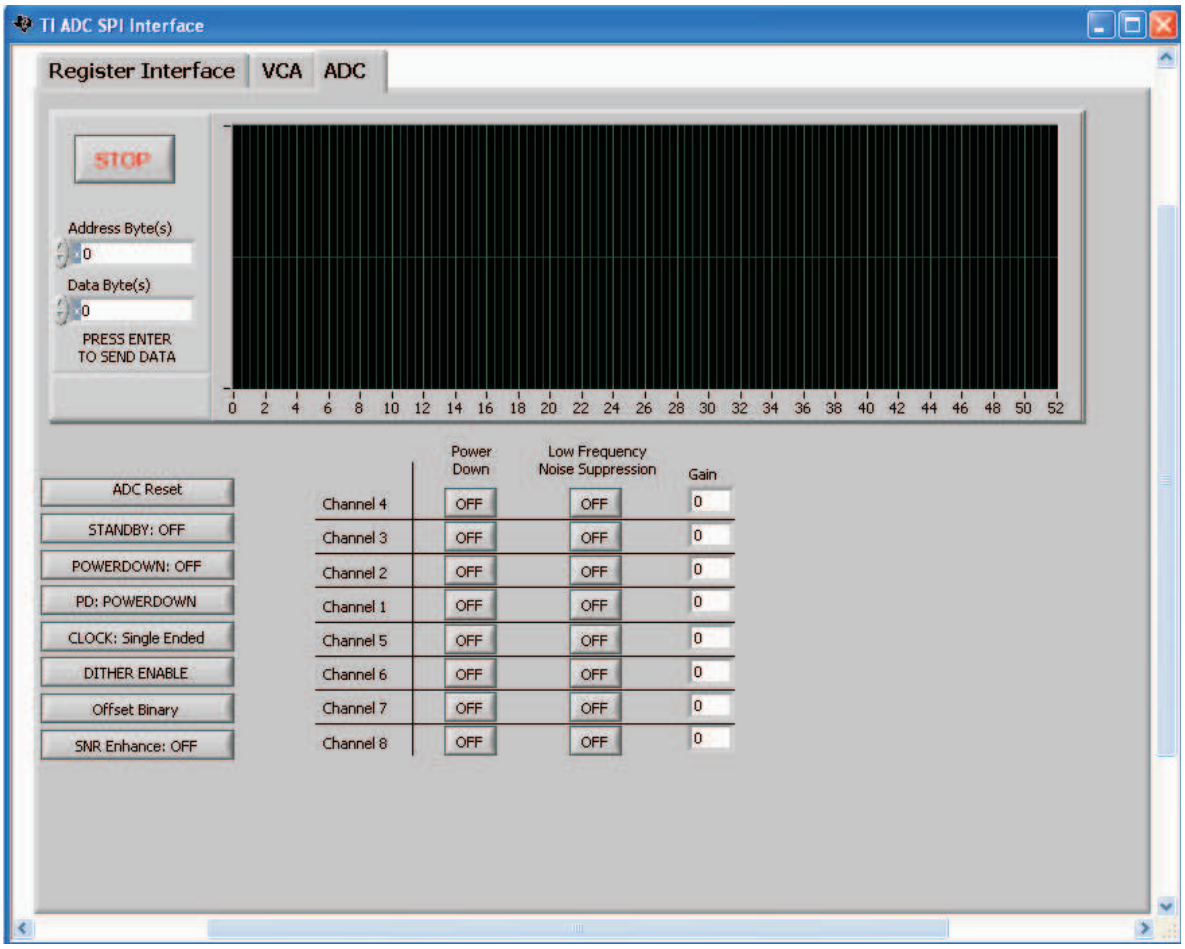


Figure 7. AFE5805EVM USB SPI Interface for ADC Setup

3.2 Hardware Setup

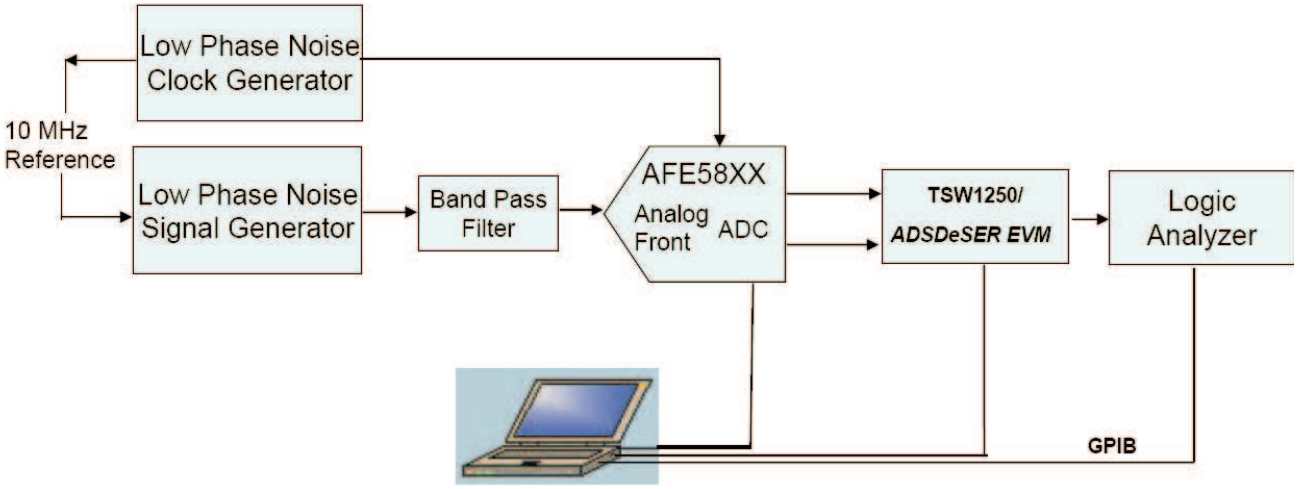
When the AFE5805EVM is powered on in the default mode, the AFE5805 is set as described in Table 1.

Table 1. AFE5805EVM Default Settings When Powered On

VCA	ADS
TGC mode	Differential clock
PGA = 20 dB	Digital Gain = 0
Clamp=Enable	Other parameters are as stated in data sheet
Filter = 15 MHz	

Initial measurements can be made under these default settings. See the AFE5805 data sheet (SBOS5805) for additional settings.

As previously mentioned, the deserializer ADSDeSER-50EVM or TSW1250EVM is required. See details in the ADSDeSER-50EVM user's guide (SBAU091) or TSW1250EVM user's guide (SLOU260A). An example bench setup is shown in Figure 8. Band-pass filters are required for signal source in order to ensure the correct SNR measurements of the AFE5805.



AFE58XX Evaluation Setup Best Practice

(1) Select the lowest phase noise models

(2) An additional Bandpass filter after the signal source is needed. This serves to filter the harmonic distortion of the signal generator and band-limit the noise. Without using filter; the SNR and SFDR will be that of the signal geverator, not that of AFE58XX.

(3) For a coherent AFE58XX evaluation, connect the 10M reference on the back of the clock and to the 10M reference input on the back of the analog input source. For some equipment, one must also use the on-screen menus to select "ext Reference"

(4) The Logic Analyzer is used when a large amount of data (> 64K samples) is needed.

(5) If ADSDeSER EVM is chosen then the Logic Analyzer is a must, ADSDeSER EVM does not provide the function to transfer the data back to PC directly.

Figure 8. Typical AFE5805 Bench Setup

The channel order of the AFE5805 outputs is not the same as that of the ADS527x outputs. Consequently, the channel number on the ADSDeSER-50EVM or AFE5805EVM can be misleading. Table 2 provides channel-to-channel sequence matching between the ADSDeSER-50EVM and the AFE5805EVM.

Table 2. Channel-to-Channel Matching Between the AFE5805EVM and ADSDeSER-50EVM

AFE5805	FCLK	CH4	CH3	CH2	CH1	CH5	CH6	CH7	CH8	LCLK
ADSDESER	FCLK	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	LCLK

For example, when an analog signal is present on CH1 of the AFE5805EVM, the corresponding 12-bit digital output can be seen on CH4 of the ADSDeSER-50EVM.

3.3 Clock Selection

The AFE5805 can be clocked through a transformer-based differential clock, single-ended clock, or future clock input options provided by U4 as Figure 9 shows.

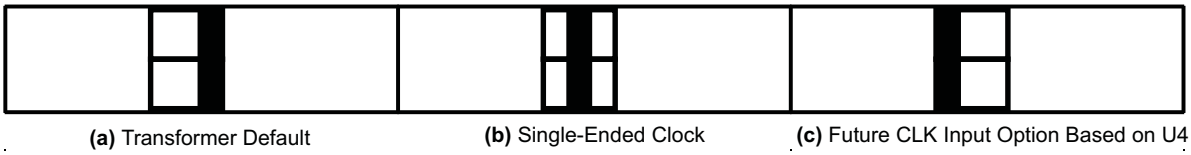


Figure 9. Clock Selection Jumper Configurations

The clock source of the EVM can be the onboard 40-MHz clock, HP8644 low-jitter clock source, or external clock source. The best performance of this EVM is achieved when the low-jitter clock source HP8644 is used. P22, P23, and P18 should be removed in order to disable the onboard clock.

When HP8644 or similar clock sources are unavailable, the onboard 40-MHz clock is the desirable source. The jumpers P22, P23, and P18 should be configured as shown in Figure 4 (i.e., the default setup for AFE5805EVM). In this mode, the transformer-based differential clock is used.

3.4 Data Analysis

Based on the data file acquired by a logic analyzer, the performance of AFE5805 can be evaluated.

Appendix A provides a solution (TI TSW1250EVM) to analyze the data file using the PC. Appendix B provides an alternate solution (TI TSW1100 software) to analyze the data file captured by a logic analyzer. Coherent sampling is recommended, but is not mandatory. Due to the frequency accuracy requirement of coherence sampling, two HP8644s are required for generating an ADC clock and analog signal. For most users, this may be infeasible. Data analysis based on windowing is a more suitable approach.

4 Schematics and Layout

This section provides the schematics, the AFE5805EVM board layout, and the bill of materials.

4.1 Schematics

The schematics appear at the end of the document.

4.2 PCB Layout

The AFE5805EVM uses a six-layer printed-circuit board. The following figures show each layer.

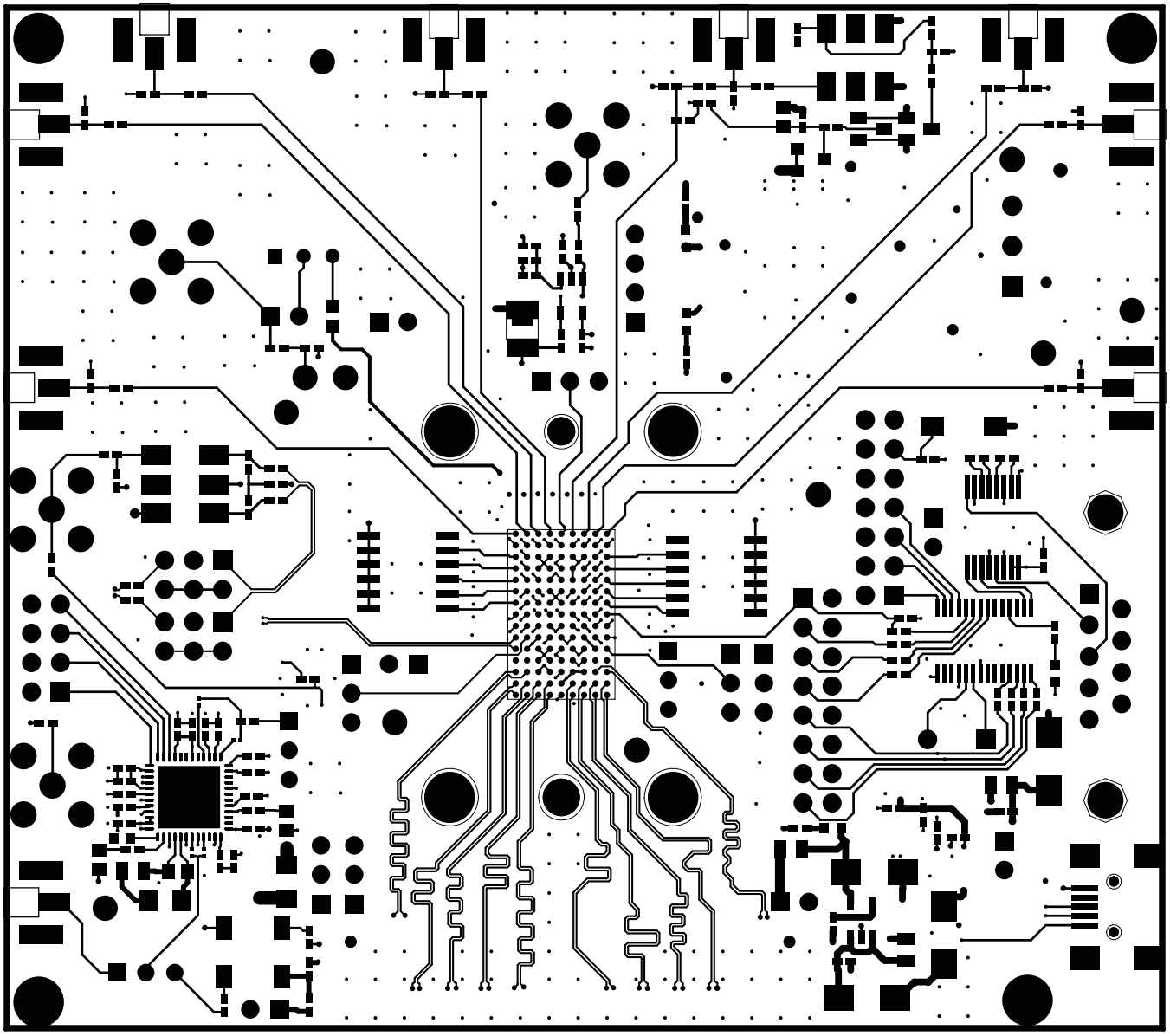


Figure 10. Top Layer, Signal

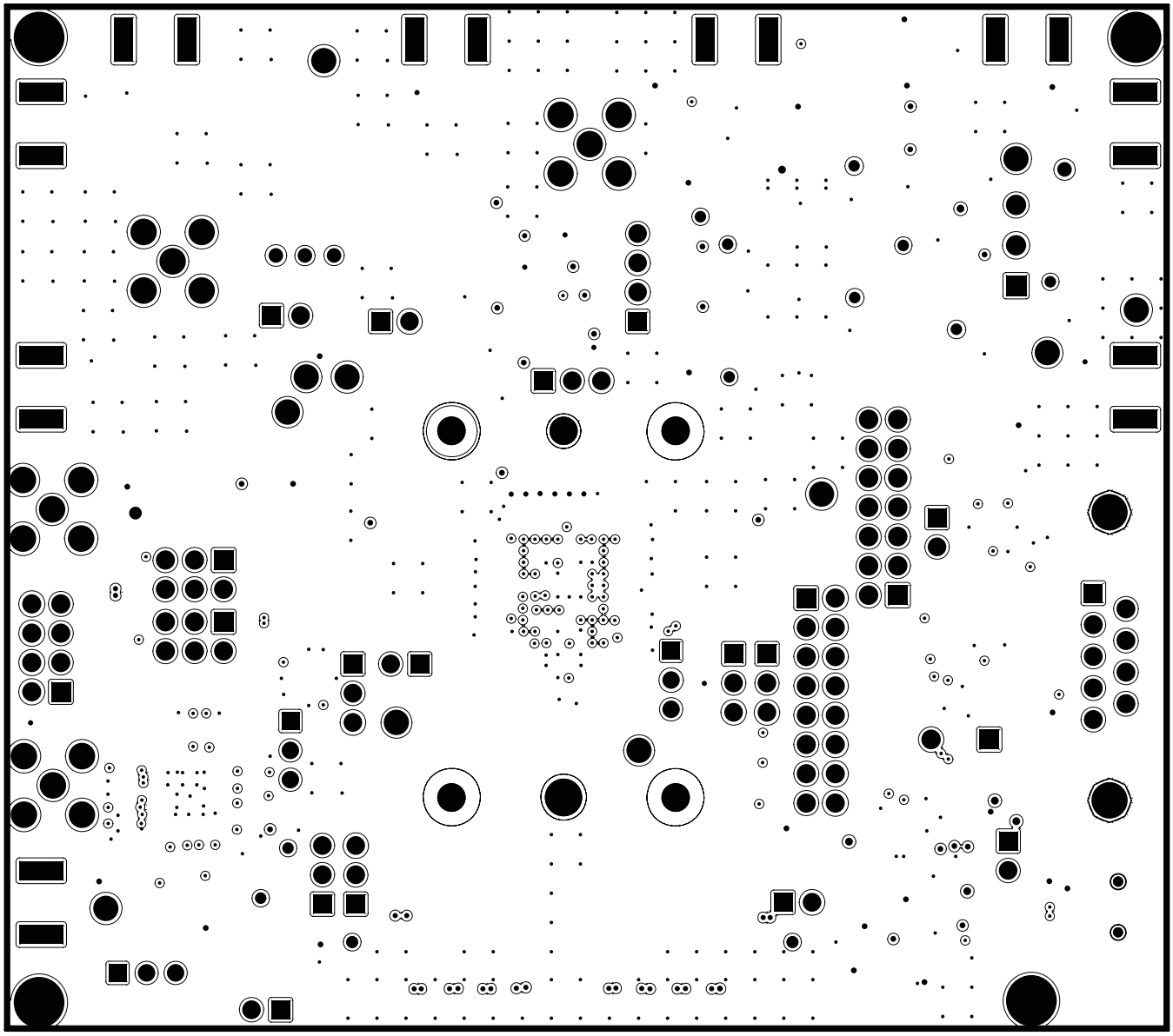


Figure 11. Inner Layer 1, Ground

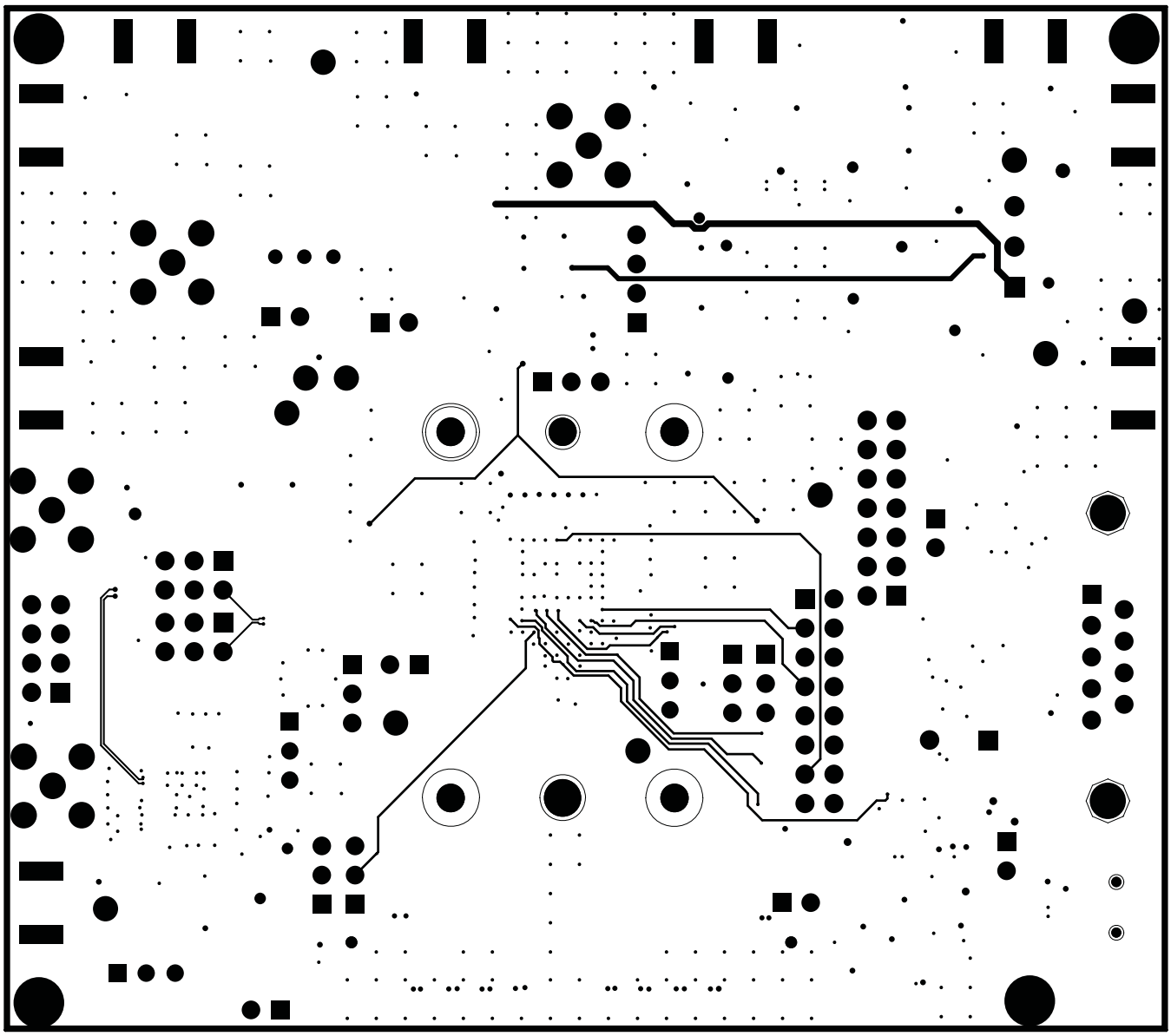


Figure 12. Inner Layer 2, Signal

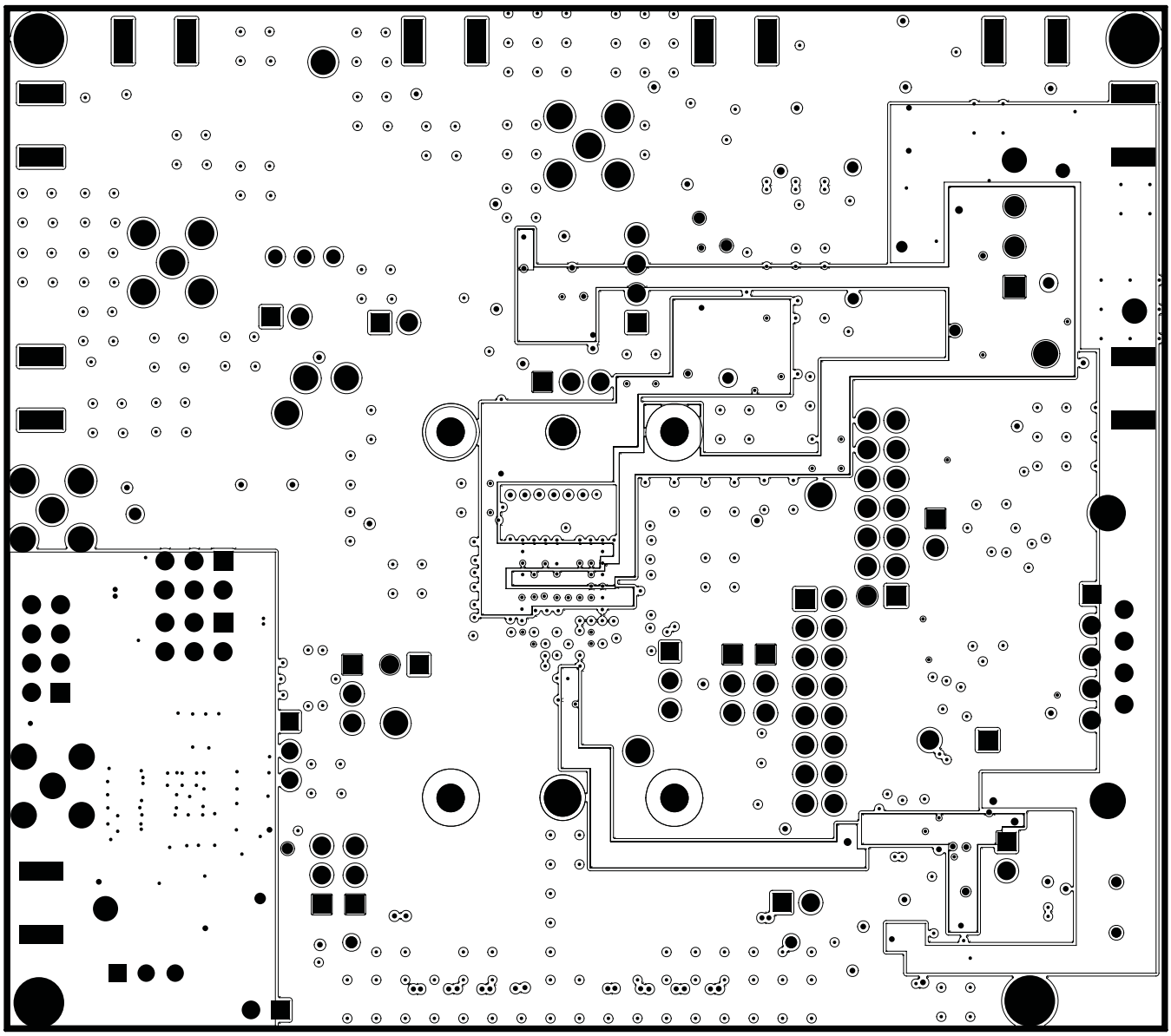


Figure 13. Inner Layer 3, Power

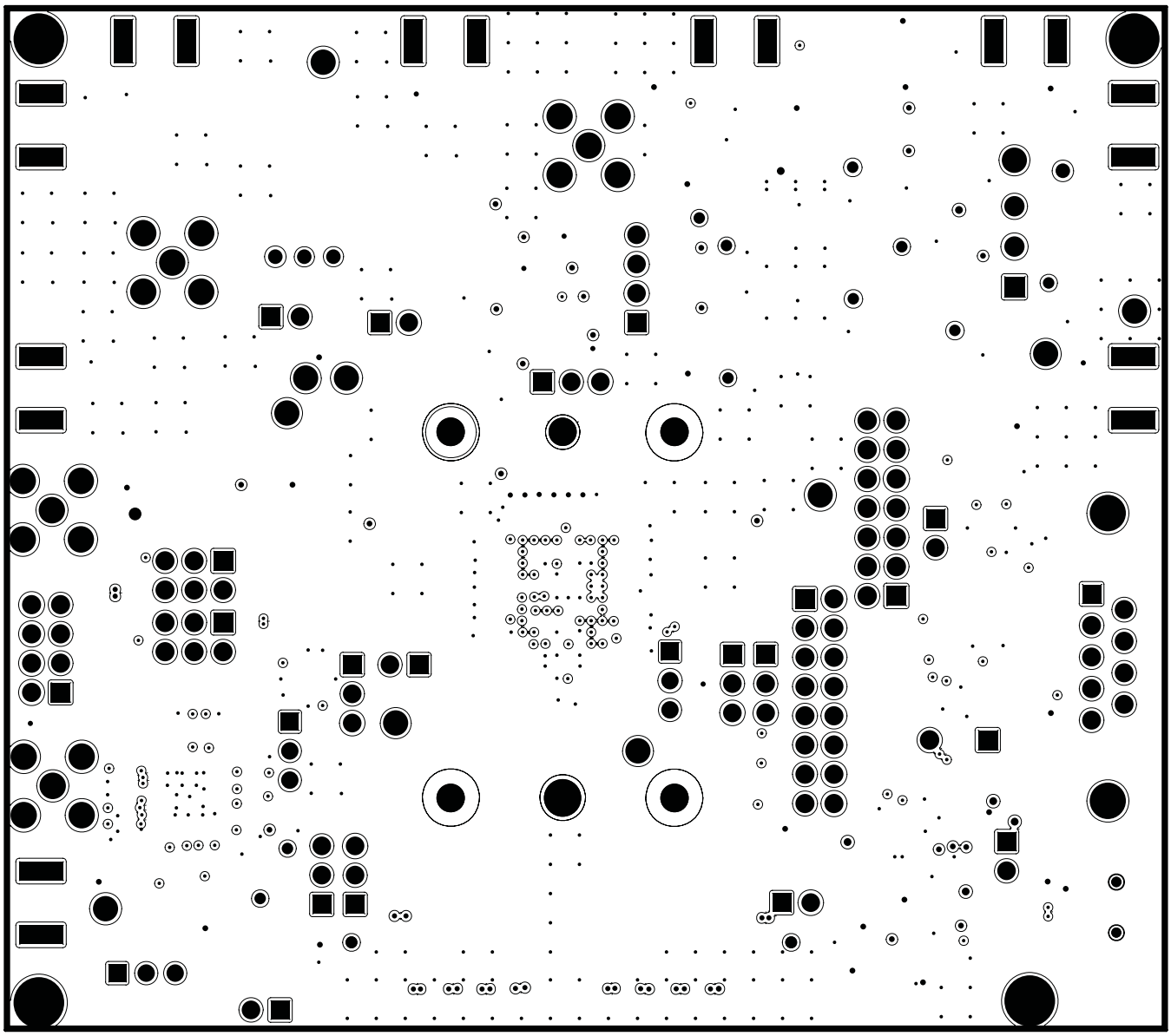


Figure 14. Inner Layer 4, Ground

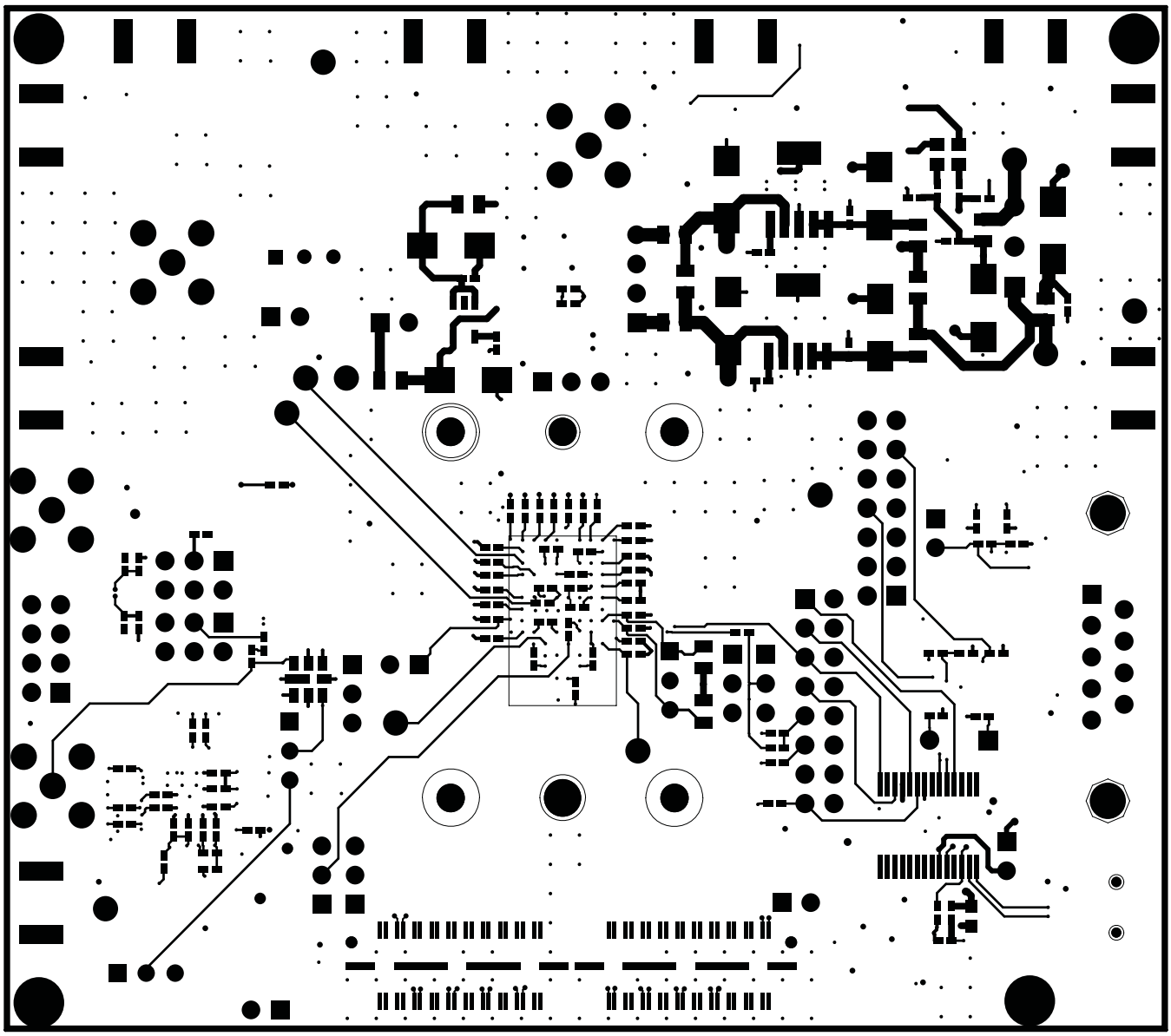


Figure 15. Bottom Layer, Signal

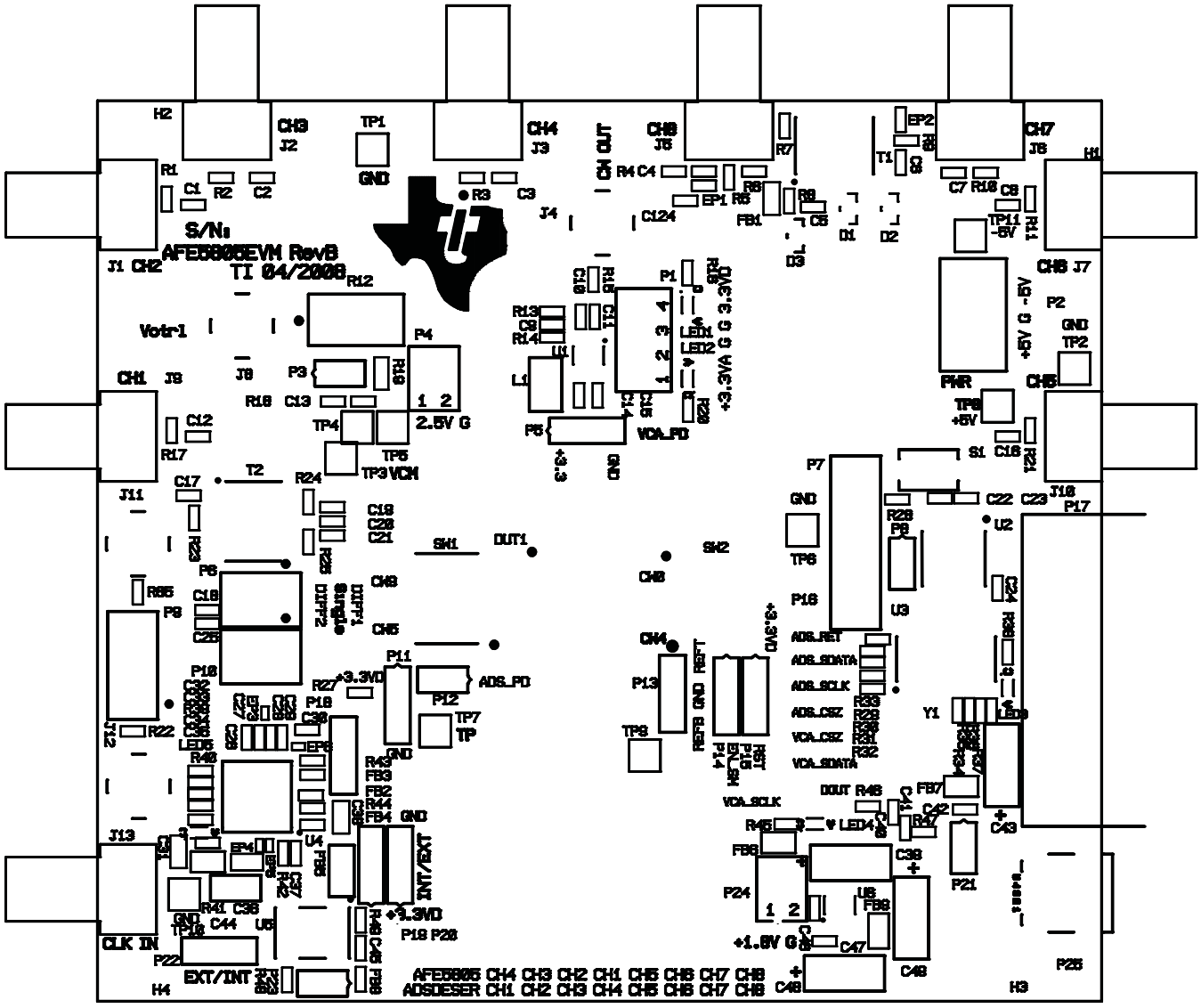


Figure 16. Top Silk Screen Layer

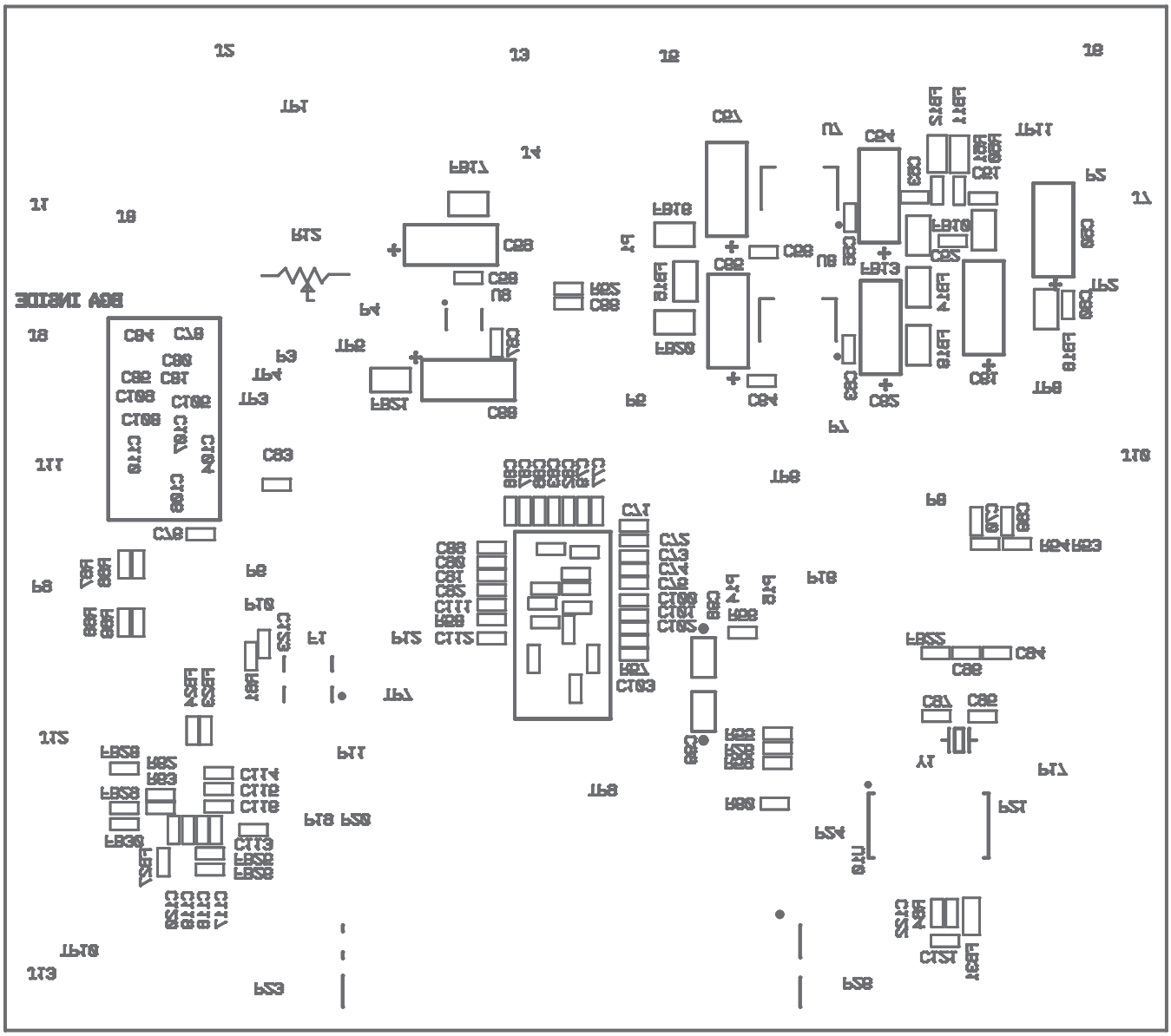


Figure 17. Bottom Silk Screen Layer

4.3 Bill of Materials

Table 3. Bill of Materials

Item	MFG	MFG Part Number	RefDes	Value or Function
1	TI	MSP430F1232IPW	U3	MIXED SIGNAL MICROCONTROLLER
2	KEMET	C0402C103K3RAC	C9	CAPACITOR,SMT,0402,CER,0.01µF,25V,10%,X7R
3	KEMET	C0402C104K8PAC	C1, C2, C3, C4, C5, C6, C7, C8, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C32, C33, C34, C35, C40, C41, C42, C45, C46, C47, C51, C52, C53, C55, C56, C58, C60, C63, C64, C67, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C93, C94, C96, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124	CAPACITOR,SMT,0402,CER,0.1µF,10V,10%,X5R
4	PANASONIC	ECJ-0EC1H100D	C66, C95, C97	CAPACITOR,SMT,0402,CER,10pF,50V,±0.5pF,NPO
5	MURATE	GRM155R60J225ME15D	C37, C92	CAPACITOR,SMT,0402,CERAMIC,2.2µF,6.3V,20%,X5R
6	PANASONIC	ECJ-1VB0J475K	C36	CAPACITOR,SMT,0603,CER,4.7µF,6.3V,10%,X5R
7	TAIYO YUDEN	JMK107BJ106MA-T	C31, C38	CAPACITOR,SMT,0603,CER,10µF,6.3V,20%,X5R
8	MURATA	GRM31CR60J476ME19B	C44	CAPACITOR,SMT,CER,1206,47µF,6.3V,20%,X5R
9	AVX	TACR475M020R	C98, C99	CAP,SMT,TAN,0805,4.7µF,20V,20%,R-CASE
10	AVX	TPSC226K016R0375	C39, C43, C48, C49, C50, C54, C57, C59, C61, C62, C65, C68	10%, 16V, 22µF
11	SAMTEC	SMA-J-P-X-ST-EM1	J1, J2, J3, J5, J6, J7, J9, J10, J13	SMA JACK EDGE MOUNT,062PCB,BRASS/GOLD,STRAIGHT,50 Ω
12	SAMTEC	SMA-J-P-H-ST-TH1	J4, J8, J11, J12	SMA COAX STRAIGHT PCB JACK,SMT,175TL,50 Ω,GOLD
13	TYCO ELECTRONICS	745781-4	P17	DSUB, 9 PIN, R/A FEM
14	ADVANCED CONNECTER	MNE20-5K5P10	P25	MINI-AB USB OTG RECEPTACLE R/A SMT TYPE
15	USCC	HC-18/U-4.1943M	Y1	4.194300 MHz
16	EPSON	HF-372A(UNINSTALLED)	F1	CRYSTAL FILTER UNINSTALLED
17	TI	CDCE62005	U4	(UNINSTALLED)
18	Not Installed	PAD0201(UN)	EP4, EP6	(Uninstalled Part) EMPTY
19	Not Installed	PAD0402(UN)	EP1, EP2	(Uninstalled Part) EMPTY
20	MURATA	BLM15BD102SN1D	FB2, FB3, FB4, FB8, FB22, FB23, FB24, FB25, FB26, FB27, FB28, FB29, FB30	FERRITE BEAD,SMT,0402,1 kΩ,200mA
21	MURATA	BLM18EG601SN1D	FB31	FERRITE BEAD,SMT,0603,600 Ω at 100MHz,25%,500mA
22	STEWARD	HI0805R800R-00	FB6, FB7, FB9, FB10, FB13, FB14, FB15, FB16, FB17, FB18, FB19, FB20, FB21	FERRITE,SMT,0805,80 Ω at 100MHz
23	STEWARD	LI1206H151R-00	FB5	FERRITE,SMT,1206,150 Ω at 100MHz,0.8A
24	MOLEX	39357-0003	P2	HEADER, THRU, POWER, 3P,3.5MM, EUROSTYLE
25	SAMTEC	QTH-040-01-L-D-DP-A	P26	HEADER,SMT,80P,0.5mm,FEM,DIFF PAIR,RECEPTACLE,168H
26	SAMTEC	SSQ-104-02-F-D	P9	HEADER,THU,8P,2x4,100LS,FEM,VERT,194TL
27	SAMTEC	TSW-103-08-G-D	P6, P10	HEADER,THU,6P,2x3,MALE,DUAL ROW,100LS,200TL
28	SAMTEC	TSW-107-07-G-D	P7	HEADER,THU,14P,2x7,MALE,DUAL ROW,100LS,100TL
29	SAMTEC	TSW-108-07-G-D	P16	HEADER,THU,16P,2x8,MALE,DUAL ROW,100LS,100TL(UNINSTALLED)
30	TYCO ELECTRONICS	103321-2	P3, P8, P12, P21, P23	HEADER W/SHUNT,2P,100LS

Table 3. Bill of Materials (continued)

Item	MFG	MFG Part Number	RefDes	Value or Function
31	MOLEX	22-23-2021-P	P4, P24	MALE,2PIN,.100CC W/ FRICTION LOCK
32	MILL-MAX	350-10-103-00-006	P13, P18, P22	HEADER,THU,MAL,0.1LS,3P,1x3,284H,110TL
33	MOLEX	22-23-2041	P1	4P, VERT, FRICTION LOCK
34	TYCO ELECTRONICS	4-103239-0x3	P5, P11, P14, P15, P19, P20	HEADER,THU,MAL,0.1LS,3P,1x3
35	TI	AFE5805	DUT1	AFE5805 8-CH ULTRASOUND ANALOG FRONT END
36	MAXIM	MAX3221CAE	U2	RS-232 TRANSCEIVERS
37	MOTOROLA	MMBD7000LT1	D1, D2	DUAL SWITCHING DIODE
38	NXP	BAS40-04	D3	PIN DIODE SOT 23 SINGLE JUNCTION
39	TI	TPS79633DCQR	U7(UNINSTALLED), U8	ULTRALOW-NOISE HI PSRR FAST RF 1-A LDO LINEAR REGULATOR,3.3V
40	TI/BURR-BROWN	OPA820IDBV	U1	UNITY-GAIN STABLE LOW NOISE VOLTAGE FEEDBACK OPAMP
41	TI	TPS79318DBV	U6	1.8V,ULTRALOW-NOISE HI PSRR FAST RF 200mA LDO LINEAR REGULATOR
42	TI	TPS79325DBV	U9	2.5V,ULTRALOW-NOISE HI PSRR FAST RF 200mA LDO LINEAR REGULATOR
43	FUTURE TECHNOLOGY DEVICE INT.	FT245RL	U10	USB FIFO IC INCORPORATE FTDICHIP-ID SECURITY DONGLE
44	PANASONIC	ELJFA221J	L1	220µH, 5%
45	TAIYO-YUDEN	LK 1608 330M	FB1, FB11, FB12	INDUCTOR,SMT0603,33.0µH,20%
46	PANASONIC	LNJ308G8PRA	LED1, LED2, LED3, LED5	LED,SMT,0603,PURE GREEN,2.03V
47	PANASONIC	LNJ808R8ERA	LED4	LED,SMT,0603,ORANGE,1.8V
48	ECS	ECS-3953M-400-BN	U5	OSC,SMT,3.3V,50ppm,–40~85C,5nS,40.000 MHz
49	PANASONIC	ERJ-2GE0R00X	R26, R27, R40, R42, R44, R48, R53, R55, R56, R63, R65	RESISTOR/JUMPER,SMT,0402,0 Ω,5%,1/16W
50	PANASONIC	ERJ-2GEJ0000(UN)	R6, R7, R29, R30, R31, R32, R34, R35, R36, R37, R39, R43, R46, R49, R54, R59, R60, R62, R64	UNINSTALLED PART
51	PANASONIC	ERJ-2GEJ131	R66, R69	RESISTOR, SMT, 0402, ±1%,130 Ω
52	PANASONIC	ERJ-2GEJ49R9(UN)	R4, R9, R22	UNINSTALLED PART
53	PANASONIC	ERJ-2GEJ563	R57	RESISTOR, SMT, 0402, 5%,56K Ω
54	PANASONIC	ERJ-2GEJ820	R67, R68	RESISTOR, SMT, 0402, ±5%,82
55	PANASONIC	ERJ-2RKF1000X	R24, R25	RESISTOR,SMT,0402,100 Ω,1%,1/16W
56	PANASONIC	ERJ-2RKF1001X	R13, R14, R18, R47	RESISTOR,SMT,0402,1.00K,1%,1/16W
57	PANASONIC	ERJ-2RKF1002X	R33, R58	RESISTOR,SMT,0402,10.0K,1%,1/16W
58	PANASONIC	ERJ-2RKF2000X	R52	RES,SMT,0402,200 Ω,1%,1/16W
59	PANASONIC	ERJ-2RKF3320X	R16, R20, R38, R45	RES,SMT,0402,332 Ω,1%,1/16W
60	PANASONIC	ERJ-2RKF4020X	R8	RES,SMT,0402,402 Ω,1%,1/16W
61	PANASONIC	ERJ-2RKF4992X	R28	RESISTOR,SMT,0402,49.9K,1%,1/16W
62	PANASONIC	ERJ-2RKF49R9X	R1, R2, R3, R5, R10, R11, R15, R17, R21, R23, R61	RESISTOR,SMT,0402,49.9 Ω,1%,1/16W
63	PANASONIC	ERJ-2RKF7500X	R50, R51	RES,SMT,0402,750 Ω,1%,1/16W
64	VISHAY	CRCW06031742F	R19	RES,SMT,0603,17.4K Ω, 1%
65	PANASONIC	ERJ-6RQF5R1V	R41	SMT,RES,0805,1/8W, 1%, 5.1 Ω
66	PANASONIC	ERJ-1GE0R00C	EP3, EP5	RESISTOR,SMT,0201,THICK FILM,0 Ω,5%,0 Ω JUMPER,1/20W
67	C&K	TD06H0SK1	SW1, SW2	DIP SWITCH,SMT,6POS,SPST,MINIATURE
68	PANASONIC	EVQPE104K	S1	SQUARE LIGHT TOUCH
69	KEYSTONE ELECTRONICS	5005	TP8	TESTPOINT,THU,COMPACT,0.125LS,130TL, RED
70	KEYSTONE ELECTRONICS	5006	TP1, TP2, TP5, TP6, TP10	TESTPOINT,THU,COMPACT,0.125LS,130TL, BLACK
71	KEYSTONE ELECTRONICS	5006(UN)	TP3, TP4, TP7, TP9	UNINSTALLED PART (TEST POINT)

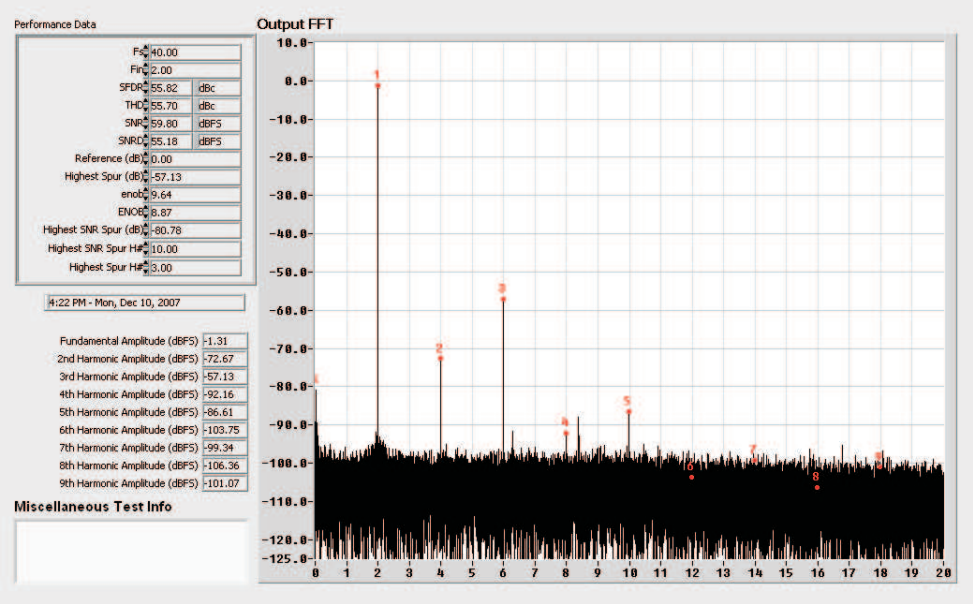
Table 3. Bill of Materials (continued)

Item	MFG	MFG Part Number	RefDes	Value or Function
72	KEYSTONE ELECTRONICS	5007	TP11	TESTPOINT,THU,COMPACT,0.125LS,130TL, WHITE
73	MINI-CIRCUITS	ADTI-6T	T1(UNINSTALLED), T2	RF TRANSFORMER WIDEBAND, 0.03-125 MHz
74	BOURNS	3296W-1-103	R12	TRIMPOT,THU,10K,10%,0.5W,100ppm,25T
75	AMP	531220-2	P3, P8, P12, P21, P23	
76	KEYSTONE ELECTRONICS	1892	H1, H2, H3(UNINSTALLED), H4(UNINSTALLED)	STANDOFF HEX 4-40 THR 0.250”L ALUM
SPECIAL NOTES AND INSTRUCTIONS: 1: ITEM 26 , 27, 28, and 29 ARE STRAIGHT DUAL ROW 72 POSITION HEADER QUANTITY OF STRIPS WILL CHANGE WITH NUMBER OF BOARDS BEING BUILT. 2: ITEM 30, 32, and 34 ARE STRAIGHT SINGLE ROW 36 POSITION HEADER QUANTITY OF STRIPS WILL CHANGE WITH NUMBER OF BOARDS BEING BUILT.				

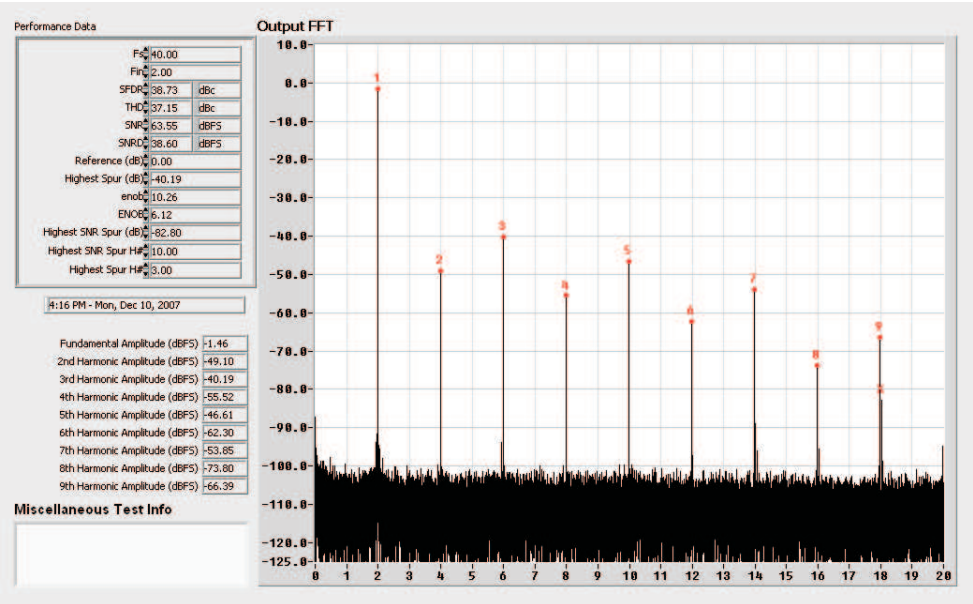
5 Typical Performance

This section provides some typical performance characteristics of the AFE5805EVM to assist users in verifying their setup.

After analysis of the data file acquired by a logic analyzer, the SNR of the AFE5805 should be better than 59 dB when the PGA is set to 30 dB and Vctnl is set as 1 V. A typical performance plot of the AFE5805 is shown in Figure 18.



(a) PGA = 30 dB, Vcntl = 1 V, Vin = 10 mVpp

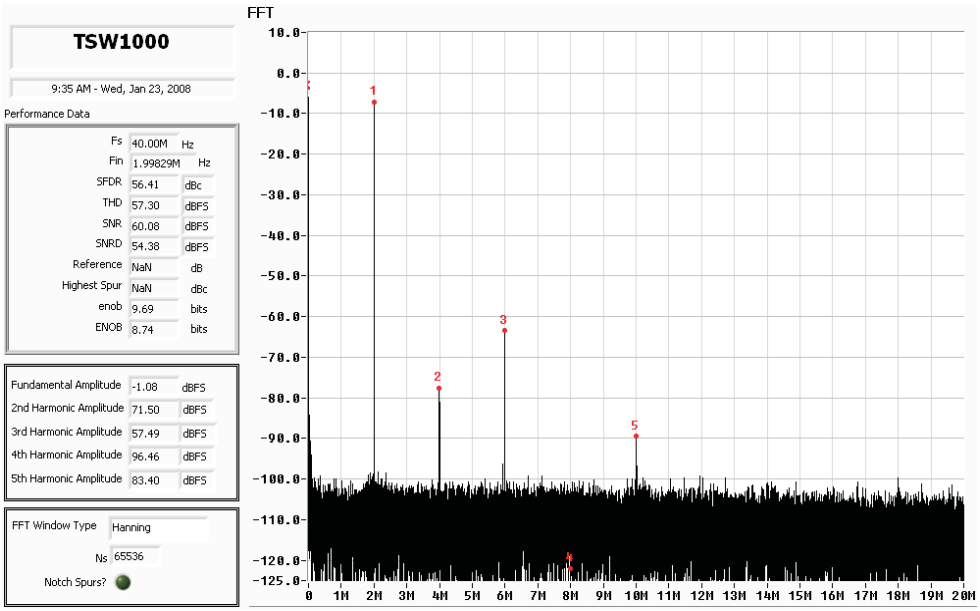


(b) PGA = 30 dB, Vcntl = 0.3 V, Vin = 250 mVpp

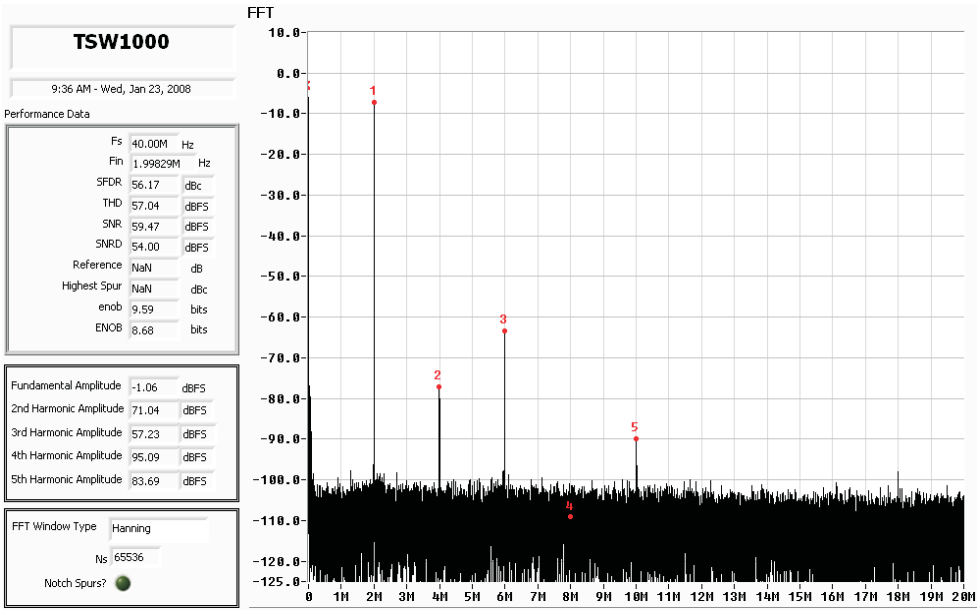
Figure 18. Typical Performances of AFE5805

As Figure 18 shows, the SNR degrades as the gain increases; the HD degrades as the input signal increases.

When the onboard 40-MHz clock is used, the measured SNR of the AFE5805 degrades, but the degradation is insignificant. In the example of Figure 19, the settings are PGA=30 dB, Vcntl=1 V, and LPF=15 MHz.



(a) HP8644 is used. SNR = 60.08 dBFS



(b) Onboard 40-MHz clock is used. SNR = 59.47 dBFS. 0.6-dBFS degradation is observed when the onboard 40-MHz clock is used. Hanning window is applied.

Figure 19. Typical Performance of AFE5805 With (a) HP8644 and (b) Onboard 40-MHz Clock

Appendix A TSW1250 for Evaluating AFE5805

This application note demonstrates typical steps of evaluating the AFE5805 using the TSW1250EVM and its associated data.

A.1 Step 1: Hardware Setup

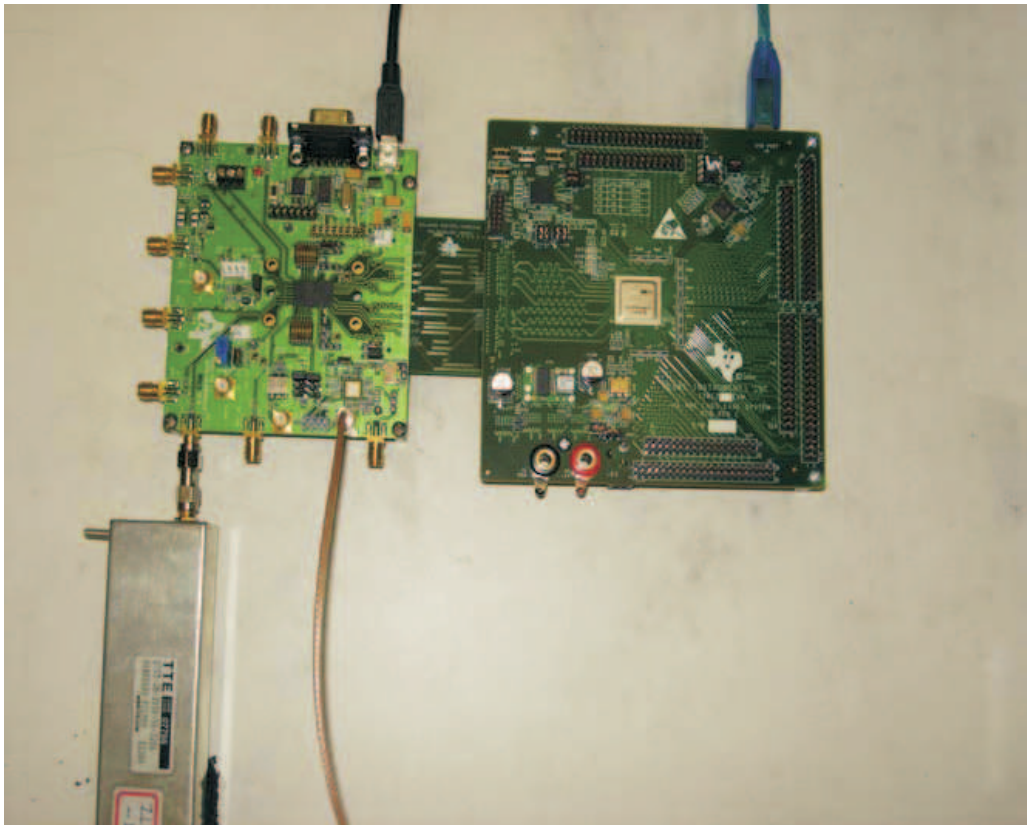


Figure 20. Connection between TSW1250EVM and AFE5805

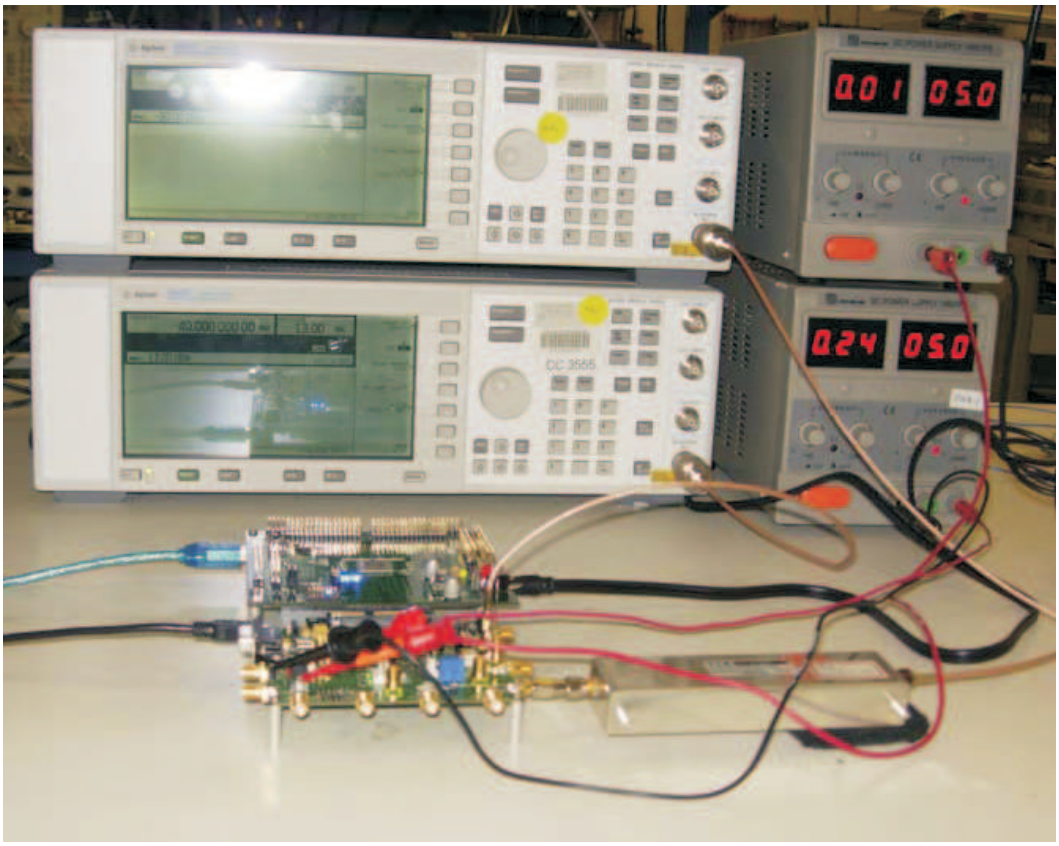


Figure 21. Connection of the Instruments

A.2 Step 2: Launch AFE5805 GUI

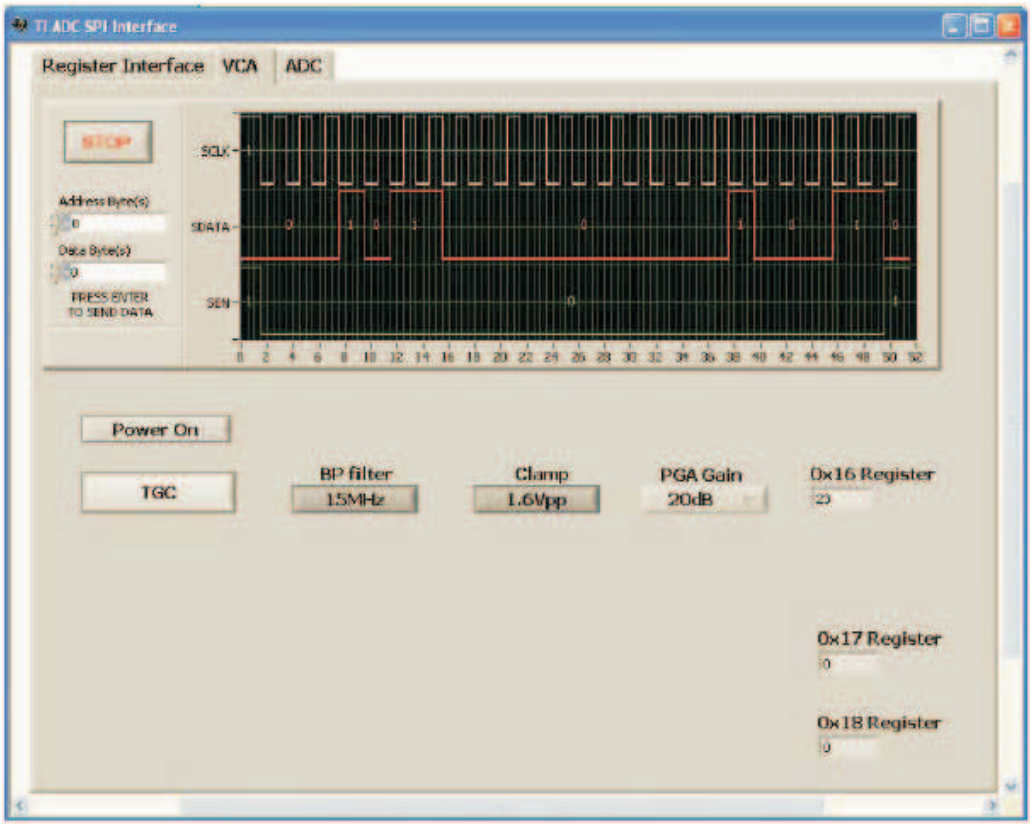


Figure 22. AFE5805 EVM GUI

Initial COMMANDS to the AFE5805 GUI:

This step is used to adjust ADC input and output configuration. Therefore, TSW1250 can correctly capture data.

1. Set Address Byte(s) = 0 Data Byte(s) = 1. Click any space area to send command to AFE5805.
2. Set Address Byte(s) = 42 Data Byte(s) = 8081. Click any space area.
3. Set Address Byte(s) = 46 Data Byte(s) = 8208. Click any space area.

Configure AFE5805 for Test

1. Press TGC button twice to observe it toggle to CW and then back to TGC. This ensures the device is in the TGC mode.
2. Press BP filter button to set it to 15MHz. If it is already at 15MHz during the startup, then press several times to cycle through different modes then back to 15 MHz.
3. Press Clamp button to set it to NO Clamp. If it is already at No Clamp during the startup, then press several times to cycle through different modes then back to No Clamp.
4. Press PGA to set it to 30dB. If it is already at 30dB during the startup, then press several times to cycle through different modes then back to 30dB.

At this stage, the AFE5805 is ready to work with TSW1250.

Instruments

Set the frequency of the signal generator to the frequency displayed in the GUI (2.00439453MHz).

Set Amplitude of the signal generator to about -3dBm – -33dBm

Set the Frequency of the Clock Generator to 40MHz.

Set Amplitude of the Clock Generator to 13 dBm.

A.3 Launch TSW1250 GUI

Test Condition

Following the steps in the orders as indicated in the following figure to set the test condition.

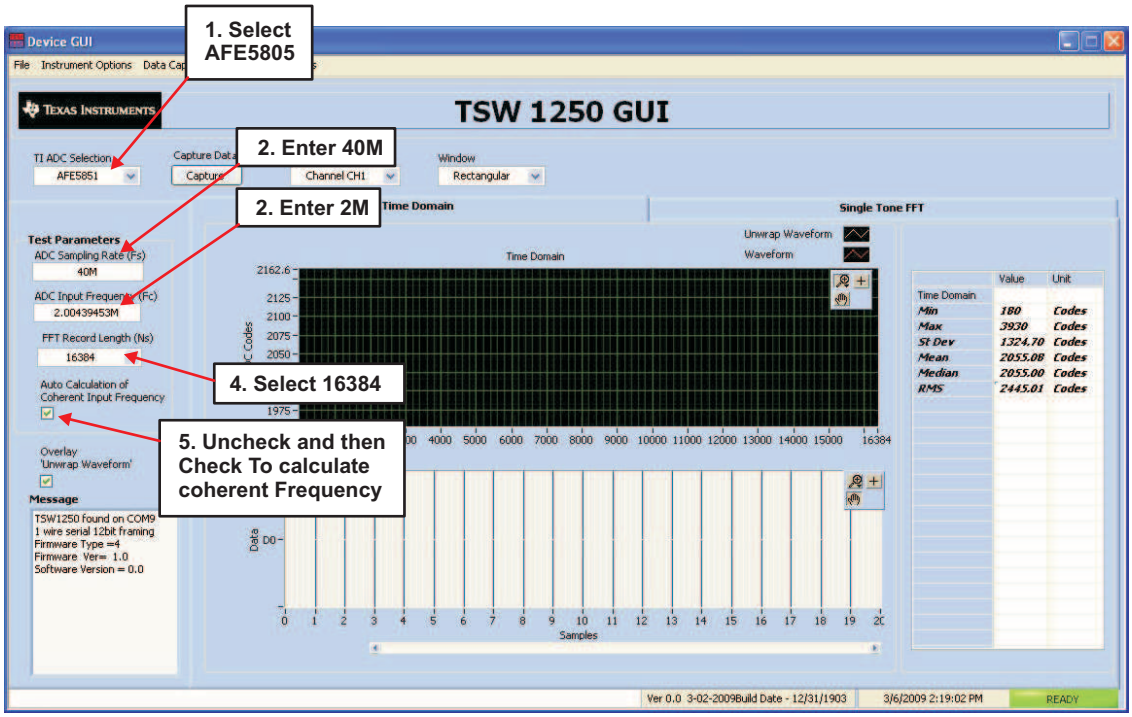


Figure 23. User Interface: Step-by-Step setup

After the above five steps is complete; the following figure appears.

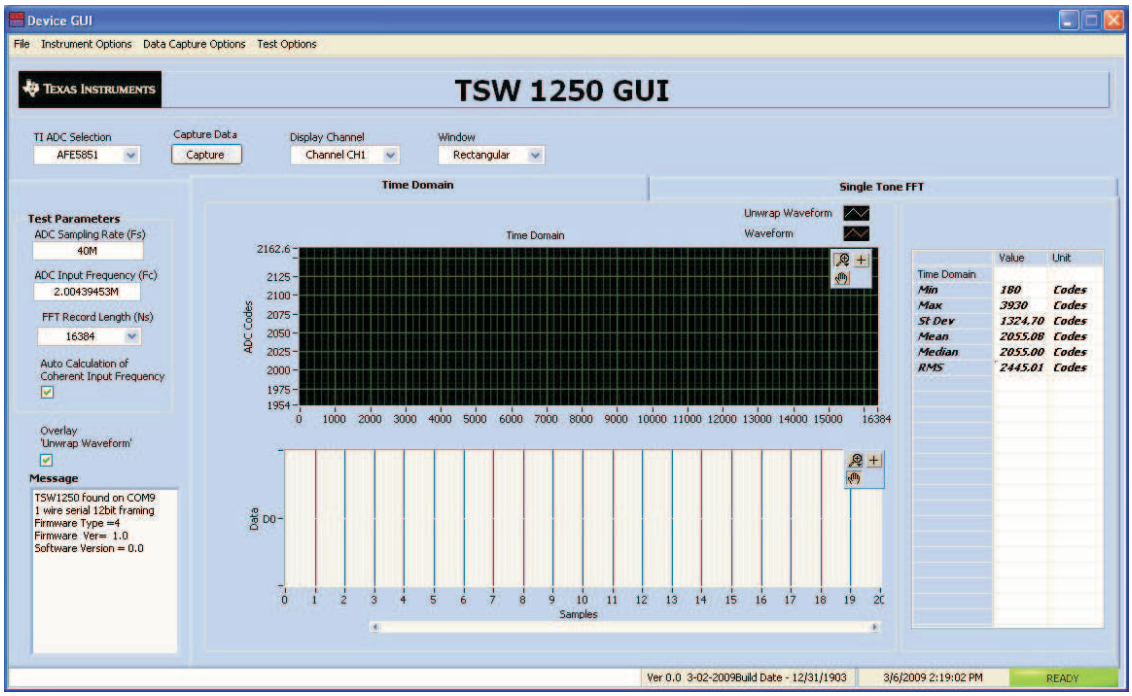


Figure 24. User Interface: Frequency Load Value to Signal Generator

Command to Run Test

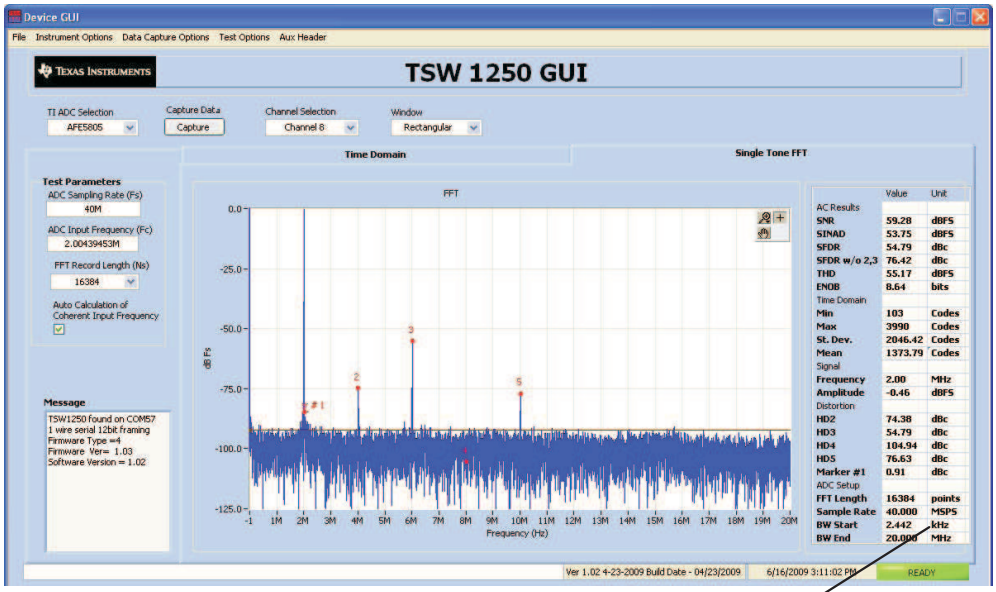
Set the test channel

Select the Window type to Rectangular.

Press the Capture Data button to start the test.

For noisy conditions, the amplitude of the signal may be too large; continue decrement the signal generator amplitude by 1dBm until the desired results are achieved.

A.3.1 Single Tone FFT Data



	Value	Unit
AC Results		
SNR	**59.28**	**dBFS**
SINAD	**53.75**	**dBFS**
SFDR	**54.79**	**dBc**
SFDR w/o 2,3	**76.42**	**dBc**
THD	**55.17**	**dBFS**
ENOB	**8.64**	**bits**
Time Domain		
Min	**103**	**Codes**
Max	**3990**	**Codes**
St. Dev.	**2046.42**	**Codes**
Mean	**1373.79**	**Codes**
Signal		
Frequency	**2.00**	**MHz**
Amplitude	**-0.46**	**dBFS**
Distortion		
HD2	**74.38**	**dBc**
HD3	**54.79**	**dBc**
HD4	**104.94**	**dBc**
HD5	**76.63**	**dBc**
Marker #1	**0.91**	**dBc**
ADC Setup		
FFT Length	**16384**	**points**
Sample Rate	**40.000**	**MSPS**
BW Start	**2.442**	**kHz**
BW End	**20.000**	**MHz**

Figure 25. Typical Performance of AFE5805

A.3.2 Single Tone FFT Data to XCELL

The test data can be saved to a spread sheet file for further processing.

1. Click File from the GUI. A pull down listing shows up.
2. Select "Save Single Tone Data". This example used the name single_tone.csv
3. In this example, the saved data was brought up to excel to plot as shown in Figure 26.

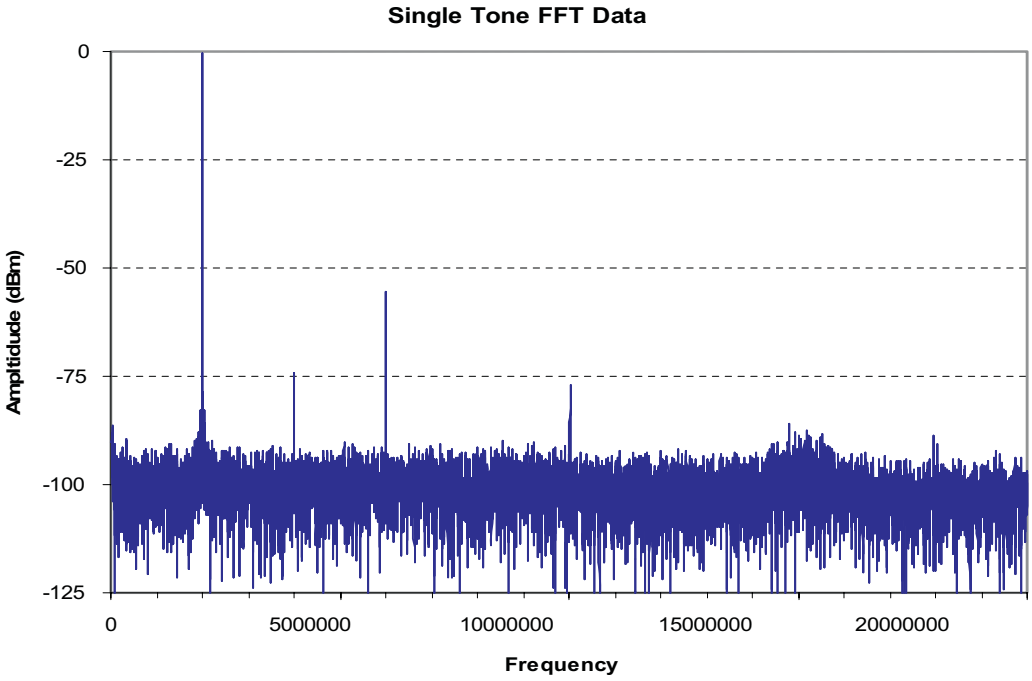


Figure 26. Single Tone FFT Test Data Plot in EXCELL

A.3.3 Single Tone FFT Data Saved as Hardcopy

The test data can be saved as a hard copy. This can be used later to see the setup parameters.

1. Click File from the GUI. A pull down listing shows up.
2. Select "Save Capture As" and "Save as JPEG"
3. The whole picture includes the setup parameter are saved.

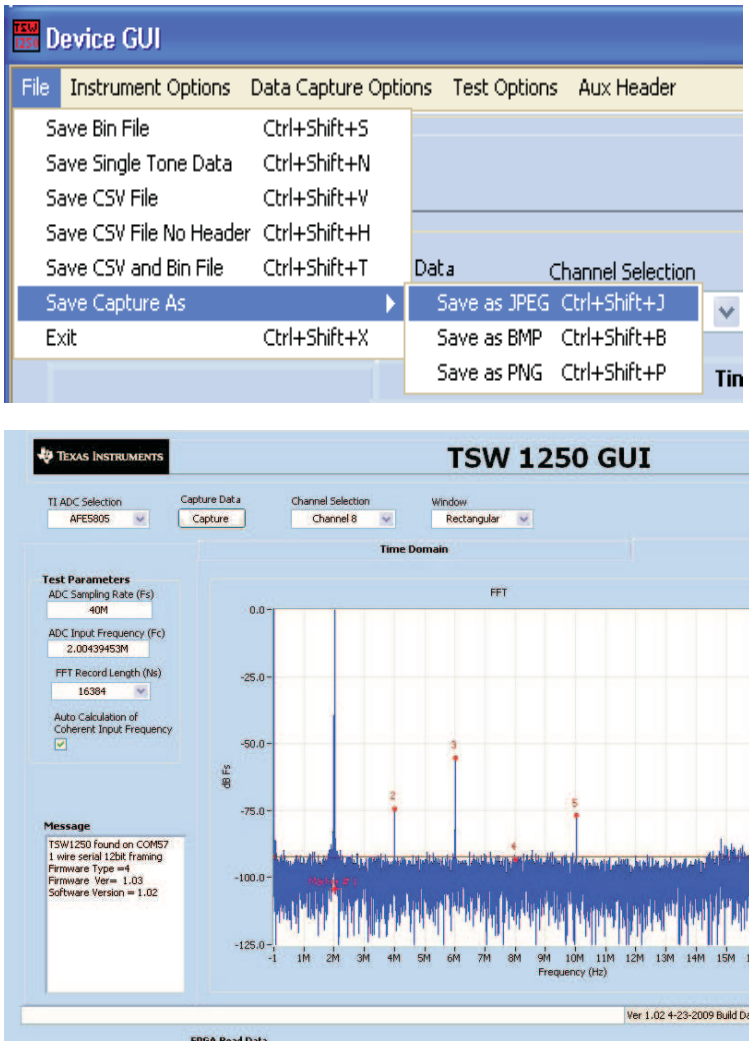


Figure 27. Single Tone FFT Test Data Saved as filename.jpeg

A.3.4 Single Tone FFT With on Board Crystal Oscillator

The AFE5805 has an on board crystal oscillator; the user can use it as the clock source instead of a clock generator. Since this is a non-coherent condition; it is necessary to choose a Window type different from Rectangular for the test. For this particular one, the Window is set to HANNING.

The signal generator is still required for the signal source.

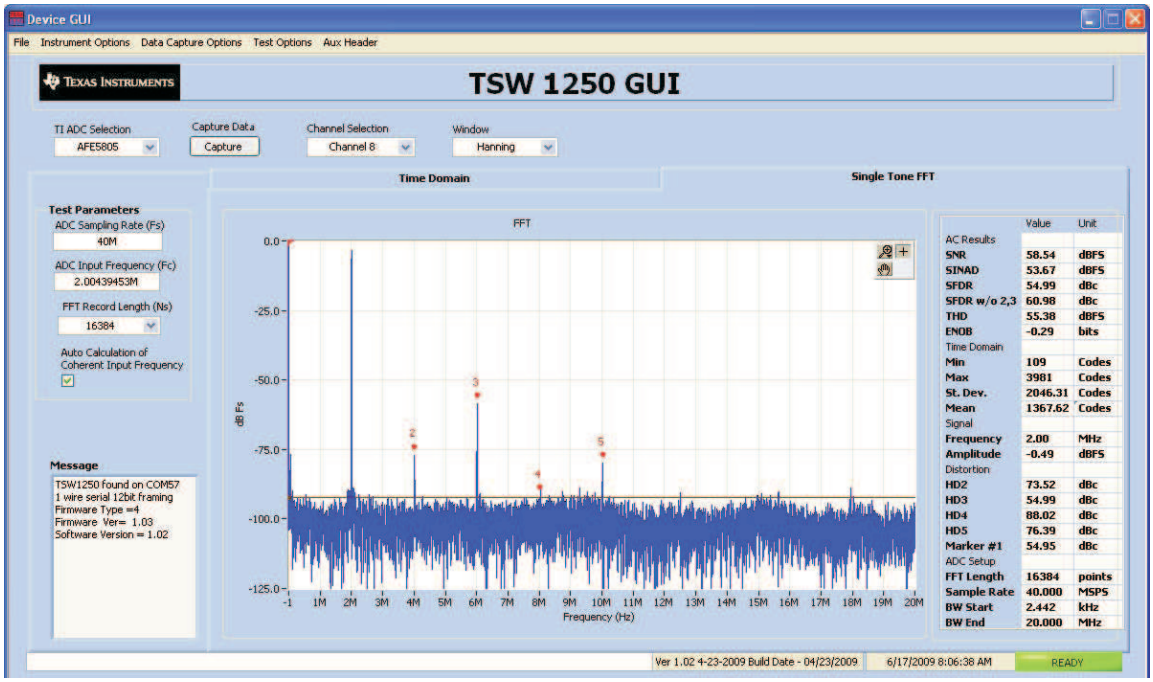


Figure 28. Typical Performance of AFE5805 in Non-Coherent Case

A.3.5 Time Domain

The Time Domain test is shown in Figure 29. The larger central pane displays the raw sampled data whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

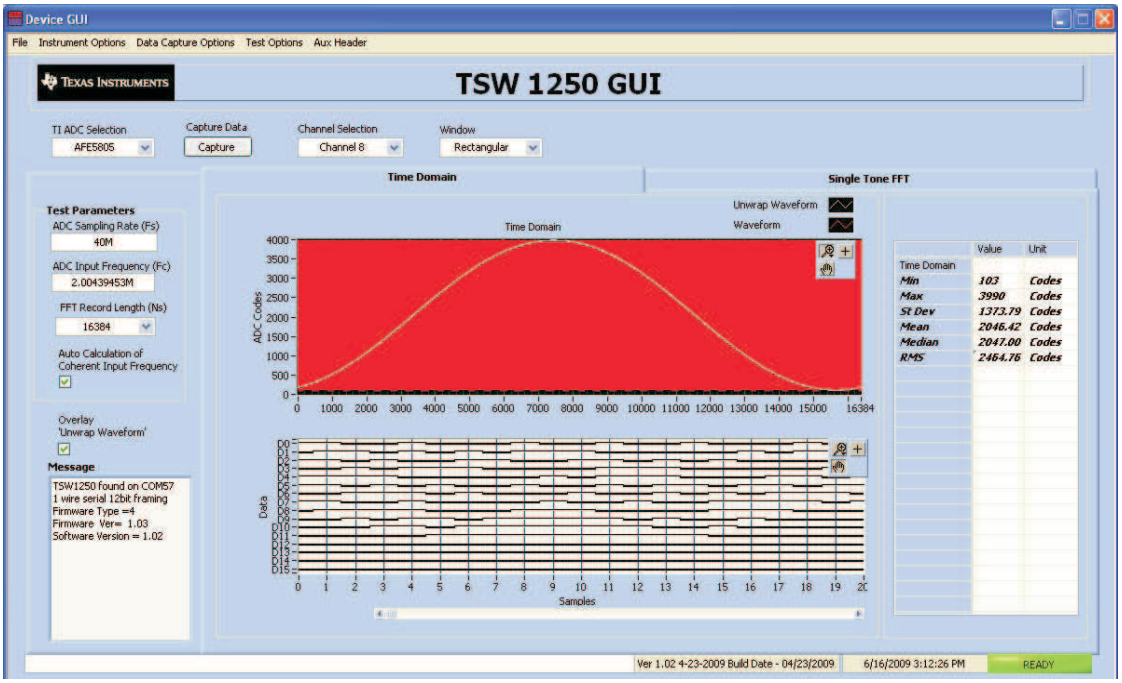


Figure 29. User Interface: Time Domain Format

Appendix B TSW1100 for Evaluating AFE5805

This appendix describes the use of TSW1100 software to analyze data files acquired by logic analyzers.

Coherent sampling is recommended when HP8644s are used. The calculation of coherent sampling rate and signal frequency can be found in the TSW1100 user's manual at the following Web site: http://focus.ti.com/docs/toolsw/folders/print/tsw1100.html

Users can set the calculated frequencies for signal generators; acquire ADC data through a logic analyzer; and save the data as a text file. A typical data file captured by a logic analyzer should be modified to the following format (i.e., containing only one column):

1981
1615
1292
1046
895
852
927
1113
1394
1737
2110
2477
2798
3044
3196
3237
3162
2978
.
.
.
.

The AFE5805 performance analysis can be done as follows:

- First, add some header information to the modified logic analyzer data file as follows. Example files are included in the TSW1100 software package. Modify time, sampling rate, and frequency-in based on your setup:

  TSW1000

  2/12/2007 12:38
  Bits =12
  Sampling Rate =40000000.000
  Frequency in =1998291.0156
  2s complement =No
  Data Format =Decimal

  Raw Captured Data:
  1981
  1615
  1292
  1046
  895
  852
  927
  1113
  1394
  1737
  2110
  2477
  2798

3044
3196
3237
3162
2978
2702
2358

- Then, select TSW1000 as the TI chip as shown in Figure 30.

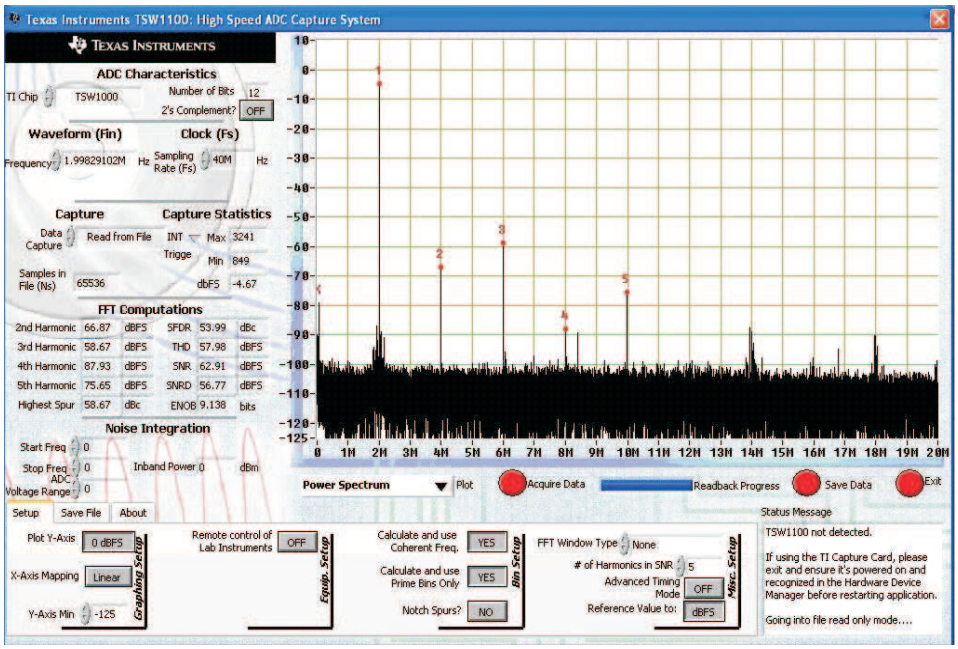
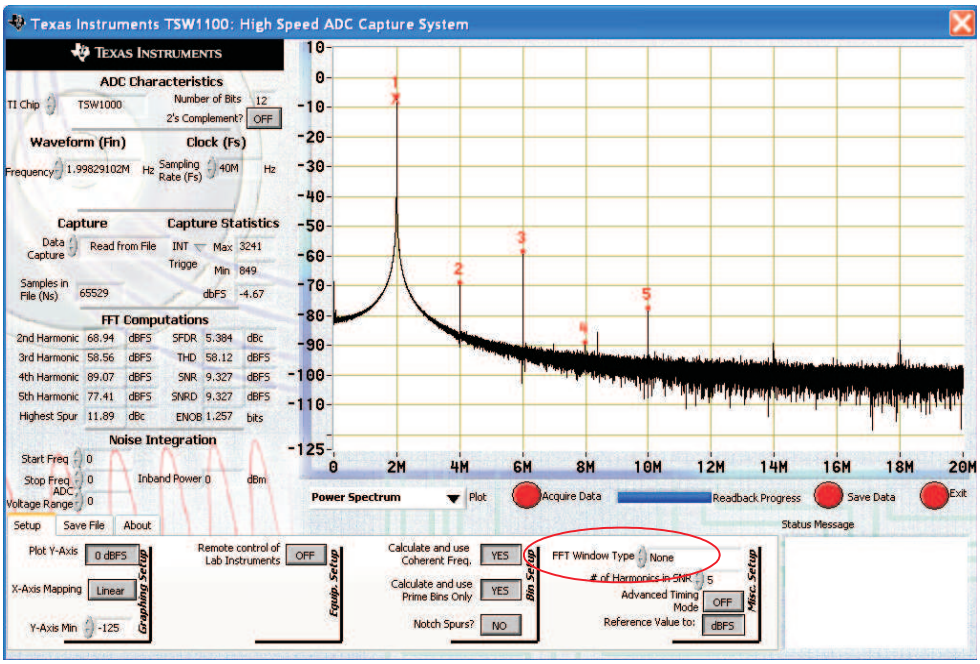


Figure 30. TSW1100 Interface

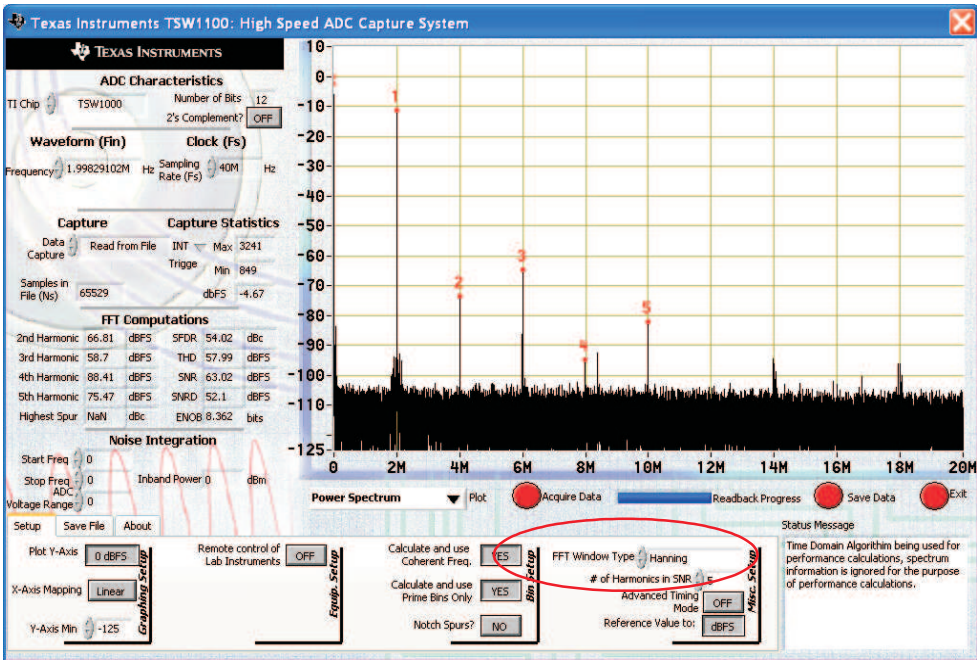
- Finally, users should click the *Acquire Data* button, select the text file with header information, and see the analysis results.

TSW1100 also supports analysis of noncoherent sampled data. However, some artifacts may be noticed during analysis. The appropriate FFT window must be applied to the data.

Users should first follow the preceding steps to get the nonwindowed analysis results shown in Figure 31(a). Then, after the appropriate FFT window is applied, the correct analysis results are obtained as shown in Figure 31(b). Note that some DC artifacts can be seen in Figure 31(b).

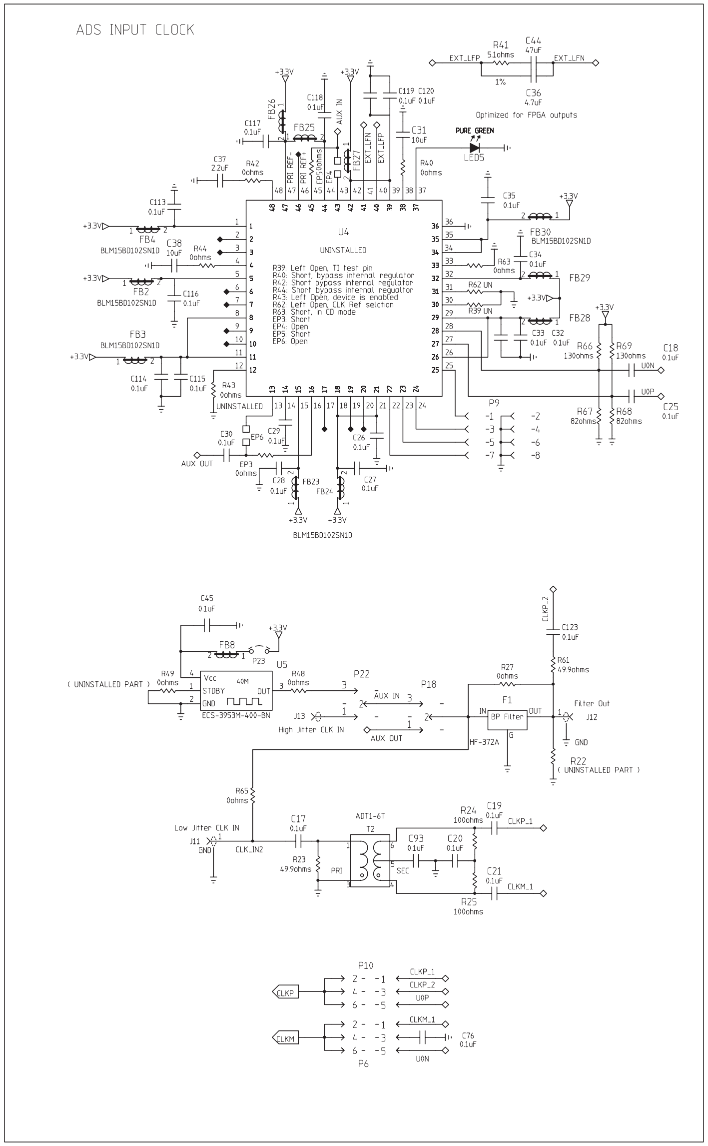
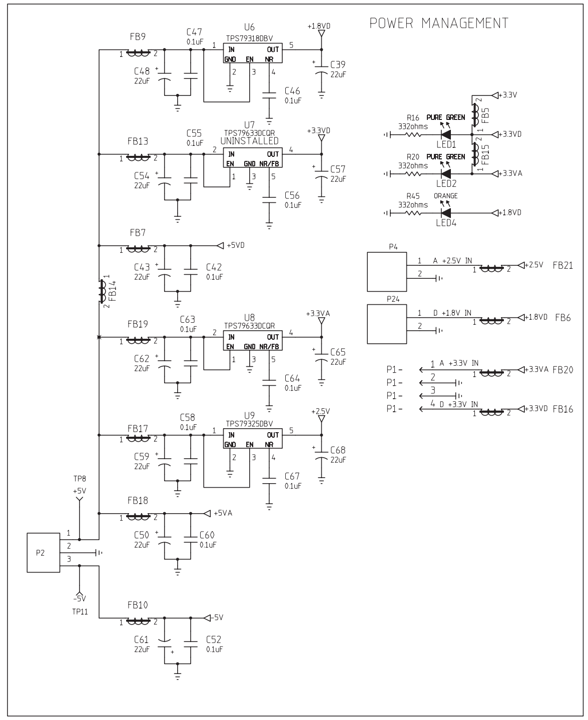
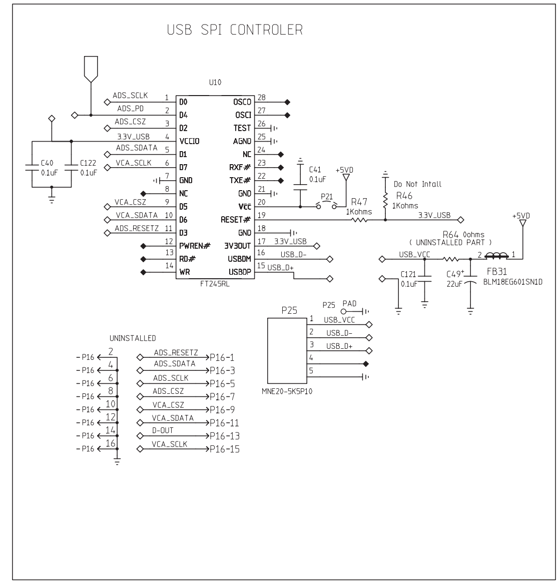
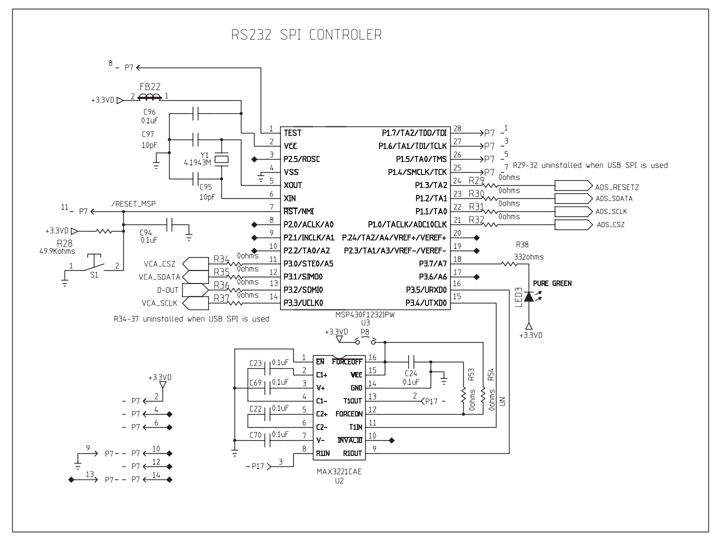
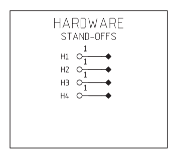


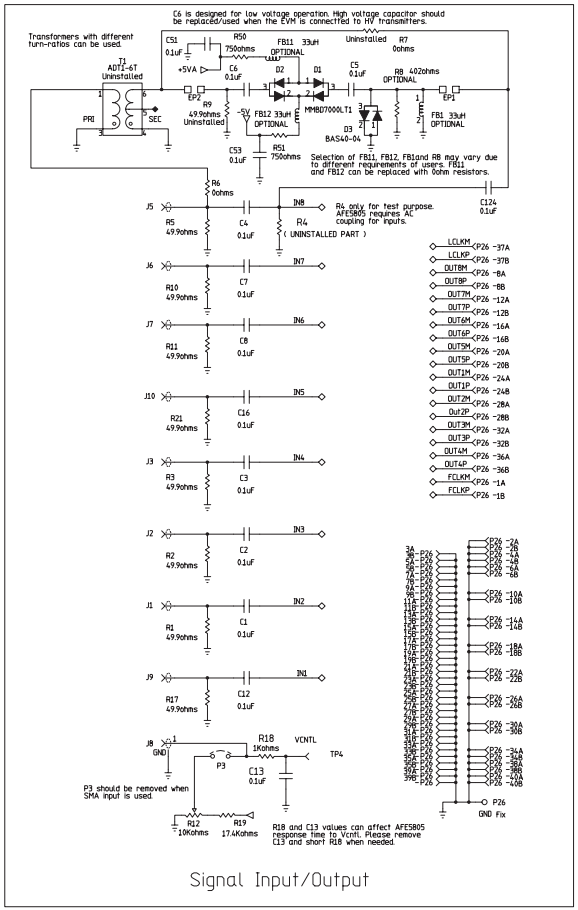
(a) No window applied



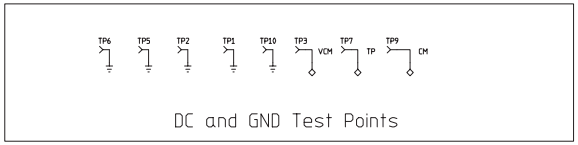
(b) Hanning window applied. Note the DC artifact that is visible.

Figure 31. Analysis of Noncoherent Sampled Data

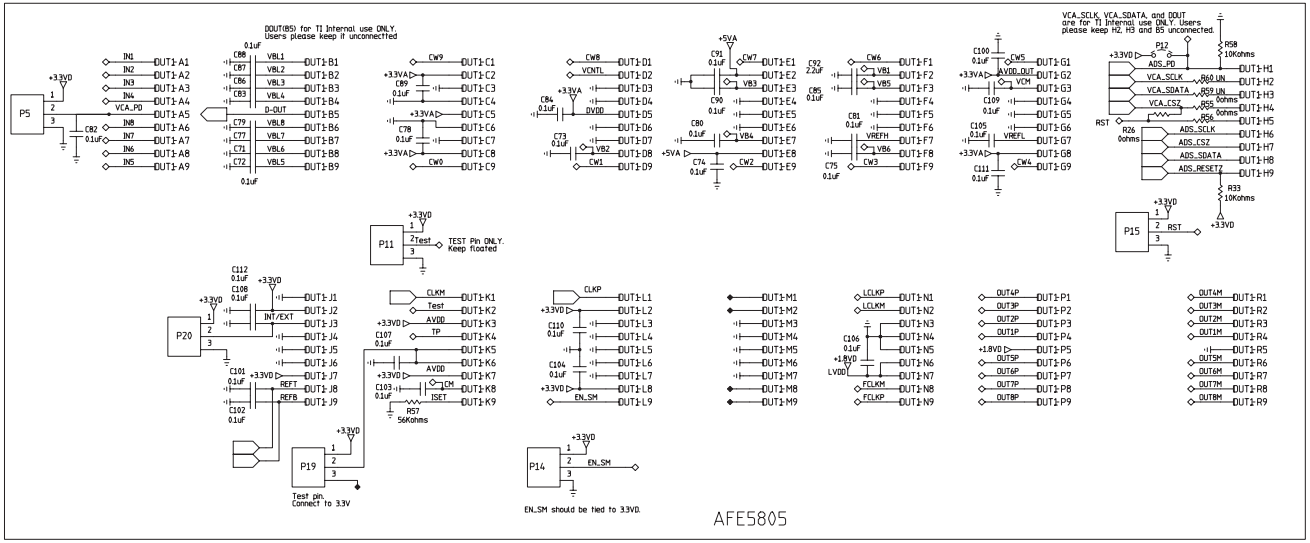

ADS INPUT CLOCK
U4
UNINSTALLED
R39: Left Open, TI test pin
R40: Short, bypass internal regulator
R42: Short, bypass internal regulator
R44: Short, bypass internal regulator
R43: Left Open, device is enabled
R62: Left Open, CLK Ref selection
R63: Short, in CD mode
EP3: Short
EP4: Open
EP5: Short
EP6: Open
Optimized for FPGA outputs
BLM15BD102SN1D
ECS-3953M-400-BN
High Jitter CLK IN
Low Jitter CLK IN
AUX IN
AUX OUT
Filter Out
BP Filter
HF-372A
(UNINSTALLED PART)
ADT1-6T

POWER MANAGEMENT
TPS79318DBV
TPS79633DCQR
UNINSTALLED
TPS79633DCQR
TPS79325DBV
PURE GREEN
ORANGE

USB SPI CONTROLER
U10
FT245RL
Do Not Intall
(UNINSTALLED PART)
BLM18EG601SN1D
UNINSTALLED
MNE20-5K5P10

RS232 SPI CONTROLER
MSP430F1232IPW
U3
R29-32 uninstalled when USB SPI is used
R34-37 uninstalled when USB SPI is used
MAX3221CAE
U2
PURE GREEN

HARDWARE
STAND-OFFS
H1
H2
H3
H4



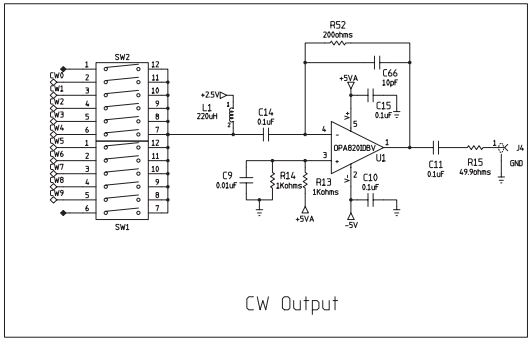
Signal Input/Output



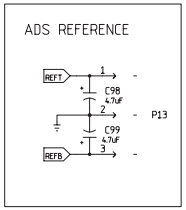
DC and GND Test Points



AFE5805



CW Output



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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of ±4.75 V to ±5.25 V and the output voltage range of -5 V to +5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 0°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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