

AFE5801 8-Channel Variable Gain Amplifier (VGA) with Octal High-Speed ADC

The AFE5801EVM is an evaluation tool designed for the ultrasound analog front-end (AFE) device AFE5801. In order to deserialize the outputs of AFE5801, an ADSDer-50EVM or TSW1250EVM is needed during the evaluation.

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1 Introduction

AFE5801 includes an 8-channel voltage-Controlled-Amplifier (VCA) with digital control and an 8-channel 65MSPS analog-to-digital converter (ADC). The outputs of the ADC are 8-channel LVDS outputs which should be deserialized by the ADSDDeSer-50EVM or TSW1250EVM. The AFE5801EVM provides an easy way to examine the performances and functionalities of AFE5801.

1.1 AFE5801EVM Kit Contents

The AFE5801EVM kit contains the following:

- AFE5801 EVM board
- USB cable
- CD-ROM containing
 - AFE5801 EVM User's Guide (this document)
 - GUI software

1.2 Features

- Characterize AFE5801
- Provide 8-channel LVDS outputs from the ADC
- Compatible to the standard TI LVDS deserializer ADSDDeSer-50EVM or TSW1250EVM
- Communicate with PC through USB interface
- Power Management provides multiple power supplies for AFE5801 and other devices.

1.3 Power Supplies

The AFE5801EVM requires only +5V power supplies for operation.

1.4 Indicators

The AFE5801EVM has 4 LEDs on the board as shown in [Figure 1](#). Their states demonstrate the normal operation of AFE5801EVM.

- **LED 1:** U1 status indicator. Its ON state indicates the clock management chip U1 works well if U1 is installed.
- **LED 3 and 2 (RED):** 1.8VD and 1.8VA power supply indicators. ON state indicates that the AFE5801 is powered correctly.
- **LED 4 (GREEN):** +3.3V power supply indicator. ON state indicates that the AFE5801 is powered correctly.

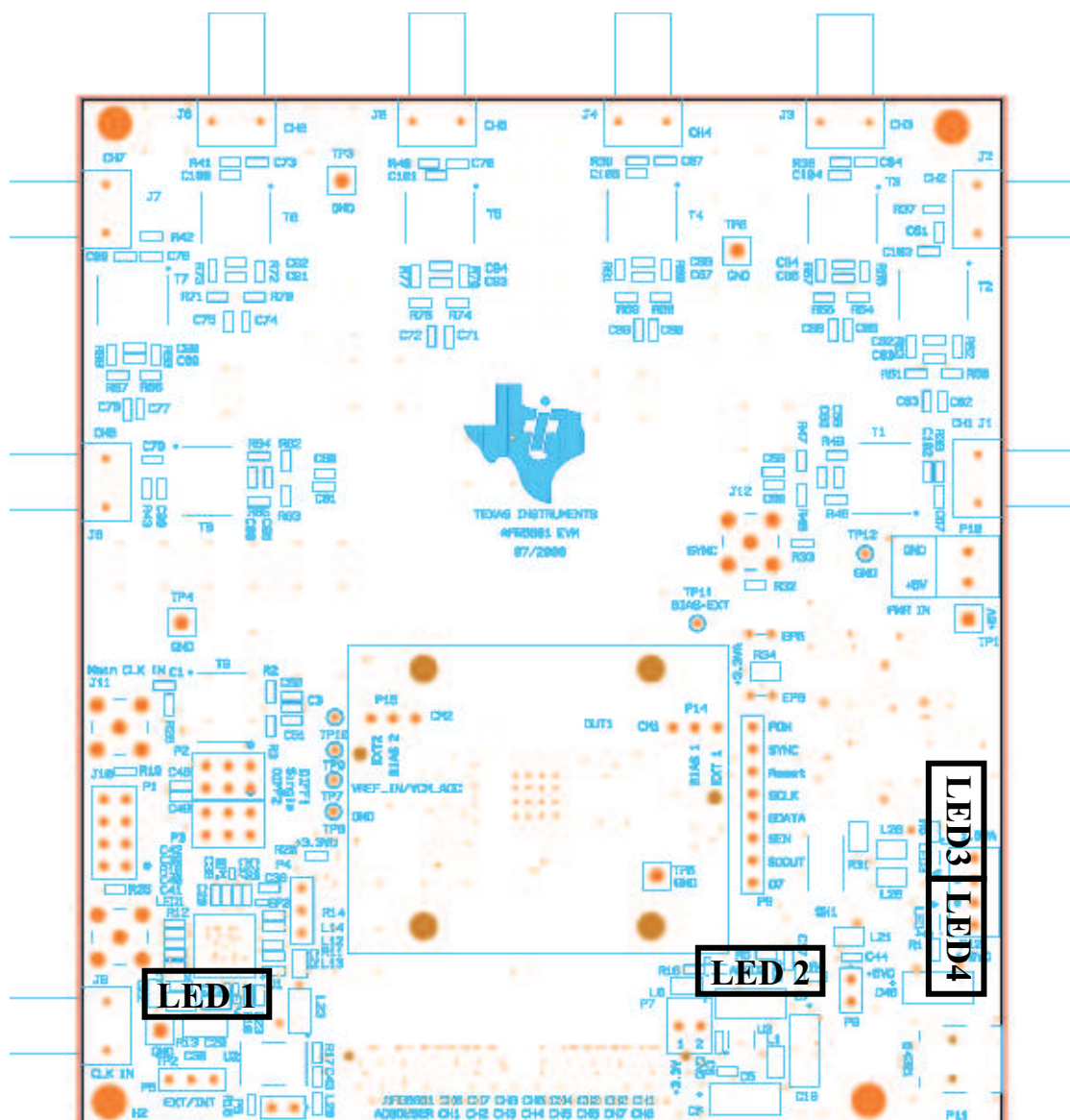


Figure 1. AFE5801EVM LED Locations

2 Board Configuration

This chapter describes the locations and functionalities of inputs, outputs, jumpers, test points of the AFE5801EVM in detail.

2.1 Board Connections Overview

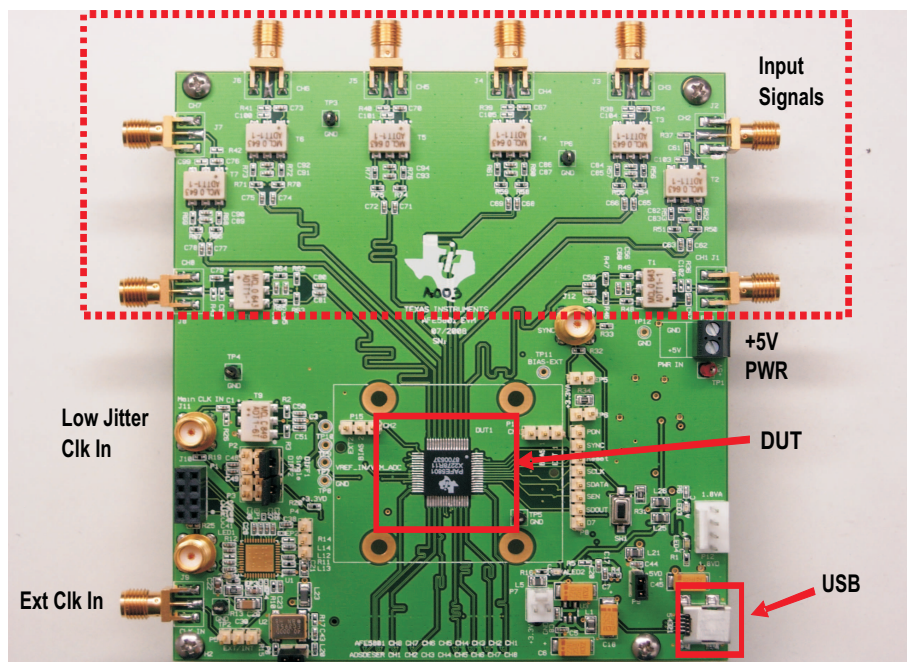


Figure 2. AFE5801EVM TOP View

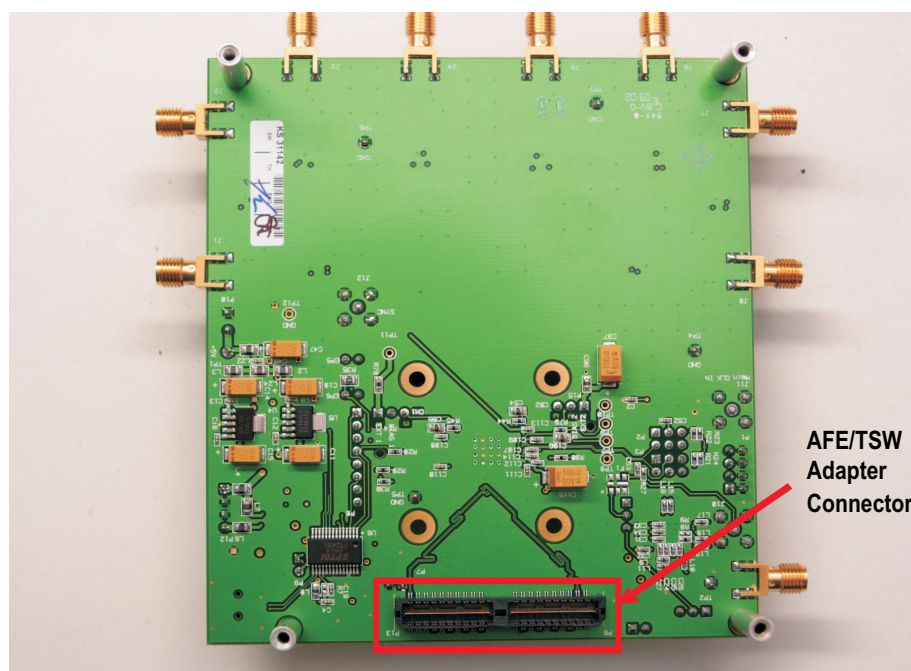


Figure 3. AFE5801EVM BOTTOM View

2.2 I/O and Power Connectors

The positions and functions of the AFE5801EVM connectors are discussed in this section.

- Analog Inputs Ch1~Ch8 (J1~J8): Single-end analog signal is converted to differential signals by transformer.
- Low Jitter CLK Source Input (J11): This input accepts clocks with low jitter noise, such as HP8644 output. 20~50MHz 50% duty cycle clock with 1~2Vrms amplitude can be used. When J11 is used, make sure shunts P4, P5, P6 are removed.
- CLK output (J10): The output of either the U1 output or the on-board 40MHz oscillator output depending on jumper P4's connection.
- External CLK Input (J9): ADC Clock input, such as FPGA outputs. FPGA outputs must be processed by U1. Otherwise, the ADC of AFE5801 will not achieve satisfactory performance.
- +5V PWR connector(P10): Power supply input
- USB input (P11): USB interface to control the AFE5801.
- LVDS Outputs Ch1~Ch8 (P13): Differential LVDS data outputs.

2.3 Jumpers and Setup

The board has been set to default mode. Detailed description can be found in [Figure 4](#) and [Figure 5](#).

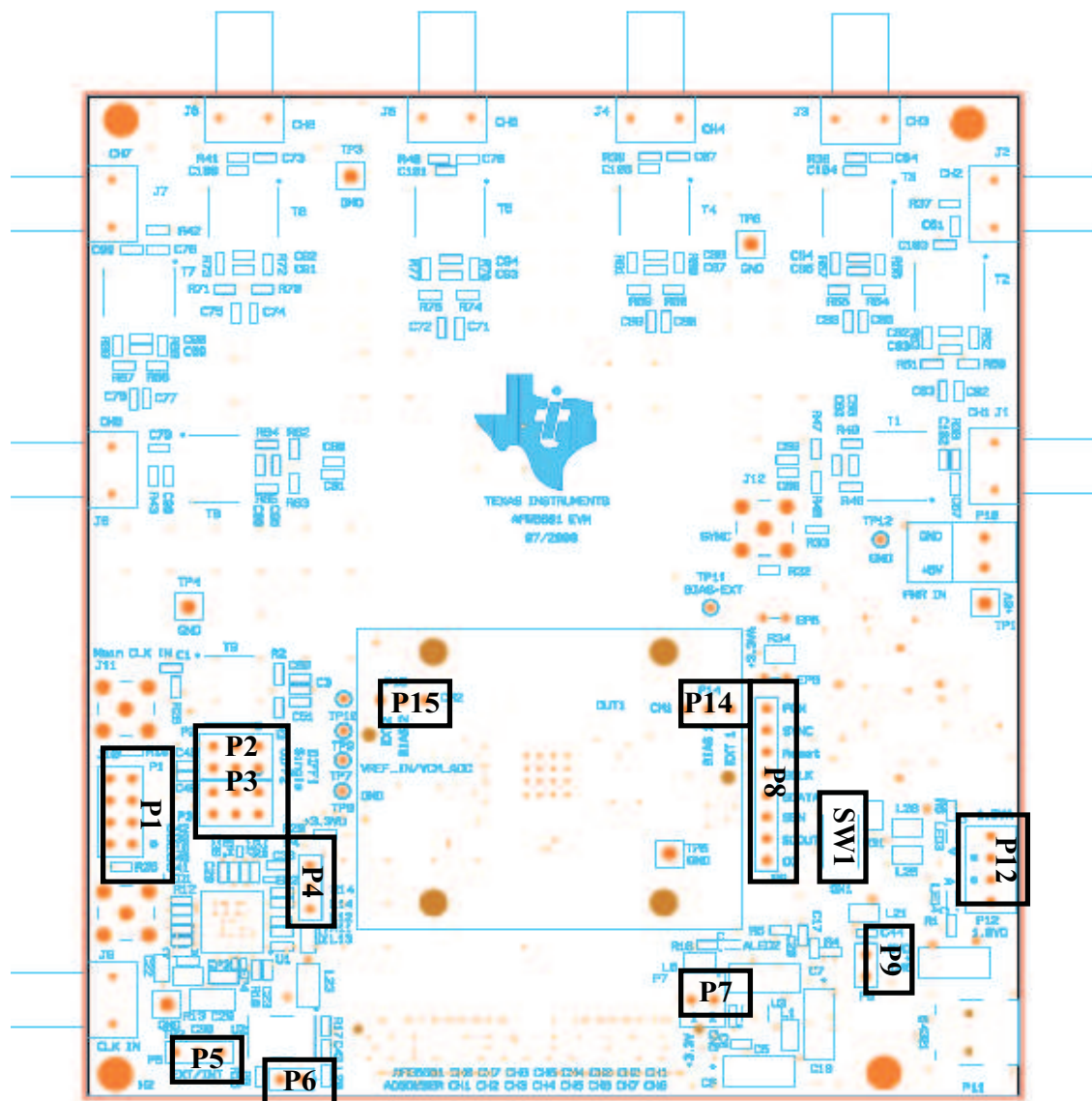


Figure 4. Locations of Jumpers, Headers and Switches on the AFE5801EVM

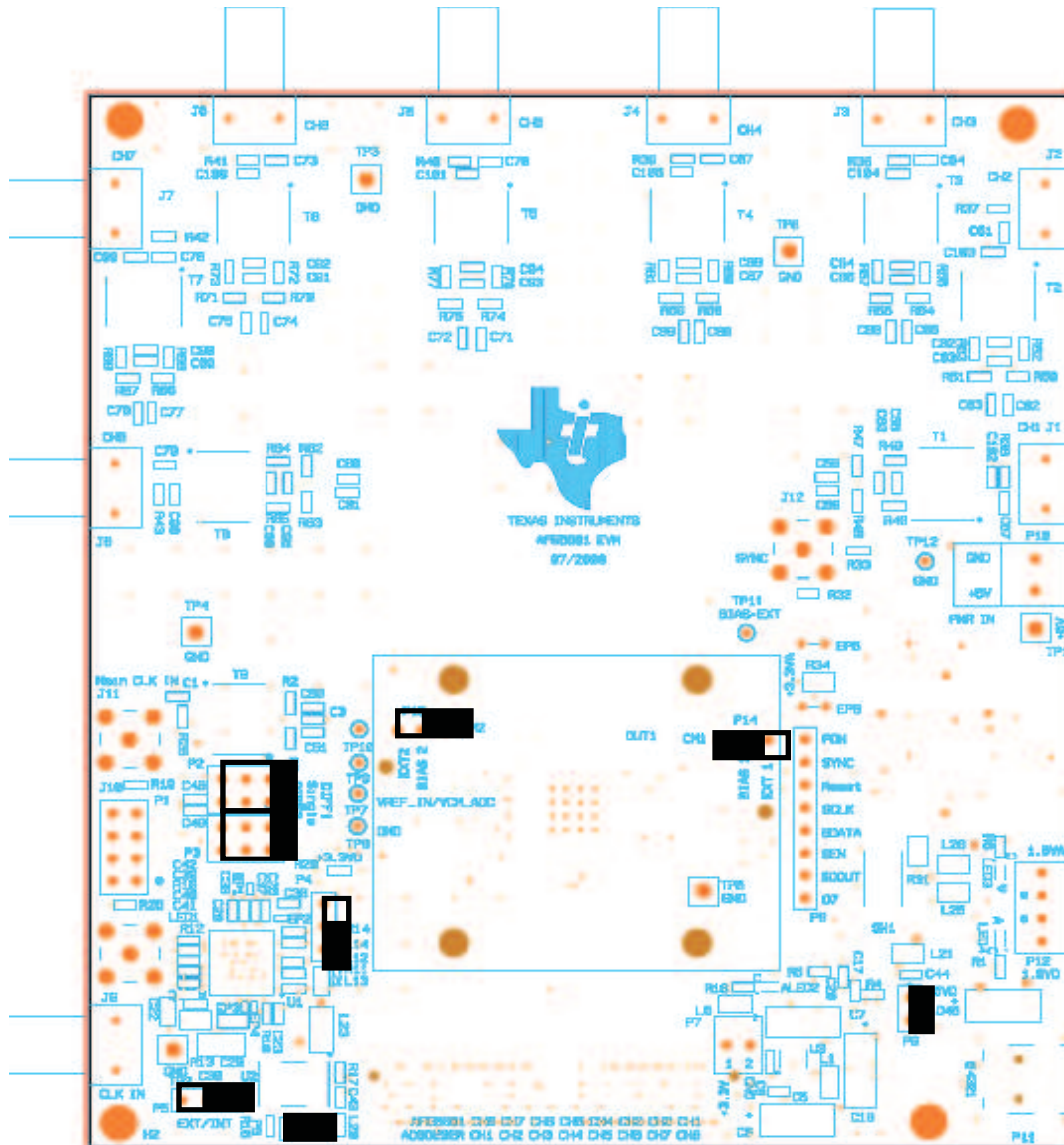


Figure 5. Default Setup for Jumpers

- P1: SPI interface for U1
- P2, P3: AFE5801 ADC clock input selection: transformer-based differential clock, single-ended LVCMOS clock, or future clock option (needs U1 to support). Default is to use transformer-based differential clock.
- P4: Select jitter-cleaned clock or non-jitter-cleaned clock. Default is to use non-jitter-cleaned clock (i.e., on-board 40MHz clock).
- P5: Use on-board 40MHz clock. Default is that the on-board clock is used.
- P6: Power on on-board 40MHz clock generator. Default is on.
- P8: Debug port for monitoring ADS SPI signals.
- P9: USB interface enable. Default is on.
- Regulated power supply outputs (P12, P7): 1.8VA, 1.8VD, and 3.3V. P12 and P7 can be configured as power supply input as well if users would like to skip the on-board regulators. Remove the ferrite beads L1, L2, L3, L7 and L24,
- SW1: Reset switch for AFE5801.

2.4 Test Points

- Multiple Test Points are provided on the EVM. Refer to the attached schematics for more information.

3 Board Operation

This chapter describes how to operate the AFE5801EVM for evaluation. Both software and hardware installation and operation are discussed.

3.1 Software Installation and Operation

The AFE5801EVM comes with a software install CD; run setup.exe to install the software.

3.2 USB Driver Installation

- Connect the USB port of EVM to your PC.
- If the driver has not been installed then the message "Windows Found New Hardware" will appear. The Wizard as the following picture will launch.
- Select "No, not this time" from the options. Press Next button

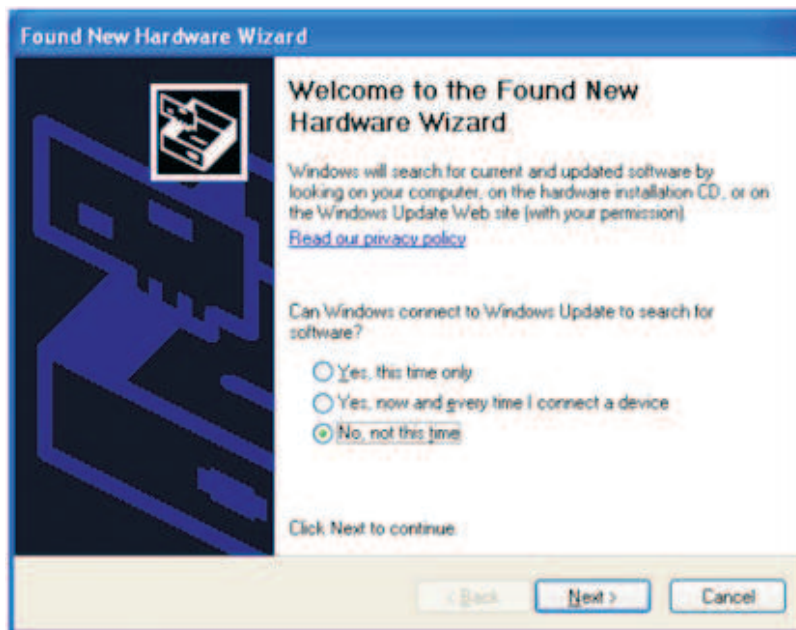


Figure 6. Found New Hardware Wizard Screen

- Select "Install from a list or specific location (Advanced)" as shown below and then click "Next".

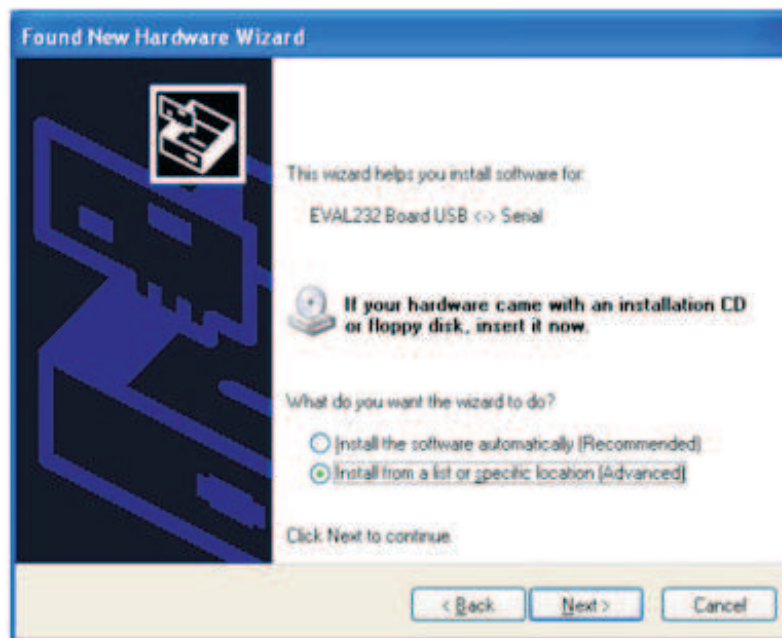


Figure 7. Found New Hardware Wizard (Next) Screen

- Select "Search for the best driver in these locations" and enter the file path for ("C:\Program Files\AFE5801\CDM 2.04.06 WHQL Certified ") in the combo-box or browse to it by clicking the browse button. Once the file path has been entered in the box, click next to proceed.
- If Windows XP™ is configured to warn when unsigned (non-WHQL certified) drivers are about to be installed, the following screen will be displayed unless installing a Microsoft WHQL certified Driver. Click on "Continue Anyway" to continue with the installation. If Windows XP is configured to ignore file signature warnings, no message will appear.

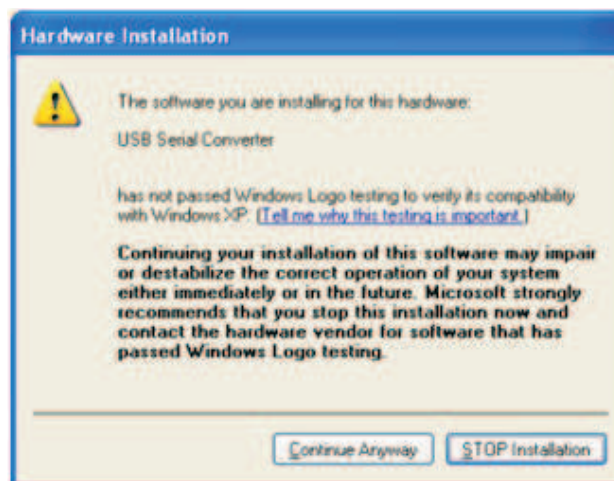


Figure 8.

3.3 GUI Startup

- Launch GUI from XP Window
- Start → All Programs\AFE5801EVM\AFE5801
- Several different screens appear displaying the different modes (Figure 9 through Figure 11)

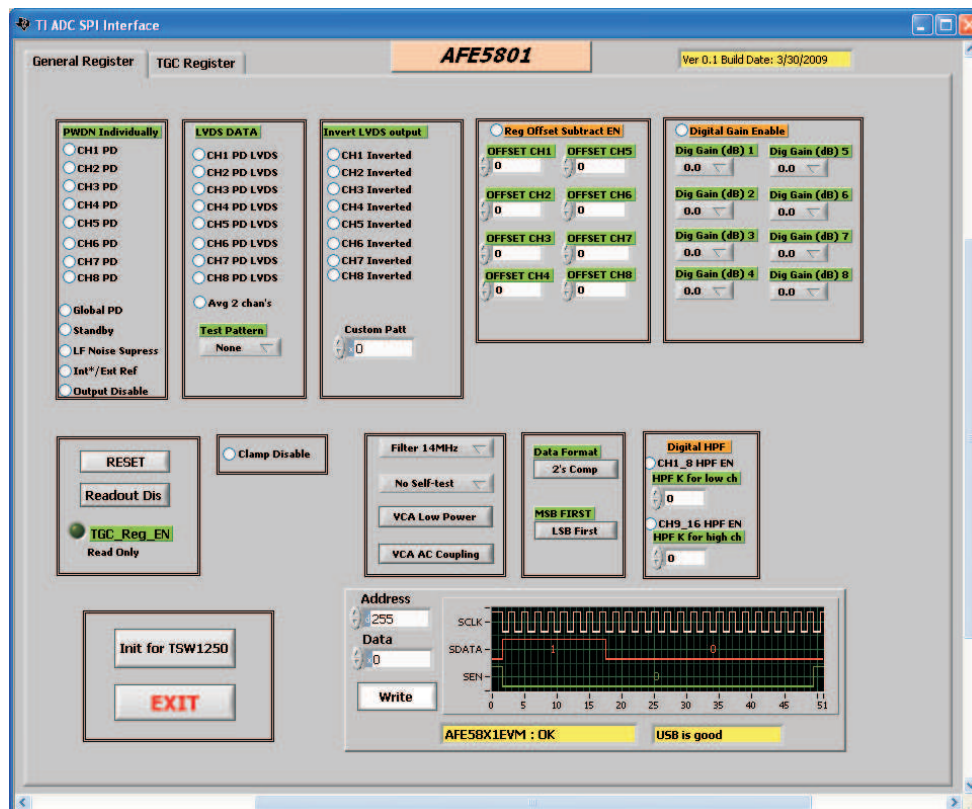


Figure 9. AFE5801EVM USB SPI Interface for General Registers.

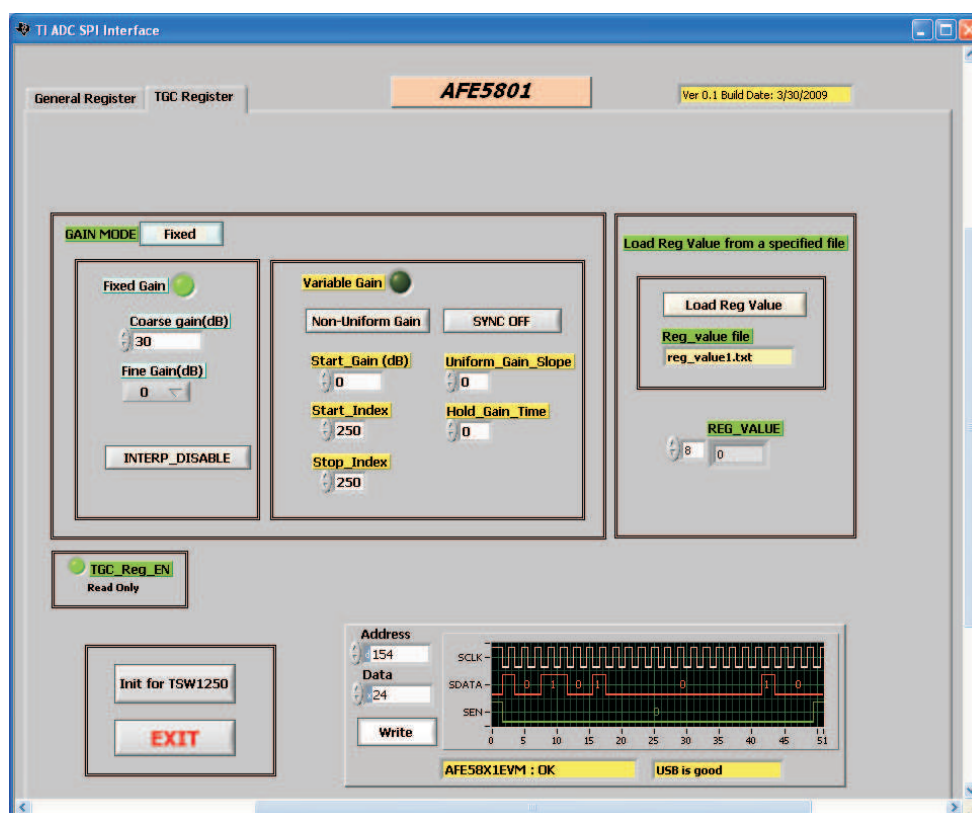


Figure 10. AFE5801EVM USB SPI Fixed Gain Mode

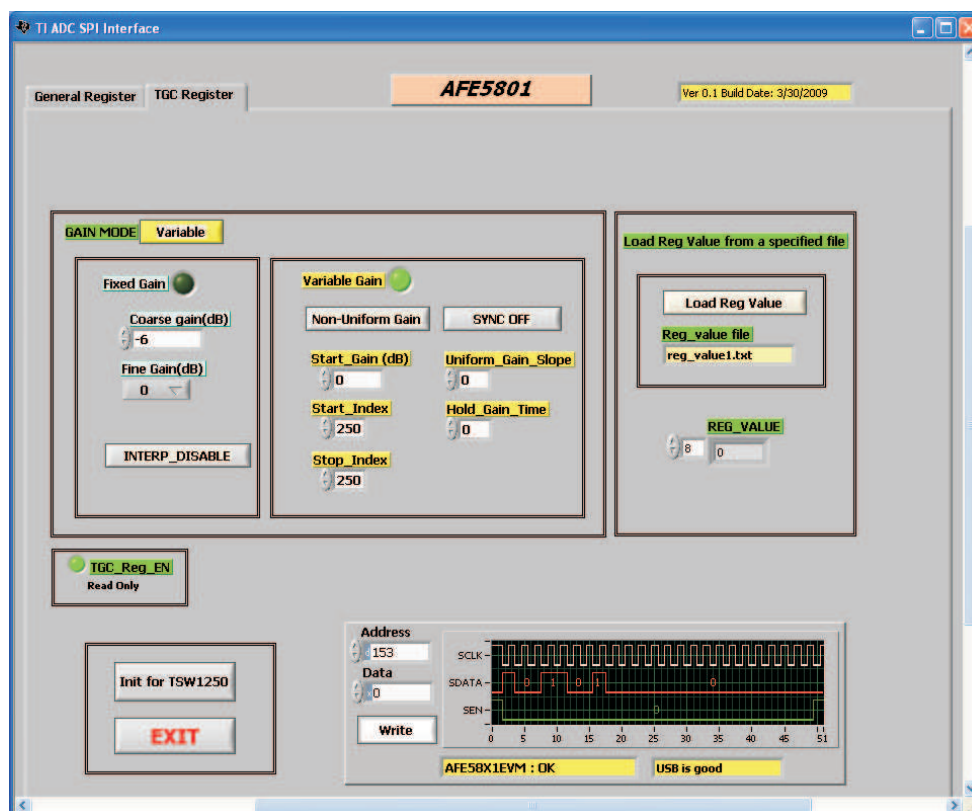


Figure 11. AFE5801EVM USB SPI Interface for Variable Gain Mode

When AFE5801EVM is powered on, all registers have been set to their default modes. Refer to the datasheet for all default settings. It is recommended to restart the SPI software when AFE5801 is powered on in order to synchronize the AFE5801 register settings to the software displays.

Users also can fill out Address Bytes and Data Bytes and press *ENTER* to configure each register.

Typical Configuration

- From [Figure 9](#) press "Init for TSW1250" button
- Select TAB "TGC Register" - [Figure 10](#) will appear
- From [Figure 11](#), press "Variable" button to get into fixed gain mode
- From [Figure 10](#) enter 30 in the "Coarse Gain(dB)" field then press "Write" button.

3.4 Hardware Setup

As mentioned before, Xilinx DeSerializer ADSDeSER-50EVM or TSW1250EVM is required. Please see details in the corresponding application notes on how to use the either of these EVMs. An example bench setup is shown in Figure 12. Band-pass filters are required for signal source in order to ensure the correct SNR measurements of the AFE5801.

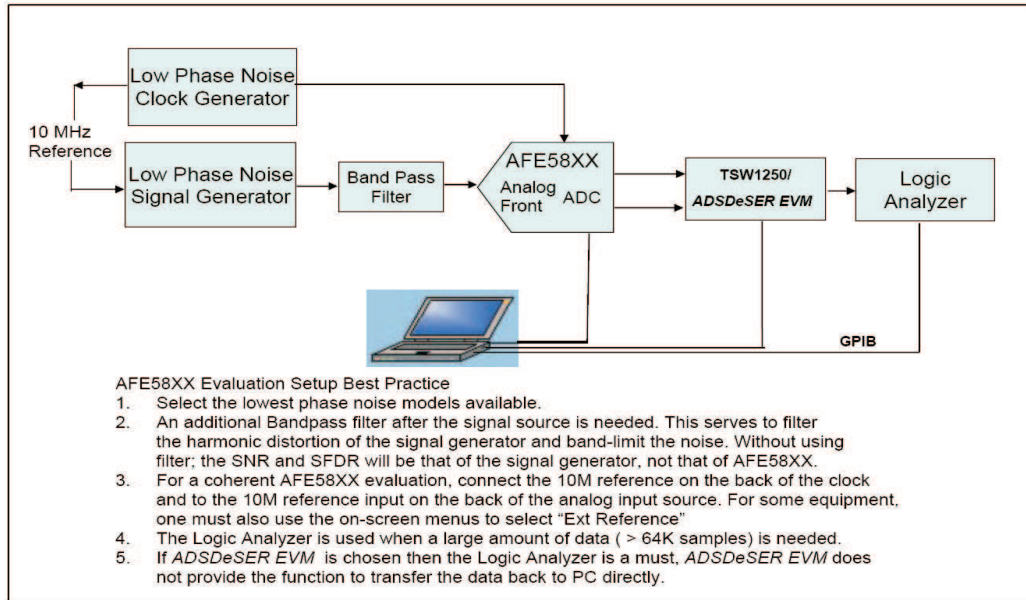


Figure 12. Typical AFE5801 Bench Setup:

The channel order of the AFE5801 outputs is not exactly the same as the one of ADS527x outputs. As a result, the channel number on the ADSDeSER-50EVM or AFE5801EVM might be misleading. Table 1 provides channel-to-channel sequence matching between the ADSDeSER-50EVM and AFE5801EVM.

Table 1. Channel-to-Channel Matching Between the AFE5801EVM and ADSDeSER-50EVM

AFE	FCLK	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	LCLK
Xilinx	FCLK	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	LCLK

For example, when an analog signal is input at CH1 on the AFE5801EVM, the corresponding 12-bit digital output will be seen at CH8 on the ADSDeSER-50EVM when the AFE5801 is configured as 8-channel mode.

3.5 Clock Selection

AFE5801 is typically clocked through a transformer-based circuit. Other options are also available if needed as shown in Figure 13.

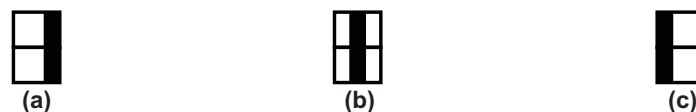


Figure 13. Clock Selection Jumper Configurations: (a) Transformer (default); (b) Single-ended Clock; (c) Future CLK Input Option Based on U1. Both (b) and (c) Configurations Need Some Modifications on the PCB.

The clock source of the EVM could be the on-board clock 40MHz, HP8644 low jitter clock source, or external clock source. The best performance of this EVM is achieved when low-jitter clock source HP8644 is used. The P4, P5, P6 should be removed in order to disable the on-board clock.

When HP8644 or similar clock sources are not available, the on-board 40MHz clock is also a desirable source. The jumpers P4, 5, 6 should be configured as [Figure 13](#) shows (i.e., default setup for AFE5801EVM). In this mode, the transform-based differential clock is used.

3.6 Data Analysis

Based on the data file acquired by a logic analyzer, the performance of AFE5801 can be evaluated.

In Appendix A, we provide one solution (TI TSW1250 EVM) to analyze the data file using the PC. Appendix B provides an alternate solution (TI TSW1100 software) to analyze the data file captured by a logic analyzer. Coherent sampling is recommended if the input and sampling clock are phase locked. Due to the frequency accuracy requirement of coherence sampling, two HP8644s for generating ADC clock and analog signal are required. For most users, this may not be feasible. Data analysis based on windowing is a more suitable approach.

This chapter provides the schematics and layout of the AFE5801EVM as well as the bill of materials.

4.1 Schematics

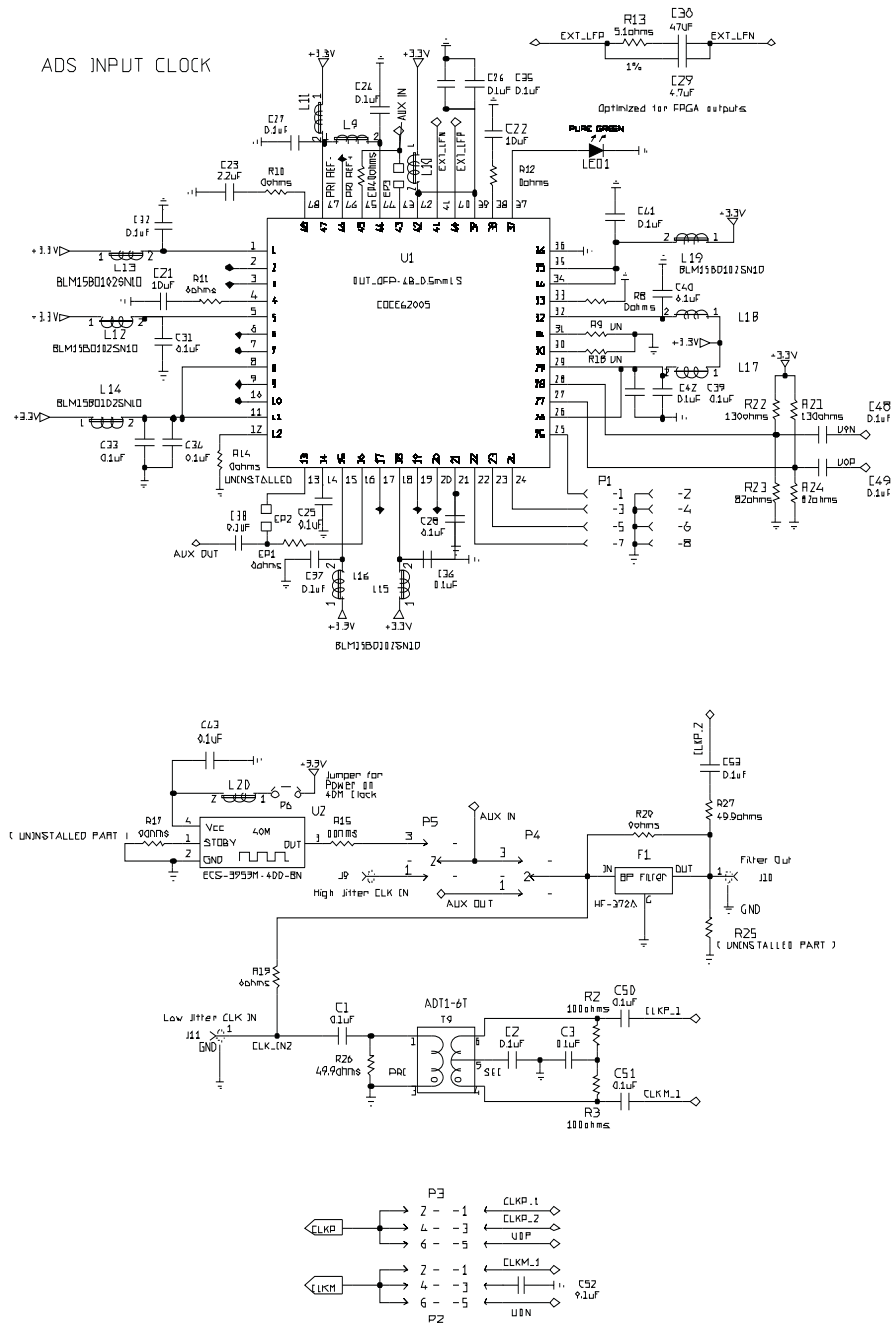
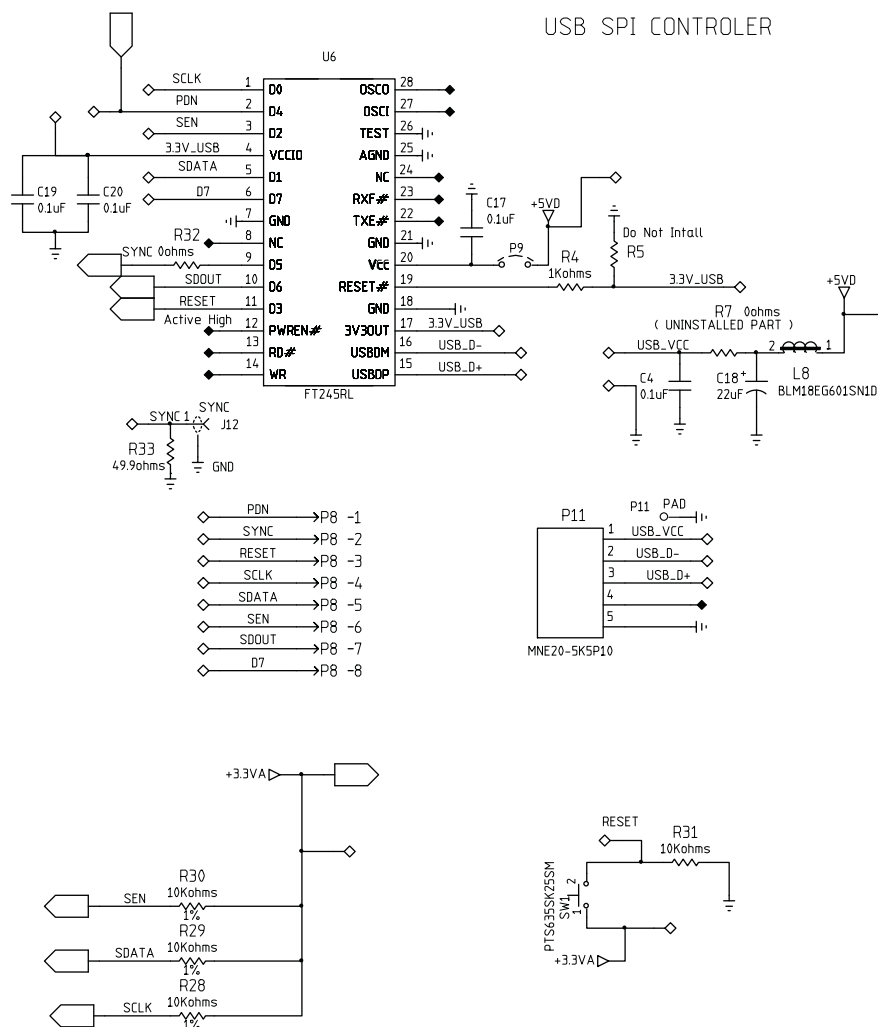


Figure 14. Schematic Page 1





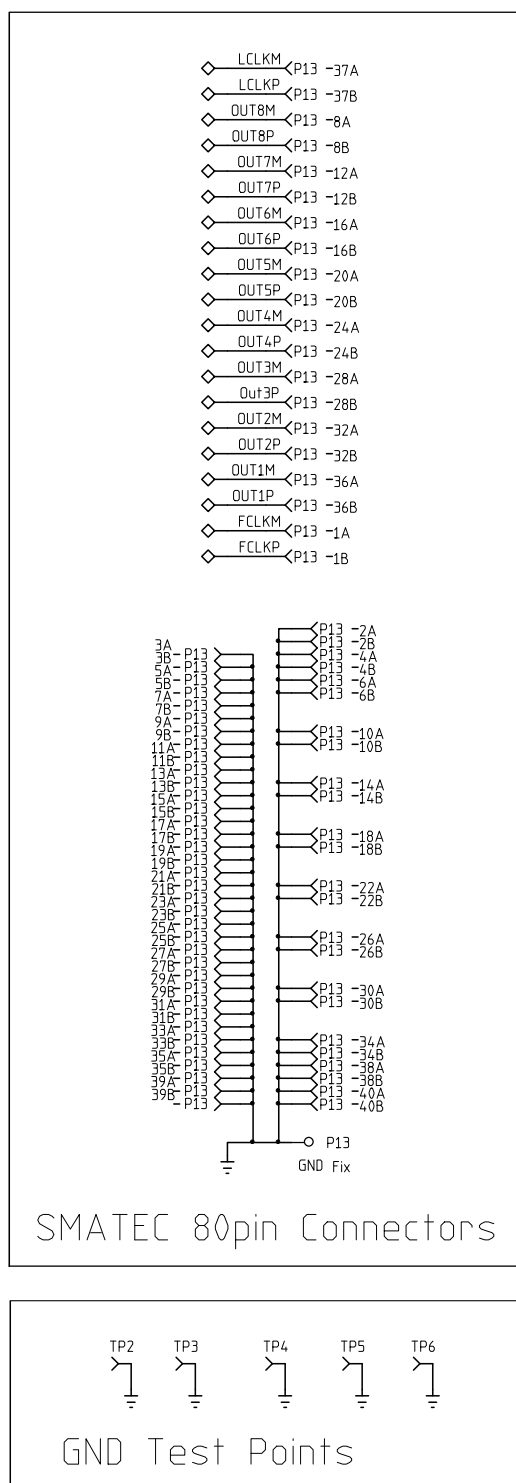


Figure 17. Schematic Page 4

INPUT CHANNELS

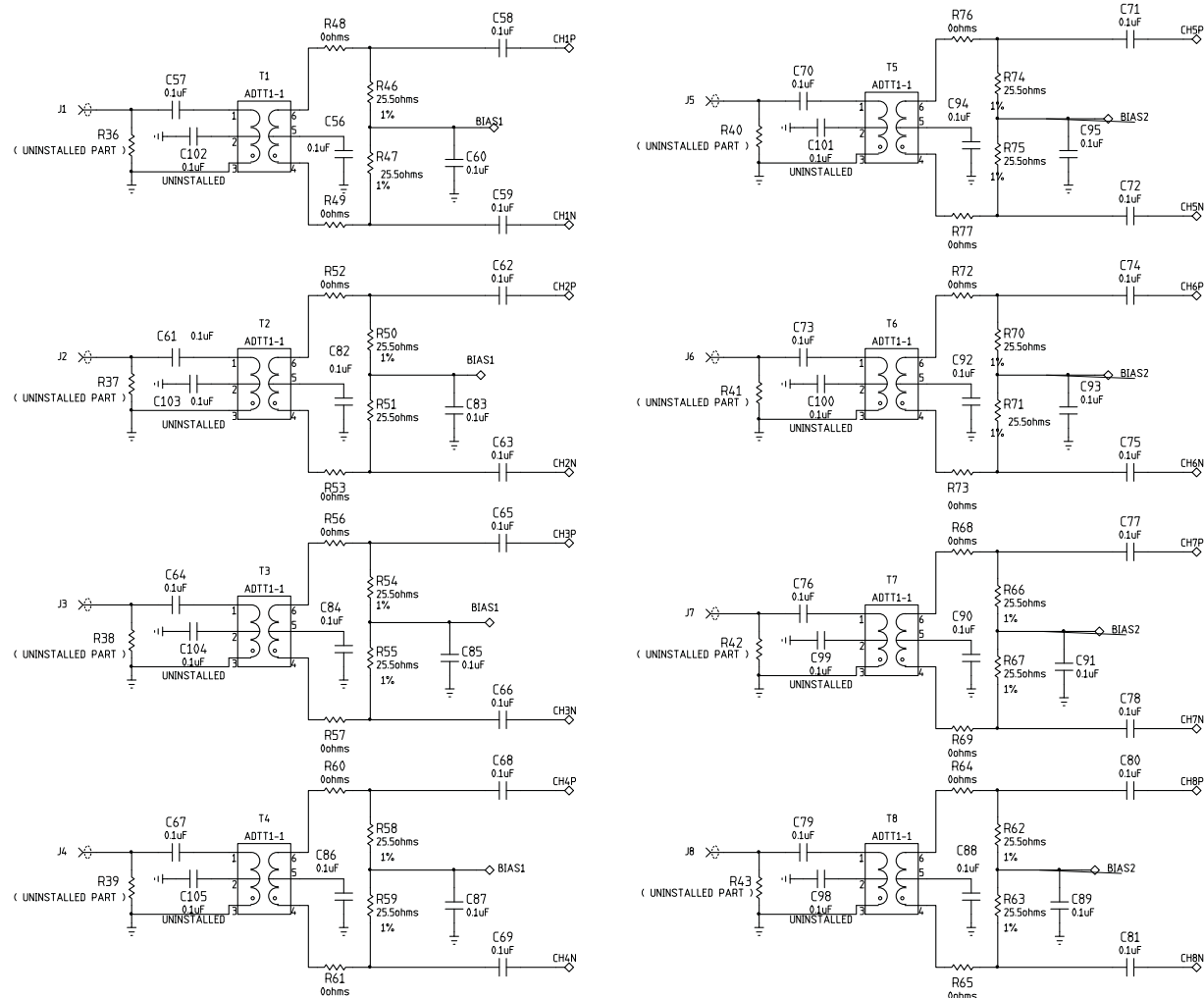


Figure 18. Schematic Page 5

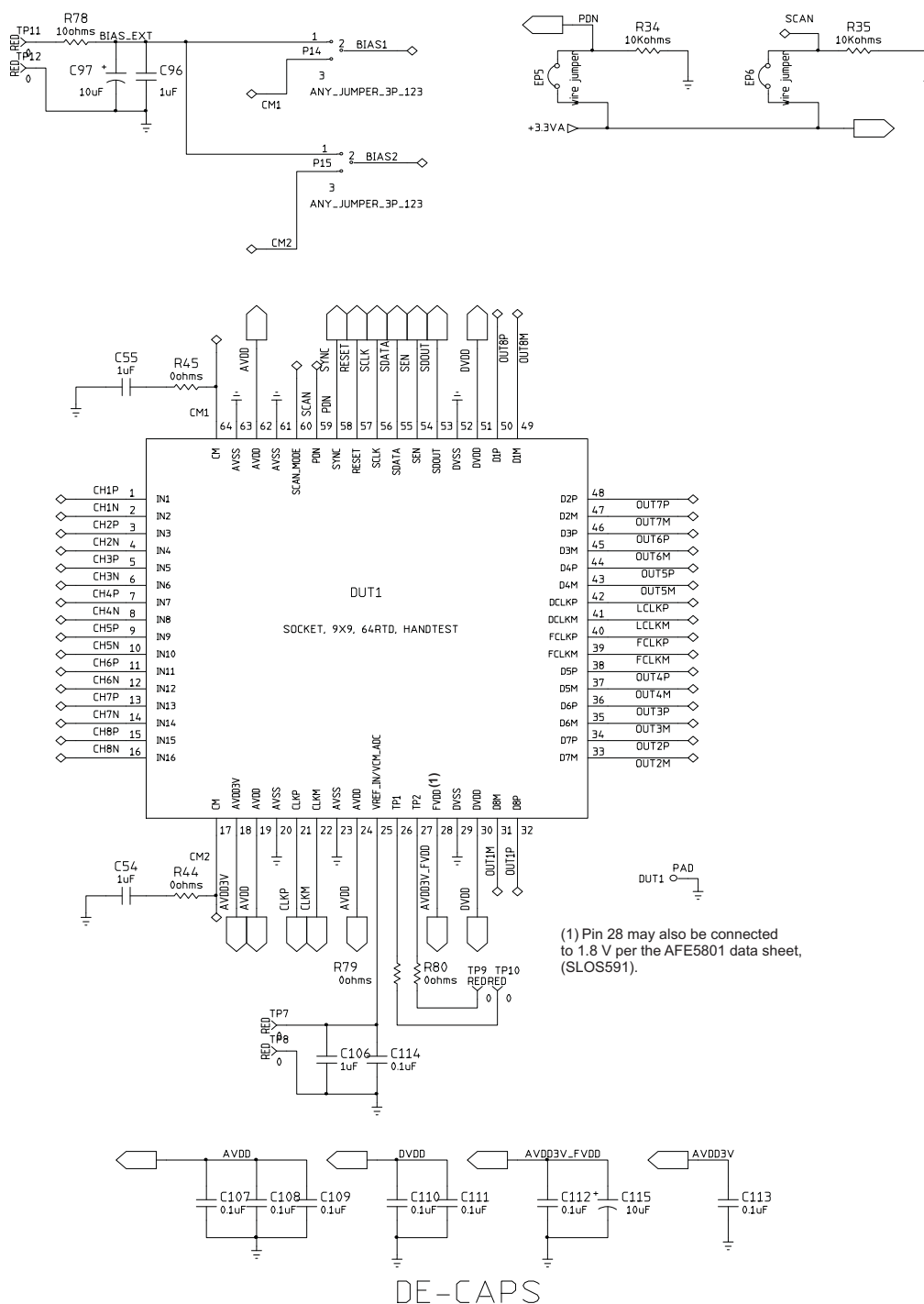


Figure 19. Schematic Page 6

4.2 PCB Layout

A six-layer printed-circuit board is used:

- Top Layer, signal
- Inner Layer 1, ground
- Inner Layer 2, signal
- Inner Layer 3, power
- Inner Layer 4, ground
- Bottom Layer, signal
- Top Silk Screen Layer
- Bottom Silk Screen Layer

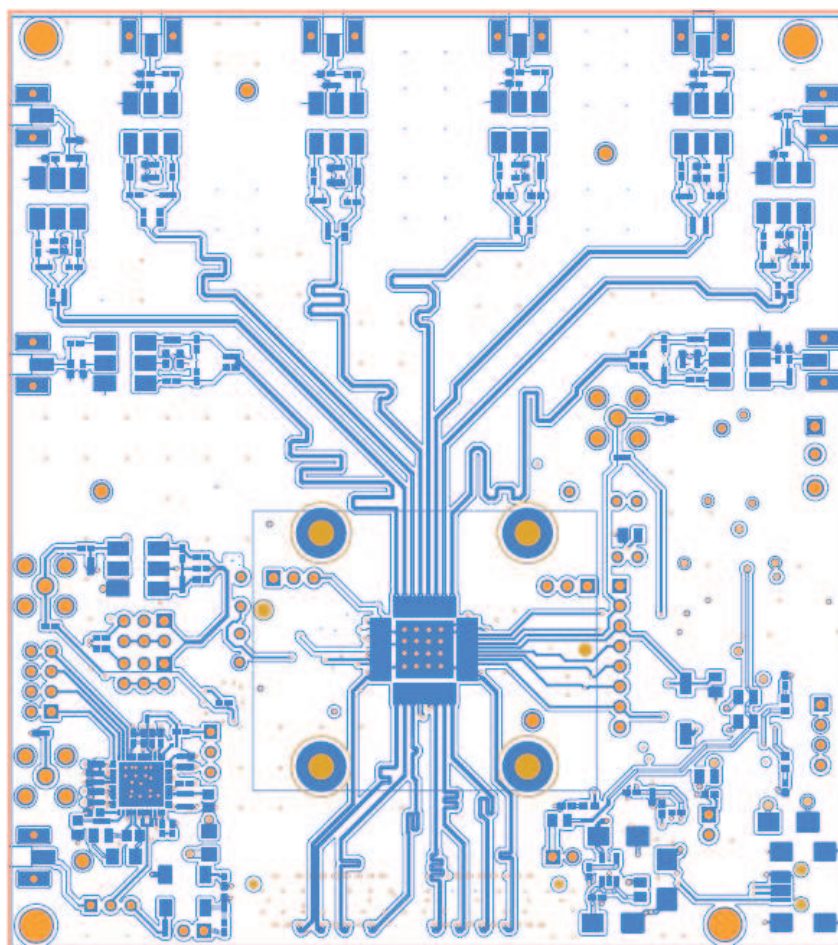


Figure 20. Top Layer Signal



Figure 21. Inner Layer 1 Ground

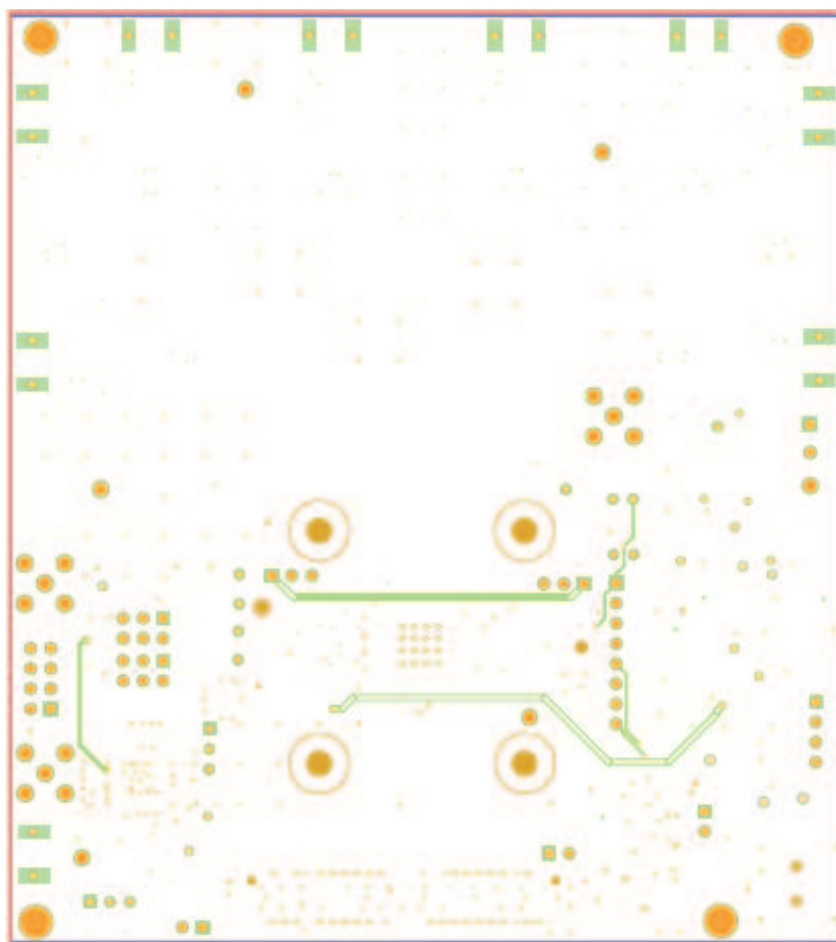


Figure 22. Inner Layer 2 Signal

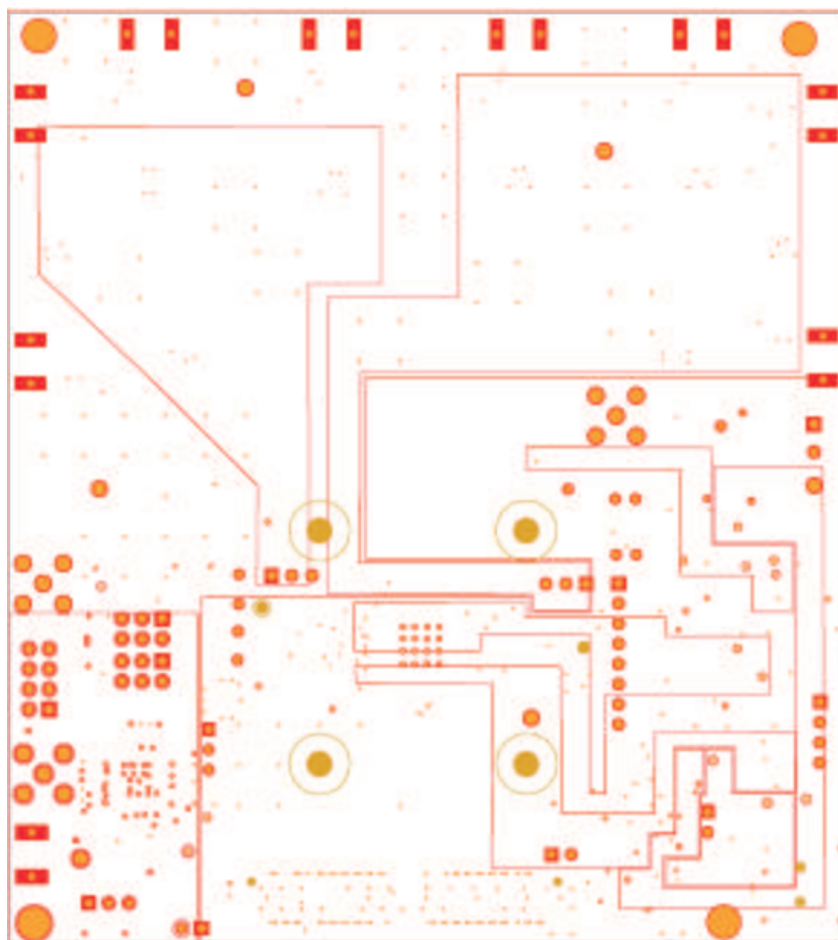


Figure 23. Inner Layer 3 Power

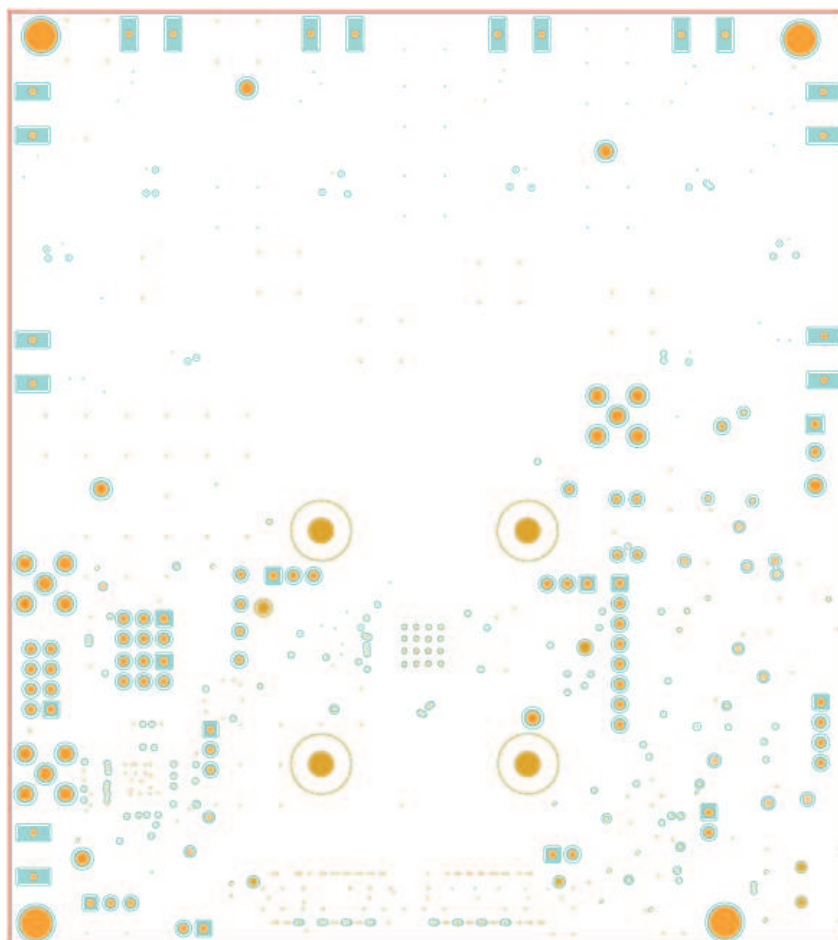


Figure 24. Inner Layer 4 Ground

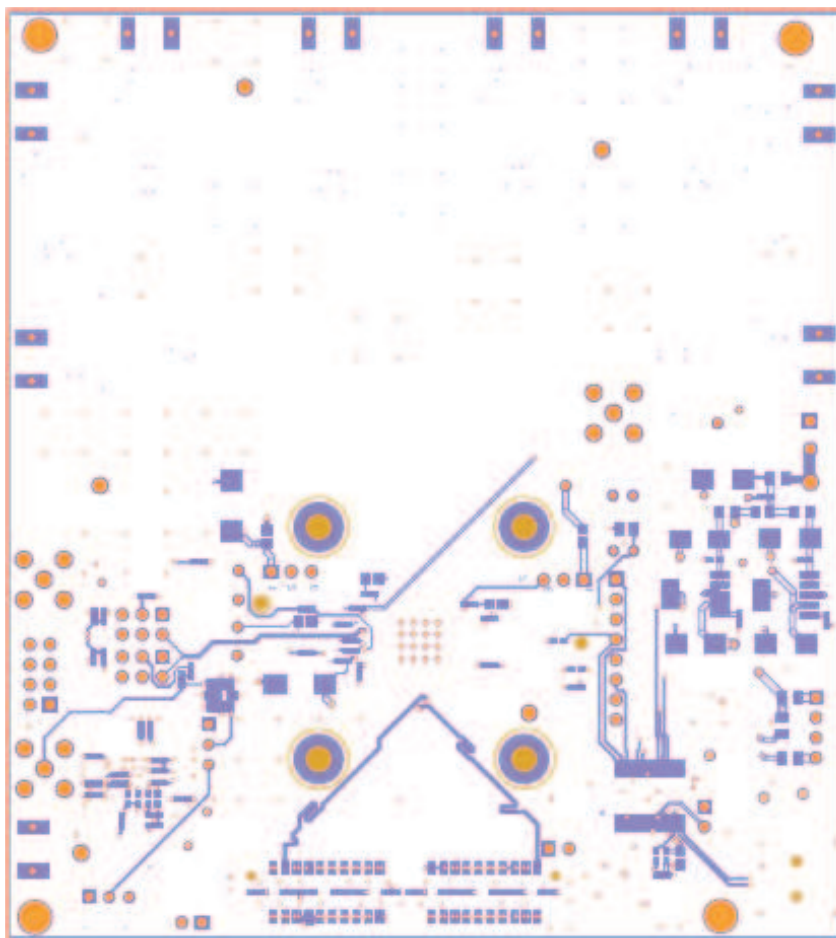


Figure 25. Bottom Layer Signal

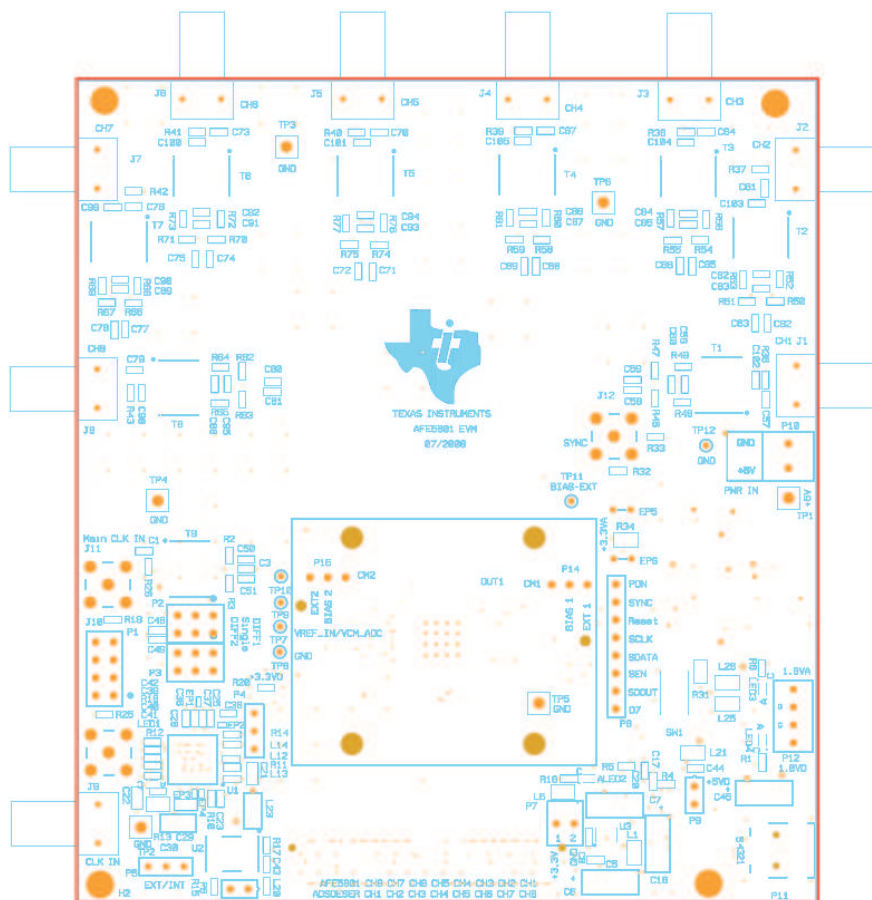


Figure 26. Top Silk Screen Layer

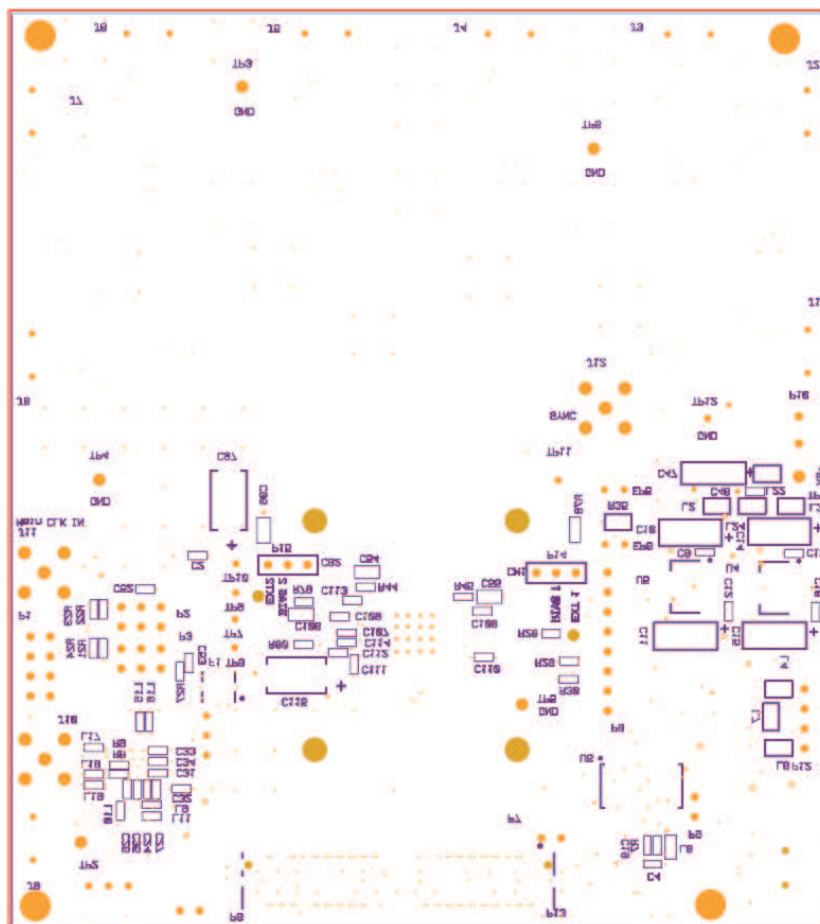


Figure 27. Bottom Silk Screen Layer

4.3 Bill of Materials

ITEM	MFG	MFG PART#	REF DES	VALUE or FUNCTION
1		UNINSTALLED	C98–C105	Capacitor, SMT, 0402 Uninstalled
2	Kemet	C0402C104K8PAC	C1–C5, C8, C9, C12, C13, C16, C17, C19, C20, C24–C28, C31–C44, C46, C48–C53, C56–C95, C107–C114	Capacitor, SMT, 0402, Ceramic, 0.1µF, 10V, 10%, X5R
3	Murata	GRM155R60J225ME15D	C23	Capacitor, SMT, 0402, Ceramic, 2.2 µF, 6.3V, 20%, X5R
4	Panasonic	ECJ-1VB0J475K	C29	Capacitor, SMT, 0603, Ceramic, 4.7 µF, 6.3V, 10%, X5R
5	Panasonic	ECJ-1VB1A105K	C54, C55, C96, C106	Capacitor, SMT, 0603, Ceramic, 1.0 µF, 10V, 10%, X5R
6	Taiyo Yuden	JMK107BJ106MA-T	C21, C22	Capacitor, SMT, 0603, Ceramic, 10 µF, 6.3V, 20%, X5R
7	Murata	GRM31CR60J476ME19B	C30	Capacitor, SMT, Ceramic, 1206, 47 µF, 6.3V, 20%, X5R
8	Vishay Sprague	293D106X5035D2T	C97, C115	Capacitor, TAN, SMT, 10uF, 35V, ±5%, –55–85C
9	AVX	TPSC226K016R0375	C6, C7, C10, C11, C14, C15, C18, C45, C47	10%, 16V, 22µF
10	Samtec	SMA-J-P-X-ST-EM1	J1–J9	SMA Jack, Edge mount, 062PCB, Brass/Gold, Straight, 50 Ω
11	Samtec	SMA-J-P-H-ST-TH1	J10–J12	SMA Coax straight PCB Jack, SMT, 175TL, 50 Ω, Gold
12	KYCON	KMBX-SMT-5S-S-30TR	P11	USB Connectors MINI-USB B-Type SCKT
13	Samtec	QTH-040-01-L-D-DP-A	P13	Connector, SMT, 80P, 0.5mm, FEM, DIFF Pair, Receptacle, 168H
14	Epson Toyocom	HF-372A	F1	(Customer Supply) Crystal filter miniature radio Equipment/IF
15	TI	CDCE62005	U1	CDCE62005 UNINSTALLED. TI supply
16	Not Installed	PAD0201(UN)	EP2, EP3	(Uninstalled Part) Empty pad, SMT, 0201
17	Murata	BLM15BD102SN1D	L9–L20	Ferrite bead, SMT, 0402, 1kΩ, 200 mA
18	Murata	BLM18EG601SN1D	L8	Ferrite bead, SMT, 0603, 600 Ω at 100 MHz, 25%, 800 mA
19	Steward	HI0805R800R-00	L1–L7, L21, L22, L24–L26	Ferrite, SMT, 0805, 80 Ω at 100 MHz, 5 A
20	Steward	LI1206H151R-00	L23	Ferrite, SMT, 1206, 150 Ω at 100 MHz, 0.8 A
21	Molex	39357-0002	P10	Header, THRU, Power, 2P, 3.5MM, Eurostyle
22	Samtec	SSQ-104-02-F-D	P1	Header, THU, 8P, 2X4, 100LS, FEM, VERT, 194TL
23	Samtec	TSW-103-08-G-D	P2, P3	Header, THU, 6P, 2X3, male, dual row, 100LS, 200TL
24	Tyco Electronics	103321-2	P6, P9	Header w/shunt, 2P, 100LS
25	Molex	22-23-2021-P	P7	MALE, 2PIN, 0.100CC w/ friction lock
26	Mill-Max	350-10-103-00-006	P4, P5	Header, THU, MAL, 0.1LS, 3P, 1X3, 284H, 110TL
27	Molex	22-23-2041	P12	4P, VERT, Friction lock
28	Samtec	TSW-108-05-G-S	P8	Header, THU, 8P, 1X8, male, single row, 100LS, 130TL
29	TI	TPS79618DCQR	U5	Ultralow-noise HI PSRR Fast RF 1-A LDO Linear regulator, 1.8V
30	TI	TPS79633DCQR	U4	Ultralow-noise HI PSRR Fast RF 1-A LDO Linear regulator, 3.3V
31	TI	TPS79318DBV	U3 (UNINSTALLED)	1.8V, Ultralow-noise HI PSRR Fast RF 200 mA LDO Linear regulator
32	Future Technology Device Int.	FT245RL	U6	USB FIFO IC Incorporate FTDICHIP-ID Security dongle
33	Any	JUMPER, 2P 0.100cc	EP5, EP6	Installed any brand 2PIN THU Jumper
34	Any	JUMPER, 3P 0.100cc 123	P14, P15	Installed jumper, THU, 3P 0.100cc, 123
35	Panasonic	LNJ308G8PRA	LED1, LED4	LED, SMT, 0603, pure green, 2.03V
36	Panasonic	LNJ808R8ERA	LED2, LED3	LED, SMT, 0603, orange, 1.8V

ITEM	MFG	MFG PART#	REF DES	VALUE or FUNCTION
37	ECS	ECS-3953M-400-BN	U2	OSC, SMT, 3.3V, 50ppm, -40–85C, 5nS, 40.000 MHz
38	Vishay	CRCW04021002F100	R28, R29, R30	Resistor, SMT, 0402, 10K, 1/16W, 1%, 100ppm
39	Panasonic	ERJ-2GE0R00X	R8, R10–R12, R15, R19, R20, R32, R44, R45, R48, R49, R52, R53, R56, R57, R60, R61, R64, R65, R68, R69, R72, R73, R76, R77, R79, R80	Resistor/jumper, SMT, 0402, 0 Ω , 5%, 1/16W
40	Panasonic	ERJ-2GEJ0000(UN)	R5, R7, R9, R14, R17, R18	(UNINSTALLED PART)
41	Panasonic	ERJ-2GEJ131	R21, R22	Resistor, SMT, 0402, thick film, 5%, 1/16W, 130
42	Panasonic	ERJ-2GEJ49R9(UN)	R25, R36–R43	(UNINSTALLED PART)
43	Panasonic	ERJ-2GEJ820	R23, R24	Resistor, SMT, 0402, thick film, 5%, 1/16W, 82
44	Panasonic	ERJ-2RKF1000X	R2, R3	Resistor, SMT, 0402, 100 Ω , 1%, 1/16W
45	Panasonic	ERJ-2RKF1001X	R4	Resistor, SMT, 0402, 1.00K, 1%, 1/16W
46	Panasonic	ERJ-2RKF25R5X	R46, R47, R50, R51, R54, R55, R58, R59, R62, R63, R66, R67, R70, R71, R74, R75	Resistor, SMT, 0402, 25.5 Ω , 1%, 1/16W
47	Panasonic	ERJ-2RKF3320X	R1, R6, R16	Resistor, SMT, 0402 332 Ω , 1%, 1/16W
48	Panasonic	ERJ-2RKF49R9X	R26, R27, R33	Resistor, SMT, 0402, 49.9 Ω , 1%, 1/16W
49	Panasonic	ERJ-3GSYJ100	R78	Resistor, SMT, 0603, 5%, 1/10W, 10
50	Vishay	CRCW08051002F	R31, R34, R35	Resistor, SMT, 0805, thick film, 1%, 1/8W, 10.0K
51	Panasonic	ERJ-6RQF5R1V	R13	Resistor, SMT, 0805, 1%, 1/8W, 5.1 Ω
52	Panasonic	ERJ-1GE0R00C	EP1, EP4	Resistor, SMT, 0201, thick film, 0 Ω , 5%, 0 Ω Jumper, 1/20W
53	AFE5801	AFE5801	DUT1	AFE5801 Analog Front End. TI supplied.
54	ITT Industries	PTS635SK25SM	SW1	Switch, SMT, 2P, SPST-NO, 2.5mm Height, MOM, rectangular, 0.05A, 12V
55	Keystone Electronics	5005	TP1	Testpoint, THU, compact, 0.125LS, 130TL, red
56	Keystone Electronics	5006	TP2–TP6	Testpoint, THU, compact, 0.125LS, 130TL, black
57	Mini-Circuits	ADTT1-1	T1–T8	RF Transformer 0.03–300 MHz
58	Mini-Circuits	ADT1-6T	T9	RF Transformer wideband, 0.03–125 MHz
59	PEM	KFS2-M2.5	PEM NUTS	UNINSTALLED
60	AMP	531220-2	P6, P9	SHUNT JUMPER 2POS

5 Typical Performance

This chapter provides some typical performance of the AFE5801EVM to assist users to verify their setup. A typical performance plot of the AFE5801 is shown in Figure 28 with 30dB digital gain setting.

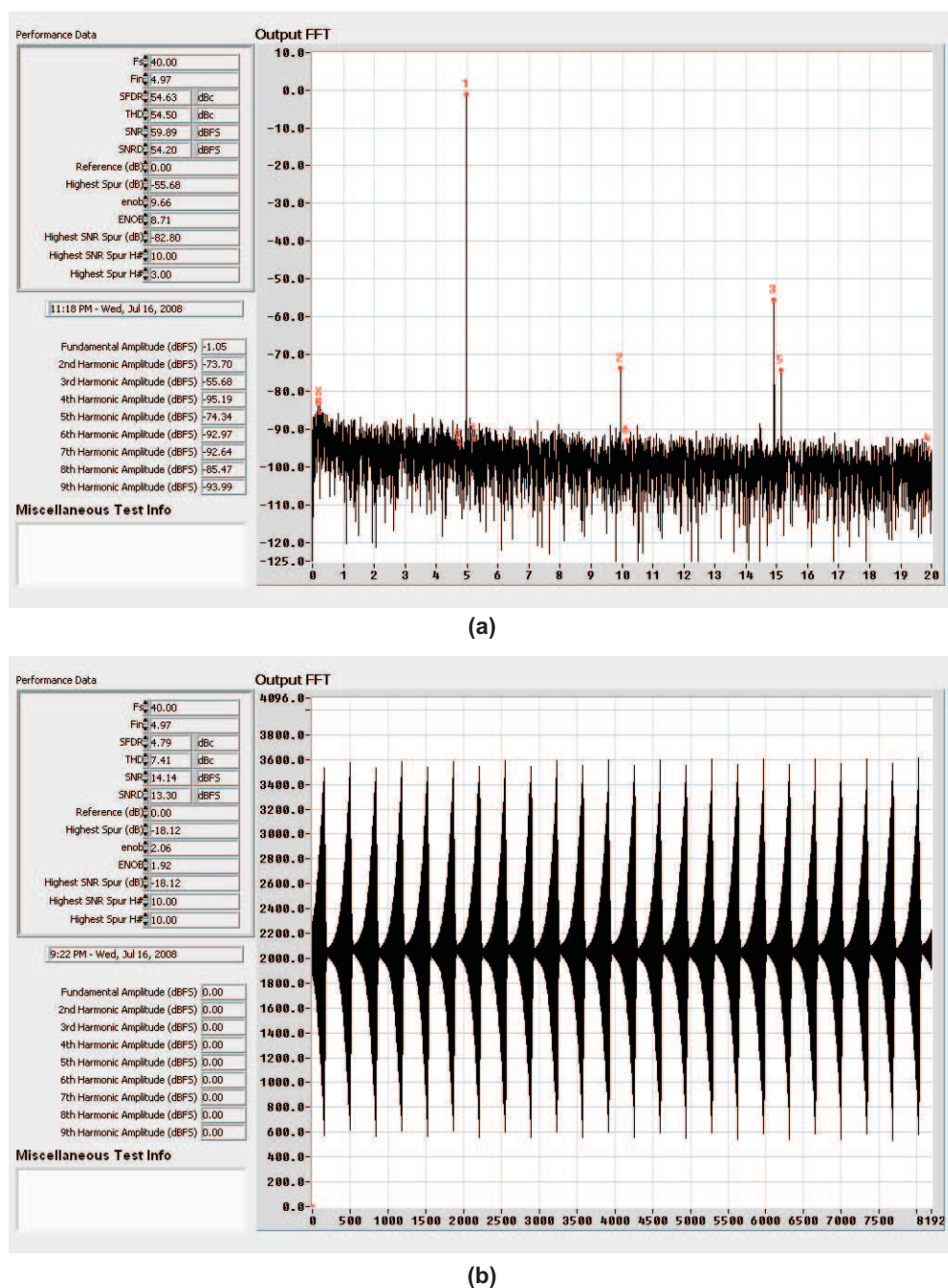


Figure 28. Typical Performance of AFE5801. (a) Fixed Gain Mode; (b) Variable Gain Mode

Appendix A TSW1250 for Evaluating AFE5801

A.1 Introduction

This application report goes through the steps of evaluating the AFE5801 using the TSW1250EVM.

A.2 Hardware Setup

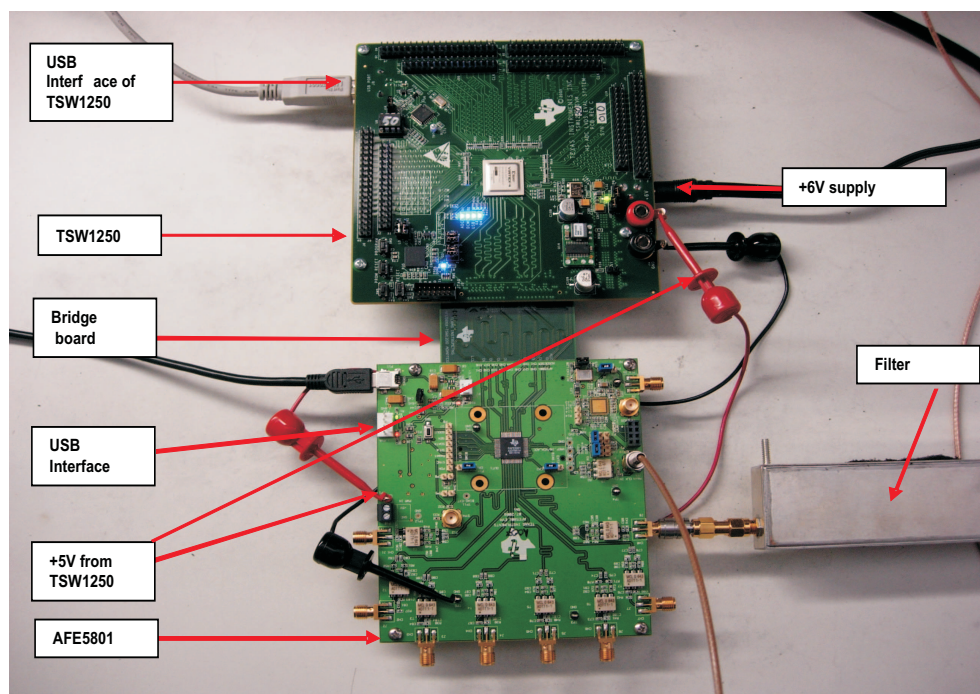


Figure 29. Connection Between TSW1250EVM and AFE5801

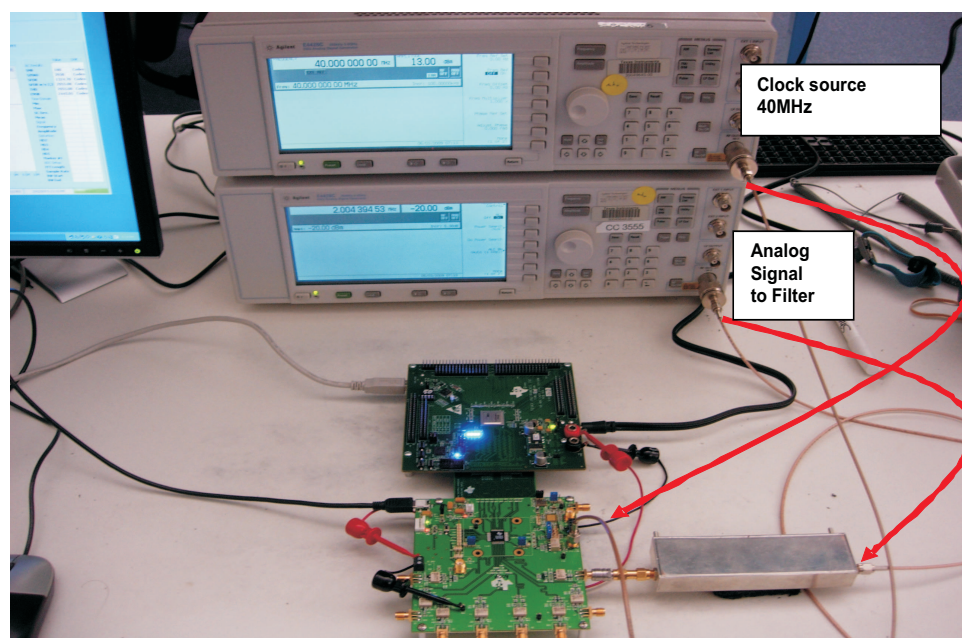


Figure 30. Connection of the Instruments

A.3 Launch AFE5801 GUI

From PC click Start Menu→All Programs→Texas Instruments→AFE5801EVM USB SPI→AFE5801EVM USB SPI

The GUI may be running if the following screen appears:

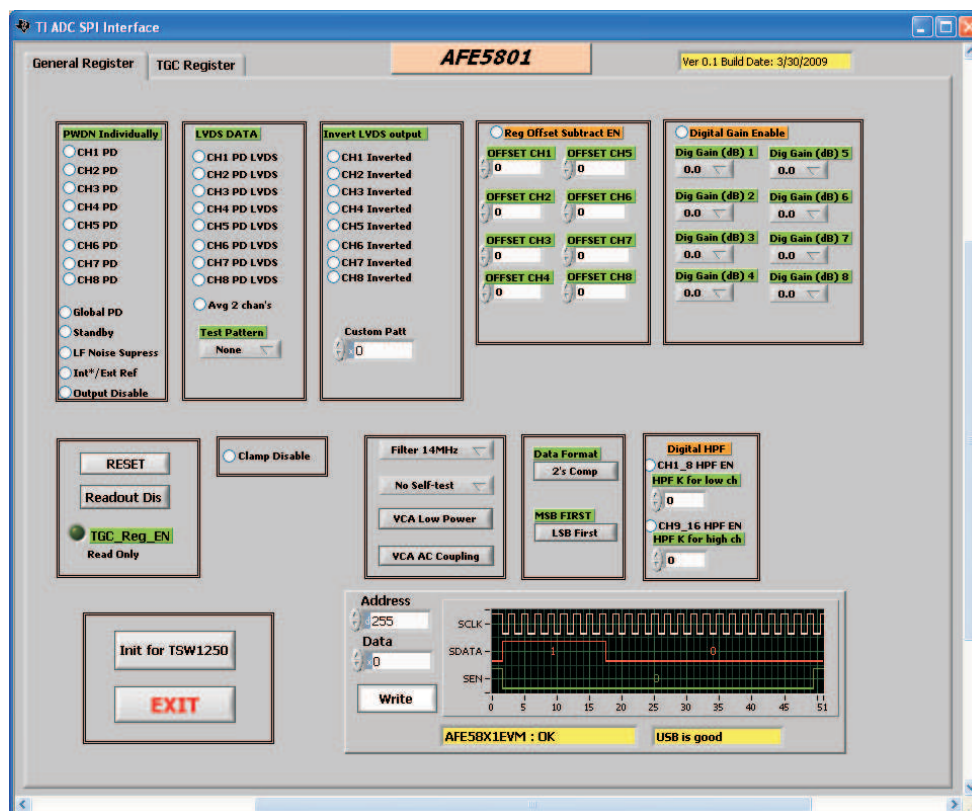


Figure 31. AFE5801EVM GUI - RUN Mode

In case the GUI is not running, then press the START button of the GUI to run it.

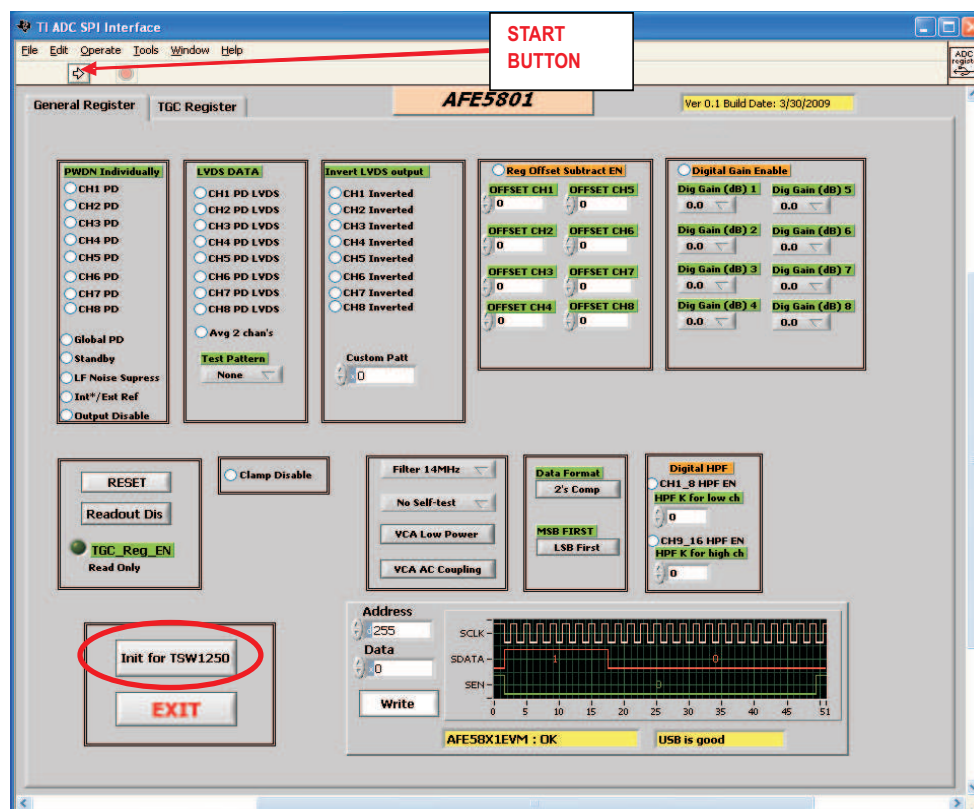


Figure 32. AFE5801 EVM GUI - START Button

• **Commands to the AFE5801 GUI:**

1. Click Init for TSW1250 to set the proper condition to work with TSW1250EVM.
2. Go to "TGC Register " Tab.
3. Press Variable button to change the mode to Fixed.

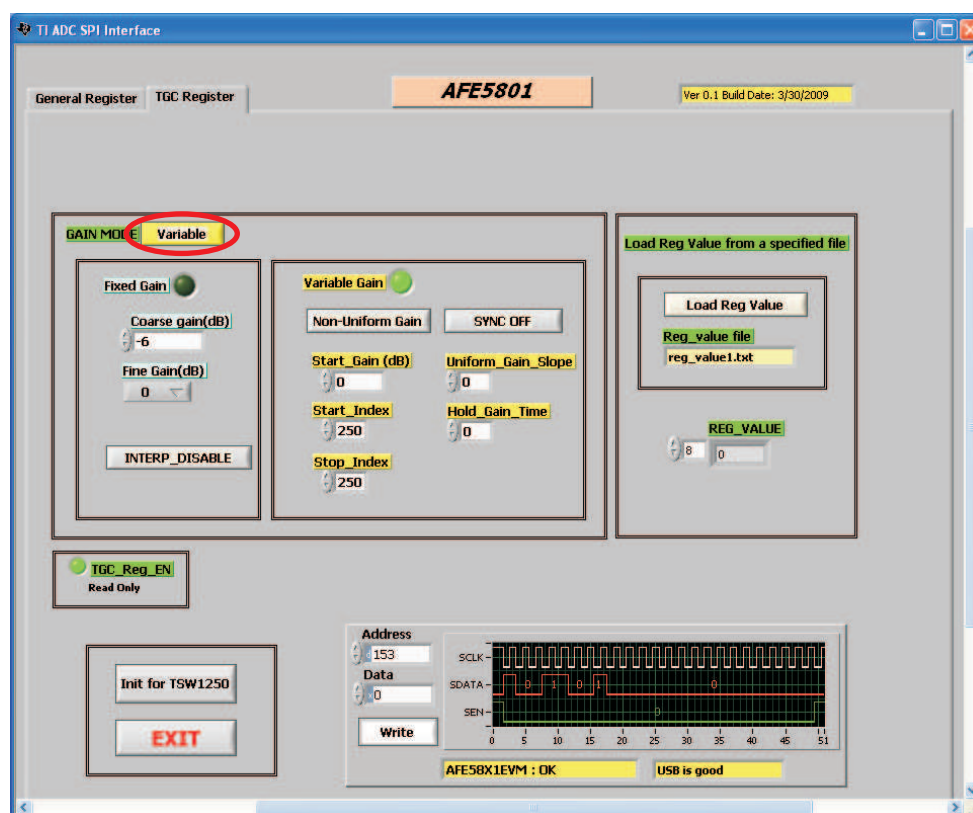


Figure 33. AFE5801EVM GUI - Variable Gain

4. Type 30 and press Write button.

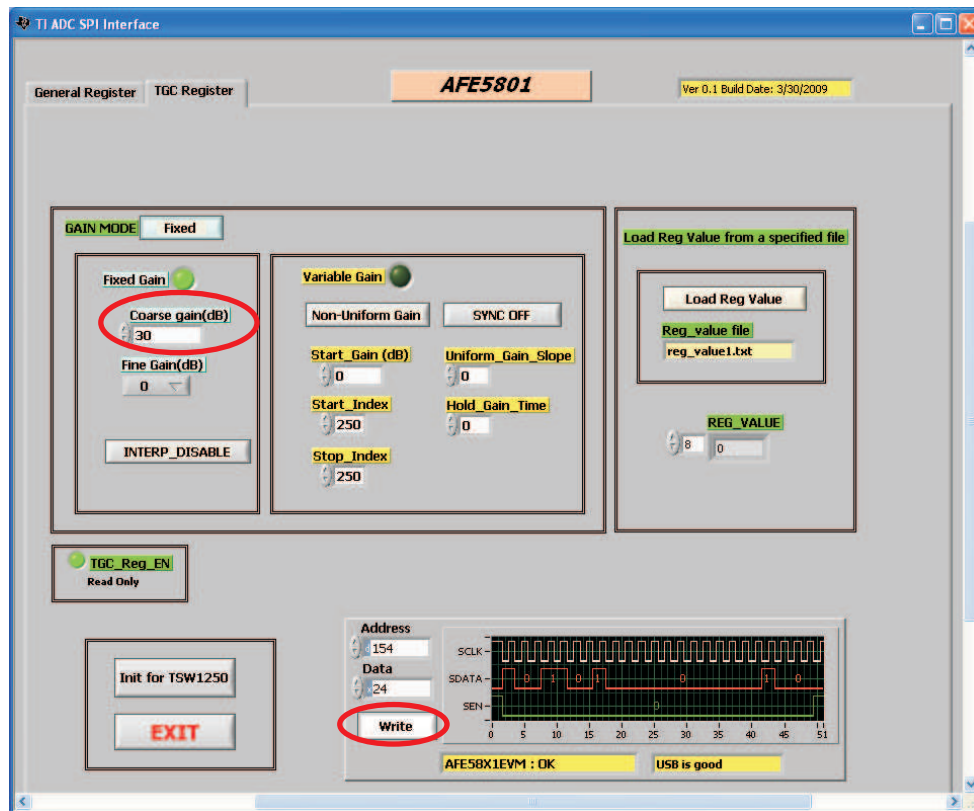


Figure 34. AFE5801EVM GUI - Setting Fixed Gain

At this stage the AFE5801 is ready.

A.4 Launch TSW1250 GUI

- **Graphics User Interface (GUI)**

TSW1250 provides a GUI for users to evaluate the performance of the device. When GUI is started, the screen of the following figure appears. There are five groups of the GUI:

1. Toolbar
2. Message Window
3. Device Specific Selections
4. Test Parameters
5. Central Pane and result data

Items 1, 3, and 4 are used to set up test conditions.

Items 2 and 5 are test results and status.

For details, see the TSW1250 User's Guide included in the CD.

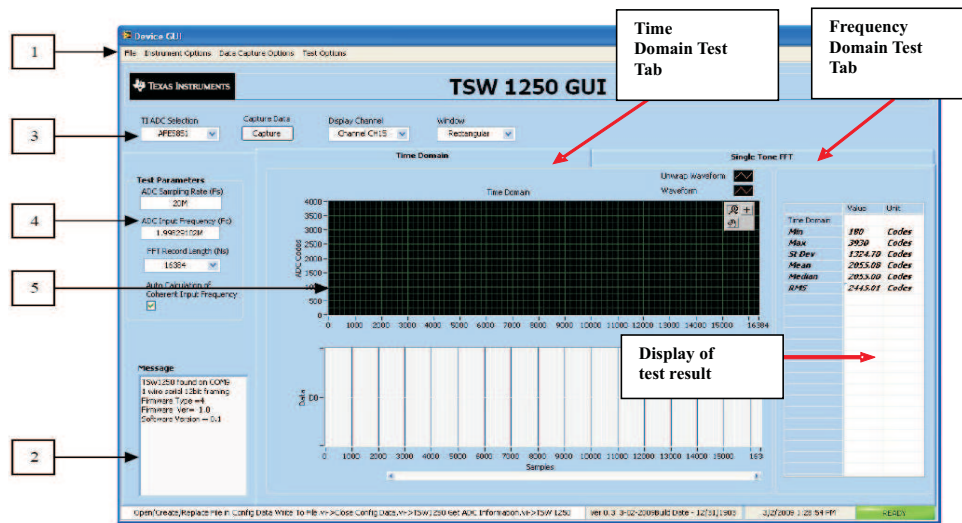


Figure 35. User Interface: Initial Setup Screen

• Test Condition

Perform the steps in the order indicated in the following figure to set the test conditions:

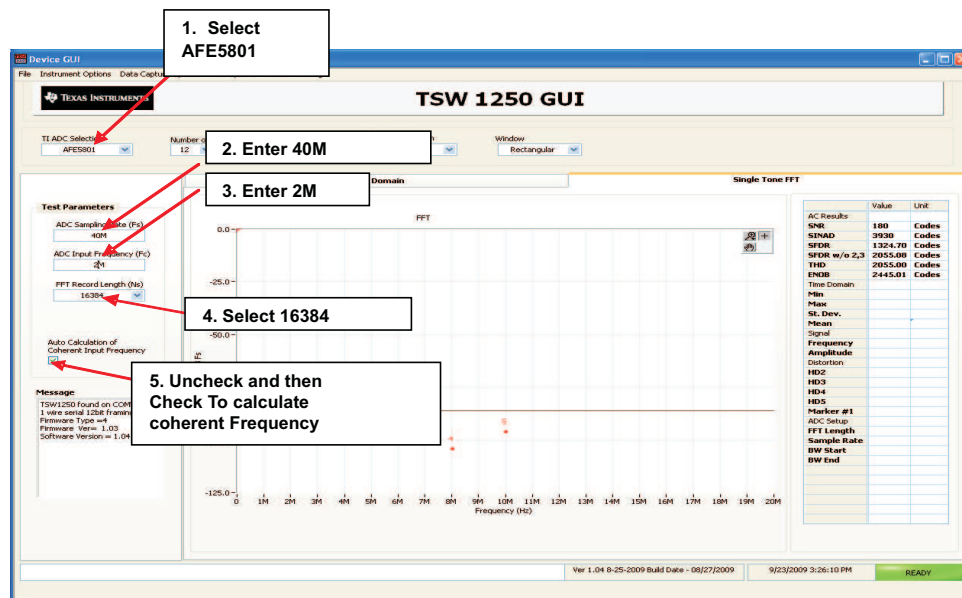


Figure 36. User Interface: Step-by-Step Setup

After completing the five steps indicated, the following figure appears:

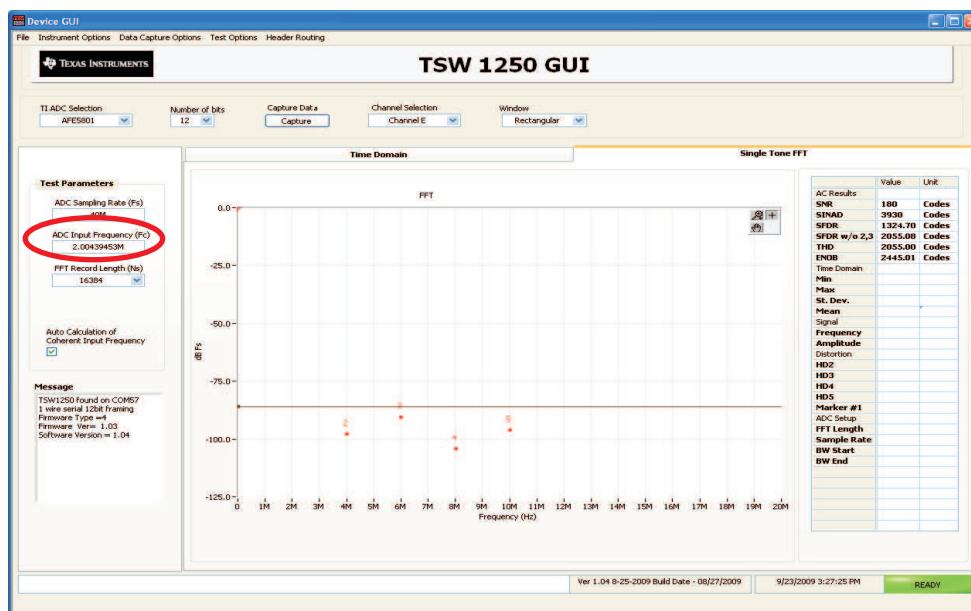


Figure 37. User Interface: Frequency Load Value to Signal Generator

Take the ADC Input frequency, and set the frequency of the signal generator to the noted ADC Input frequency.

Set the Amplitude of the signal generator to -18 to -20 dBm (input amplitude should be between -1dBFS to -3dbFS)

Set the Frequency of the Clock Generator to 40 MHz.

Set the Amplitude of the Clock Generator to 13 dBm.

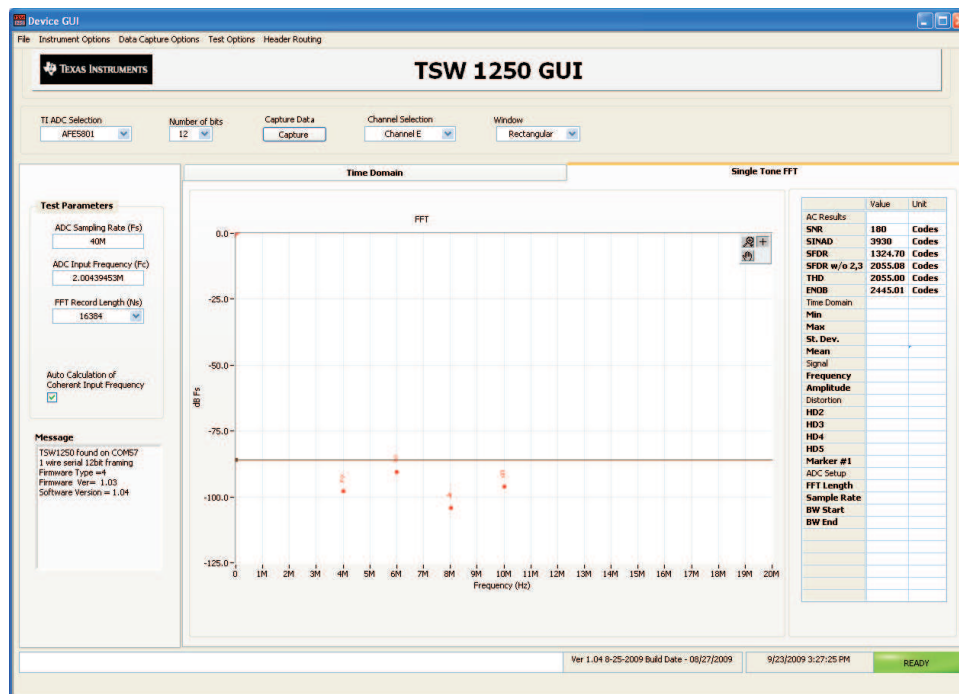


Figure 38. User Interface: Final Setup Screen

Now the user can select the test channel, select the test type by choosing the Single Tone Tab, or Time Domain Tab, and begin testing.

- **Single Tone FFT**

The Single Tone FFT test is shown in [Figure 39](#). The larger central pane displays the FFT power spectrum, whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

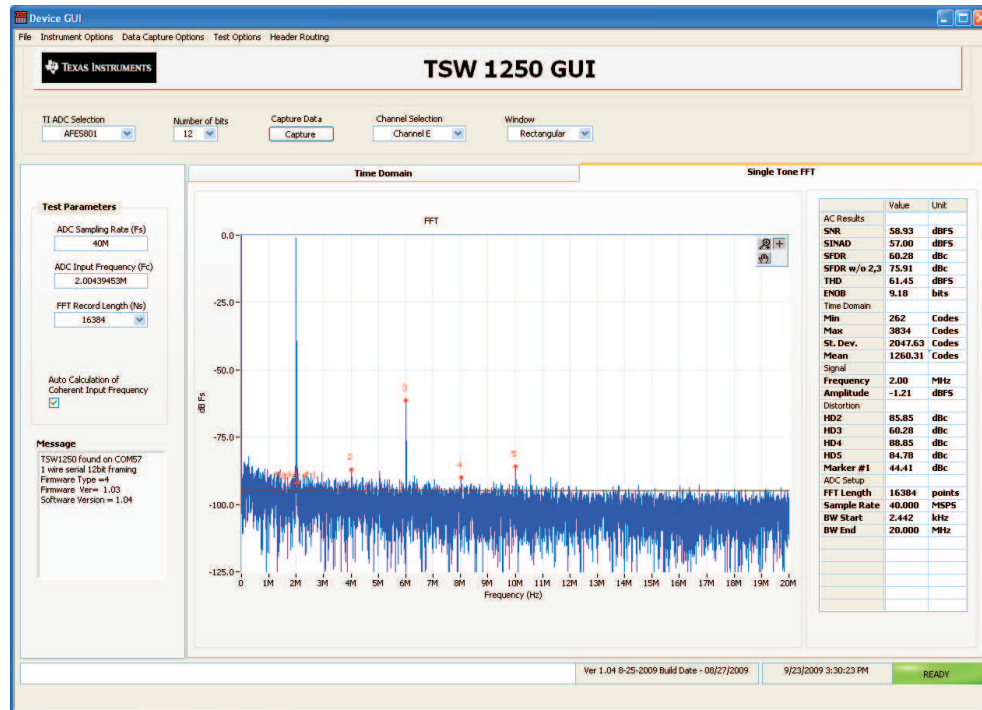


Figure 39. User Interface: Single FFT Format

- **Time Domain**

The Time Domain test is shown in [Figure 40](#). The larger central pane displays the raw sampled data whereas the calculated statistics are grouped into categories on the right of the screen. Settings and inputs relevant to the test are entered in drop-down menus or text input boxes on the left portion of the window.

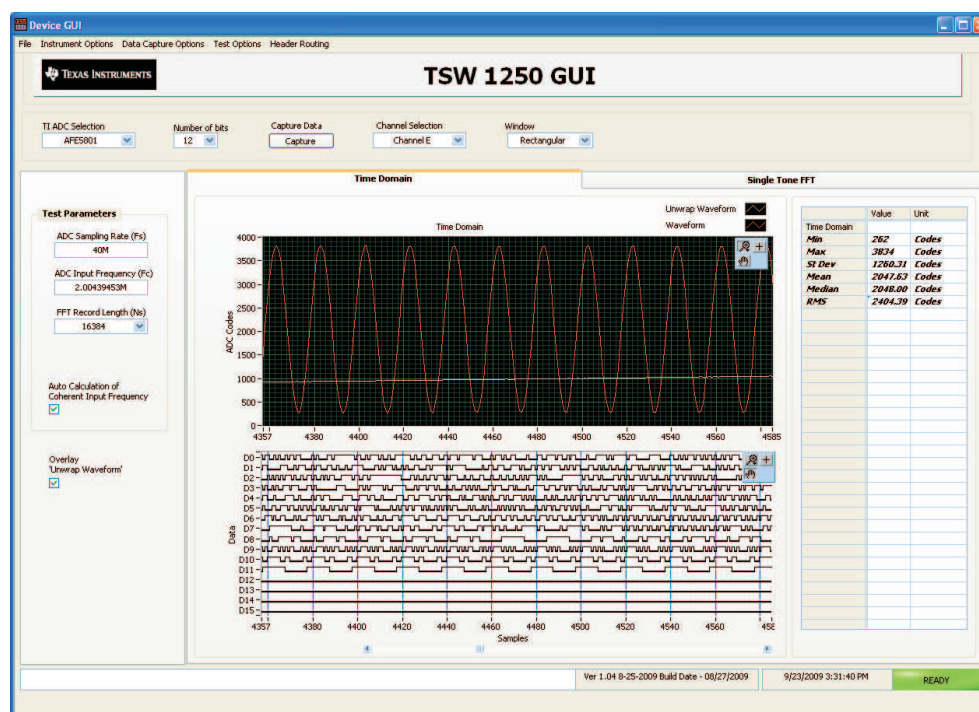


Figure 40. User Interface: Time Domain Format

- **EXCEL**

The raw test sampled data can be saved to a file and processed by EXCEL or some other software.

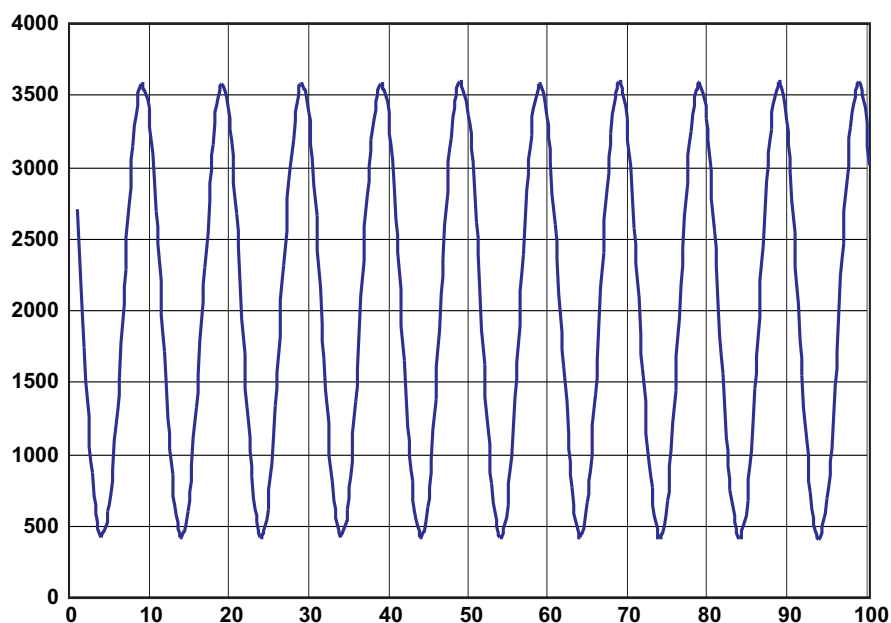


Figure 41. Plot of Saved Sample Data

Appendix B TSW1100 for Evaluating AFE5801

B.1 Introduction

This appendix describes the use of TSW1100 software to analyze data files acquired by logic analyzers.

As mentioned before, coherent sampling is recommended when HP8644s are used. The calculation of coherent sampling rate and signal frequency can be found in the TSW1100 user manual at following website:

<http://focus.ti.com/docs/toolsw/folders/print/tsw1100.html>

Users can set the calculated frequencies for signal generators; acquire ADC data through a logic analyzer; and save the data as a txt file. Typical data file captured by logic analyzer should be modified to the following format (i.e., containing only one column):

```
1981
1615
1292
1046
895
852
927
1113
1394
1737
2110
2477
2798
3044
3196
3237
3162
2978
.
.
.
.
```

The AFE5801 performance analysis can be done as follows:

- First of all, some header information should be added to the modified logic analyzer data file as per the following. Example files were included in the TSW1100 software package. Time, sampling rate, frequency, and 2's complement should be modified based on your setup. An example data file is listed below.

```
TSW1000
2/12/2007 12:38
Bits =12
Sampling Rate =40000000.000
Frequency in =1998291.0156
2s complement =No
Data Format =Decimal
Raw Captured Data:
1981
1615
1292
1046
895
852
927
1113
1394
1737
2110
2477
2798
3044
3196
3237
3162
2978
2702
2358
```

- The TI chip should be selected as TSW1000 in the interface shown in [Figure 42](#).

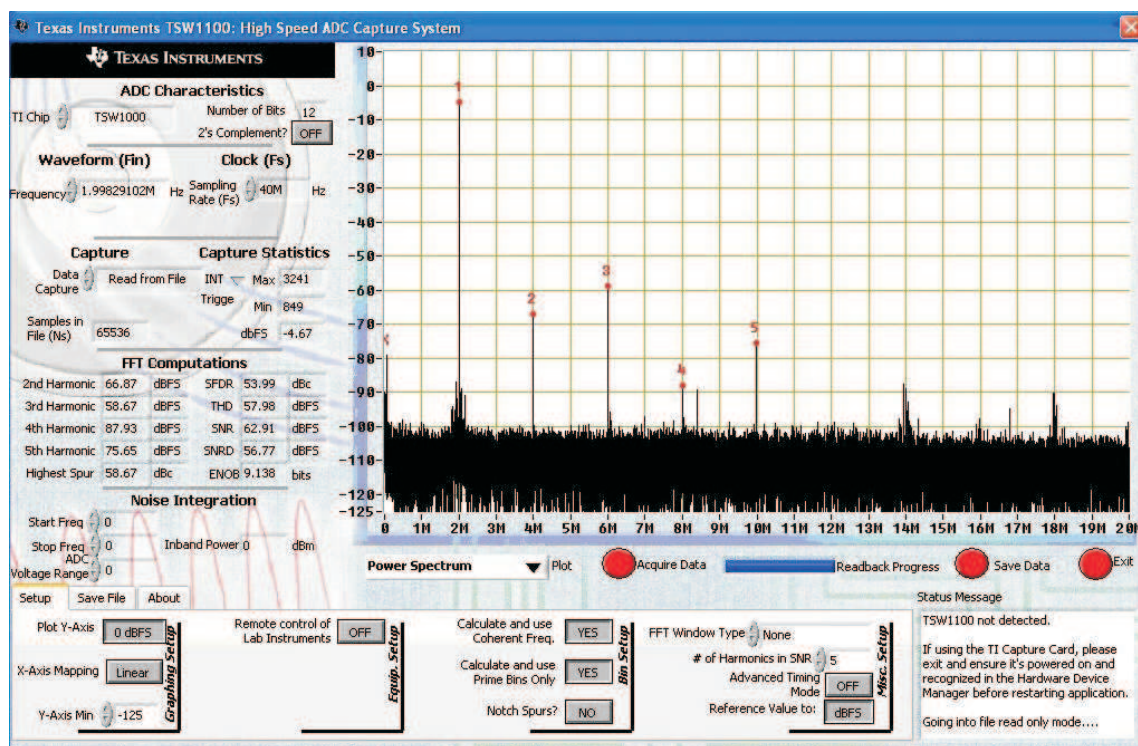
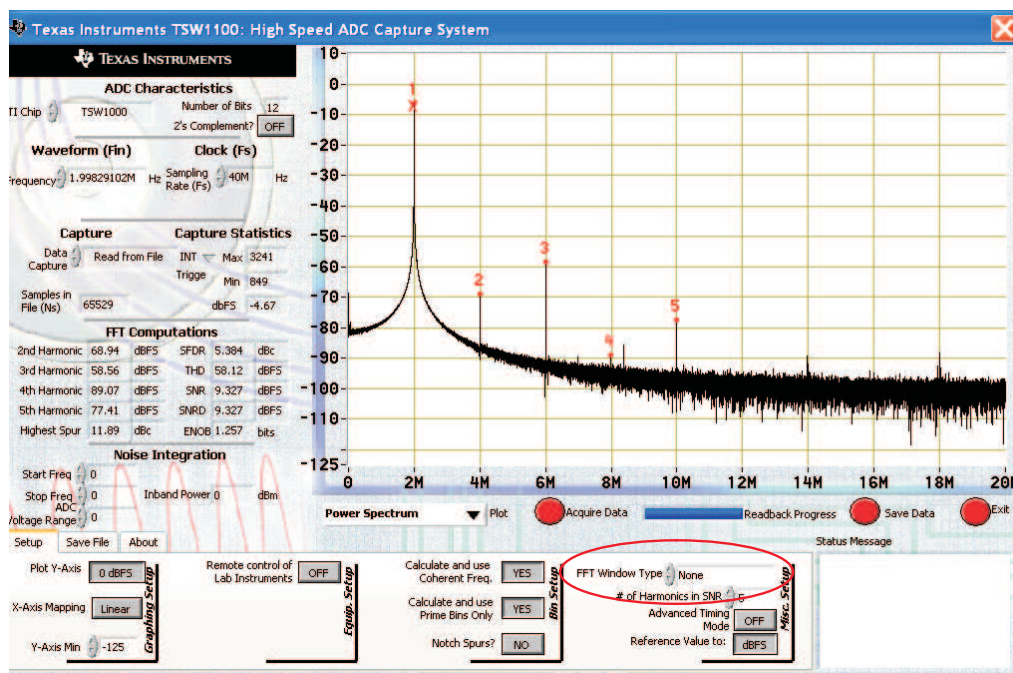


Figure 42. TSW1100 Interface

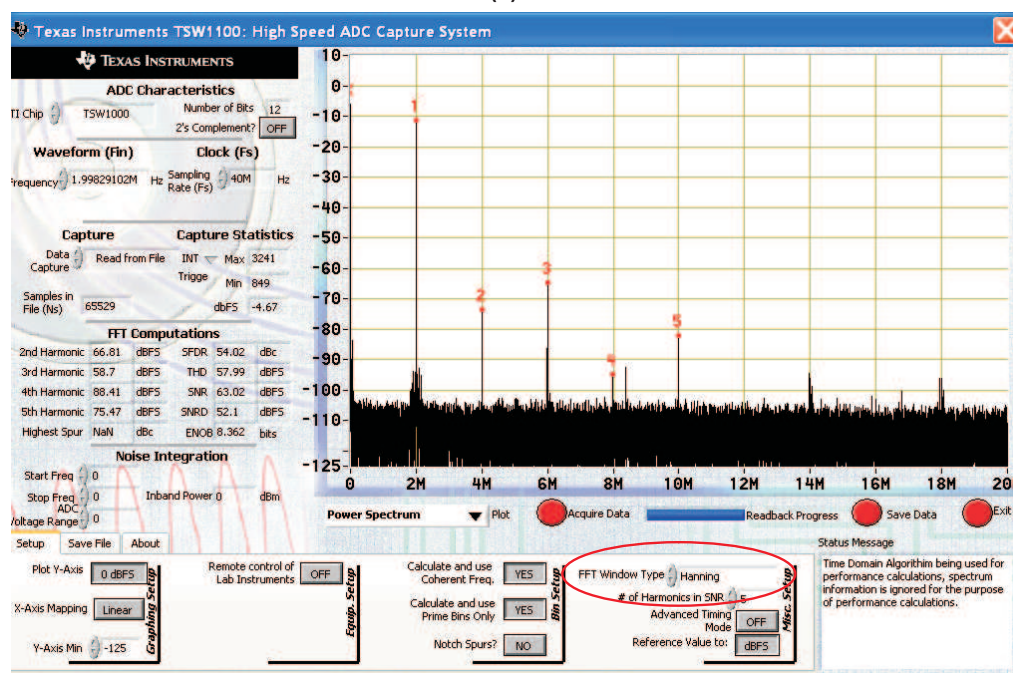
- Finally, users should click *Acquire Data* button, select the txt file with header information, and see the analysis results.
- The 2s complement setting can be changed in the software based on your setting.

TSW1100 also supports to analyze non-coherent sampled data. However some artifacts may be noticed during analysis. Appropriate FFT window must be applied to the data.

Users could follow the steps described above to get the non-windowed analysis results first as show in [Figure 43\(a\)](#). After appropriate FFT window applied, the correct analysis results is shown in [Figure 43\(b\)](#). Note that some DC artifact is noticed in (b).



(a)



(b)

Figure 43. Analysis of Non-Coherent Sampled Data.
(a) No window applied; (b) Hanning window applied.

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During normal operation, some circuit components may have case temperatures greater than . The EVM is designed to operate properly with certain components above as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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