UNITRODE

DV2005L1

Fast Charge Development System

Control of PNP Power Transistor

Features

- bq2005 fast-charge control evaluation and development
- Charge current sourced from two on-board frequency-modulated linear regulators (up to 3.0 A)
- Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells
- Sequential charging of two battery packs
- Fast-charge termination by delta temperature/delta time (ΔT/Δt), negative delta voltage (-ΔV), maximum temperature, maximum time, and maximum voltage
- -ΔV enable, hold-off, top-off,trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- Selectable pulsed "top-off" charge and trickle charge

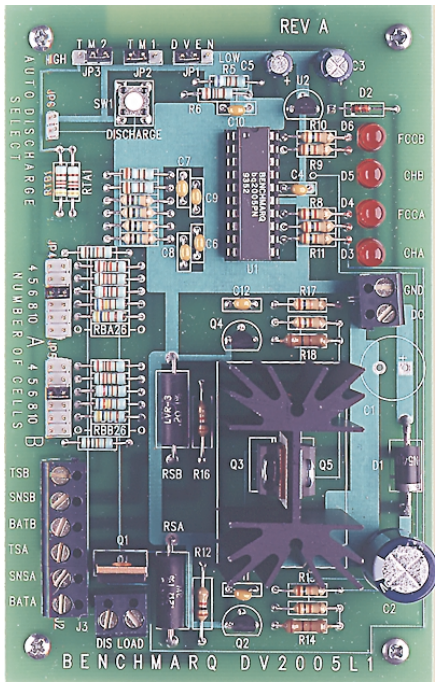
General Description

The DV2005L1 Linear Development System provides a development environment for the bq2005 Dual-Battery Fast-Charge IC. The DV2005L1 incorporates a bq2005 and two frequency-modulated linear regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

Review the bq2005 data sheet and the application note, "Using the bq2005 to Control Fast Charge," before using the DV2005L1 board.

The fast charge is terminated by any of the following: ΔT/Δt, -ΔV, maximum temperature, maximum time, and maximum voltage. Jumper settings select the -ΔV enabled state, and the hold-off, top-off, trickle, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2005L1 for the number of cells, charge termination, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch SW1.



Connection Descriptions

J1

	DC	DC input from charger supply
	GND	Ground from charger supply

J2

	$TS_{A,B}$	Thermistor connection, battery A and B
	$BAT_{A,B}$	Positive battery terminal and high side of discharge load, battery A and B
	$SNS_{A,B}$	Negative battery terminal and thermistor connection, battery A and B

J3	DISLOAD	Discharge load
JP1	DVEN	Negative delta voltage termination enable
JP2	TM_1	TM_1 setting

JP3 TM_2	TM_2 setting
JP4	Select number of cells, battery A
JP5	Select number of cells, battery B
JP6	Automatic discharge select

Fixed Configuration

The DV2005L1 board has the following fixed characteristics:

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector J1 (DC:GND).

LEDs indicate charge status of both battery A and battery B.

Charge initiation is provided on application of DC, which provides V_{CC} to the bq2005, or on installation of the battery following power application.

Pin $\overline{DCMD}_A$ is connected to switch SW1. A toggle of switch SW1 momentarily pulls $\overline{DCMD}_A$ to GND and initiates a discharge-before-charge. Automatic discharge-before-charge can also be achieved by connecting $\overline{DCMD}_A$ directly to GND at JP6. The bq2005 output activates FET Q1, allowing current to flow through an external current-limiting load between battery A and SNS_A at J3 (DISLOAD).

As shipped from Benchmarq, the DV2005L1 linear regulators are configured to a charging current of 1.13A. This current level is controlled by the value of sense resistors RS_A and RS_B by the relationship:

$$I_{CHG} = \frac{0.225V}{RS_{A,B}}$$

The value of RS_A and RS_B at shipment is 0.200Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2005L1 board is 3A for each battery due to the power-dissipation limits of Q2 and Q4. ***Q3 and Q5 must be mounted to an appropriate heat sink.***

Resistors R14/R18 should be selected to divert power dissipation from transistors Q2 and Q4. They are shipped at values of 100Ω ½W. Select appropriate values based on voltage source and fast charge current from Table 1.

With the provided NTC thermistor connected between $TS_{A,B}$ and $SNS_{A,B}$, values are: LTF = 10°C, HTF = 49°C, and TCO = 50°C. The ΔT/Δt settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix on the board as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01

Jumper-Selectable Configuration

The DV2005L1 must be configured as described below.

Jumper Setting	Pin State
[1 2] 3	Enabled (high)
1 [2 3]	Disabled (low)

DVEN (JP1): Enables/disables -ΔV termination (see bq2005 data sheet).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

TM1 and TM2 (JP2 and JP3): Select fast charge safety time/hold-off/top-off (see bq2005 data sheet).

Number of Cells (JP4/JP5): A resistor-divider network is provided to select 4 to 10 cells (the resulting resistor value equals $N/_{2.375}$ – 1 cells). RBA_1 and RBB_1 are 150KΩ resistors, and RBA_2 and RBB_2 (R21–R26) are jumper-selected.

Closed Jumper	Number of Cells
RBA/RBB 26	user-defined
25	10
24	8
23	6
22	5
21	4

Temperature Disable: Connecting a 10KΩ resistor between $TS_{A,B}$ and $SNS_{A,B}$ disables temperature control.

Table 1. Lookup Table for R14/R18 Selection

Input Voltage	Current	Resistance	Wattage
to 15V	1A	100Ω	½W
	2A	100Ω	½W
	3A	62Ω	3W
15–20V	1A	360Ω	½W
	2A	150Ω	2W
	3A	87.5Ω	5W
20–25V	1A	510Ω	½W
	2A	200Ω	2W
	3A	120Ω	5W
25–30V	1A	680Ω	1W
	2A	240Ω	3W
	3A	Not recommended	
30–35V	1.5A	910Ω	1W
	2A	Not recommended	
	3A	Not recommended	

Note: Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 25V.

Setup Procedure

1. Configure DVEN, TM_1, TM_2, and number-of-cells jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between $TS_{A,B}$ and $SNS_{A,B}$.

   Note: $RT_{A1,B1}$ and $RT_{A2,B2}$ match the thermistor provided and must be changed if a different thermistor type is used (see Appendix A in the application note, "Using the bq2005 to Control Fast Charge").
3. If using the discharge-before-charge option, connect a current-limiting discharge load between DIS and LOAD.
4. Attach the battery pack (+) to $BAT_{A,B}$ and (–) to $SNS_{A,B}$. For temperature control, the thermistor must contact the cells.
5. Attach DC current source to DC+ (+) and GND (–) connections in J1.

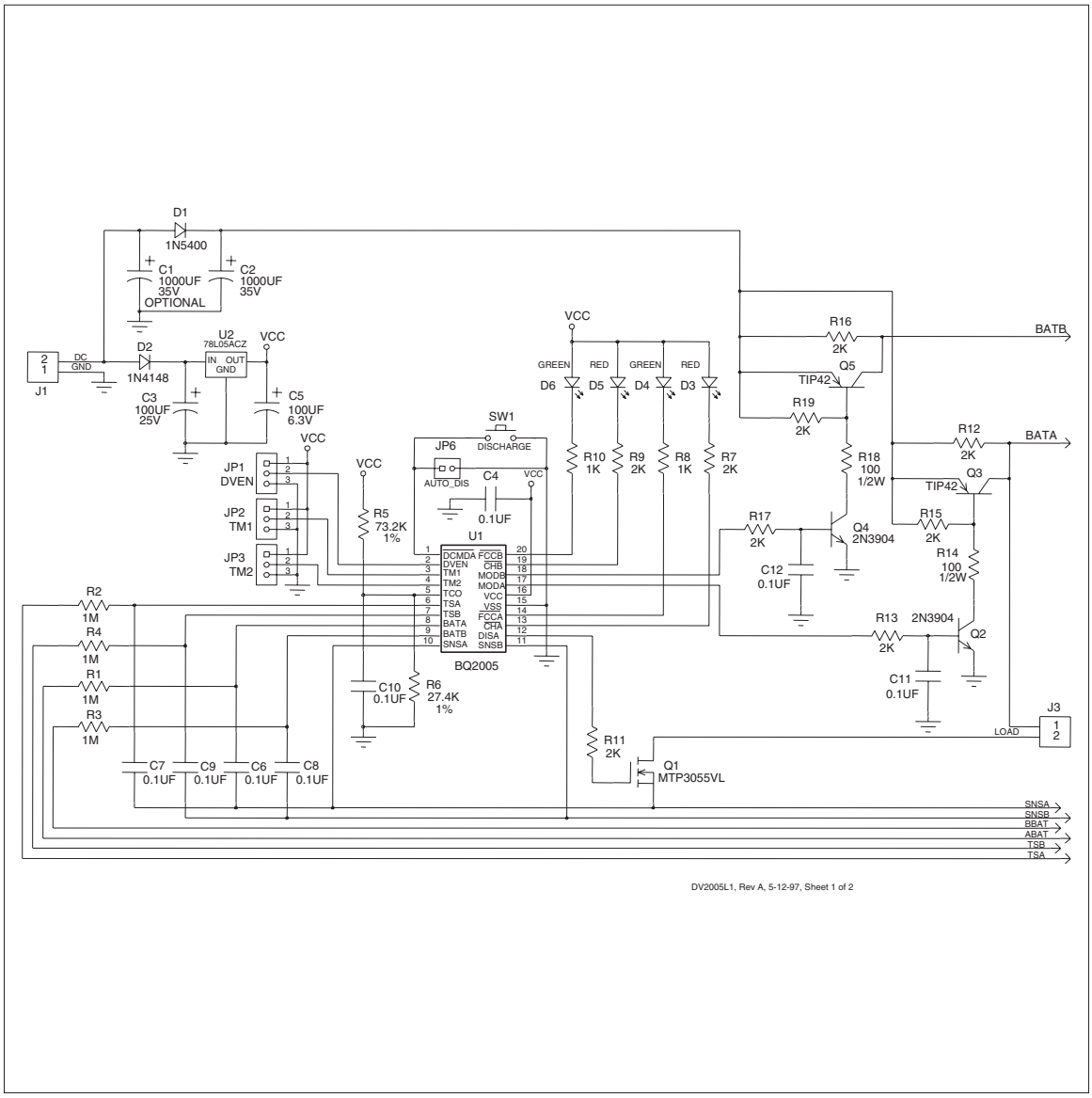
Recommended DC Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC+}	Maximum input current	-	-	3	A	
V_{DC+}	Input voltage	$2.0 + V_{BAT+}$ or 8.5	-	$18 + V_{BAT+}$ or 35	V	Note 1
$V_{BATA/B}$	BAT+ input voltage	-	-	30	V	
V_{THERM}	TSA,B input voltage	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

Note: 1. The voltage at R14/R18 is application-specific and limits the dissipation of Q2/Q4 to a safe limit during Q3/Q5 conduction. See Table 1 for recommended R14, R18 selections per V_{DC+} and I_{CHARGE}.

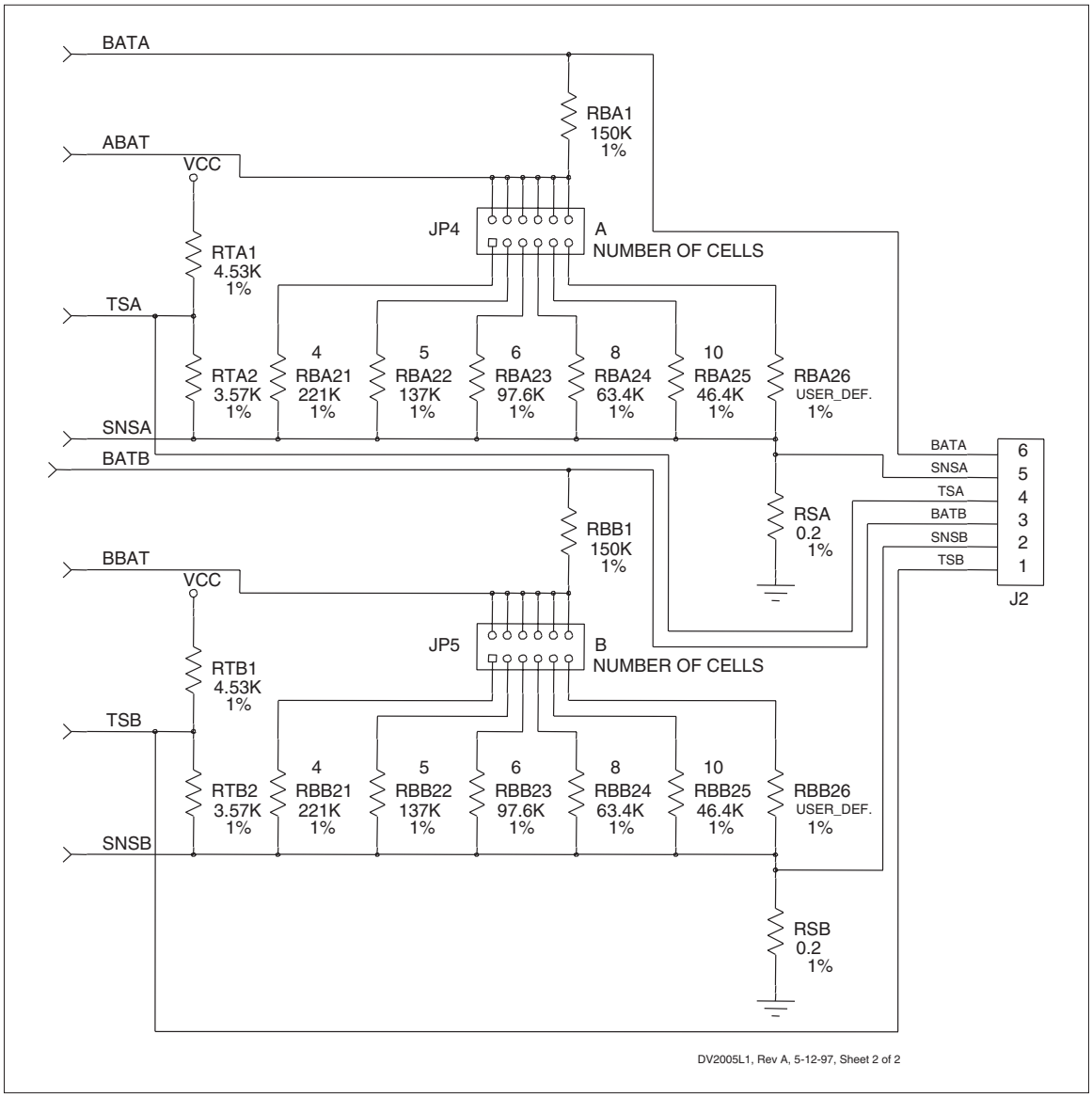
Rev. A Board

DV2005L1 Board Schematic



Rev. A Board

DV2005L1 Board Schematic Continued



Rev. A Board

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