bq77910EVM

The bq77910EVM-001 evaluation module (EVM) is a complete evaluation system for the bq77910, a four- to ten-cell Li-ion battery protection integrated circuit. The EVM consists of a bq77910 circuit module and a resistor cell simulator module which can be used for simple evaluation of the bq77910 functions. The circuit module includes one bq77910 integrated circuit (IC), sense resistor, power FETs and all other onboard components necessary to protect the cells from overcharge, over discharge, short circuit, and over current discharge in a 10 series cell Li-ion or Li-polymer battery pack. The circuit module connects directly across the cells in a battery. With a compatible interface board and Windows™-based PC software, the user can view the bq77910 registers and program the IC configuration and protection limits.

Contents

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1 Features

- Complete evaluation system for the bq77910 four to ten series cell lithium-ion or lithium-polymer battery protector
- Populated circuit module for 10 cell parallel FET configuration for quick setup
  - Pads for components for configuration of additional cell counts and series FETs
- Power connections available on terminal blocks or banana jacks
- Control and status signals available on terminal blocks
- Resistor cell simulator for quick setup with only a power supply
- PC software available for configuration

1.1 Kit Contents

- bq77910 circuit module
- Resistor cell simulator
- Set of support documentation

Table 1. Ordering Information

EVM Part Number	Chemistry	Configuration	Capacity
bq77910EVM-001	Li-ion	10 cells	Any

NOTE: Although capacity is show as "Any", practical limits of the physical construction of the module will typically limit the operation of the EVM to a 1P or 2P battery construction. Refer to the physical construction section for board details.

1.2 Required equipment

The following equipment is required to operate the bq77910 EVM in a simple demonstration

- DC power supply, 0-43V at 0.5A
- DC voltmeter or oscilloscope,
- DC power supply, ~3V at .1A or an approximately 15k ohm 1/4W resistor
- Test leads to connect equipment

The following equipment is required to operate the bq77910 with a more extensive demonstration

- TI USB-TO-GPIO interface adapter
- Computer with USB port and compatible Windows 32 bit operating system
- Electronic load
- Additional power supplies
- TI bq77910GUI Evaluation Software - refer to the software installation section

2 bq77910 Circuit Module and Interfaces

The bq77910 circuit module contains the bq77910 IC and related circuitry to demonstrate the features of the IC. A FET with heatsink is provided for the high current discharge path. A lower current FET is provided for the charge path. A thermistor provides temperature sensing for the device. Other components provide support for the IC and connections to the board.

2.1 Circuit Module Connections

Connections are provided for the following interfaces:

- Direct cell connections
- PACK connections

- Programming interface

2.2 Signal Descriptions

Signals available on the EVM are described in this section. For details on the location and connector types, refer to the physical construction section. High current signals can be connected at either the terminal block or banana jack. Refer to the physical construction section for identification.

Cell connections are described in Table 2. The default board assembly supports only 5 cells, so the upper cell connections are not used. CELL0 and CELL5 are connected to the high current paths on the board through zero ohm resistors. This allows operation of the resistive cell simulator without external connections. If the on-board resistors are removed, connections must be made off the board. Refer to the physical construction section for resistor identification. Cell connection sequence is described in Section 3.6.

Table 2. Cell Connections

Reference Designator	Pin Number	Signal	Description
J13, J15	All	BATT–	Negative electrode of first (bottom) cell, high current connection
J5	6	CELL0	Negative electrode of first (bottom) cell, optional separate monitor connection to cell
	5	CELL1	Positive electrode of first (bottom) cell
	4	CELL2	Positive electrode of second cell
	3	CELL3	Positive electrode of third cell
	2	CELL4	Positive electrode of fourth cell
	1	CELL5	Positive electrode of fifth cell,
J4	5	CELL6	Positive electrode of sixth cell
	4	CELL7	Positive electrode of seventh cell
	3	CELL8	Positive electrode of eighth cell
	2	CELL9	Positive electrode of ninth cell
	1	CELL10	Positive electrode of tenth cell, optional separate monitor conneciton to cell
J10, J11	All	PACK+	Most positive cell output, high current connection, shared with PACK+

Load connections are described in Table 3.

Table 3. PACK Connections

Reference Designator	Pin Number	Signal	Description
J10, J11	All	PACK+	Positive output of evaluation board, shared with the battery high current connection
J12, J14	All	DSG–	Negative output of evaluation board for discharge
J16, J17	All	CHG–	Negative input to evaluation board for charge

Programming signals are described in Table 4. J3 signals are 3.3V logic level.

Table 4. Programming Interface Connections

Reference Designator	Pin Number	Signal	Description
J3	1, 2, 5, 7, 8		Not used
	3	PGM	Control signal for EEPROM programming voltage.
	4	ZD	Control signal for device ZEDE
	6	GND	Signal reference for the IC
	9	ECLK	Serial interface clock connection
	10	EDATA	Serial interface data connection
J2	1	14V	Regulated 14V input for IC programming
	2	GND	Signal reference for the IC

Test header or pattern signals are described in Table 5.

Table 5. Test Header Signals

Reference Designator	Useage	Pin Number	Signal	Description
J1	Default: shunt installed for normal operation. Remove shunt for U1 supply current measurement	1	Battery feed	Power feed to 100 ohm shunt resistor
		2	BAT	Output of 100 ohm shunt resistor to IC BAT pin
J6	Default: no shunt. Install shunt to hold ZEDE high	1	VREG	IC regulator output
		2	ZEDE	IC zero delay test point and input pin, also connected to J3
		3	PD	Pull down resistor for strong pull down of ZEDE if required
J8	Not populated. Alternate test point or remote thermistor connection	1	TS	IC temperature sense pin
		2	GND	Signal reference for the IC

Control and status signals are provided on terminal blocks. These signals are described in Table 6.

Table 6. Control and Status Connections

Reference Designator	Pin Number	Signal	Description
J7	1	TS	IC TS signal through a resistor
	2	GND	Signal reference for the IC
J9	1	CHGCTL	Control signal for charger detection, connects through a resistor to the IC CHGST pin
	2	DSGFLAG	Diode and resistor isolated DSG signal
	3	CHGFLAG	Diode and resistor isolated CHG signal

3 bq77910 EVM Hardware Connection and Operation

This section describes the connection of the circuit module and EVM and simple operation in its default configuration.

3.1 Initial Considerations

Boards are tested after assembly with a basic functional test. This test may not check every connection on the board. Boards should be checked for function in the user's environment before relying on the safety features of the board. Operation of the board with test equipment before connecting cells is recommended and described in this document.

The default configuration of the board is 10 cells with parallel FETs. Modifying the EVM for different cell counts or FET configuration requires solder connections. It is recommended that the user familarize themselves with operation of the board in the default configuration before modifying the board, and check the operation of the board with test equipment after any modification. Configuration of the board is described in Section 7.

Be sure to observe the cautions and warnings in this document.

A variety of connections are provided on the EVM. The manufacturer's rating for the terminal blocks for Pack and Battery connections is 32A nominal. Parallel connections are provided for high current operation. The banana jacks are rated at 15A. Safety agency ratings may be lower than the manufacturer ratings, limit currents to appropriate values for your evaluation. Cell monitor terminal blocks and the control signal terminal blocks are rated at lower currents and should not be used for high current paths.

A communication interface is not required for basic operation, and it should be connected to the computer and EVM circuit module only after proper installation of software. The software along with an appropriate communication interface allows setting the programmable safety limits of the device and checking the staus after fault detection. Installation of the software and its use are described in a later section.

3.2 Connecting the cell simulator

The cell simulator consists of headers to mate the board and ten (10) 200 ohm resistors to divide the battery voltage between the inputs. Power is provided through the Cell0 and Cell10 connections on the terminal block headers. Various test points are provided on the board. Refer to physical construction section for additional details.

- Be certain no power is applied to the board.
- Unplug the screw terminal blocks from J4 and J5 of the EVM and save these for later use.
- Plug the cell simulator board onto J4 and J5. Support may be required on the bottom of the EVM while the connectors are pressed together firmly.

CAUTION

Do not connect or remove the cell simulator board while power is applied to the EVM. The resistor pull down or up from intermittant connections will overstress the device inputs.

3.3 Simulated battery connection

Connect a power supply between BATT- (negative) and PACK+ (positive). This power supply will connect to the resistor cell simulator through default connecitons on the bq77910 circuit module.

3.4 Pack Connections

A load or charger is connected to the pack terminals using the terminal blocks provided. It is recommended that the load or charger be connected with the current switched off to prevent arcing or transients during connection of the wires to the terminal blocks. Charger detection is required for the bq77910 with a signal at the CHGST pin. Charger detection can be provided by connecting a resistor from the CHGCTL terminal of the board to the PACK supply, or with a logic level voltage supply for evaluation.

An external resistor is required due to the low resistance pull down on the board. The selected resistor should keep the CHGST voltage above the VCHG_DET1 data sheet threshold over the entire evauation voltage range while limiting the power in the 1k ohm pulldown resistor to 1/16W or less. A 15k ohm 1/4W resistor is typically suitable for the default configuration, a smaller value may be requied for low voltage or if the configuration is changed.

WARNING

The CHGCTL should not be tied to the power supply without the external resisor since the 1k resistor on the board will become very hot and may damage the board.

Although designed for 30A operation, the board may not dissipate enough power to operate without exceeding all component ratings. The user should monitor the temperature of the board and components during evaluation and provide cooling air and/or heatsinks as required for operation. The thermal sensor on the board may not respond to protect the FETs from damaging temperatures due to its location and possible thermal gradients on the board.

CAUTION

The bq77910 circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling as needed for your system environment.

WARNING

The bq77910 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply check your equipment requirements and use blocking diodes or other isolation techniques as needed to prevent damage to your equipment.

The connection of the EVM will look similar to Figure 1.

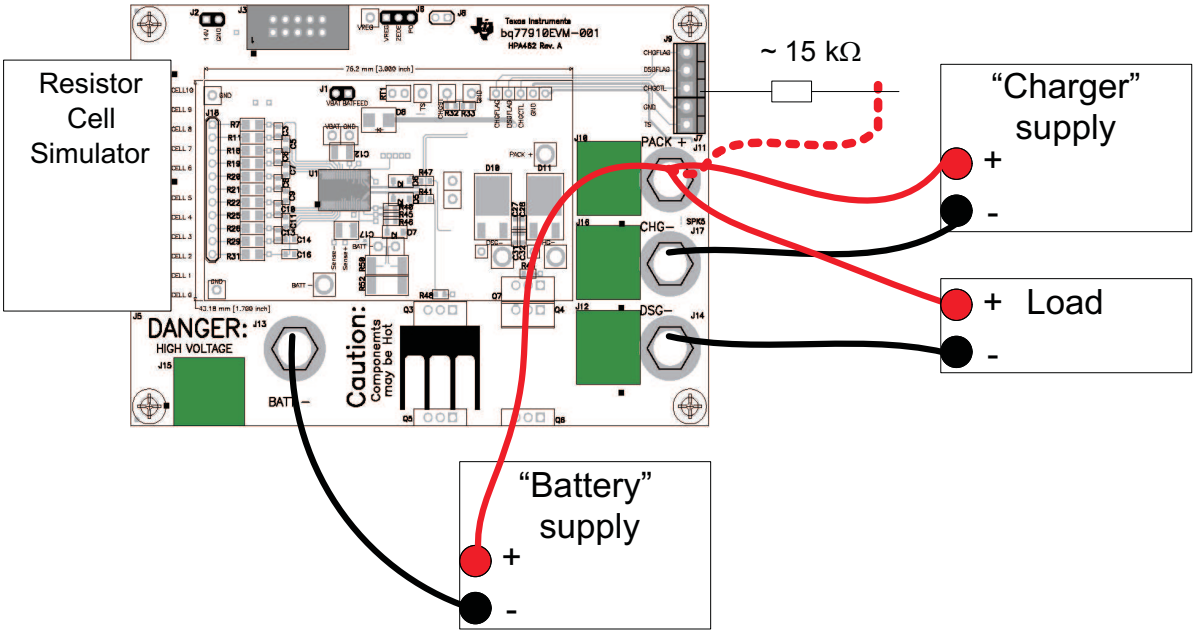

Figure 1. Basic EVM setup

3.5 Basic Operation

The following steps are suggested for basic operation of a default EVM with the cell simulator and the default configuration in EEPROM.

1. Confirm the cell simulator board is installed on the EVM.
2. Connect a power supply between the BATT- (negative) and PACK+ (positive) terminals.
3. Connect a 15k ohm 1/4W resistor to the CHGCTL terminal of the board.
4. Set the bench supply to approximately 36V.
5. Connect a disabled load between the DSG- (negative) and PACK+ (positive) terminals.
6. Wake up the part by momentarily connecting the 15k resistor to the bench supply positive.
7. Monitor the CHG and DSG test points using a meter or oscilloscope as desired.
8. Enable the load with a nominal 0.2A or other current within the capability of the supply.
9. Increase the bench supply voltage to ~43V and observe the CHG output goes low.
10. Reduce the voltage to ~36V and observe the CHG output returns high.
11. Decrease the voltage to ~25V and observe the DSG output goes low and the load current drops. The device will shut down after 9 seconds at low voltage.
12. Remove the load and connect the CHGCTL resistor to the supply to simulate a charger.
13. Increase the supply voltage to ~36V and observe the DSG test point goes high, and if the load is re-connected that current flows again.

3.6 Cell Connections

For initial evaluation, it is suggested power supplies be used for cell simulation to observe the behavior of the device. An isolated power supply with a resistor connected across its terminals may be connected to test points on the resistor simulator to vary the voltage above or below the voltage of the other cells, or a similar configuration may be used. The smaller the resistor value, the more current is required from the battery simulator power supply and the smaller the influence on the voltages if cell balancing is operated.

Whether power supplies or cells are used, inductance in the high current path should be minimized. Inductance in this path can cause inductive transients at the board when the load current is stopped or the bq77910 opens the discharge FET with current flow. Use heavy gauge wires for the high current connections; minimize inductances by keeping leads close together.

When connecting cells to the EVM, the user should use care not to exceed the absolute maximum ratings of the device. The bq77910 is designed with open cell (wire) detection, however fixturing should not pull un-connected signals up or down. Signal reference (VSS) for the part is from the BATT- terminal of the EVM, and this lowest potential should be connected first. Cells should be connected in sequence from lowest to highest voltage as described in the data sheet. When terminating the cells to the removable terminal blocks prior to connection to the EVM, the following steps are recommended:

1. Be sure the charger and any load is disconnected (CHGCTL is open).
2. Connect the cell stack negative high current terminal to the EVM BATT- terminal.
3. Connect the lower cell group to the J5 connector.
4. Connect the upper cell group to the J4 connector.
5. Connect the cell stack positive high current terminal to the EVM PACK+ terminal.
6. When removing cells, remove any charger and CHGCTL conntection, then disconect in the reverse order.

4 Software Installation

This section describes how to install the software for the bq77910EVM-001.

4.1 System Requirements

The bq77910 evauation software requires a 32 bit version of Windows XP, Windows Vista® or Windows 7. The computer must also have Microsoft .NET framework version 2.0 or higher installed. Examples in this document are from Windows XP.

4.2 Interface Adapter

The bq77910 evaluation software supports either the TI USB-TO-GPIO adapter (TI USB Interface Adapter) or the TotalPhase Aardvark to provide communication with the EVM board from the computer. The , the Aardvark must be selected if desired. The EVM connector supports the TI USB Interface Adapter, a special cable must be constructed if you wish to use the Aardvark.

4.2.1 TI USB Interface Adapter

The TI USB Interface Adapter is default option for the bq77910 evaluation software. Its pinout is compatible with the bq77910 EVM board J3 connector.

The TI USB Interface Adapter http://focus.ti.com/docs/toolsw/folders/print/usb-to-gpio.html is actually a separate EVM from Texas Instruments and its default firmware is not compatible with the bq77910. If the firmware has already been updated to version 2.0.19 to work with other BMS-HCE products, additional update is not required. If required, update the firmware using the following steps.

1. Obtain the USB to GPIO EVM Firmware Loader from http://focus.ti.com/docs/toolsw/folders/print/usb2gpio-loader-sw.html or search from power.ti.com
2. Download, extract and run the installer
3. Installation requires the Microsoft .NET connection software. If a suitable version is not found on the system by the installer, the user will be prompted to obtain and install .NET
4. Connect the TI USB Interface Adapter to the computer with the USB cable. The green LED should illuminate.
5. Run the program, typically from Start>Run>Texas Instruments> USB-TO-GPIO Firmware Loader
6. Detailed instructions are provided in the Readme.txt file.

CAUTION

Do not disconnect the USB cable to the Interface Adapter during firmware update. Loss of power may leave the adapter with corrupt firmware and be unable to further update the firmware.

7. If you want to be able to return to the original configuration, backup the installed firmware before update.
8. Load and Update to the 2.0.19 version using the instructions provided.
9. If an error occurs, do not unplug the adapter. Re-try loading, load a different firmware or re-start the software and repeat until a load is successful.
10. After successful update, the window should appear as Figure 2
11. After update, exit the program

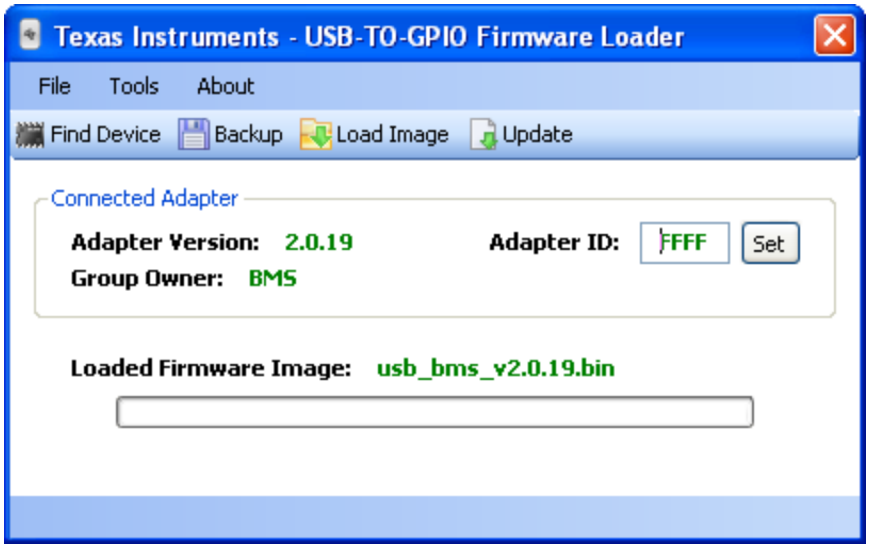

Figure 2. Successfully updated TI USB Interface Adapter

4.2.2 Aardvark adapter

Although the TotalPhase Aardvark adapter will physically mate to the EVM J3 connector, the pinout is incompatable. A special interface cable must be constructed to use the Aardvark. Refer to the schematics and Table 7 below for information.

CAUTION

Do not connect the Aardvark to the EVM without a properly constructed cable. Damage may result to the EVM and/or Aardvark.

Table 7. Adapter cable pinout

IC pin name or description	USB-TO-GPIO (mates to J3)		Aardvark	
	Pin	Signal	Pin	Signal
VSS – signal reference	6	GND	2	GND
SCLK	9	SCL	1	SCL

Table 7. Adapter cable pinout (continued)

IC pin name or description	USB-TO-GPIO (mates to J3)		Aardvark	
SDATA	10	SDA	3	SDA
ZEDE - communication enable	4	GPIO4	5	MISO/GPIO
Programming voltage control signal for EEPROM	3	GPIO5	7	SCLK/GPIO

4.3 Install The bq77910GUI Evaluation Software

Find the latest software version in the bq77910GUI Evaluation Software tool folder on http://www.ti.com/tool/bq77908-10-gui-sw or search from power.ti.com. Check periodically for software updates. Use the following steps to install the bq77910 Evaluation Software:

1. Copy the archive file to a directory of your choice, extract and run the bq77910 setup.msi installer.
2. Follow the instructions and make selections as required on the setup windows selecting next as required.
3. On the last window, select "close" to complete the bq77910 software installation.

5 Software Operation

This section describes conneciton of the communication interface to the EVM and operation of the software.

Although the software will run without connection to a powered device it is recommended to have the device on when starting the software. Figure 3 shows connections for operation with the GUI software.

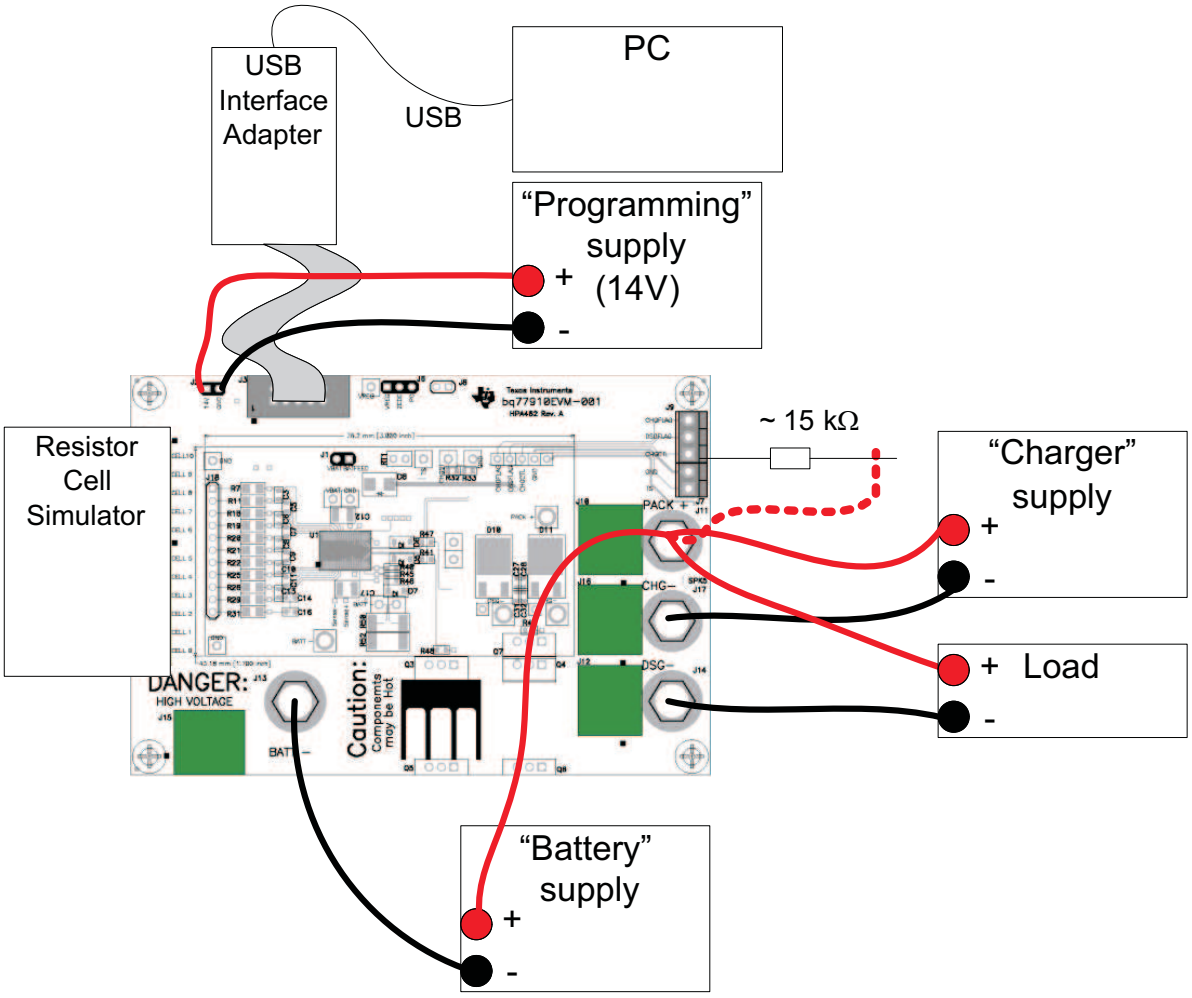

Figure 3. EVM Connection for Communication and Programming

To connect the computer to the GUI and start the software use the following steps:

1. Connect the TI USB interface adapter to the computer
2. Connect the 10 pin connector from the interface adapter to the EVM J3

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer will be referenced to the Battery- potential of the EVM.

3. Remove any shunt installed on J6 so the inteface can control ZEDE
4. Connect the "battery" power supply to the EVM, adjust to approximately 30 to 40VDC.
5. Wake the bq77910 by connecting CHGCTL high
6. Start the software, typically using Start > All Programs > Texas Instruments > bq77910 Evaluation

When started, the software will look for the communication interface and the device. When communication is established with the device, the main window appears as shown in Figure 4.

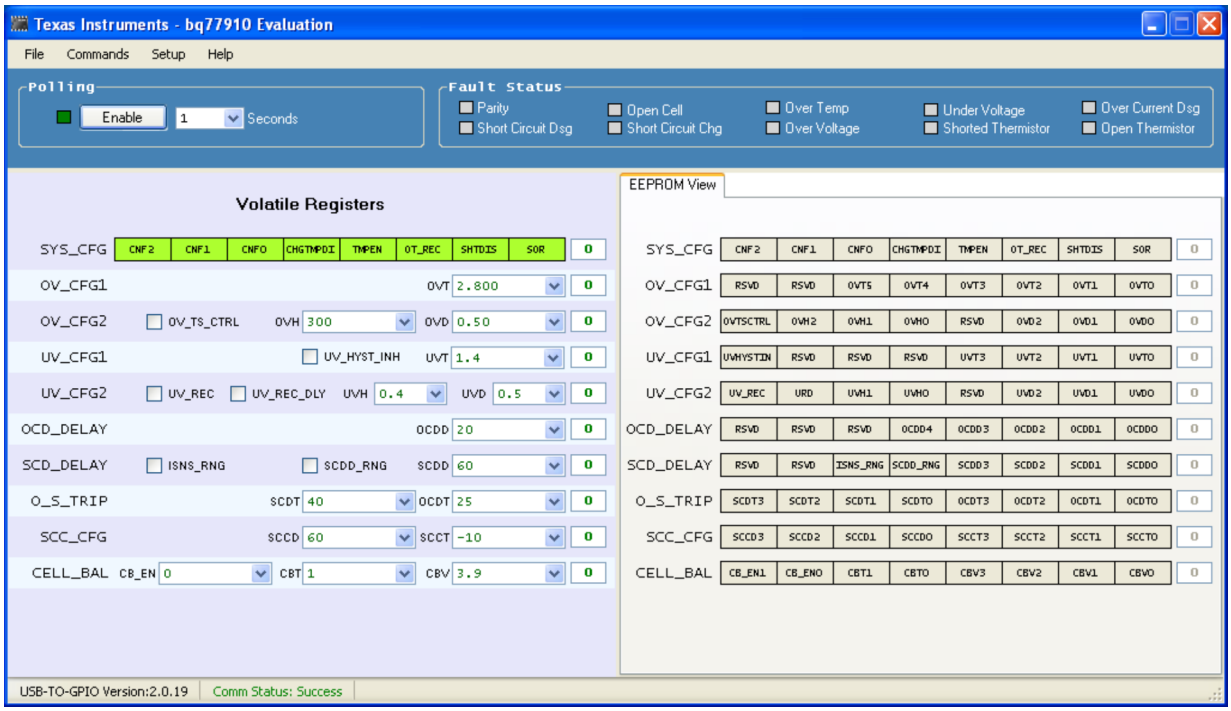

Figure 4. GUI with communication established

Other than the menu selections, the software window has 3 sections. In the bottom border is a status section. The middle section is a register section. The top section is a status area useful for checking the device status when a fault is detected. Details are described in following sections.

5.1 Menu commands

5.1.1 Help Menu

The Help > About menu selection displays version information about the program

5.1.2 Setup Menu

The Setup > Communication selection allows selection of either the USB Interface Adapter or the Aardvark. Default is the TI USB Interface Adapter and this window will not be needed. Selecting the Save and Exit button will check for the adapter, If the selected adapter is not present, a communications error window will appear. Selecting OK in the window will return to the Communicaiton Seleciton Window. To exit without having the selected adapter connected, use the close window tool (red X button). Selection of an adapter other than the 2 shown is not supported.

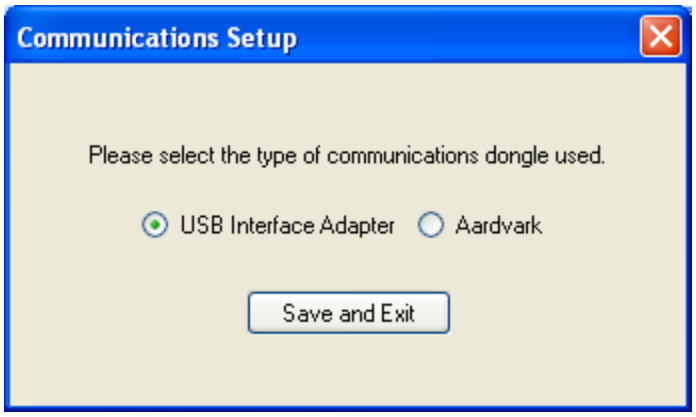

Figure 5. Communication Selection Window

5.1.3 Commands Menu

Most commands are only available after communication is established with the device. Figure 6 shows the command window when communicaiton is not yet established.

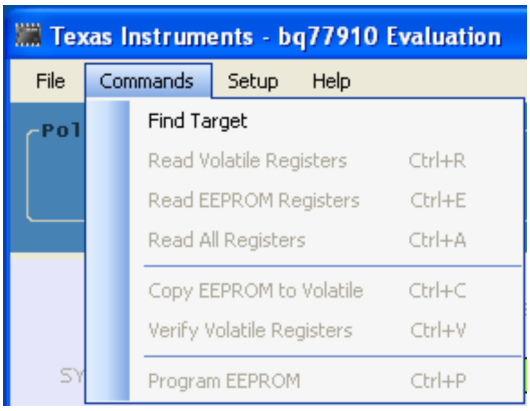

Figure 6. Commands without communication established

The communication status in the bottom border of the window shows the adapter in use and the device communication status. If the software is started and the adapter is not found, a Communication Error message box is displayed. Selecting OK on the box will display the main window. If the device is not recognized, a Device Not Found box is displayed. Selecting OK to this box will also display the main window. The communication fault will be displayed in the status area of the window. Communication can be re-tried by selecting the menu command Commands > Find Target. Once communicaiton is established with the part, the Find Target command is no longer available.

The other commands relate to the register section. The register seciton is shown in Figure 7. Two sets of registers are displayed, the right section can display the EEPROM settings, the left side can display the volatile registers waiting to be programmed in the EEPROM. When the software is first started, all values are shown as zero.

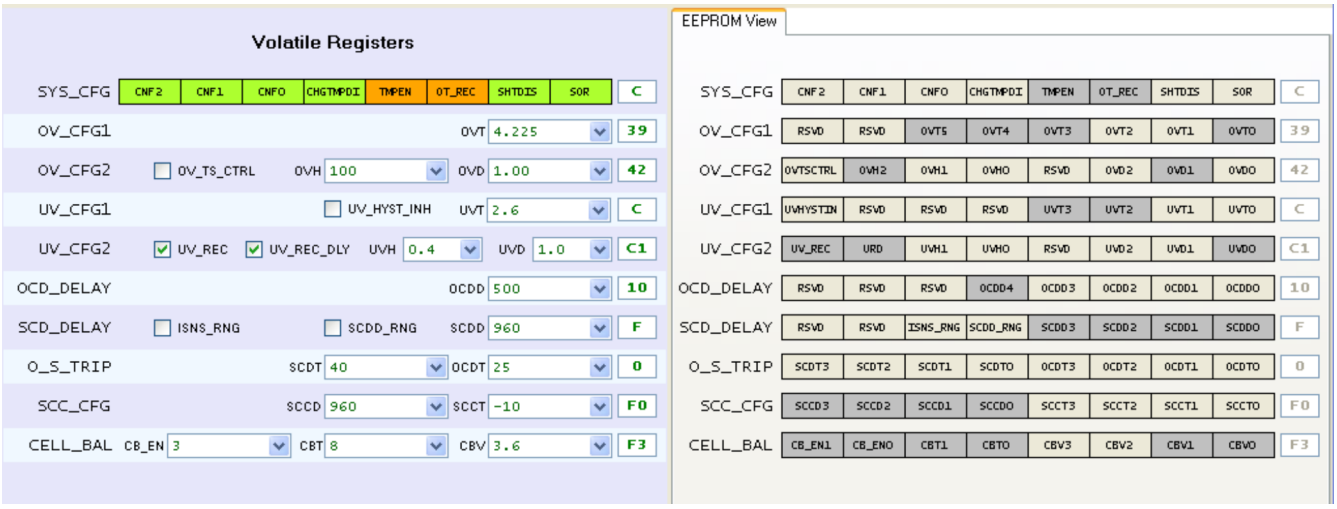

Figure 7. Register Section

The Read Volatile Registers command will read the values from the registers in the part and display them in the GUI window. When a part is first powered, these will typically be zero. When connecting to a powered part, they will likely contain residual values.

The Read EEPROM Registers command will read the EEPROM values from the device and display them in the EEPROM registers section of the window for viewing. This is a viewing operation and data maniuplation is not allowed in the displayed EEPROM data.

The Read All Registers command reads both the volatile and EEPROM registers from the device and displays the values.

The Copy EEPROM to Volatile command will copy the EEPROM register values to the corresponding volatile registers and display both in the GUI. This is a good starting point for making incremental changes to the device settings.

The Verify Volatile Registers command checks whether the volatile registers match the contents of the device. This can be useful as a check before programming the EEPROM.

The Program EEPROM command will write the volatile register values

5.1.4 File Menu

The Load Registers from File command will read a properly formatted file and fill the volatile register seciton with the values. This is useful to load a device with a saved configuration. A windows navigation tool allows selection of the file. While files could be edited, it is recommended to load files saved by the software, and if any editing is performed on the file, check all values before programming the device.

The Save Registers to File command will create a file. A windows navigation tool allows selection of the location and file name. Files have the .cfg extension.

The Exit command will exit the program.

5.2 Working with register values

EEPROM values are displayed but are not directly editable in either the device or the GUI. Changes are made to a volatile register set by changing the volatile register value which is written to the volatile register in the device and later written to the device EEPROM by the programming process. Changes in the volatile registers do not affect operation of the device until written into the EEPROM.

Values in the Volatile Registers section can be typically be changed in 3 ways:

- Loading a register file
- Changing a check box or dropdown selection
- Entering a data value in the box corresponding to the register name

The SYS_CFG register bits are displayed as selection boxes, these are green for a value “0” and orange for a value “1”.

The following steps describe changing a device EEPROM setting on the EVM using the GUI with a connected adapter:

1. Power the EVM (device) with the "battery" supply, and wake it up with charger detection
2. Maintain a logic high on the CHGCTL pin of the EVM (CHGST device pin)
3. Copy the EEPROM values to the volatile registers with the Copy EEPROM to Volatile command.
4. Edit the values in the “Volatile Registers” section as desired.
5. Provide a 14 +/- 0.5V at approx 0.1A programming voltage at the EVM J2 connector.
6. Select the “Program EEPROM” command.
7. After a short delay a programming complete status window should appear. Select OK in this window.
8. Disconnect the programming voltage from the EVM J2 connector.

Programming the EEPROM from a file uses a very similar sequence. This can be useful in evaluation when replacing a device or duplicating a design on a small number of boards. The following steps describe programming a device EEPROM on the EVM from a saved configuration file using the GUI with a connected adapter:

1. Power the EVM (device), and wake it up with charger detection
2. Maintain a logic high on the CHGCTL pin of the EVM (CHGST device pin)
3. Select the File > Load Register File command, navigate to and open the desired file.
4. Provide a 14 +/- 0.5V at approx 0.1A programming voltage at the EVM J2 connector.
5. Select the “Program EEPROM” command.
6. After a short delay a programming complete status window should appear. Select OK in this window.
7. Disconnect the programming voltage from the EVM J2 connector.

After programming it may be necessary to clear fault status since programming requires communication with the device and that requires setting ZEDE high. ZEDE high may make the part respond to noise. SCC is typically the lowest value threshold in the device and is common after programming or other communicaiton with the part, depending on the device settings and operating environment.

CAUTION

While the software may be useful for producing a small number of boards, it is not intended as a production programming tool. Accidental manipulation of the data between when the file is loaded and when the programming command is sent is not prohibited.

During programming the software checks that the device volatile registers match the values shown. If they do not match, an error message is displayed. Continuing with programming when the values do not match will unexpectedly alter the configuration of the device. If the error is displayed it is recommended to read the volatile registers to examine the contents, correct any communication error and re-start the software or device as needed for proper programming.

5.3 Status Section

The status section of the GUI is shown in Figure 8. This section allows the user to display internal status registers of the devices fault condition. This data is not part of normal operation of the device and is not shown in the data sheet. Accessing the data is disruptive to the device, however it can be beneficial in evaluation.

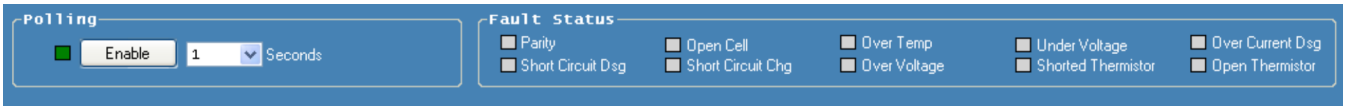

Figure 8. Status Section

The status is read by selecting the Polling "Enable" button on the left side of the status section. This will periodically set ZEDE high to the device, read the status registers, and return ZEDE low. The polling period can be selected with the drop down box next to the button. The button function and label change to "Disable". The button label indicates the action of the next button actuation.

A consequence of polling is that a pending fault delay will be terminated by the status read. Polling is typically independent of any system change and a fault may be recorded as soon as the poll occurs. This may lead to unexpected results in evaluation. The following describe a couple examples which may occur:

- The user has selected a 2 second under voltage delay wants to observe the timing on a scope. The user leaves polling active and decreases the device voltage. The poll occurs just after the voltage drops and the zero delay causes the fault to be registered. The FETs turn off and the user thinks the delay setting is not working. The situation here is the poll set ZEDE high and terminated the under voltage delay.
- The user is polling status to watch faults. CHGST is tied high to prevent the part from shutting down due to under voltage. The user begins switching currents and is suprised when a SCC fault occurs. Observing the sense resistor voltage, the user does not see a charge current. The situation here is the poll set zero delay and eliminates noise filtering on the current. The SCCT is typically a low and thus most sensitive to any noise; having CHGST high prevents recovery from the fault.

The values display in several colors. See Table 8.

Table 8. Status Section Indicator Colors

Color	Meaning
gray	status is not read
bright green	device is polling and status is normal with connected device, or adapter is not connected
bright red	device is polling and status is fault
dark green or dark red	device is not polling and value is residual from last poll

Figure 9 shows a typical status display polling with undervoltage.

Figure 9. Polling Status with Under-Voltage Condition

Another use of the status section is to determine the reason the part has turned off the FETs. For example if during test the EVM has turned off the FETs but the VREG is still on, the interface might be connected and the status polled to see what fault the device identifies.

5.4 Basic Operation With Software

The following steps are suggested for exercise of more of the device features using the EVM in its default 10 cell configuration and EEPROM settings. The board is connected as shown in Figure 3. Remember that timing will be incorrect as described in section zz.

1. Install the software.
2. Connect the USB Interface Adapter to the computer with the USB cable.
3. Remove the screw terminal blocks from J4 and J5 and save for later use. Connect the cell simulator board to the bq77910 main board J4 and J5. Support the under side of the EVM board as the connectors are pressed together.

> **CAUTION**
>
> Do not connect or remove the resistive cell simulator from the board with power applied. The resistor pull down or up from intermittant connections will overstress the device inputs.

4. Connect the 10 pin ribbon cable from the USB Interface Adapter to the EVM J3.
5. Connect an isolated power supply negative to BATT- and positive to PACK+. Adjust the voltage to approximately 32V.
6. Connect a ~15k resistor from the power supply positive to the CHGCTL terminal. This will wake the part; leave the resistor connected.
7. Start the software.
8. Connect a disabled load to the pack terminals.
9. Select the polling Enable button in the software window.
10. Observe the status values are bright green.
11. Set a current on the load within the capability of the supply and board.
12. Decrease the power supply voltage to approximately 25V. Observe using load current stops and the UV status indicator turns red.
13. Increase the supply voltage to approximately 31V. Observe the UV indicator turns green.
14. Load current may not resume until the load is disabled or disconnected.
15. Increase the supply voltage to approximately 43V. Observe the OV status indicator turns red.
16. Decrease the power supply voltage to approximately 32V. Observe that the OV indicator turns green.
17. Disable polling.
18. Disable the load
19. Set the supply to 0V and turn off equipment.

5.5 Operation with other interfaces or hosts

The bq77910 GUI software does not support other interfaces.

Communication with the bq77910 from other hosts should be straightforward. Refer to the datasheet for timing and interface details. On the EVM, zero delay mode can be set to allow communication using a 0.1" shunt (not provided) at J6 pins 1 to 2, or a signal at ZD on J3. To program, the on-board programming voltage switch can be used by controlling the PGM signal on J3. Signals should be 3.3V CMOS levels.

6 Related Documents From Texas Instruments

To obtain a copy of any of the following TI document, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this document by its title and literature number. Updated documents can also be obtained through the TI Web site at www.ti.com

Document	Literature Number
bq77910 data sheet	SLUSA07

7 bq77910 EVM Circuit Description and Configuration

This section describes the circuit on the bq77910 circuit module and how to configure it for changes the user may want to make to the board for specific evaluations. In many cases, an EVM schematic is used as a starting point for a circuit design. This can result in extra components on the product design which are not needed but take up space and in some cases add unnecessary expense. Refer to the schematic in the physical construction section while reading the following descriptions. Note that the schematic has 2 pages, the first shows the main funcitons, the second page shows primarily cell count configuration and protection components.

7.1 Battery voltage clamp

The TVS diode D9 provides a clamp for transients on the pack. A common transient is due to system inductances and sudden load shutoff. The breakdown voltage of D9 should be set near or below the 5V per cell abs max of the device. As a transient pushes the voltage up the I-V curve, a substantial device here reduces the demands on other clamping components in the system which may be needed to protect the device. Alternatives to D9 might be to control the system inductance and current switching rate, use capacitance to absorb transients, or other transient protectors such as MOVs where appropriate.

7.2 Device power

The device is powered through the BAT pin. C12 is a bypass capacitor near the IC, the footprint is large to make it easy to mount larger capacitors in case this is desired in evaluation. R5 and J1 provide a way to measure current to the device during evaluation and are not needed in an application. D2 provides power from the battery to the IC and prevents the IC power from being pulled down when the battery voltage dips suddenly due to a heavy load on the battery. C2 provides an operating resorvoir for device current during battery voltage droop. D1 limits the voltage to the BAT pin preventing over voltage from rectification of transients by D2.

Power is provided through R4. The 200 ohm resistor provides for a voltage drop when an over voltage charger pulls down BAT through D8. For lower cell counts, this resistor may be a smaller value. R3 is a zero ohm connection to the high current battery positive connection BATT+ which is shared with the PACK+. This jumper is provided in case the user wants to power the part from the current monitor line instead.

7.3 Cell Monitor Inputs and Configuration

The cell monitor inputs are provided through a RC filter network. The series resistors R_{VCX} connect the cells to the device to allow voltage measurement and limit the balancing current. Balancing current is approximately the cell voltage divided by twice the resistor. The EVM is circuit is designed to use the internal balancing path at near the maximum current. The 47 ohm R_{VCX} value on the EVM is nominallly within 10% of the 50 ohm minimum recommended in the datasheet and will prevent exceeding the absolute maximum balancing current up to 4.3V per cell. The input capacitance is typically connected between cell inputs, except the capacitances at VC10 and VC11 are connected to ground to avoid pushing the inputs below ground during transients. The capacitance should not be increased beyond the 1uF shown since the capacitors are discharged into the device during balancing. The filter effect will both reduce cell transients to the device inputs, and slow voltage recovery after balancing. The resulting time constant is complicated due to the multiple components but relatively short due to the small resistors used for high balancing current. Due to the cell input voltage measurement after balancing, the time constant (R_{VCX}) should not be made too large.

The user should note there are 2 limits implied by the absolute maximum cell-to-cell differential rating of the part. One is the applied differential voltage, or 5V on any cell regardless of the other inputs. Note also this is an applied voltage, not the voltage induced by the part during balancing, which may be higher. The second voltage limit is the voltage to ground the cumulative voltage from summing the individual limits. Since the input filter time constant is small, clamping the inputs to safe values may be required. While a

zener or TVS diode per cell may be a suitable way to protect the device in some applications, the EVM provides patterns D12 to D18 to clamp the inputs for cells 10 to 4 to ground. The top cell input is clamped (VC1 with D12 on the EVM), and cell 4's input, VC7 is clamped with D18 on the EVM since this input showed more sensitivity than others in testing. For nominal transients, these clamps in conjunction with the capacitors between cells should hold the inputs to safe values, however different or additional clamping may be required in evaluation or the target application.

The EVM has resistor jumper positions and is populated to connect to the cells with N+1 wires where N is the number of cells. R42 connects the high current BATT- connection to the lowest cell monitor point. Similarly R59 connects cell 10 input to the high current path through R3. Additional resistor patterns R53 to R58 allow the same connections when the board is configured for other series cell counts. The board may be configured to monitor the cell voltages directly at the cells (N+3 wires) by removing R42 and R59 or its equivalent.

When configuring the part for fewer than 10 cells, the unused inputs should not be left floating and must be connected to avoid exceeding absolute maximums. The EVM provides patterns to allow flexible connections. The unused pin group may be connected together on the EVM by shorting the capacitors between them or shorting the appropriate resistor jumper positions R60 to R64. The unused pin group then needs to be connected to a safe level, either to the top cell through one of the unused cell R_{VCX} patterns or to the highest used VCx pin using the appropriate R61 to R65. When configuring for fewer than 10 cells and using the cell simulator, be sure to remove components to avoid parallel paths. Due to the flexibility allowed by the EVM for configuraiton it is recommended the evaluator study the schematic before modifying the board to achieve their desired configuration. Table 9 shows possible configurations for different cell counts assuming use of the cell simulator, retaining the N+1 wiring plan and adjusting the transient protection. The board will operate at a lower cell count without the transient protection adjustment, but the user should be sure they provide adequate protection for the IC in the evaluation and system design to prevent damage. The table describes a change from the 10 cell default to one of the other configurations, the users should check configurations if multiple changes are made. D12 is shown removed in the table for less than 10 cells to avoid any possible leakage current or unexpected clamp during evaluation.

Table 9. Cell Count Component Configuration

Cell Count/ reference designator	10 cells (default)	9 cells	8 cells	7 cells	6 cells	5 cells	4 cells
C3	installed	Remove	installed	installed	installed	installed	installed
C5	installed	installed	Remove	installed	installed	installed	installed
C6	installed	installed	installed	Remove	installed	installed	installed
C7	installed	installed	installed	installed	Remove	installed	installed
C8	installed	installed	installed	installed	installed	Remove	installed
C9	installed	installed	installed	installed	installed	installed	Remove
D1	installed	< 45V	< 40V	< 35V	< 30V	< 25V	< 20V
D9	installed	< 45V	< 40V	< 35V	< 30V	< 25V	< 20V
D12	installed	Remove	Remove	Remove	Remove	Remove	Remove
D13	-	< 45V	-	-	-	-	-
D14	-	-	<40 V	-	-	-	-
D15	-	-	-	<35V	-	-	-
D16	-	-	-	-	< 30V	-	-
D17	-	-	-	-	-	< 25V	-
D18	installed	installed	installed	installed	installed	installed	installed
R7	installed	Remove	Remove	Remove	Remove	Remove	Remove
R11	installed	installed	Remove	Remove	Remove	Remove	Remove
R18	installed	installed	installed	Remove	Remove	Remove	Remove
R19	installed	installed	installed	installed	Remove	Remove	Remove
R20	installed	installed	installed	installed	installed	Remove	Remove
R21	installed	installed	installed	installed	installed	installed	Remove
R53	-	-	-	-	-	-	0Ω
R54	-	-	-	-	-	0Ω	-
R55	-	-	-	-	0Ω	-	-
R56	-	-	-	0Ω	-	-	-
R57	-	-	0Ω	-	-	-	-
R58	-	0Ω	-	-	-	-	-
R59	installed	Remove	Remove	Remove	Remove	Remove	Remove
R60	-	100Ω	0Ω	0Ω	0Ω	0Ω	0Ω
R61	-	-	100Ω	0Ω	0Ω	0Ω	0Ω
R62	-	-	-	100Ω	0Ω	0Ω	0Ω
R63	-	-	-	-	100Ω	0Ω	0Ω
R64	-	-	-	-	-	100Ω	0Ω
R65	-	-	-	-	-	-	100Ω

The cell count programmed in the EEPROM must match the physical connection for proper operation. If the device is programmed for more than the connected cells, the unused cells will still be checked by the device and will show undervoltage or open cell faults. If the device is programmed for fewer than the connected cells, the upper cells are ignored and faults on these cells are not checked. Also be aware of the voltage applied to the part could exceed the absolute maximum or show undervoltage when used with the resistor simulator.

WARNING

When the device is configured for fewer than the connected cells the device does not monitor the upper cells and will not protect against faults on those un-monitored cells.

7.4 Ground Connection

The IC VSS (ground) reference on the bq77910EVM-001 circuit module is connected to the BATT– at the sense resistor. Note the range of the inputs when considering moving the ground location in an application design. The ground connection should be made at one location on the high current path to avoid differential voltages on the board ground due to high currents.

7.5 Current Sense Connections

R50 and R52 in parallel make the current sense resistor. Two resistors allow for lower heat dissipation per component at a given current, and allow flexibility in evaluation. R43 and R44 isolate the sense input pins from the current path transients, C20 and C25 provide filtering. Be aware that C20 and C25 will add a time delay to the system current response depending on where sense resistor voltage falls in relation to the threshold voltage. A mismatch in C20 and C25 can convert a common mode signal to a differential signal at the device pins, the C22 pattern is available if a differential filter is desired.

7.6 Filter Capacitors

The regulator filter capacitor C17 value of 4.7µF exceeds the minimum datasheet value of 1µF. The 1µF DCAP and CCAP filter capacitors C21 and C26 are the data sheet recommended typical values

7.7 FET circuits

The circuit board has 5 TO-220 power FET patterns to allow flexibility in evaluation. By default the board is populated for parallel FET operation. The Q3 discharge FET is mounted to a heatsink expecting high discharge currents. The user should monitor temperature in their evaluation environment and provide additional cooling if required. Q7 is the parallel charge FET. Anticipating a low charge current of up to a couple amps, Q7 does not have a heatsink. The user should measure the device temperature in their evauation environment and provide heatsinking and cooling if required.

The Q4 pattern allows a FET to be installed instead of Q7 to provide series FET configuration. In this case the pack negative would be the CHG- terminal. HS2 pattern is provided for Q4. If configured for series FETs it is recommended to insulate DSG- to avoid erroneous connections. Patterns Q5 ane Q6 are in parallel with Q3 and Q4 to provide for optional patterns, to allow parallel FET connection, to provide for a large heatsink to be mounted to the FETs off the board edge if desired, or to provide connection points for additional circuitry.

C34 and C35 provide a ESD path and high frequency bypass during switching of the discharge FET. Two capacitors in series are used so that if one is shorted, the other still blocks DC signals. C36 and C37 provide a similar funciton for the charge FET or across both FETs in series configuraiton.

Several other components relate to the FET operation. R48 and R49 pull down the gate to source voltage for the FETs to keep them off when the bq77910 is shut down. R41 is the discharge FET gate drive resistor, 1k on the EVM. This value will adjust the turn off time of the discharge FET. Increasing the turn off time will reduce the inductive transients during a protection event, but will increase heating in the discharge FET. FET turn on is also affected, be sure to consider this if the system can turn on with load applied. The 1k value may need to be adjusted for your application or other FETs, consult the FET vendor data. R51 and C33 patterns provide locaitons to provide feedback to slow the discharge FET switching if appropriate in your application. The charge FET typically can be allowed to switch faster due to lower current. The value of R47 can be adjusted if desired.

When no FETs are desired, Q7 and Q3 can be shorted source to drain. Shorting the FETs is important in this case both to provide a high current output path and to provide a proper reference for the DPCKN, CPCKN and CCAP signals. Adjustments to the flag circuitry may also be desired in this configuration.

7.8 Detection Sensing

The device detects load presence with the DPCKN pin. This is connected to the discharge negative signal DSG- with R45. The 100 ohm value is the datasheet recommended typical R_{DPCKN} and provides some isolation of the pin from load transients. C29 provides some filtering to avoid transients pushing DPCKN above its absolute max. D7 is an optional diode to limit the DPCKN voltage to the BAT pin clamp if reqired, in testing it has not appeared necessary. R46 is the R_{LDRM_DET} resistor in the datasheet. This resistor discharges the load capacitance and in series FET configuraiton pulls down CPCKN to allow turn on of the CHG output. Note that this resistor provides an un-switched load and should not be made too small. R46 might be removed in parallel FET configuraitons to reduce the battery drain during continued loads after protection since the device has a weak internal pull down on DPCKN.

CPCKN is the charge negative sense which is used by the device to sense the charge FET source voltage. It is also the negative power supply for the CHG output driver. R40 is the datasheet R_{CPCKN} and is the typical recommended value. C30 is an optional pattern for filtering if desired. D8 limits the voltage across BAT to CPCKN during transients or situations when the applied charger voltage exceeds the device absolute maximum. D8 also functions in the series FET configuration to prevent CPCKN from significantly exceeding BAT.

7.9 Output Protection Components

D10 is an inductive clamp diode also known as a flyback or freewheel diode. It would conduct if the discharge FET opens with an inductive load to clamp the DSG- to the BATT+. Note that inductance of the cells and interconnect is clamped by D9, but load current is handled by D10. D11 prevents CHG- from significantly exceeding BATT+. It provides an inductive load clamp in the series FET configuration when D10 is likely removed. Also in the series FET configuration D11 shorts a reversed charger after the FETs open.

The EVM contains some features to avoid ESD on several of the signals that come to the output side of the board. Spark gaps are provided at most outputs. Pairs of series capacitors bypass most signals to CHG-. If one capacitor is shorted, the other may remain functional. ESD performance of the EVM was not tested, the user should test their system to applicable standards.

7.10 Reserved pins

Pins 23, 24 and 25 of the bq77910 must be tied to GND for normal operation of the device. In an application these might normally be tied directly to VSS, on the EVM they are individually pulled down for possible future use. Pin 30 should not be connected in normal operation. The EVM provided the R30 pattern for possible future use, this would be omitted for normal designs. Pins 2, 4, and 37 are not connected.

7.11 Flag Outputs

CHGFLAG and DSGFLAG are signals output from the board for indicating the CHG and DSG pin status. These are isolated from the device pins by R39 and R34 which should prevent excessive loading from shorting the device pins and forcing the FETs off. D6 and D5 prevent current from the board connector pins from driving the device or turning on the FETs due to external connections. If used for monitoring the status these should have some large value pull down. Note the reference level of the CHGFLAG will vary with CHG- when the charge FET is off. If the board is configured to not use a FET and the flag terminals are used as outputs, the appropriate diode can be shorted and resistors adjusted as needed.

7.12 Thermal Sensor

The thermal protection on the bq77910EVM circuit module is set to provide a trip threshold between 65 and 70°C with nominal values. Component tolerances and substitute values may alter this trip point. An on-board thermistor RT1 is mounted near the center top of the board. If RT1 is removed an off-board thermistor could be connected at J7 or J8 and used for sensing temperature closer to the cells. To adjust the value of the trip point, change the value of R27: Trip ratio is nominally 0.2 = $R_{T(trip)}/(R_{T(trip)}$ + R27);

consider component and device tolerances as needed for your design. C15 provides some filtering for TS on switching of VTSB, its value can vary but it should not be so large that it prevents the TS signal from stabilizing before temperature measurement. A charger could access the thermistor through J7 and R28. R28 provides for some isolation of the external connection, but is small to reduce error. Adjust R28 as needed for evaluation or the system design.

7.13 ZEDE

ZEDE is the zero delay test mode control pin of the bq77910. This pin also provides the communicaiton enable to the device for programming and checking the device status. R37 provides a pull down for ZEDE for normal operation. R9 connects the pin to J3 to allow control by a communication interface. The TI USB-TO-GPIO Interface Adapter has a weak pull up for the signal used to control ZEDE, so the 100k value of R37 is larger than the strong pull down recommended by the datasheet. Connecting J6 pins 2 to 3 will provide a lower value pull down of ZEDE through R23 if needed for evaluation, but will prevent data access by the TI Interface Adapter. Connecting J6 pins 1 to 2 will pull up ZEDE to test zero delay mode and allow communication with hosts which do not control ZEDE.

7.14 Programming Interface

The serial communication interface is connected to J3 with isolation resistors R12 to R15. D3 provides ESD protection. R16 and R17 pull the lines low when not connected. Pull up resistors for communication with the EVM must be provided by the host or other off-board conneciton.

Q1, Q2 and related components provide a switch for the 14V programming voltage controlled by the interface adapter. It is expected this circuitry would be on a production fixture in a system design. R24 provides a pulldown for the EEPROM pin when programming voltage is not present, this resistor can be smaller to avoid noise depending on the capability of the programming power supply and switch. When programming the EVM with software other than the bq77910GUI Evaluation Software and supported host interface, provide a logic control to the J3 PGM pin at the appropriate time indicated in the data sheet programming diagram.

8 bq77910 Circuit Module Physical Construction

This section contains the pcb layout, bill of materials and schematic of the bq77910EVM circuit module.

The bq77PL910EVM-001 consists of 2 circuit module assemblies, the bq77PL910EVM main board or HPA462, and the resistor simulator or HPA582

8.1 Main Board

8.1.1 Board Layout

The bq77910EVM circuit module is a 4.5-inch × 3.25-inch 2-layer circuit card assembly. It is designed for easy connection with cell connections on the left side and load connection on the right using standard wires to the terminal blocks. The board was planned for 30A current flow. Wide trace areas are used to reduce voltage drops. The EVM layout and construction allows easy understanding of the connections for evaluation, but the connector area and programming features result in a large board. The main solution components are outlined on the silkscreen layer, the discharge FET can be envisioned moving into this area, and area might further be reduced by careful layout.

See additional information in the configuration and operation sections of this document. Figure 10 to Figure 17 show the board layout.

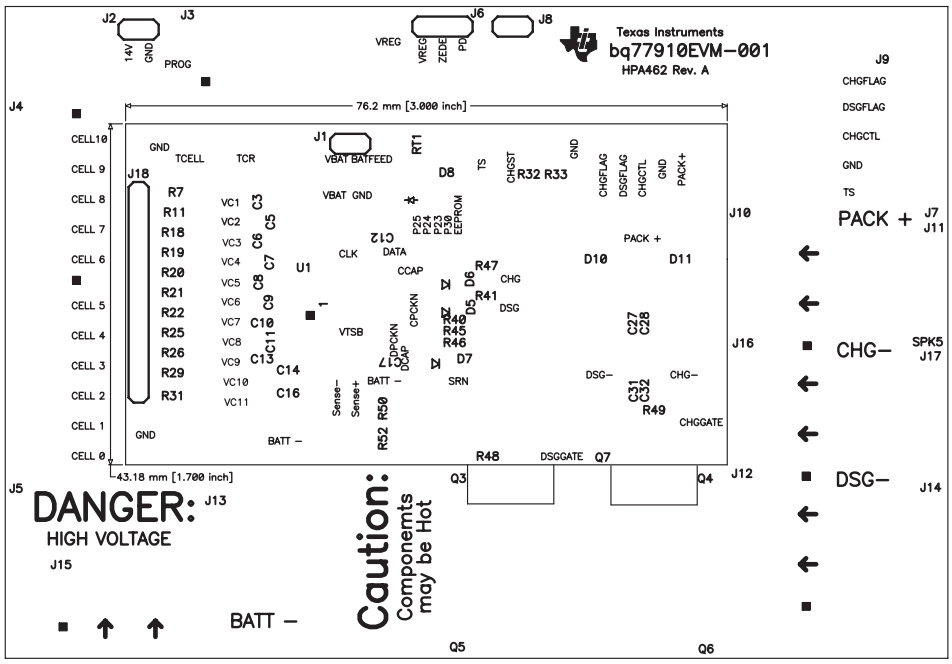

Figure 10. Top Silk Screen

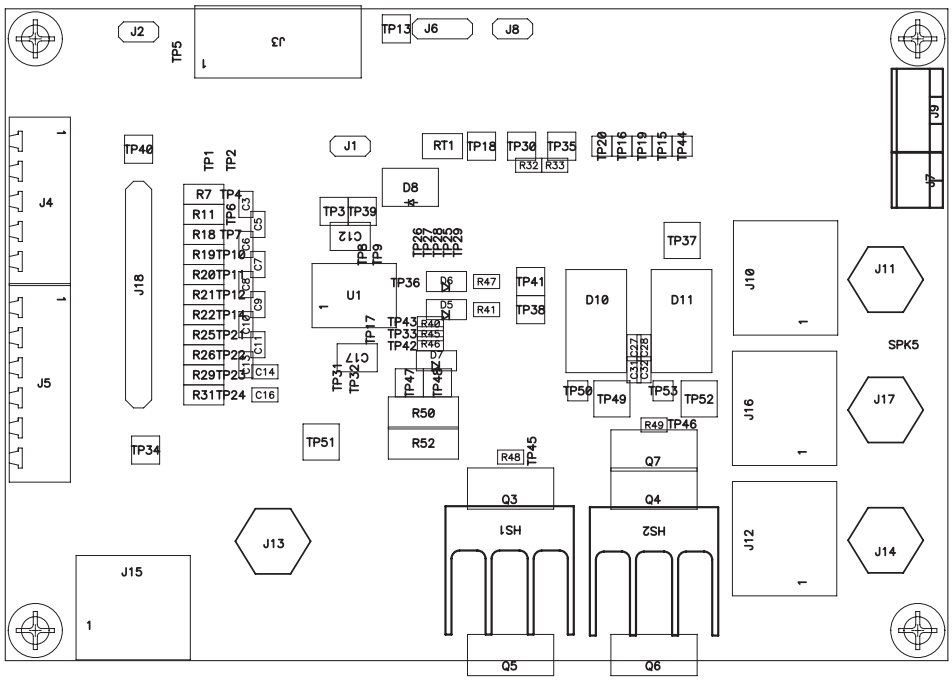

Figure 11. Top Assembly

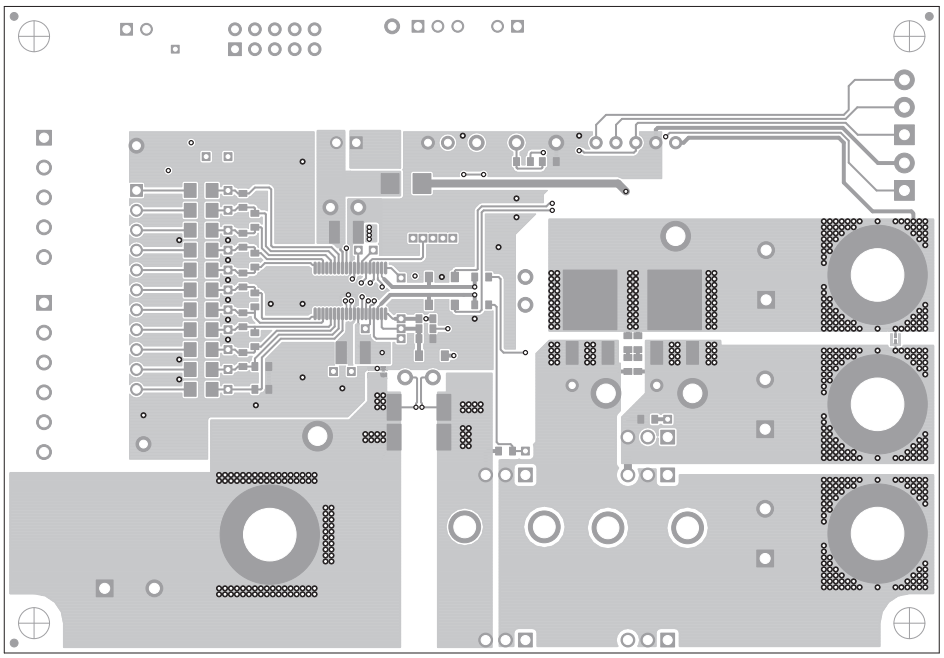

Figure 12. Top Layer

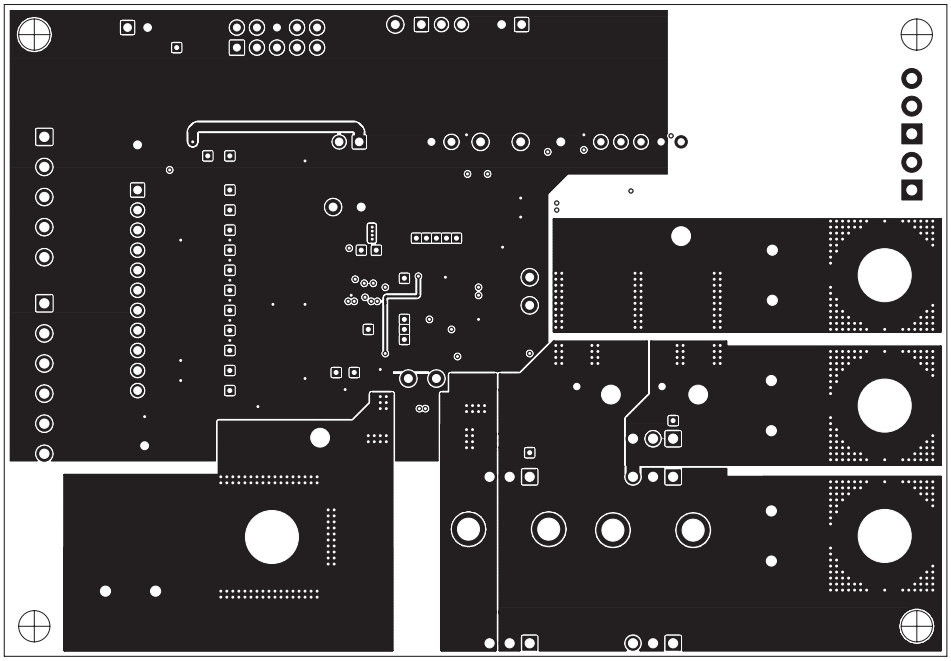

Figure 13. Layer 2

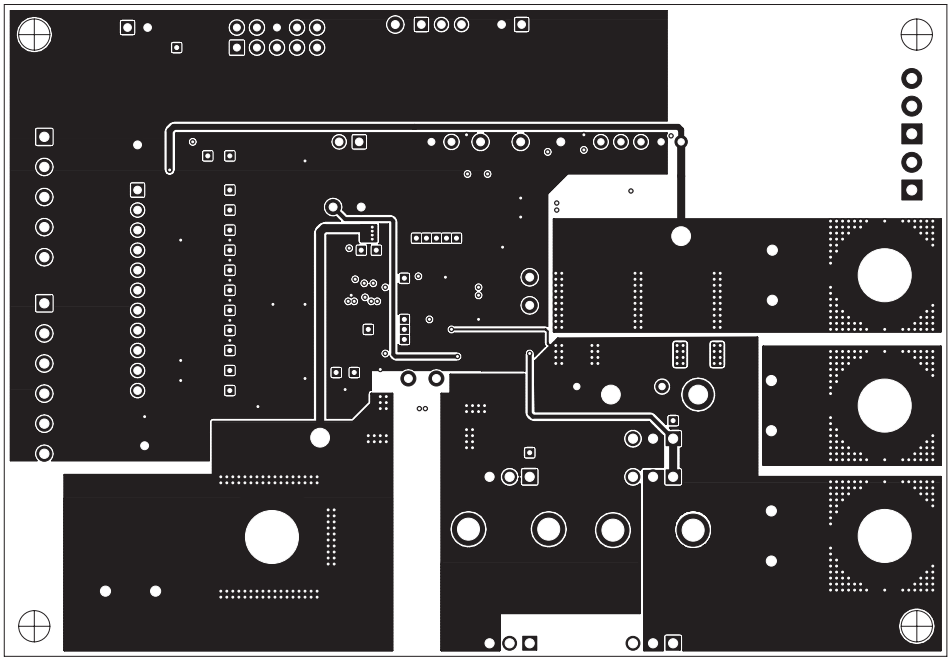

Figure 14. Layer 3

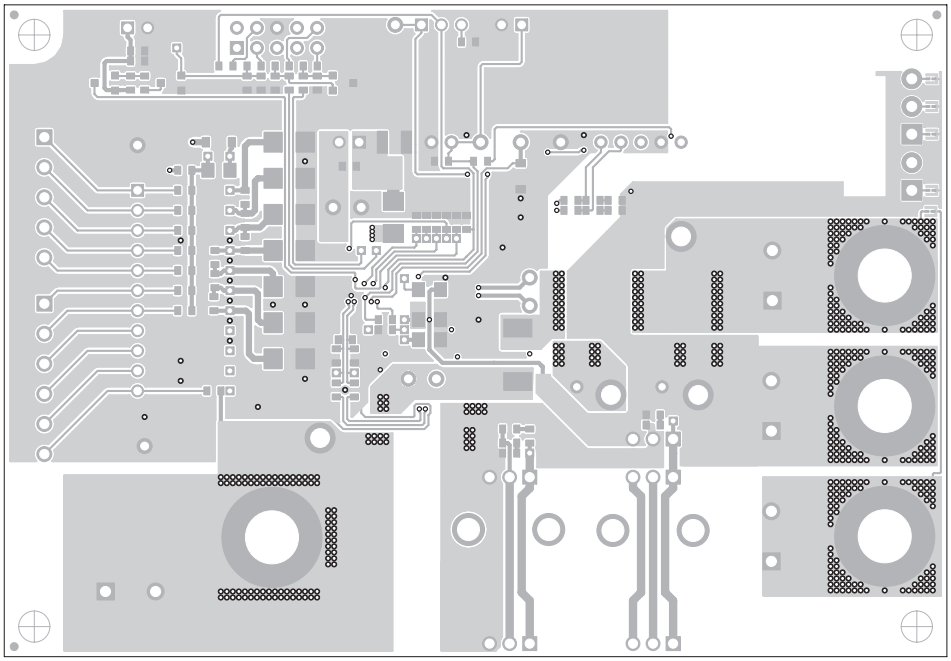

Figure 15. Bottom Layer

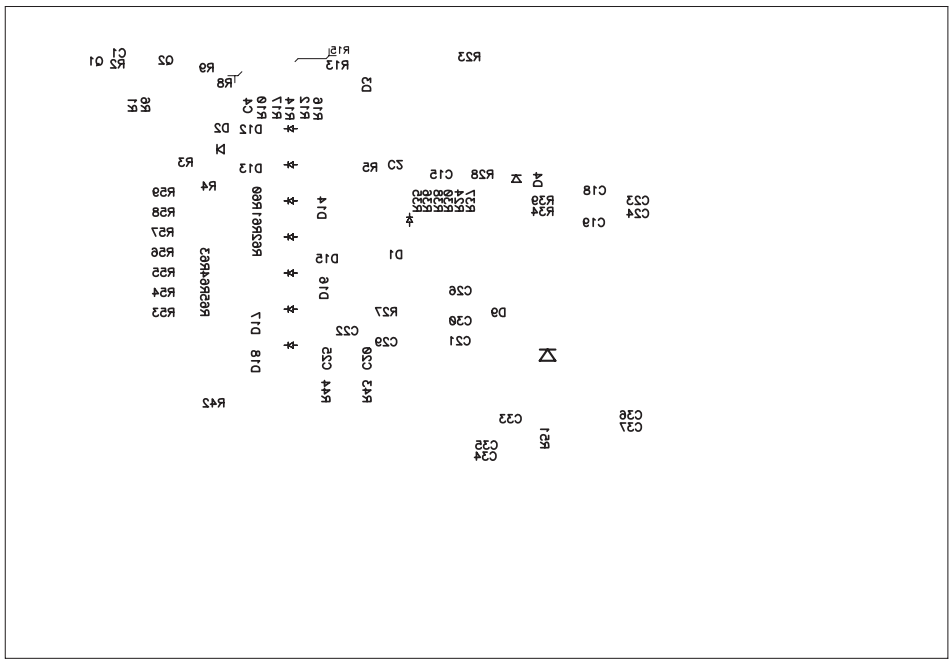

Figure 16. Bottom Silk Screen

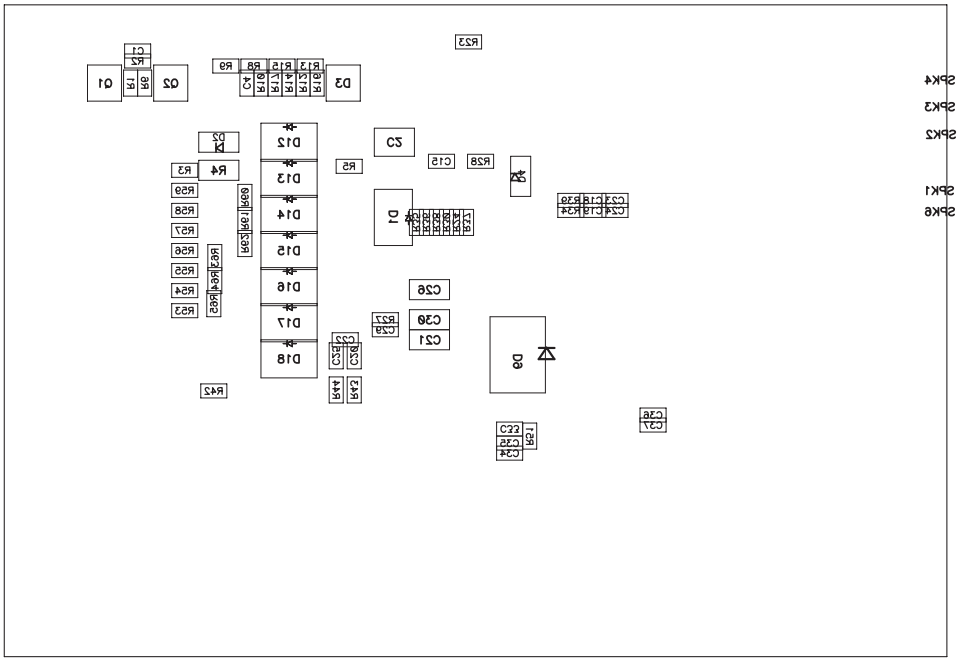

Figure 17. Bottom Assembly

8.1.2 Bill of Materials

The bill of materials for the circuit module is shown in Table 10. Substitute parts may be used in the manufacturing of the assembly.

Table 10. bq77910 Circuit Module Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
17	C1, C4, C18, C19, C20, C23, C24, C25, C27, C28, C29, C31, C32, C34, C35, C36, C37	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C12	0.1 uF	Capacitor, Ceramic, 50V, X7R, 10%	1210	Std	Std
1	C15	10nF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C17	4.7 uF	Capacitor, Ceramic, 50V, X7R, 10%	1210	Std	Std
1	C2	10 uF	Capacitor, Ceramic, 50V, Y5V, 20%	1210	Std	Std
2	C21, C26	1 uF	Capacitor, Ceramic, 25V, X5R, 10%	1206	Std	Std
0	C22		Capacitor, 0603, Not installed	0603		
11	C3, C5, C6, C7, C8, C9, C10, C11, C13, C14, C16	1 uF	Capacitor, Ceramic, 10V, X7R, 10%	0603	Std	Std
0	C30		Capacitor, 1206, Not installed	1206		
0	C33		Capacitor, Ceramic, 50V, X7R, 10%	0603		
3	D1, D8, D12 **	40V TVS	Diode, TVS, Unidirectional, 600-W	SMB	1SMB40AT3G	ON Semiconductor
2	D10, D11	MURD620CT	Diode, Fast rectifier, 200V, 5A	D-PAK	MURD620CTG or UF5A400D1-13 or RF505B6STL	ON Semiconductor or Diodes or Rohm
0	D13, D14, D15, D16, D17		Diode, TVS, Pattern only, 600-W	SMB		
1	D18 **	17V TVS	Diode, TVS, Unidirectional, 600-W	SMB	1SMB17AT3G	ON Semiconductor
4	D2, D4, D5, D6	1N4148W	Diode, Signal, 300-mA, 75-V, 350-mW	SOD-123	1N4148W-7-F	Diodes
1	D3	AZ23C5V6	Diode, Dual, Zener, 5.6V, 300mW	SOT23	AZ23C5V6	Vishay-Telefunken
0	D7		Diode, Signal, 300-mA, 75-V, 350-mW	SOD-123		
1	D9 **	40V TVS	Diode, Unidirectional TVS, 1500W	SMC	SMCJ40A	Littelfuse
1	HS1	634-15	Heatsink, TO-220/218 veritcal	0.640 x 0.640 inch	634-15ABP	Wakefield
0	HS2		Heatsink, Pattern only,TO-220/218 veritcal	0.640 x 0.640 inch		
2	J1, J2	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
0	J8		Header, Male 2-pin, 100mil spacing			
4	J10, J12, J15, J16	1714955	Header, 32A, 500V, 2-pin, 250 mil spacing	0.492 x 0.500 inch	1714955	Phoenix Contact
4	J11, J13, J14, J17	3267	Connector, Banana Jack, Uninsulated	0.500 dia. inch	3267	Pomona
0	J18		Header, 11-pin, 100mil spacing,	0.100 inch x 11		
1	J3	5103308-1	Header, 2x5-pin, 100mil spacing	0.330 x 0.800 inch	5103308-1	Tyco
1	J4 **	1803455	Header, 8A 300V, 5-pin Vert. Entry	0.280 x 0.700 inch	1803455	Phoenix Contact
1	J5 **	1803468	Header, 8A 300V, 6-pin Vert. Entry	0.2800 x 0.750 inch	1803468	Phoenix Contact
1	J6	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	J7	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
1	J9	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
1	Q1	BSS84	MOSFET, Pch, -50V, -0.13A, 10 Ohm	SOT23	BSS84	Fairchild
1	Q2	BSS138	MOSFET, Nch, 50V, 0.22A, 3.5 Ohm	SOT23	BSS138	Fairchild
1	Q3	IRFB3207ZPBF	MOSFET, Nchan, 75V, 170A, 4.1 milliohm	TO-220AB	IRFB3207ZPBF	IR
0	Q4, Q5, Q6		MOSFET, Nchan, Pattern only	TO-220AB		
1	Q7	IRFB3607PBF	MOSFET, Nchan, 75V, 80A, 9 milliohm	TO-220AB	IRFB3607PBF	IR
3	R1, R16, R17	1M	Resistor, Chip, 1/16W, 5%	0603	Std	Std
2	R10, R37	100k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
3	R2, R6, R46	47k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
8	R23, R33, R35, R36, R38, R41, R43, R44	1k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
4	R24, R27, R34, R39	10k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
2	R28, R47	47	Resistor, Chip, 1/16W, 5%	0603	Std	Std
3	R3, R42, R59	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
0	R30, R51, R53, R54, R55, R56, R57, R58, R60, R61, R62, R63, R65		Resistor, Chip, 1/16W, 5%	0603		
1	R4	200	Resistor, Metal Film, 1/4 watt, ± 5%	1206	Std	Std
2	R48, R49	5.1M	Resistor, Chip, 1/16W, 5%	0603	Std	Std

Table 10. bq77910 Circuit Module Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR
10	R5, R8, R9, R12, R13, R14, R15, R32, R40, R45	100	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R50, R52	0.002	Resistor, 2 milliOhm, 1W, 1%	2512	WSL25122L000FEA	Vishay
0	R64		Resistor, Chip, 1/16W, 1%	0603		
11	R7, R11, R18, R19, R20, R21, R22, R25, R26, R29, R31	47	Resistor, Metal Film, 1/4 watt, ± 5%	1206	Std	Std
1	RT1	10k	Thermistor, TH, ±1%	0.095 X 0.150 inch	103AT-2	Semitec
0	SPK1, SPK2, SPK3, SPK4, SPK5, SPK6		Spark Gap, 0.010 inch space	0.050 x 0.070 inch		
0	TP37, TP49, TP51, TP52		Plated Through Hole, Dia. 0.094	0.150 x 0.150 inch		
4	TP34, TP35, TP39, TP40	5020	Test Point, loop	0.100 x 0.100 inch	5020	Keystone
8	TP13, TP18, TP3, TP30, TP38, TP41, TP47, TP48	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
0	TP1, TP10, TP11, TP12, TP14, TP17, TP2, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP31, TP32, TP33, TP36, TP4, TP42, TP43, TP45, TP46, TP5, TP6, TP7, TP8, TP9		Test Point, 0.020 Hole			
0	TP15, TP16, TP19, TP20, TP44, TP50, TP53		Test Point, 0.032 Hole			
1	U1	BQ77910DBT	IC, Multicell Lithium-Ion/Lithium Polymer Pack Protection	TSSOP-38 (DBT)	BQ77910DBT	TI
1	--		PCB, 4.7 In x 3.25 In x 0.062 In		HPA462	Any
1	--		Shunt, 100-mil, Black	0.100	929950-00	3M
1	--		Thermal pad		SP900S-0.009-00-54	Bergquist
1	--		Screw, 6-32 x 0.375", pan head, Nylon		Std	Std
1	P4 (##) **		TERMBLOCK PLUG 5POS 3.81MM		1827156	Phoenix Contact
1	P5 (##) **		TERMBLOCK PLUG 6POS 3.81MM		1827169	Phoenix Contact
4	--		Standoff, M-F threaded 6-32, 0.5", Nylon		4816	Keystone
4	--		Nut, Hex, 6-32, Nylon		Std	Std
1	--		Resistive Cell Simulator		HPA582	TI

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.
5. Install thermal pad between heatsink & Q3 and secure with screw. If heatsink is substituted, use appropriate screw thread
6. Provide connectors (##) with assembly, install on J4 and J5 after test
7. Install shunt on J1 during test
8. Install standoffs at board corners, nut on top

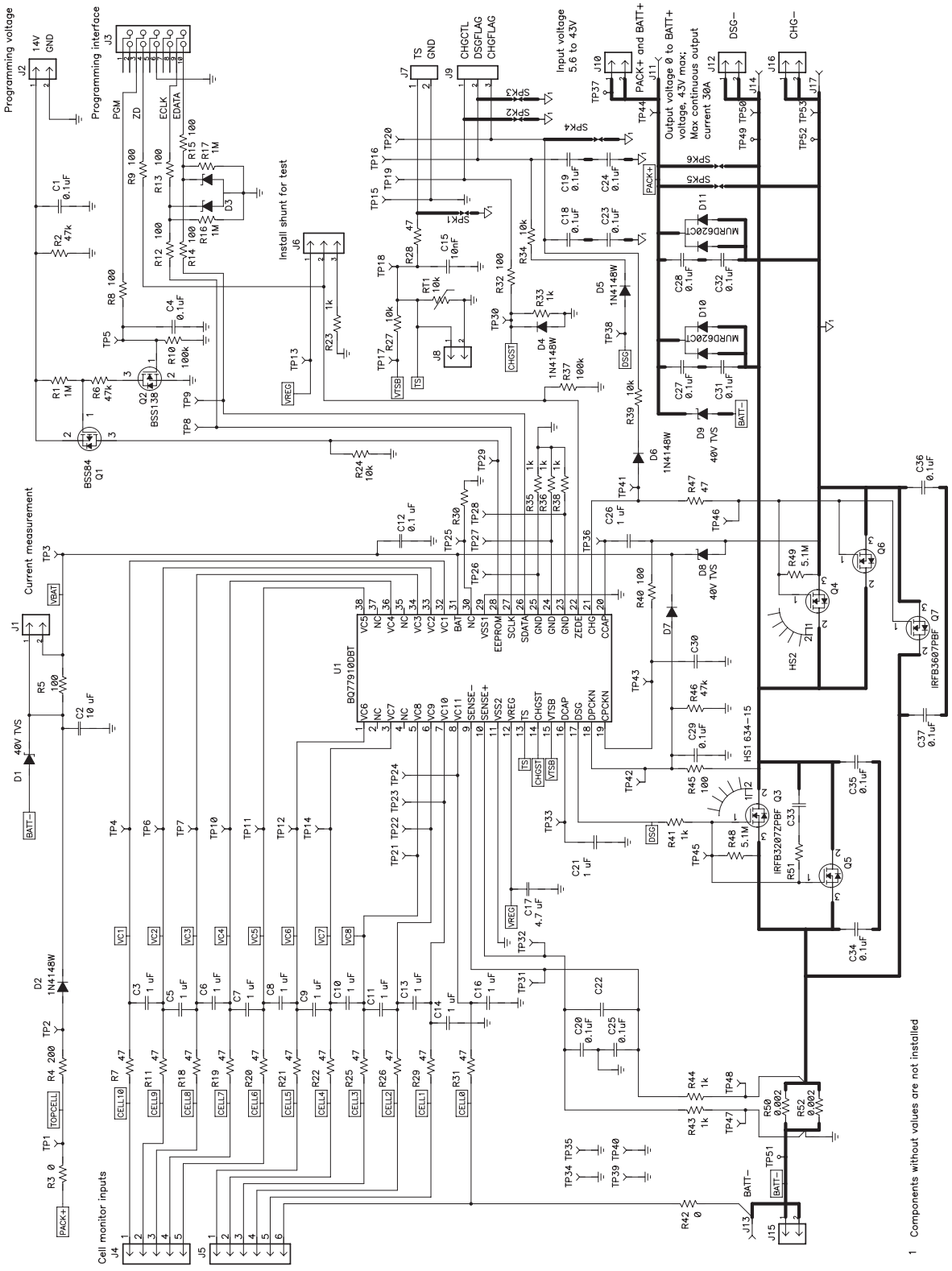

Figure 18. Schematic Diagram page 1

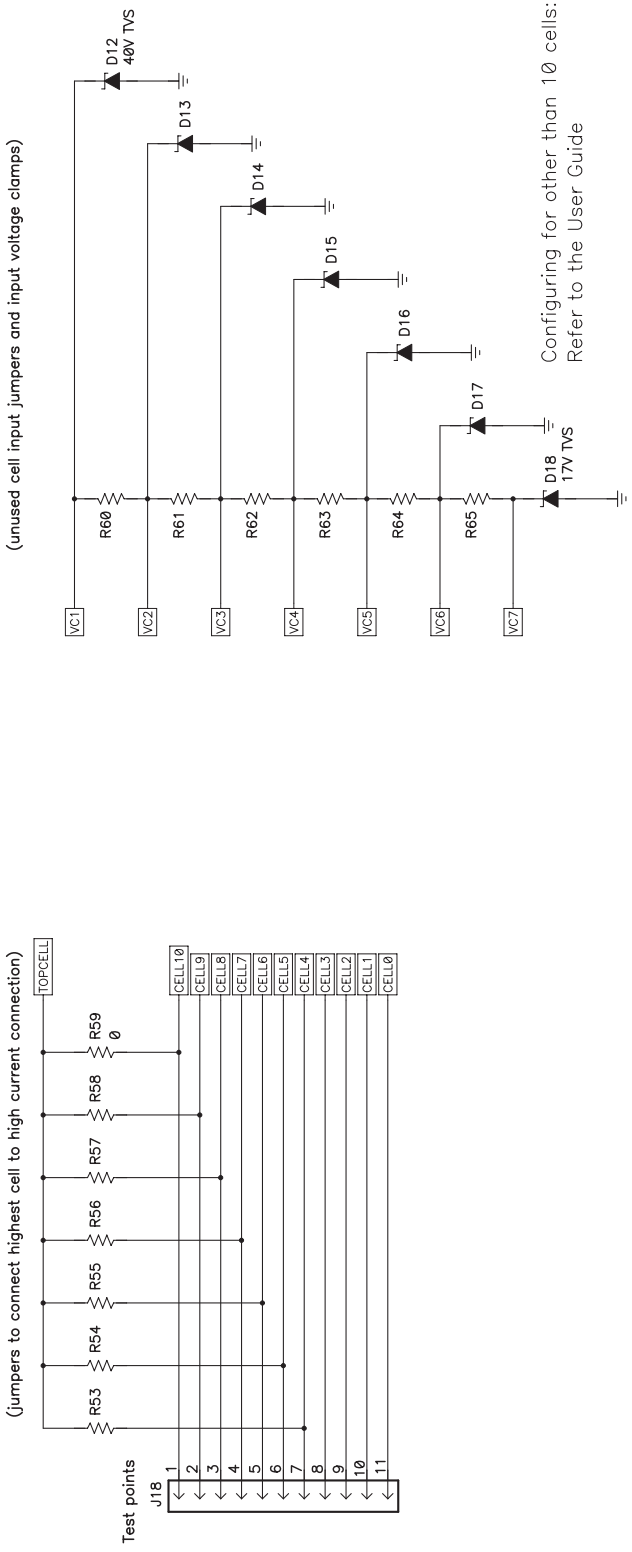

Figure 19. Schematic Diagram page 2

8.1.3 bq77910 Circuit Module Performance Specification Summary

This section summarizes the performance specifications of the bq77910 circuit module in its default 10 cell parallel FET configuration.

Typical voltage will depend on the number of cells configured. Typical current will depend on the application. Board cooling may be required for continuous operation at or below maximum current.

Table 11. Performance Specification Summary

Specification	Min	Typ	Max	Unit
Input voltage PACK+ with respect to BATT-, CHG–, or DSG-	5.6	–	43	V
Continuous discharge current (current into DSG- terminal)	0	–	30	A
Continuous charge current (current into CHG- terminal)	0	-	-6	A

8.2 Resistor Cell Simulator

8.2.1 Board Layout

The resistor cell simulator is a 1.75-inch x 2.00-inch 2-layer circuit card assembly. It is designed for easy connection to the bq77910 circuit card assembly using the connectors on the bottom side. Additional patterns are included on the board for test points.

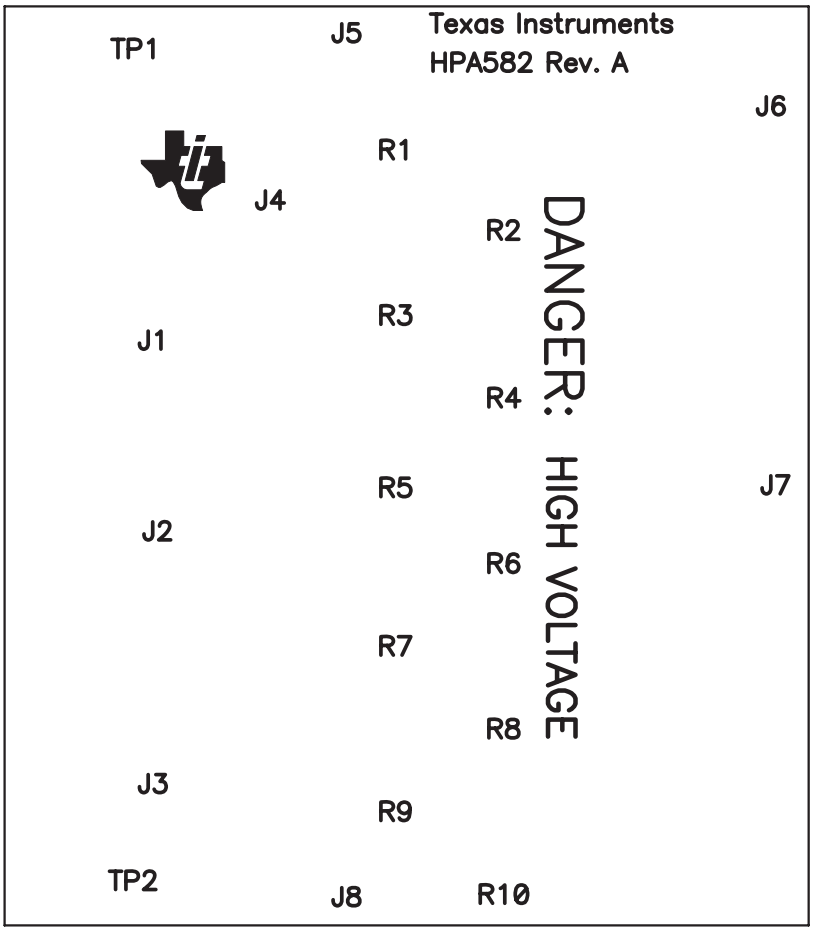

Figure 20. Resistor Simulator Top Silk Screen

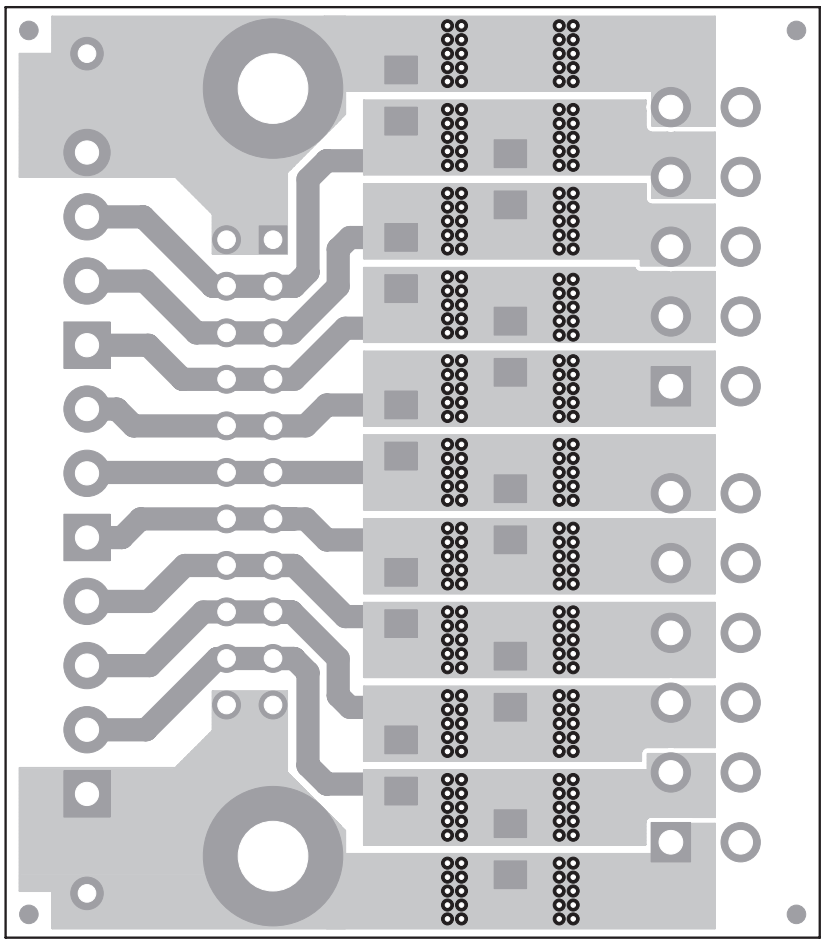

Figure 21. Resistor Simulator Top Layer

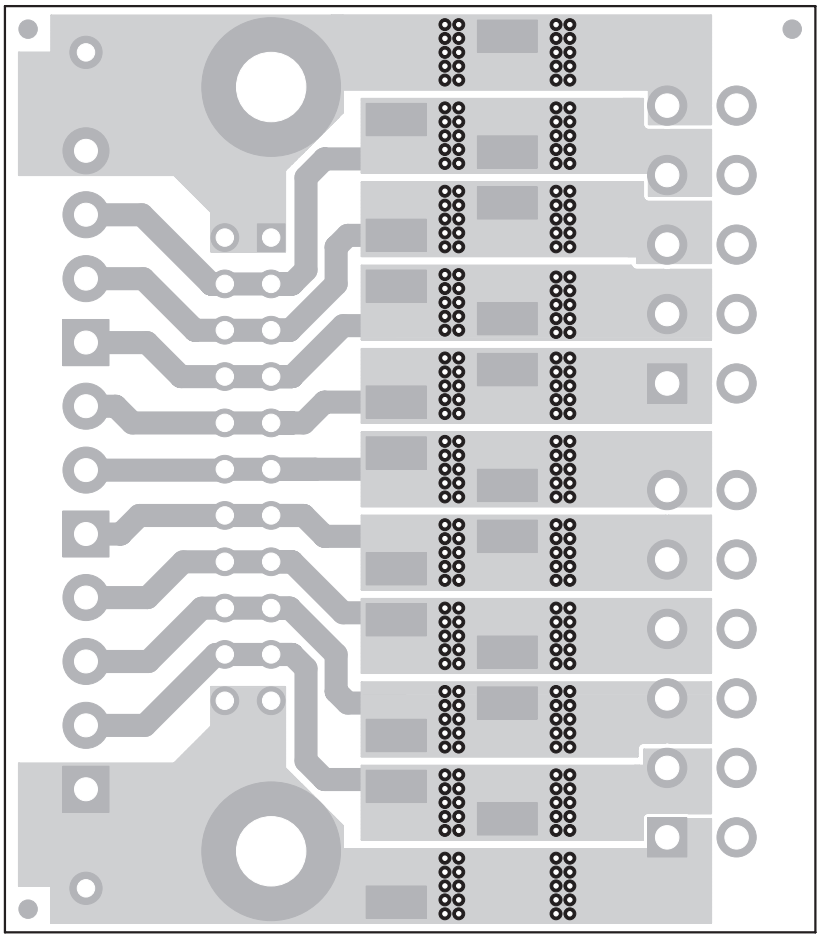

Figure 22. Resistor Simulator Bottom Layer

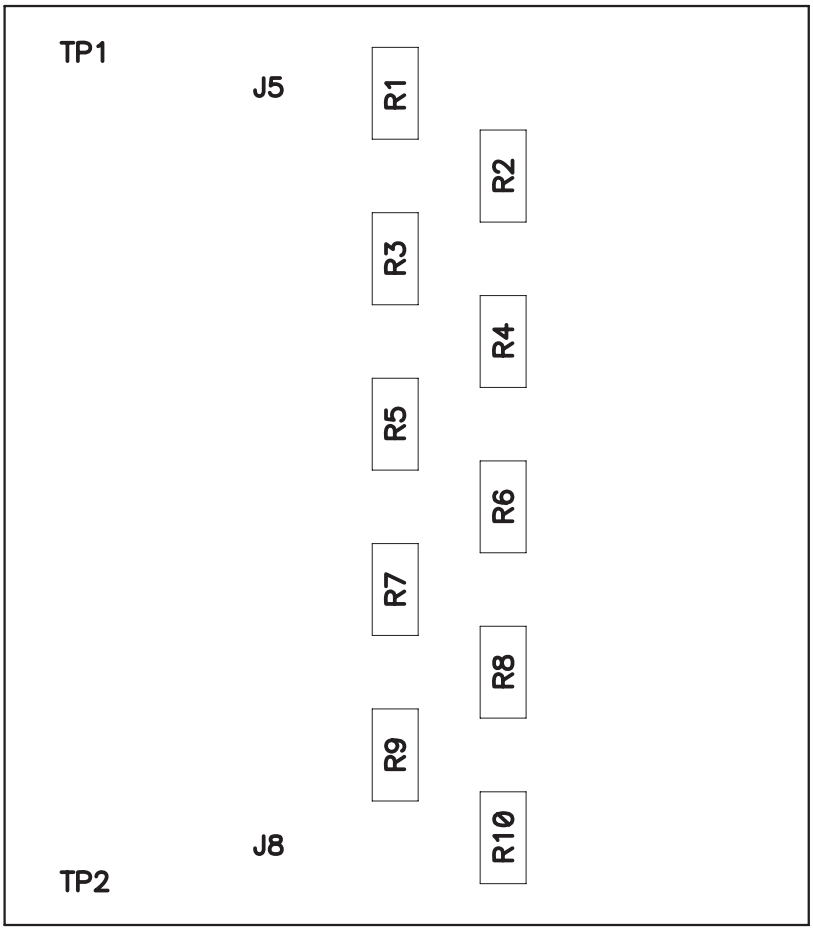

Figure 23. Resistor Simulator Top Assembly

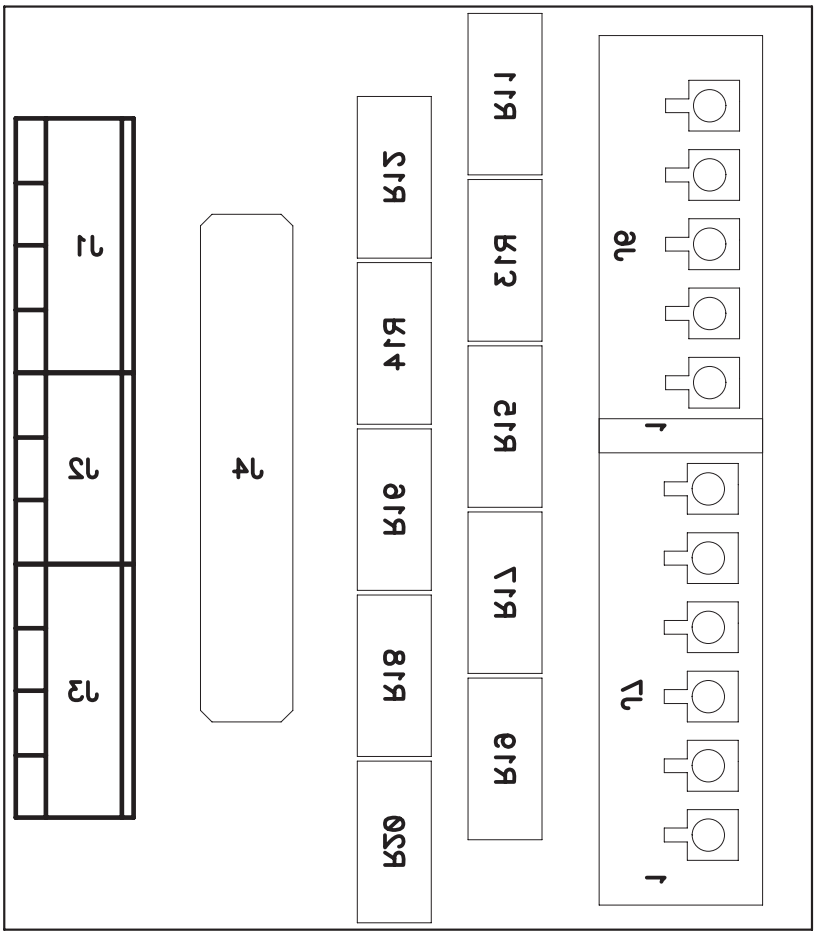

Figure 24. Resistor Simulator Bottom assembly

8.2.2 Resistor Simulator Bill of Materials

The bill of materials for the Resistor Simulator circuit module is shown inTable 12.

Table 12. Resistor Simulator Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	J1, J3		Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25 inch	ED555/4DS	OST
0	J2		Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
0	J4		Header, Male 2x11-pin, 100mil spacing	0.100 inch x 11 x 2	PEC11DAAN	Sullins
0	J5, J8		150-mil hole for standard banana plug	0.300 dia inch		
1	J6 **	1875454	Header, 8A, 160V, 5-pin, 3.81 mm spacing, Top Entry	6.85 x 22.96 mm	1875454	Phoenix Contact
1	J7 **	1875467	Header, 8A, 160V, 6-pin, 3.81 mm spacing, Top Entry	6.85 x 26.77 mm	1875467	Phoenix Contact
10	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10,	200	Resistor, Metal Film, 1/4 watt, ± 1%	1206	STD	STD
0	R11, R12, R13, R14, R15, R16, R17, R18, R19, R20		Resistor, Chip, 1W, 1%	2512		
0	TP1, TP2		Pad, TH	0.038 inch		
1	--		PCB, 2 In x 1.75 In x 0.062 In		HPA582	Any

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

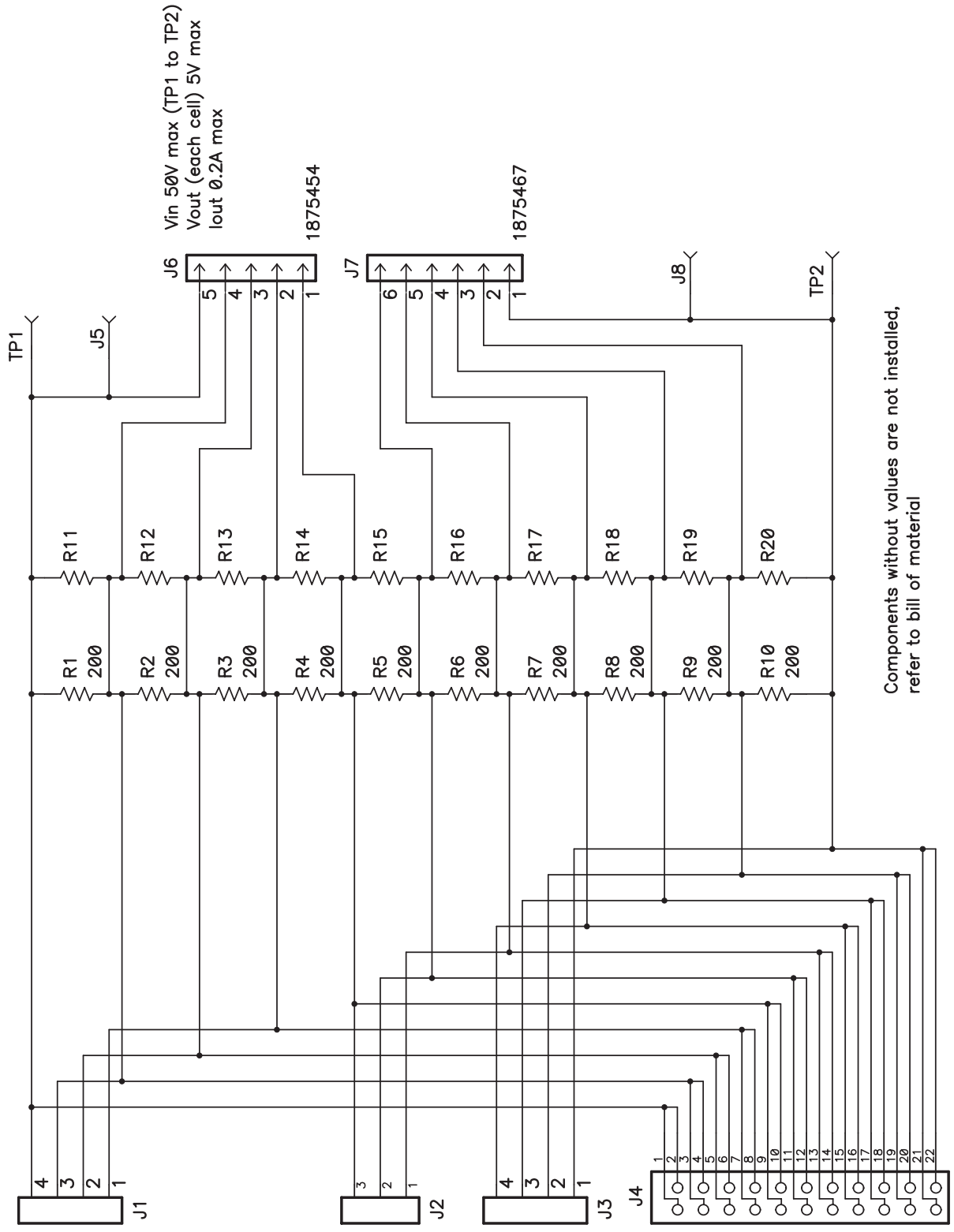

Figure 25. Resistor Simulator Schematic Diagram

Table 13. EVM IMPORTANT NOTICE (CATEGORY B)

IMPORTANT: TI is providing the enclosed bq77910EVM-001 evaluation module under the following conditions:

This evaluation module (EVM) being provided by Texas Instruments (TI) is intended for use for ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY and is not considered by Texas Instruments to be fit for commercial use. As such, this EVM may not be complete in terms of design and/or manufacturing related protective considerations including product safety measures typically found in the end-product incorporating the module. As a prototype, this product does not fall within the scope of the European Union Directive on electromagnetic compatibility and on low voltage and therefore may not meet the technical requirements of the directive. This EVM is not subject to the EU marking requirements.

- **Should this EVM not meet the specifications indicated in the User's Guide the EVM may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**
- The user assumes all responsibility and liability for proper and safe handling of the EVM. The user acknowledge that the use of the EVM could present serious hazards and that it is the user's responsibility to take all precautions for the handling and use of the EVMs in accordance with good laboratory practices. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.
- **NEITHER PARTY WILL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.**
- TI is currently dealing with various customers for products, and therefore our arrangement with the user **will not be exclusive**.
- TI **assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.
- Please read the User's Guide and specifically the section in the User's Guide pertaining to warnings and restrictions prior to handling the product. This section contains important information regarding high temperature and voltages which TI recommends to be read before handling the EVMs. In case of any doubt regarding safety, please contact the TI application engineer.
- Persons handling the product should have electronics training and observe good laboratory practice standards.
- No license is granted under any patent right or other intellectual property right of TI covering or relating to any combination, machine, or process in which such TI products or services might be or are used.
- This Agreement is subject to the laws of the State of Texas, excluding the body of conflicts of laws and the United Nations Convention on the International Sale of Goods, and will be subject to the exclusive jurisdiction of the courts of the State of Texas.

Table 14. EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage and the output voltage ranges as specified in the table below.

Input Range, $V_{BATTERY+}$	0 V to 43 V
Output Range, V_{PACK+}	0 V to 43 V

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Table 15. FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265