bq24185 Evaluation Module

The bq24185 evaluation module allows for the complete evaluation of the bq24185, a switch-mode, charge-management device for single-cell, Li-ion and Li-polymer batteries used in a wide range of portable applications. This document provides a test summary, equipment setup, and the procedures for using with a single-cell battery or a simulated battery load.

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1 Introduction

1.1 EVM Features

- Evaluation module for bq24185
- High-efficiency, fully integrated NMOS-NMOS synchronous buck charger with 3-MHz frequency
- Integrated power FETs for up to 1.5-A charge rate
- Programmable battery voltage, charge current, and input current via I^2C interface
- Input operating range 4-V to 9.5-V normal and 9.5-V to 16-V limited operation
- Switched battery power, DCOUT
- LED indication for status signals
- Test points for key signals available for testing purpose. Easy probe hook-up
- Jumpers available. Easy-to-change connections.

1.2 General Description

The bq24185 evaluation module is a complete charger module for evaluating compact, flexible, high-efficiency, USB-friendly, switch-mode, charge-management solutions for single-cell, Li-ion and Li-polymer batteries used in a wide range of portable applications.

The bq24185 integrates a synchronous PWM controller, power MOSFETs, input current sensing, high-accuracy current and voltage regulation, and charge termination into a small WCSP package.

The charge parameters can be programmed through an I^2C interface.

For details, see the bq24185 data sheet (SLUSA43).

1.3 I/O Description

Jack	Description
J1–DC+	AC adapter or USB, positive output
J1–GND	AC adapter or USB, ground
J2–(CSOUT)	Connect to battery positive terminal
J2–BAT– (GND)	Battery negative terminal, connect to ground (DC–)
J5–SCL	I^2C clock, connect to SCL pin
J5–SDA	I^2C data, connect to SDA pin
J5–GND	AC adapter or USB, ground
J4–Communication Connector	Connect to 10-pin ribbon cable to USB interface adapter
J3–DCOUT	Switched battery connection
J3–GND	AC adapter or USB, ground
J6–TS	Connect to external 4.7-kΩ NTC thermistor if JMP4 is removed.
J6–STAT	External status monitor connection; set JMP3 shunt to EXT
J6–INT	Status indication for host processor
J6–GND	Ground reference connection
J7 +	I^2C optional bias (+)
J7 -	I^2C optional bias return (-)

1.4 Control and Key Parameters Setting

Jack	Description	Factory Setting
JP1	HI 1-2: CD high (Disables charge) LO 2-3: CD low (Enables charge)	Jumper on LO (2-3)
JP2	HI 1-2: high (USB source connected) LO 1-2: low (Adapter source connected)	Jumper on (1-2)
JP3	LED 1-2: Connect STAT pin to LED on EVM EXT 2-3: Connect STAT pin to J6-3	Jumper on LED (1-2)
JP4	Shunt off: High Impedance (Charger disabled in Default mode) Shunt on 1/2: TS biased with fixed 4.7-kΩ resistor	Jumper on TS (1-2)
JP5	SCL 1-2: Available pullup to I^2C bias (J7 - 1/2)	No jumper
JP6	SDA 1-2: Available pullup to I^2C bias (J7 - 1/2)	No jumper

1.5 Recommended Operating Conditions

		Min	Typ	Max	Unit	Notes
Supply voltage, V_{IN}	Input charger voltage from ac adapter input, J1	4	5	9	V	Change mode
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal of J8	0	3-4.2	4.44	V	
Supply current, I_{AC}	Maximum input current from ac adapter input	0	0.1–0.5	1.5	A	
Charge current, I_{chrg}	Battery charge current	0.55	0.7	1.5	A	
Operating junction temperature range, T_J		0		125	°C	
5 Vdc out on J1	Boost Mode Output (USB) on J1		5.05		V	Boost mode

2 Test Summary

2.1 Equipment

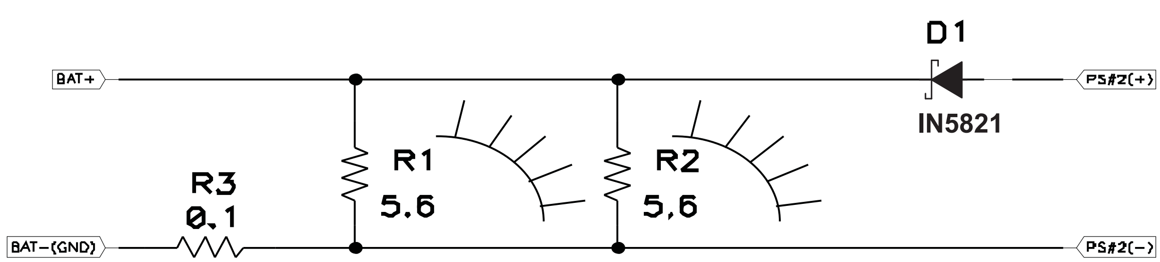
2.1.1 Power Supplies

Power Supply 1 (PS#1) is a power supply capable of supplying 5 V at 2 A.

Optional Power Supply 2 is for use with optional battery simulated load (PS#2), a power supply capable of supplying 5 V at 2 A.

2.1.2 Battery Pack or Simulated Load

A Li-ion, single-cell pack with capacity of at least 1200 mAh can be used or a simulated load of 2.8 Ω (two 5.6-Ω, ≥ 10-W power resistors in parallel), with a 0.1-Ω current sense in the return to the unit under test and a power silicon diode (cathode) connected to the BAT+ side of the load.



Simulated Battery Load Circuit

2.2 DCOUT Load #2

A ≥ 25-Ω, ≥ 3-W power resistor

2.3 Multimeters and Oscilloscope

Three Fluke 75, (equivalent or better) multimeters

Oscilloscope that can capture 10-MHz waveforms

2.4 Computer

A computer with at least one USB port and a USB cable. The bq24185 evaluation software must be properly installed.

2.5 HPA172 Communication Kit

A HPA172 USB to I^2C communication kit.

2.6 Software

1.0 bq24185A_Gui_Software.Zip

Double-click on the SETUP.EXE file. Follow the installation steps.

3 Equipment Setup

1. Set PS#1 for 5 V ±100 mVdc, 1.7 ±0.1-A current limit and then turn off supply. Connect the output of PS#1 to J1 (DC+, DC–).
2. If simulated battery circuit is used in place of a battery, set the PS#2 for 3.5 V ±100 mVdc, 1.8 ±0.1-A current limit and then turn off supply.
3. Connect the battery (discharged to ~3.1 V) or simulated battery load to J2 as shown in Figure 2. If simulated load is used, connect the output of PS#2 (+ lead) to the anode of the simulated load and return to ground (DC–).
4. Connect the system load to J3 (DCOUT, GND).
5. Connect digital multimeter 1 (DMM#1) across J2 (BAT+, GND), and set to measure DCV (5-V range).
6. Connect DMM#2 across BAT– Sense Resistor (0.1 Ω, ≥ 2 W), and set to measure mVdc (< 300-mV range).
7. Connect DMM#3 across the J3 (DCOUT, GND), and set to measure DCV (5-V range).
8. Connect J4 to HPA172 kit by 10-pin ribbon cable. Connect the USB port of the HPA172 kit to the USB port of the computer. The connections are shown in Figure 1.

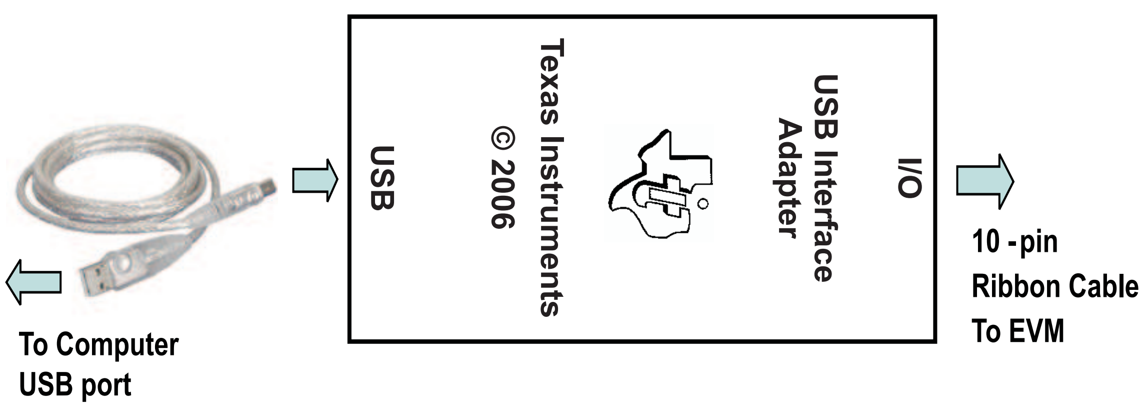


Figure 1. Connections of HPA172 Kit

9. Install jumpers JMP1-2/3 (CD, GND); JMP2-1/2 (PSEL, HI); JMP3-1/2 (LED); JMP4-2/3 (TS_4.7k, GND)
10. Connect scope to TP9 and set to 2 V/div and 200 ns/div (not shown in setup).

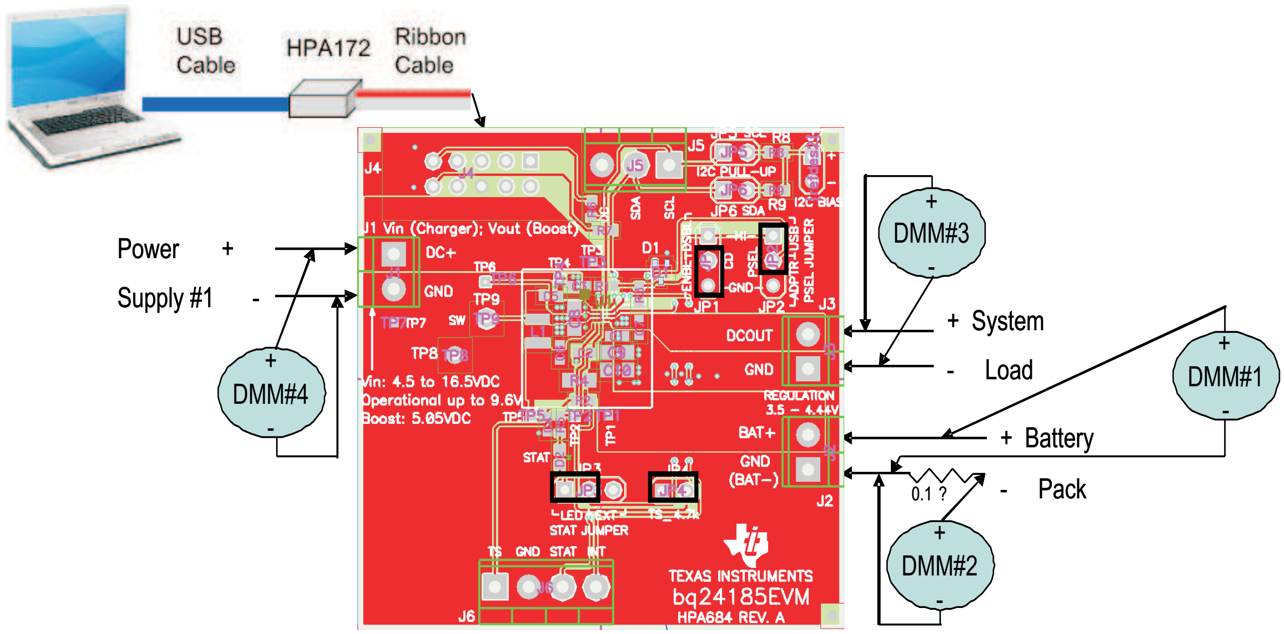


Figure 2. Evaluation Setup

11. Ensure that EQUIPMENT SETUP steps are followed. Turn on the computer. Open the bq24185 evaluation software, by double-clicking on bq24185.exe (file found in the product folder, but needs to be uploaded to the computer running the test). The main window of the software is shown in Figure 3.

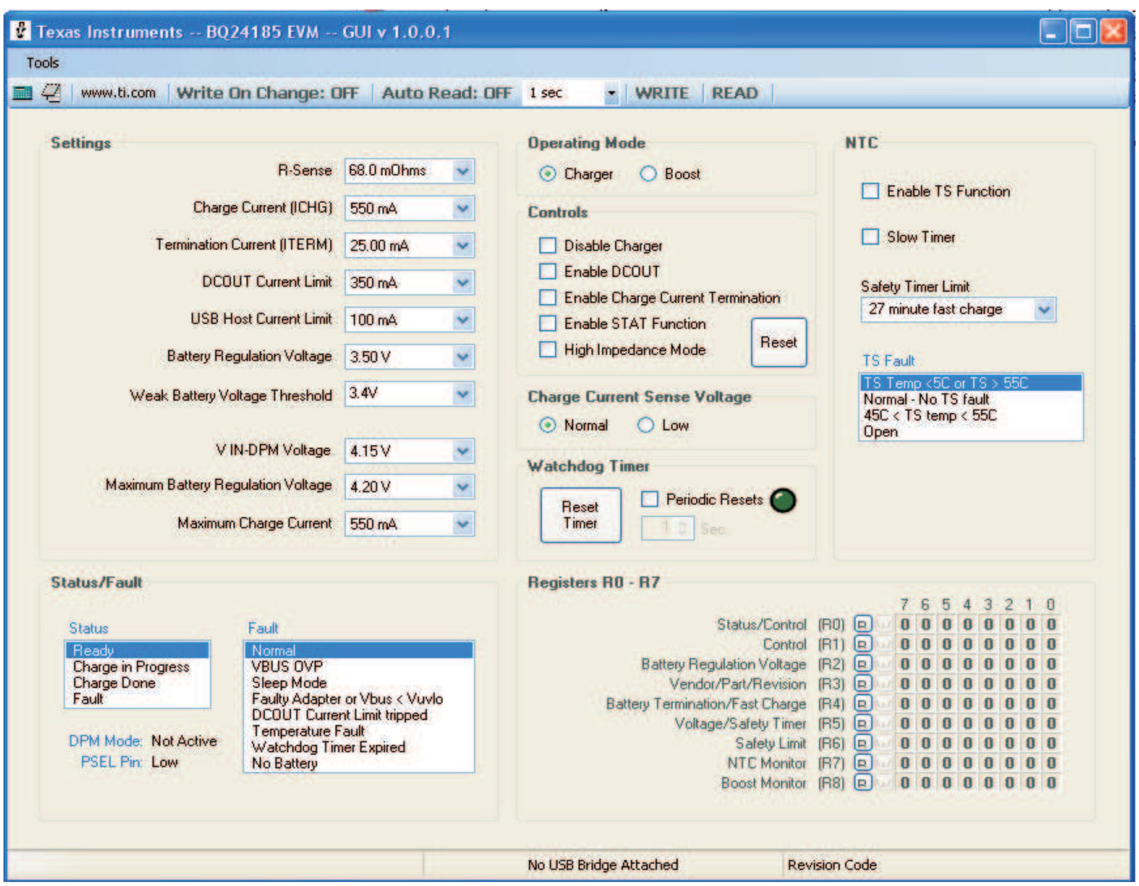


Figure 3. Main Window of bq24185 Evaluation Software

4 Procedure for Use With a Single-Cell Li-Ion Battery or a Simulated Battery Load

4.1 Charge Voltage and Current Regulation

- Turn on PS#2 if simulated battery load is used and then PS#1.
- Software setup:
  (a) Under **Settings**: Set ***Maximum Battery Regulation Voltage*** to 4.3 V via the pulldown window.
  (b) Under **Settings**: Set ***Maximum Charge Current*** to 1.55 A via the pulldown window.
  (c) Under **Registers R0-R7**: Click the Write button ***(W)*** by the ***Safety Limit (R6)*** in the lower right corner. These values can only be changed on the first write command after having been powered by the battery.
  (d) Under **Watchdog Timer**: Check the ***Periodic Resets*** box, and set time to 20 s.
  (e) On the **Top Tool Bar**: Select the ***Write On Change*** button to turn to ON.
  (f) On the **Top Tool Bar**: Select the ***Auto Read*** button to turn to ON, and set the time to 10 s via the pulldown window.
- Measure and verify the following conditions:
  - **Verify** → Meter #1 is between 3.0 and 3.4 V. (If battery is used and its voltage is over the default regulation voltage, then there is no charge current.)
  - **Verify** → Meter #2 is between 9 mV and 15 mV (90 mA to 150 mA)
  - **Verify** → Meter #3 is between 0.0 and 0.1 V.
  - **Verify** → Input Current of PS#1 is between 80 mA and 100 mA.
  - **Verify** → The ***STAT* LED**, on the UUT, is off (disabled).

  This is an example of default mode where the input current limit is 100 mA, maximum, with a maximum regulation of 3.5 V. If V_{BAT} > 3.5 V, then the charge current goes to zero.
- Operation changes via software:
  (a) Under **Settings**: Set ***Battery Regulation Voltage*** to 4.0 V via the pulldown window.
  (b) Under **Settings**: Set ***USB Host Current Limit*** to ***No Limit*** via the pulldown window.
  (c) Under **Settings**: Set ***Charge Current (ICHG)*** to 1.15 A via the pulldown window.
  (d) Under **Controls**: Check the ***Enable DCOUT*** box.
  (e) Under **Controls**: Check the ***Enable STAT Function*** box.
- Measure and verify the following conditions:
  - **Verify** → Meter #1 is between 3.2 V and 3.6 V.
  - **Verify** → Meter #2 is between 80 mV and 120 mV (800 mA to 1200 mA).
  - **Verify** → Meter #3 is between 3.2 V and 3.6 V.
  - **Verify** → Input Current of PS#1 is between 75 mV and 100 mV (750 mA and 1000 mA).
  - **Verify** → The ***STAT* LED**, on the UUT, is on (enabled).

  This shows operation in fast charge constant current.
- Measure TP9 with ground sleeve of oscilloscope probe touching TP8 (GND). Set the oscilloscope to 200 ns/div and 2 V/div. The waveform must look like Figure 4 with the following boundaries: frequency must be 3 MHz ±20%, the amplitude is +5 V ±0.5 V and 0 V to –0.5 V and the duty cycle is 30 ±10% duty cycle.
- Uncheck the Watchdog Timer box, and wait until the charge goes into default mode (less than 35 seconds), and observe that the charge current has dropped to ~125 mA (USB 100-mA input current limit).
- Ground the TS pin by placing a short between J6-TS and J6-GND. This simulates a high-temperature fault in default mode and shuts down the charge current in less than 35 seconds. To return to default mode, remove the short.

  A temperature fault in default mode shuts off the charge, whereas a temperature fault in normal communication mode only notifies the host of a change in its register and does not disable the charge.
- See the data sheet for complete information on all specifications and functions.
- The software menu is intuitive and can be used to change many parameters.
- After evaluation, turn off PS#1 and then PS#2, if used.

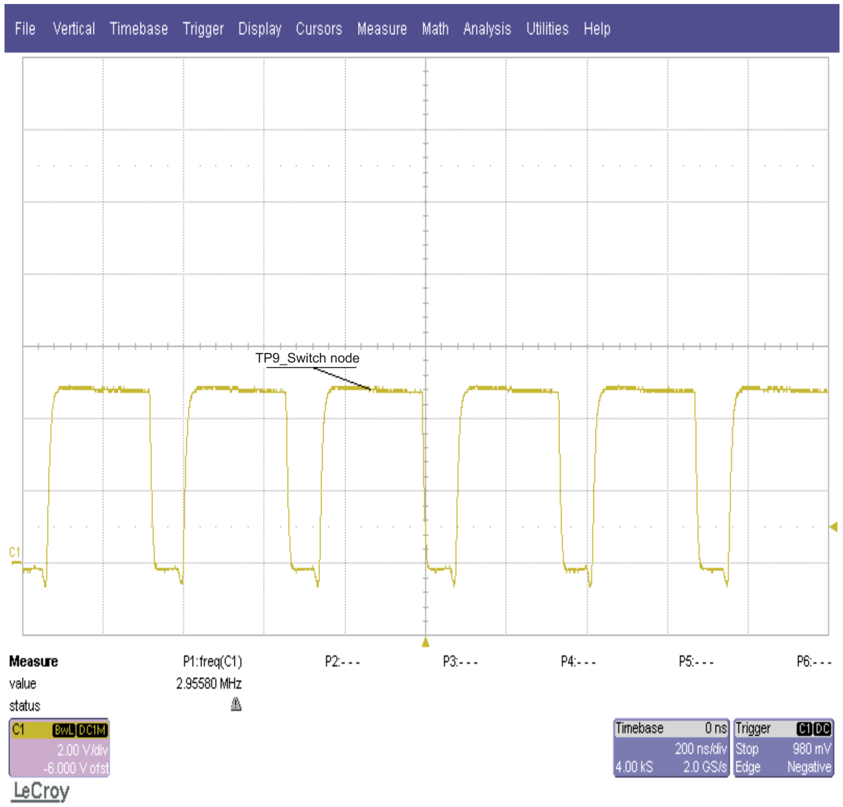
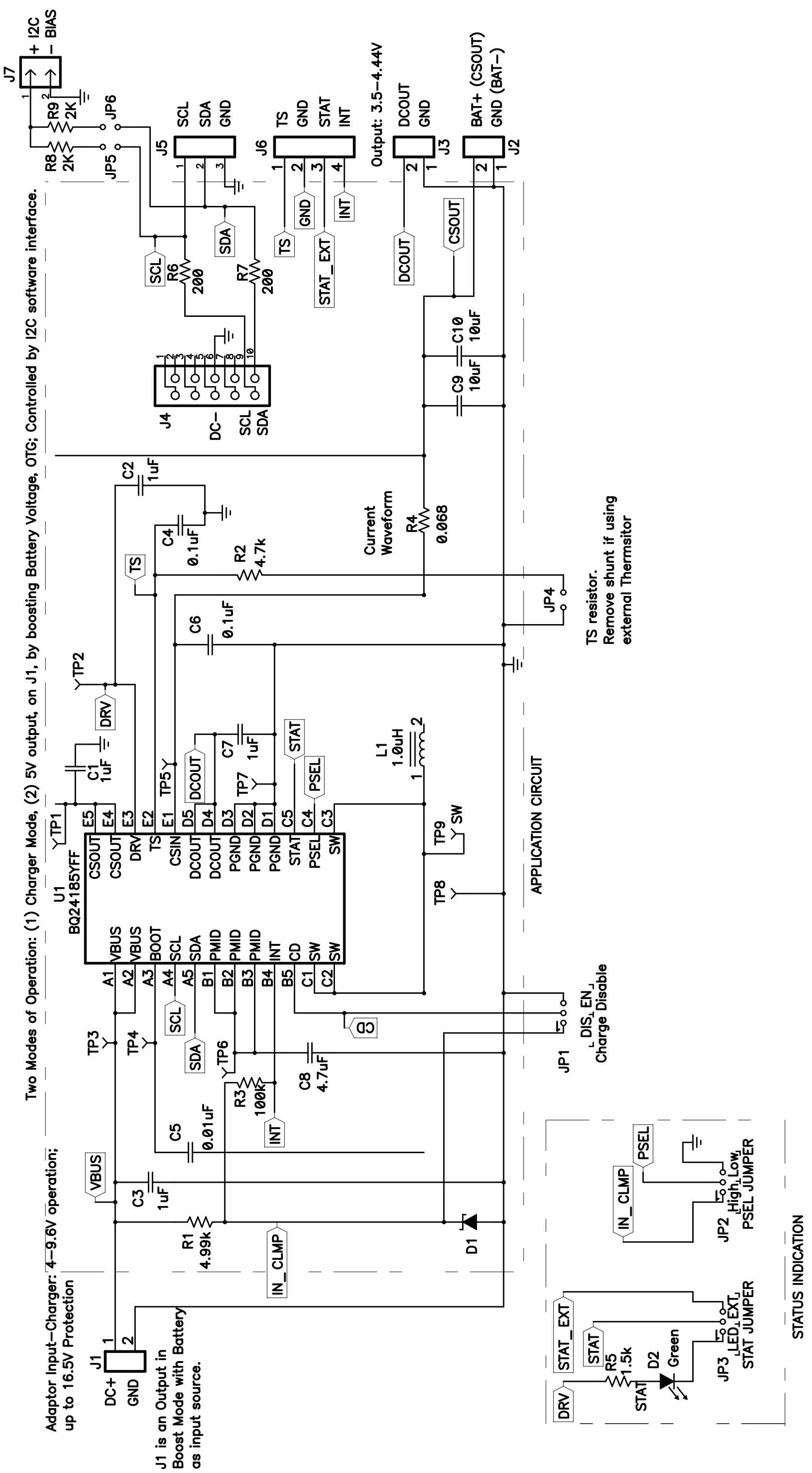


Figure 4. TP9 – Switch Node at 5-Vdc Input and 1.15-A Charge With 3.3-Vdc Battery

5 Schematic



6 Boost Converter Operation (From the Battery to the Input Connector) – OTG

- Remove P/S#1 from J1, and apply 25-Ω load to J1 between pins 1 and 2.
- Turn on P/S#2 and adjust the battery voltage between 3.5 V and 4.2 V, or apply a battery between these voltages to J2.

- Software: Click on Boost under the Charger Mode to enable the boost mode. The watch dog timer "Periodic Resets" box must be set and the time must be less than 25 seconds in order for the boost charger not to shut down.
  - Verify → Meter 4 is between 5.0 and 5.1 Vdc.

7 PCB Layout

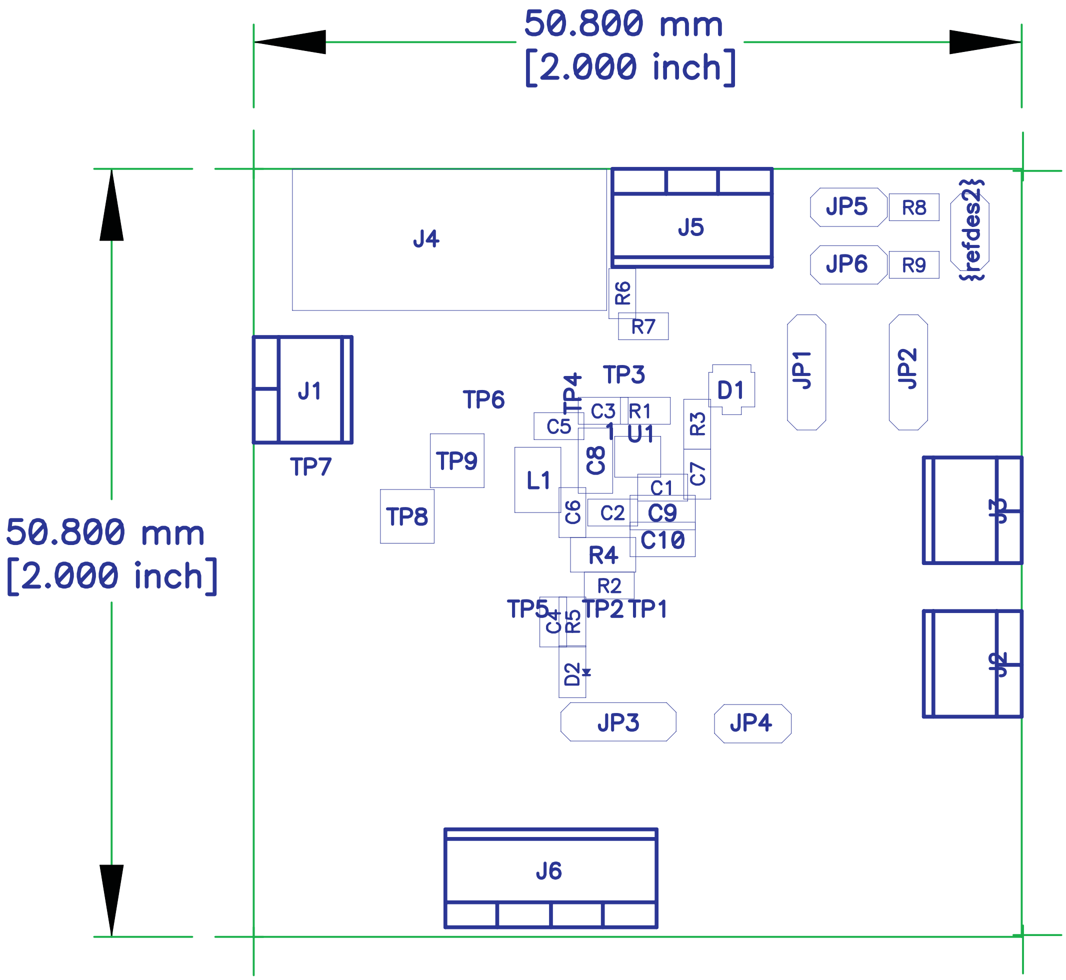


Figure 5. Top Assembly

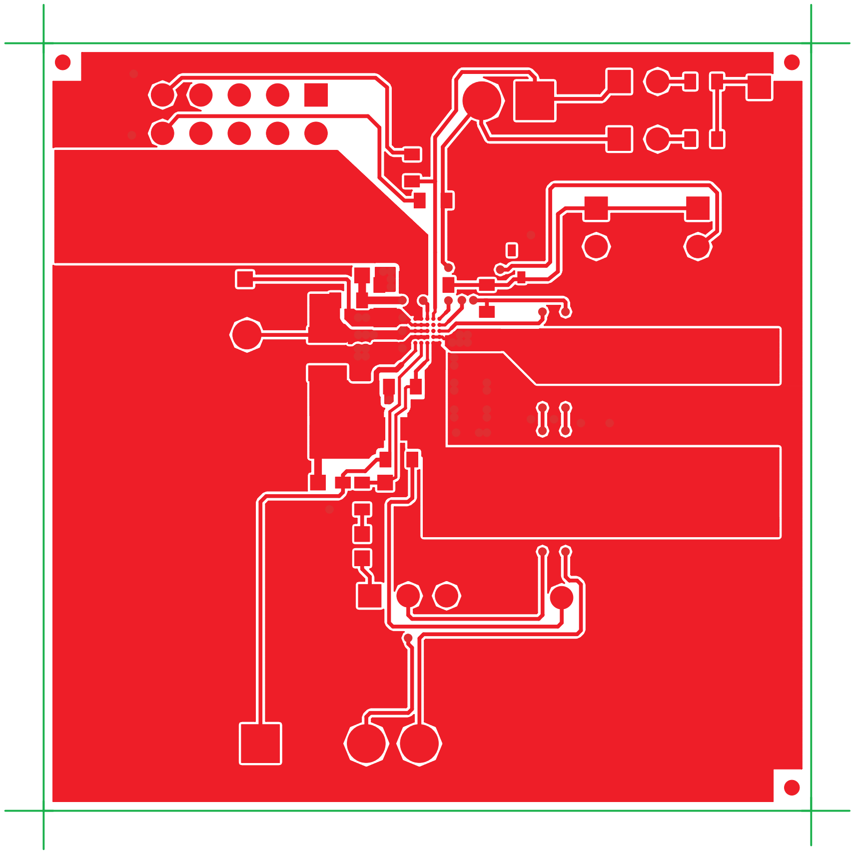


Figure 6. Layer 1

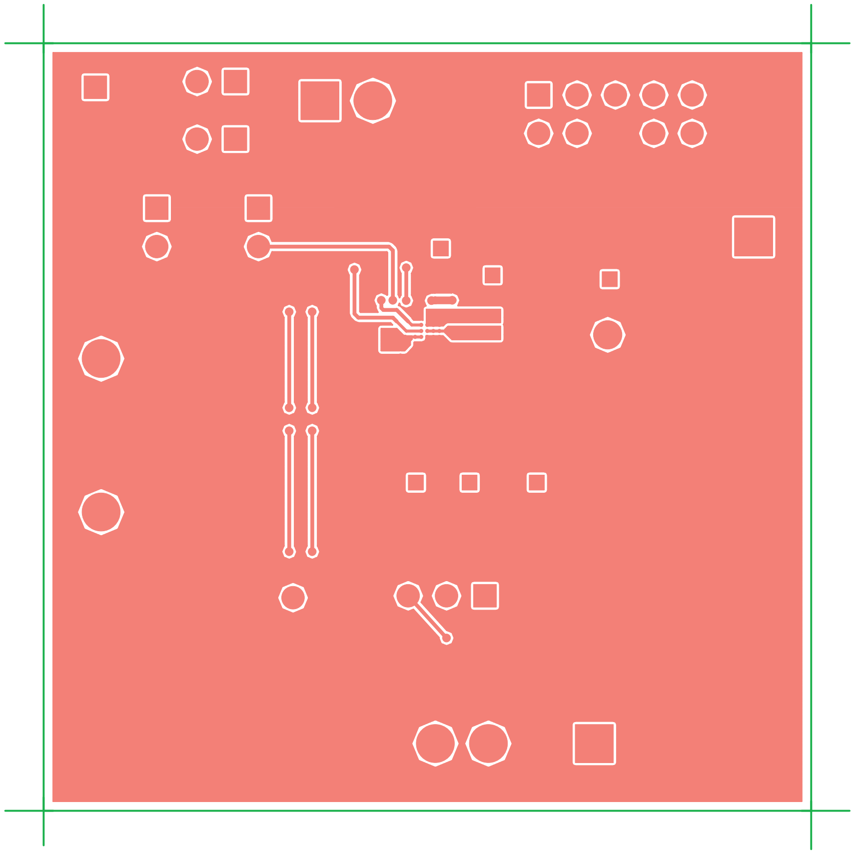


Figure 7. Layer 2

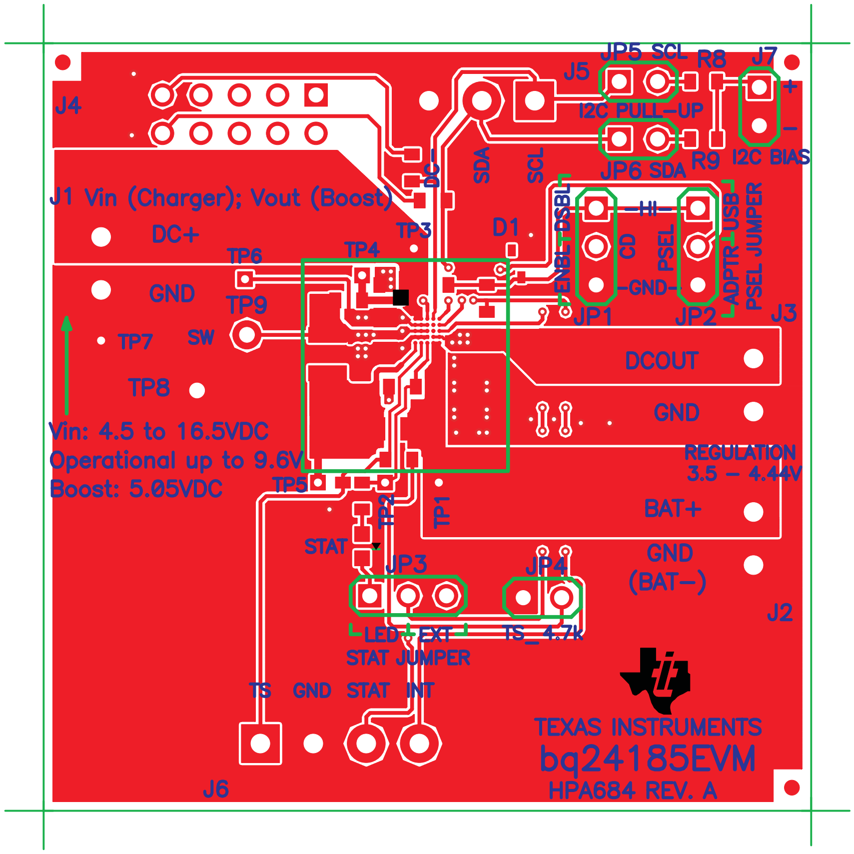


Figure 8. Top Silk

7.1 PCB Layout Guide

1. To obtain optimal performance, the power input capacitors, connected from input to PGND, must be placed as close as possible to the IC.
2. The output inductor must be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high-frequency oscillation problems, proper layout to minimize high-frequency current path loop is critical.
3. The sense resistor must be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers. Do not route the sense leads through a high-current path.
4. Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals must be routed away from the high-current paths.
5. The PCB must have a ground plane (return) connected directly to the return of all components through the vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small-signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power, small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, no ground-bounce issue exists, and having the components segregated minimizes coupling between signals.
6. The high-current charge paths into VBUS, PMID and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins must be connected to the ground plane to return the current through the internal low-side FET.

8 Bill of Materials

Table 1. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
3	C1, C2, C7	1 µF	Capacitor, Ceramic, Low Inductance, 10V, X5R, 10%	0603	Std	Std
1	C3	1 µF	Capacitor, Ceramic, X5R, 16V, ±10%	0603	GRM188R61C105KA93D	Murata
2	C4, C6	0.1 µF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 10%	0603	Std	Std
1	C5	0.01 µF	Capacitor, Ceramic, Low Inductance, 25V, X7R, 10%	0603	Std	Std
1	C8	4.7 µF	Capacitor, Ceramic, 16V, X5R, 10%	0805	GRM21BR61C475KA88L	Murata
2	C9, C10	10 µF	Capacitor, Ceramic, 10V, X5R, 10%	0805	Std	Std
1	D1	BZX84C6V2W-7-F	Diode, Zener, 6.2V, 200-mW	SOT-323	BZX84C6V2W-7-F	Diodes
1	D2	Green	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	0603	LTST-C190GKT	Lite On
3	J1–J3	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
1	J4	2510-6002UB	Connector, Male Straight 2x5 pin, 100mil spacing, 4 Wall	0.338 x 0.788 inch	N2510-6002-RB	3M
1	J5	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
1	J6	ED555/4DS	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25 inch	ED555/4DS	OST
1	J7	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
3	JP1–JP3	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
3	JP4–JP6	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	1.0uH	Inductor, SMT, 1.5A, 80milliohm, ±30%	2.5 x 2.0 mm	LQM2HPN1R0MJ0 or MDT2520-CN1R0M or CP1008	Murata or TOKO or Inter-Technical
1	R1	4.99k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	4.7k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	0.068	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R5	1.5k	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
2	R6, R7	200	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R8, R9	2K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	TP8	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	TP9	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
1	U1	BQ24185YFF	IC, Fully Integrated Switch-Mode One-Cell Li-Ion Charger with Full USB Compliance	WCSP	BQ24185YFF	TI
6		929950-00	Shunts	100 mill	929950-00	3M
1	—		PCB, 2 In x 2 In x 0.031 In		HPA684	Any

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.
5. Installed jumpers JMP1-2/3 (CD, GND); JMP2-1/2 (PSEL, HI); JMP3-1/2 (LED); JMP4-1/2 (TS_4.7k, GND), J5 and J6 on just pin 1.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 16 V and the output voltage range of 0 V to 4.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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