# Using the UCC27611OLEVM-203

# User's Guide

Literature Number: SLUUA64
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# Using the UCC27611OLEVM-203

## 1 Introduction

This EVM is to aid in evaluating UCC27611. UCC27611 is a high-speed, single channel, low-side driver capable of driving eGANFETs. The UCC27611 device can accept a wide range VDD input (4 V to 18 V) and provide a regulated 5-V output which is well-suited to drive GaN FETs without exceeding their maximum gate-to-source voltage ratings.

## 2 Description

The EVM consists of a single UCC27611 device with all its pins accessible through test points. The EVM is designed to drive a capacitive load on the output of the device, but connectors are provided to offer flexibility to bring the output signal outside the board. The EVM allows user to evaluate the UCC27611 device standalone operation under different VDD bias voltages, capacitive loads, switching frequencies and with either non-inverting or inverting input signals. In summary, the EVM is an extremely useful tool for determining the drive circuit component parameters for the relevant end application.

### *2.1 Typical Applications*

- Demonstrate driving eGaNFETs such as EPC2001 with 6-V gate-to-source voltage absolute maximum ratings.
- Determine UCC27611 gate drive circuit component parameters relevant for end application by emulating eGANFET $Q_G$ with a fixed capacitive load and study performance.

### *2.2 Features*

- All pins of UCC27611 accessible through test point.
- Test points, jumper heads, and switches to facilitate evaluation.
- Provision for testing under no load, 100 pF, 1 nF load or user selectable load (C6).

## 3 Electrical Performance Specifications

**Table 1. UCC27611OLEVM-203 Electrical Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Input Characteristics** | | | | | |
| Voltage range $V_{DD}$ | | 4 | 10 | 18 | V |
| Input current limit | | | 1 | | A |
| Input PWM signal | | >2.4 | | $V_{DD}$ | V |
| **Output Characteristics** | | | | | |
| Output voltage | magnitude | | 5 | | V |

Operational frequency subject to thermal consideration based on load and package power dissipation.

## 4 Schematic

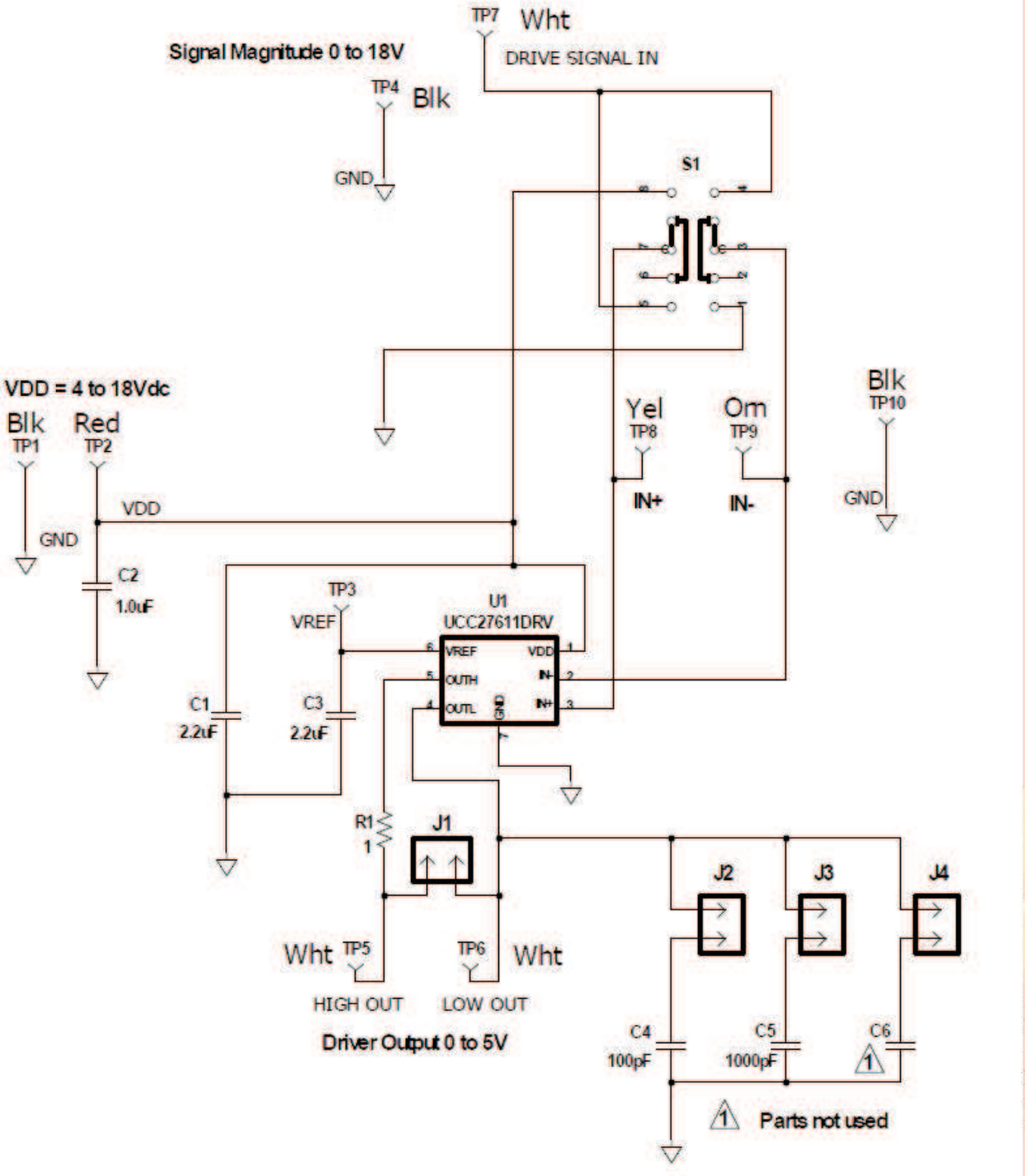


**Figure 1. UCC27611OLEVM-203 Schematic**

# 5 Test Setup

## 5.1 Test Equipment

**Voltage Source for VDD:** 10 V and 1 A.

**Function Generator:** 4 MHz, 50% duty cycle, 0-V to 5-V magnitude.

**Oscilloscope:** 350-MHz bandwidth, three channels, 2 V/div. and 5 ns/div.

**Recommended Wire Gauge:** AWG #18.

## 5.2 Recommended Test Setup

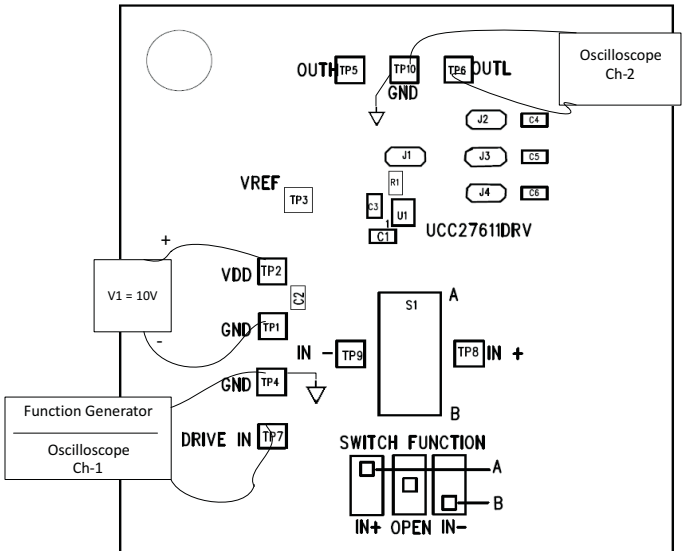


**Figure 2. Recommended Test Set Up**

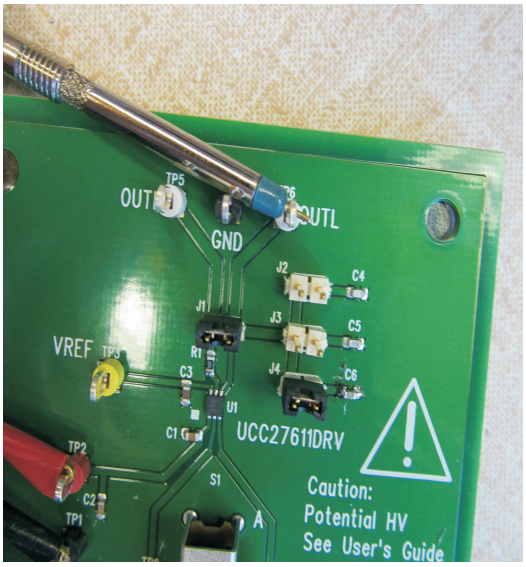


**Figure 3. Recommended Probe Set Up for the measurements on TPS 6**

## 5.3 List of Test Points

**Table 2. Test Point Functions**

| TEST POINTS | NAME | DESCRIPTION |
|---|---|---|
| TP1 | GND | Ground |
| TP2 | VDD | UCC27611 pin 1 |
| TP3 | VREF | Reference voltage |
| TP4 | GND | Ground |
| TP5 | OUTH | UCC27611 pin 5 |
| TP6 | OUTL | UCC27611 pin 4 |
| TP7 | DrIn | Drive Signal Input |
| TP8 | IN+ | UCC27611 pin 3 |
| TP9 | IN- | UCC27611 pin 2 |
| TP10 | GND | Ground |
| J1 | | Jump connection of internal totem pole output |
| J2 | | 100-pF output capacitance selection |
| J3 | | 1000-pF output capacitance selection |
| J4 | | No load or user selectable load (C6) |

# 6 Test Procedure

Set up the EVM based on Figure 2.

## 6.1 Output and Input Relationship

1. Connect voltage source 10 V to TP1 and TP2 to bias UCC27611.
2. Connect function generator to TP4 and TP7 and set up 4 MHz, 50% duty cycle, and magnitude between 0 V and 5 V.
3. Test under no load, place a jumper on J1 and Verify J2, J3 and J4 are open.
4. Connect oscilloscope channel one to input drive signal between TP7 signal and TP4 ground.
5. Connect oscilloscope channel two to output drive signal between TP6 signal and TP10 ground using the method shown in Figure 3.
6. Connect oscilloscope channel three to the $V_{REF}$ signal between TP3 signal and TP10 ground.
7. Power on V1 set switch S1 on position A for non-inverting output.
8. Record reference waveform as shown in Figure 4 through Figure 6.
9. Set switch S1 on position B, and record inverting output as shown in Figure 7 through Figure 9 .

## 6.2 Equipment Shutdown

1. Power off 10-V voltage source.
2. Power off function generator.

# 7 Typical Characteristic

The following figures show the operation of the driver. The first series of three scope shots show the operation of the device with the non-inverting operation and no load on the output. The bottom trace is the input voltage and the top trace is the output. The middle trace is the output of the internal reference. The next two images measure the delay of both the leading edge and training edge of the incoming signal to the leading and trailing edge of the output.

## 7.1 Non-inverting Output

Figure 4 through Figure 6 show the operation with no load on the output and non-inverting input.

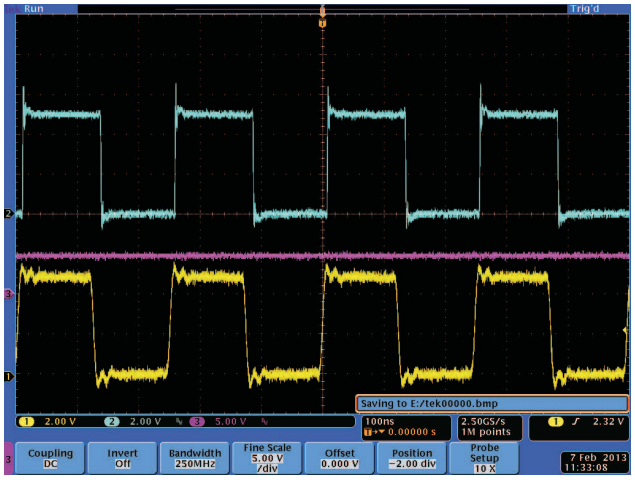


**Figure 4. Non-Inverting Output**

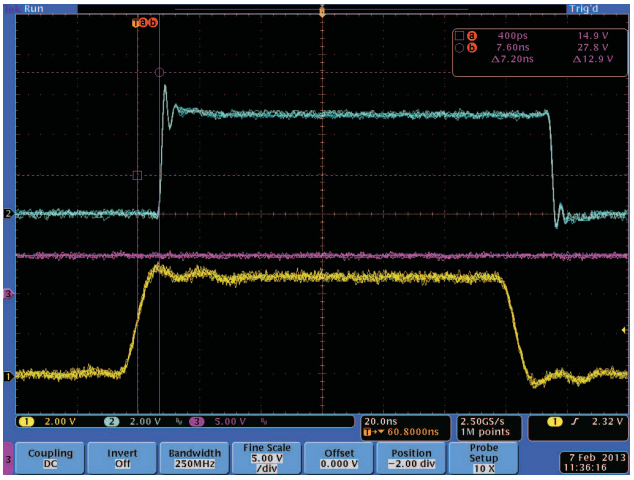


**Figure 5. Non-inverting Output, Input Rising Edge Propagation Delay**

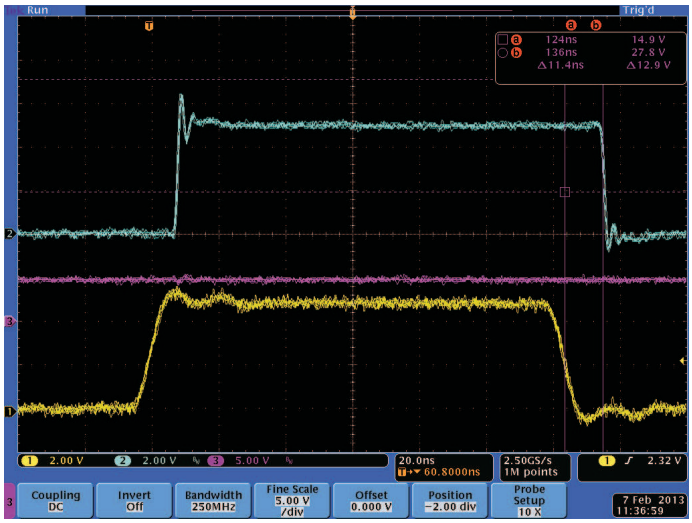


**Figure 6. Non-inverting Output, Input Falling Edge Propagation Delay**

## 7.2 Inverting Output

Figure 7 through Figure 9 have the same conditions as the above but with the input signal going into the inverting input and the operation has with no load on the output and inverting input.

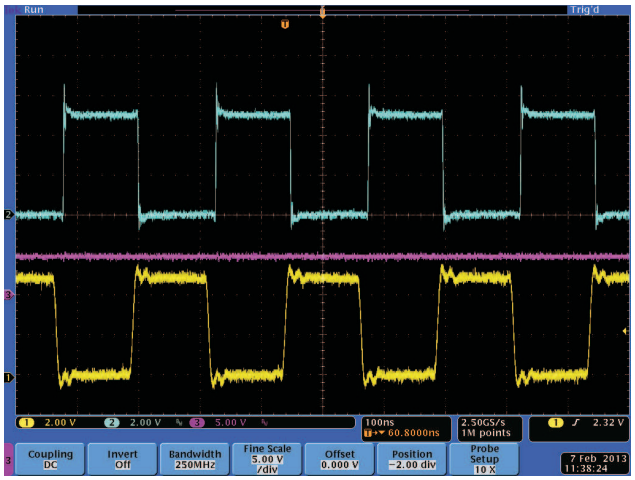


**Figure 7. Inverting Output**

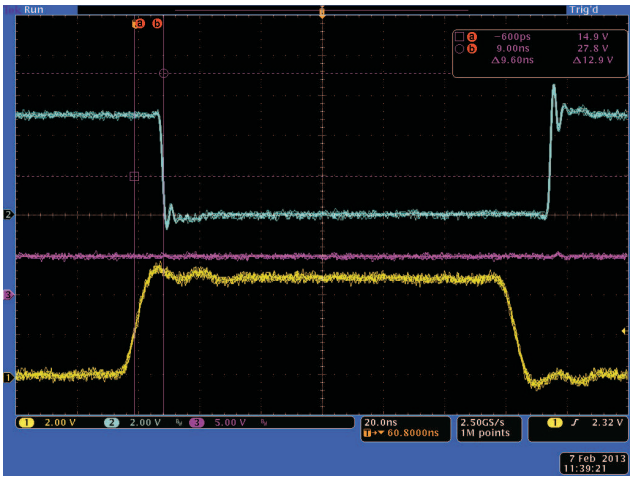


**Figure 8. Inverting Output Input Rising Edge Propagation Delay**

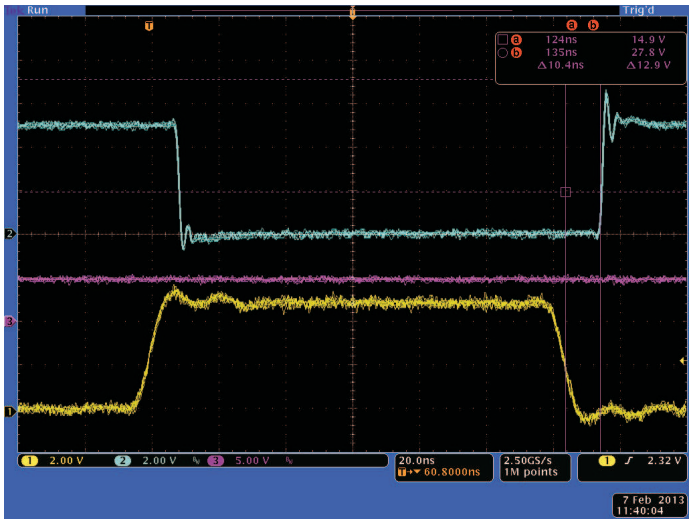


**Figure 9. Inverting Output Input Falling Edge Propagation Delay**

## 8 EVM Assembly Drawing and PCB Layout

The following figures (Figure 10 through Figure 12) show the design of the UCC27611OLEVM-203 printed circuit board. PCB dimensions: L x W = 2.8 inch x 3.5 inch, PCB material: FR402 or compatible, two layers and 2oz copper on each layer.

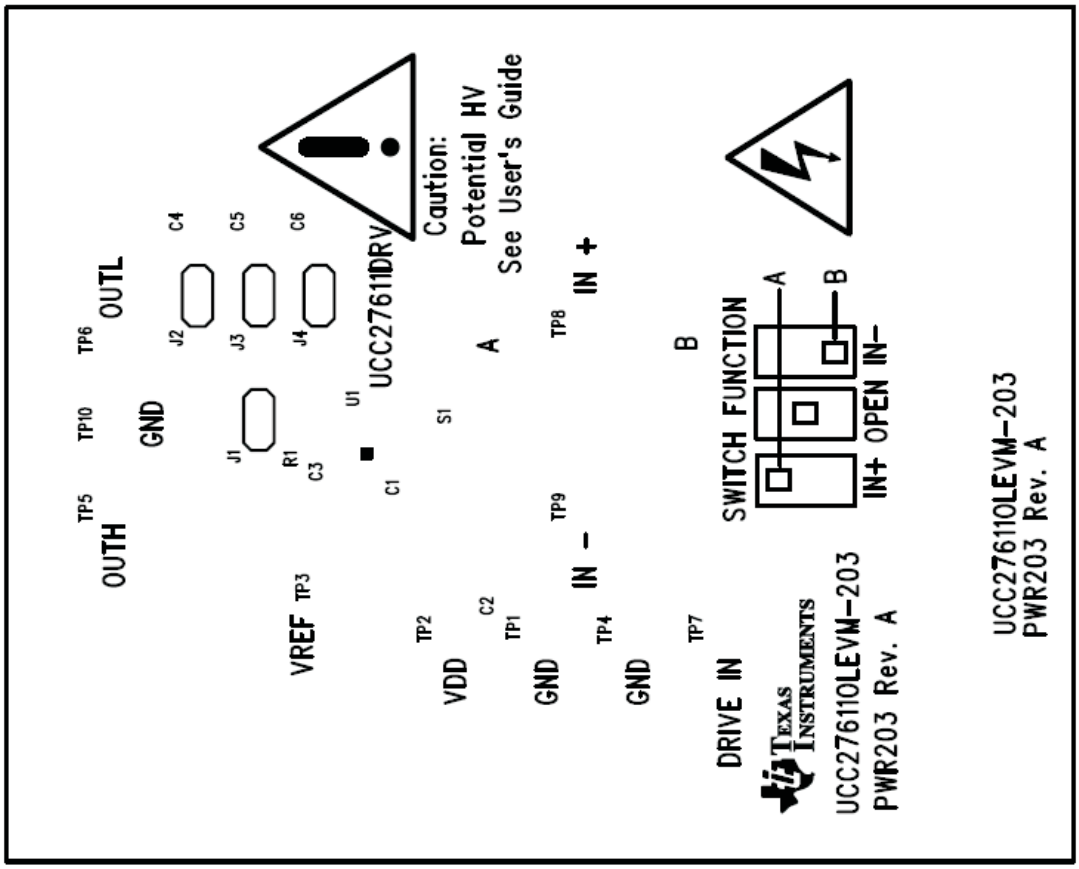


**Figure 10. UCC27611OLEVM-203 Top Layer Assembly Drawing (top view)**

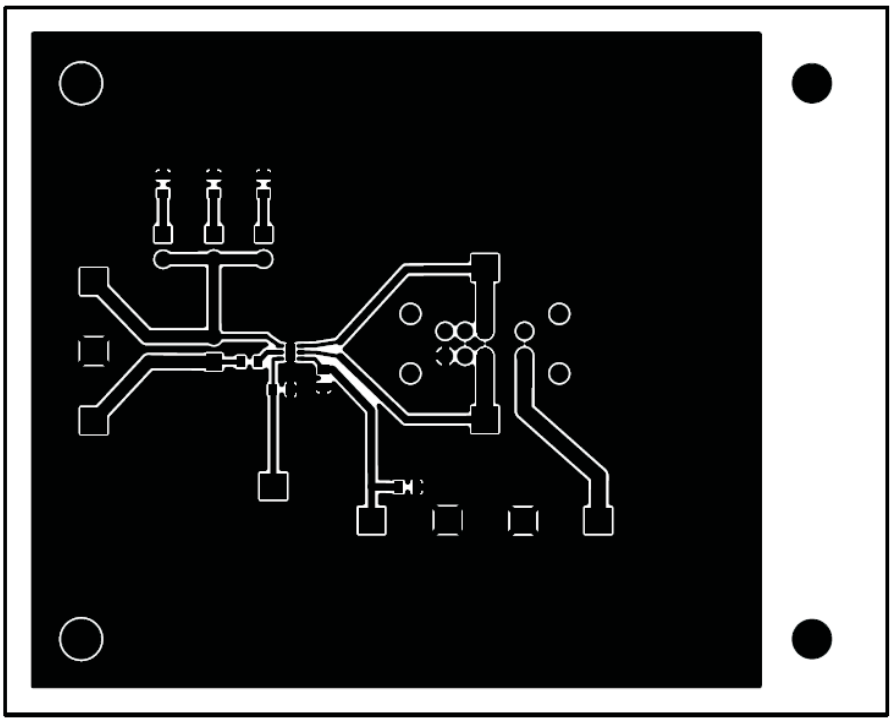

**Figure 11. UCC27611OLEVM-203 Top Copper (top view)**

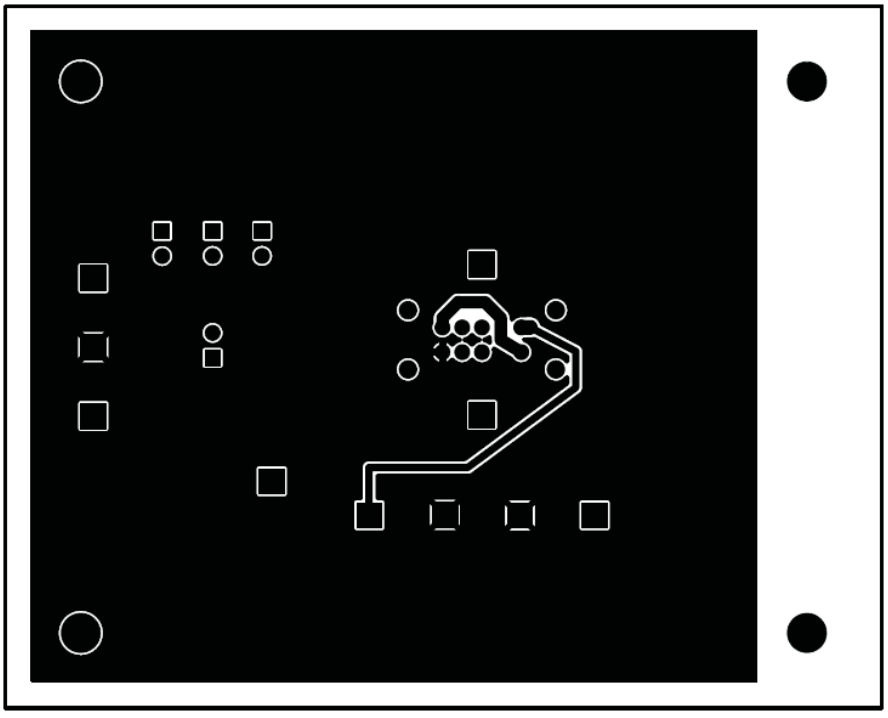

**Figure 12. UCC27611OLEVM-203 Bottom Copper (top view)**

## 9 Listof Materials

The EVM components list according to the schematics shown in Figure 1.

**Table 3. UCC27611OLEVM-203 List of Materials**

| QTY | REF DES | DESCRIPTION | PART NUMBER | MFR |
|---|---|---|---|---|
| 2 | C1, C3 | Capacitor, ceramic, 25 V, X5R, 10%, 2.2 µF, 603 | STD | STD |
| 1 | C2 | Capacitor, ceramic, 25 V, X5R, 10%, 1.0 µF, 603 | STD | STD |
| 1 | C4 | Capacitor, ceramic, 50 V, X7R, 10%, 100 pF, 603 | STD | STD |
| 1 | C5 | Capacitor, ceramic, 50 V, X7R, 10%, 1000 pF, 603 | STD | STD |
| 0 | C6 | Capacitor, ceramic, 50 V, X7R, 10%, OPEN, 603 | STD | STD |
| 4 | J1, J2, J3, J4 | Header, male 2-pin, 100-milimeter spacing, 0.100 inch x 2 inch | PEC02SAAN | Sullins |
| 1 | R1 | Surface mount, I Ω, 603 | STD | STD |
| 1 | S1 | Switch, slide DP3T, 6.5 mm x 16 mm | EG2301A | E-Switch |
| 1 | U1 | 4-A and 8-A Single Channel High-Speed Low-Side Gate Drivers, SOT23-6 | UCC27611DRV | TI |

## 10 References

1. *Driving eGaNTM Transistors for Maximum Performance*, http://epc-co.com/epc/documents/articles/EPC_Driving_eGaN_Transistors_fro_Maximum_Performance.pdf
2. UCC27611, *4-A and 6-A High-Speed 5-V Drive Optimized Single Gate Driver*, (Texas Instruments Literature Number SLUSBA5)

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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