300-mA 40-V LOW-DROPOUT REGULATOR WITH 25-µA QUIESCENT CURRENT

Check for Samples: TPS7A6550-Q1

FEATURES

- **Low Dropout Voltage**
  - **300mV at I_{OUT} = 150mA**
- **4-V to 40-V Wide Input Voltage Range With up to 45-V Transients**
- **300-mA Maximum Output Current**
- **25-µA (Typ) Ultra Low Quiescent Current at Light Loads**
- **3.3-V and 5-V Fixed Output Voltage with ±2% Tolerance**
- **Low-ESR Ceramic Output Stability Capacitor**
- **Integrated Fault Protection**
  - **Short-Circuit/Over-Current Protection**
  - **Thermal Shutdown**
- **Low Input Voltage Tracking**
- **Thermally Enhanced Power Package**
  - **3-pin TO-252 (KVU /DPAK)**

APPLICATIONS

- **Qualified for Automotive Applications**
- **Infotainment Systems with Sleep Mode**
- **Body Control Modules**
- **Always ON Battery Applications**
  - **Gateway Applications**
  - **Remote Keyless Entry Systems**
  - **Immobilizers**

DESCRIPTION

The TPS7A65xx is a series of low dropout linear voltage regulators designed for low power consumption and quiescent current less than 25 µA in light load applications. These devices feature an integrated over-current protection and are designed to achieve stable operation even with low-ESR ceramic output capacitors. Low voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, these devices are well suited in power supplies for various automotive applications.

TYPICAL REGULATOR STABILITY

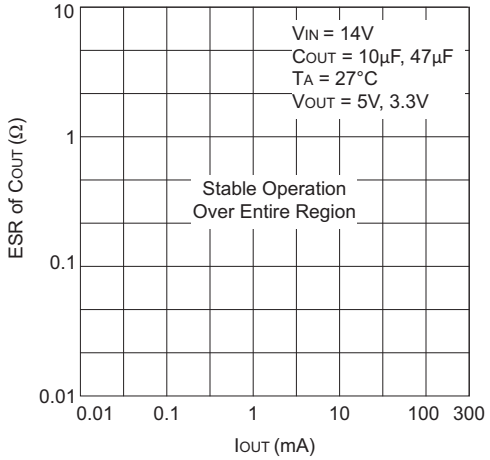

Figure 1. ESR vs Load Current for TPS7A65xx

TYPICAL APPLICATION SCHEMATIC

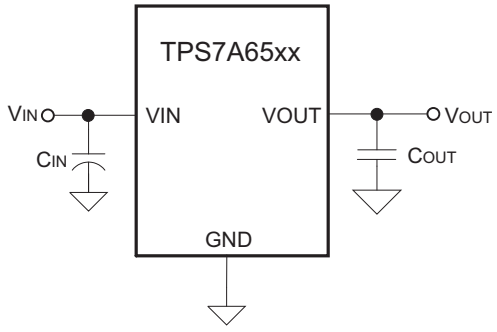

Figure 2. Application Schematic

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

OUTPUT VOLTAGE	PACKAGE		TOP-SIDE MARKING	ORDERABLE PART NUMBER(2)
5 V	3 pin KVU	Tube of 70	7A6550Q1	TPS7A6550QKVUQ1
		Reel of 2500	Product Preview	TPS7A6550QKVURQ1
3.3 V	3 pin KVU	Reel of 2500	Product Preview	TPS7A6533QKVURQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

NO.	DESCRIPTION		VALUE	UNIT
1.1	V_{IN}	Unregulated input(2)(3)	45	V
1.2	V_{OUT}	Regulated output	7	V
1.3	θ_{JP}	Thermal impedance junction to exposed pad KVU (DPAK) package	1.2	°C/W
1.4	θ_{JA}	Thermal impedance junction to ambient KVU (DPAK) package(4)	29.3	°C/W
1.5	θ_{JA}	Thermal impedance junction to ambient KVU (DPAK) package(5)	38.6	°C/W
1.6	ESD	Electrostatic discharge(6)	2	kV
1.7	T_{OP}	Operating ambient temperature	125	°C
1.8	T_S	Storage temperature range	-65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute negative voltage on these pins not to go below –0.3V.
(3) Absolute maximum voltage for duration less than 480ms.
(4) The thermal data is based on JEDEC standard high K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(5) The thermal data is based on JEDEC standard low K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(6) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

DISSIPATION RATINGS

NO.	JEDEC STANDARD	PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (°C/W)	T_A = 85°C POWER RATING (W)
2.1	JEDEC Standard PCB - low K, JESD 51-3	3 pin KVU	3.24	38.6	1.68
2.2	JEDEC Standard PCB - high K, JESD 51-5	3 pin KVU	4.27	29.3	2.22

RECOMMENDED OPERATING CONDITIONS

NO.	DESCRIPTION		MIN	MAX	UNIT
3.1	V_{IN}	Unregulated input voltage	4	40	V
3.2	T_J	Operating junction temperature range	-40	150	°C

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ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4. Input Voltage (VIN pin)							
4.1	V_{IN}	Input voltage	Fixed 5V output, I_{OUT} = 1mA	5.3		40	V
			Fixed 3.3V output, I_{OUT} = 1mA (Preview Only)	3.6		40	
4.2	$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2V to 18V, I_{OUT} = 0.01mA to 0.75mA		25	40	µA
4.3	$V_{IN-UVLO}$	Under voltage lock out voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
4.4	$V_{IN(POWERUP)}$	Power up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
5. Regulated Output Voltage (VOUT pin)							
5.1	V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3V or 5V as applicable), I_{OUT} = 10mA	-2		2	%
5.2	$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 5V			15	mV
			V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 3.3V (Preview Only)			20	mV
5.3	$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10mA to 300mA, V_{IN}= 14V, V_{OUT} = 5V			25	mV
			I_{OUT} = 10mA to 300mA,V_{IN} = 14V, V_{OUT} = 3.3V (Preview Only)			35	mV
5.4	$V_{DROPOUT}$ (1)	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 250mA			500	mV
			I_{OUT} = 150mA			300	mV
5.5	R_{SW} (2)	Switch resistance	VIN to VOUT resistance			2	Ω
5.6	I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
5.7	I_{CL}	Output current limit	V_{OUT} = 0V (VOUT pin is shorted to ground)	350		1000	mA
5.8	PSRR (2)	Power supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300mA, frequency = 100 Hz, V_{OUT} = 5V and V_{OUT} = 3.3V (Preview Only)		60		dB
			$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300mA, frequency = 150 kHz, V_{OUT} = 5V and V_{OUT} = 3.3V (Preview Only)		30		
6. Operating Temperature Range							
6.1	T_J	Operating junction temperature		-40		150	ºC
6.2	$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
6.3	T_{HYST}	Thermal shutdown hysteresis			10		ºC

(1) This test is done with V_{OUT} in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} (3.3 V or 5.0 V) drops by 100 mV at specified loads.
(2) Specified by design – not tested

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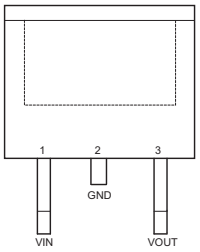
DEVICE INFORMATION

KVU PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NO.	NAME	TYPE	DESCRIPTION
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	GND	I/O	Ground pin: This is signal ground pin of the IC.
3	VOUT	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3V or 5V, as applicable) pin with a limitation on maximum output current. In order to achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and GND pin.

FUNCTIONAL BLOCK DIAGRAM

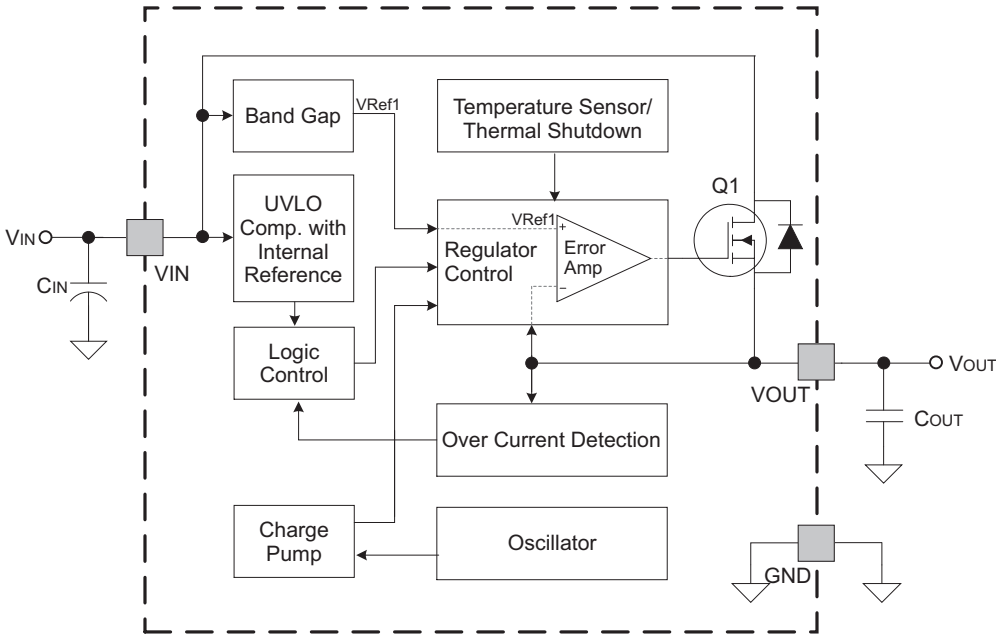


Figure 3. TPS7A65xx Functional Block Diagram

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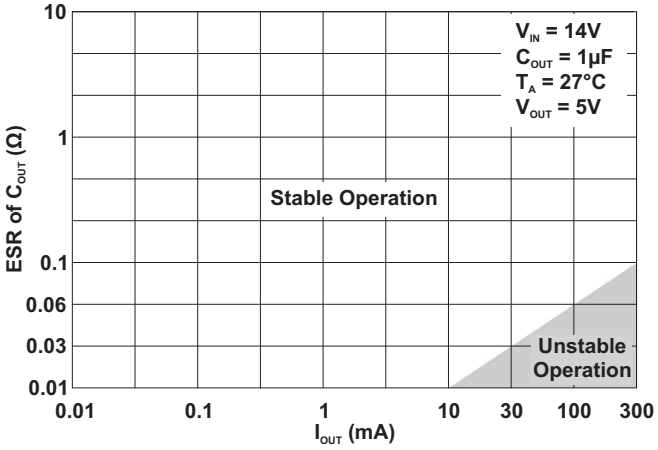
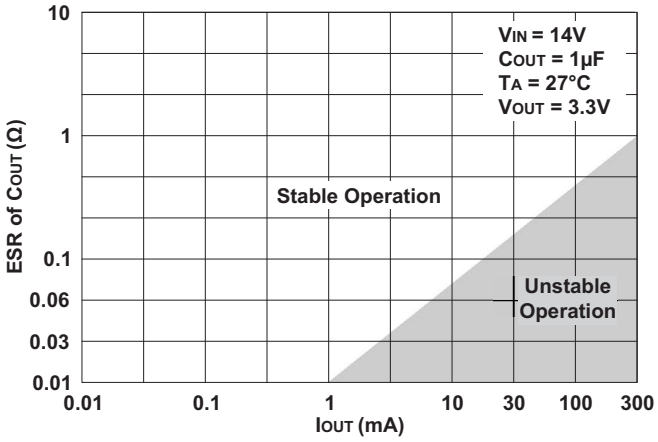
TYPICAL CHARACTERISTICS

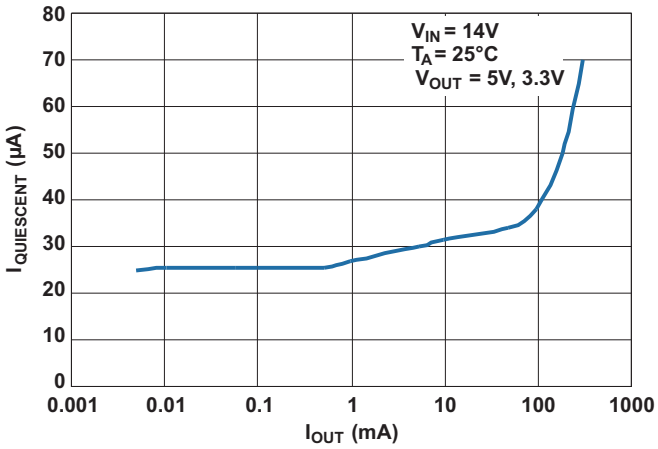
ESR vs LOAD CURRENT



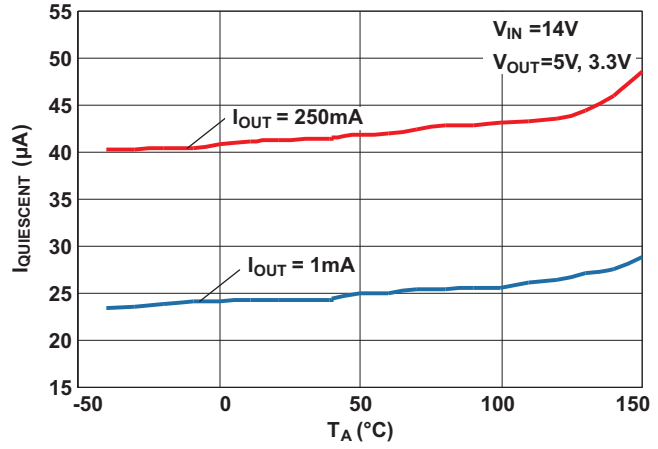
ESR vs LOAD CURRENT



QUIESCENT CURRENT vs LOAD CURRENT



QUIESCENT CURRENT vs AMBIENT AIR TEMPERATURE



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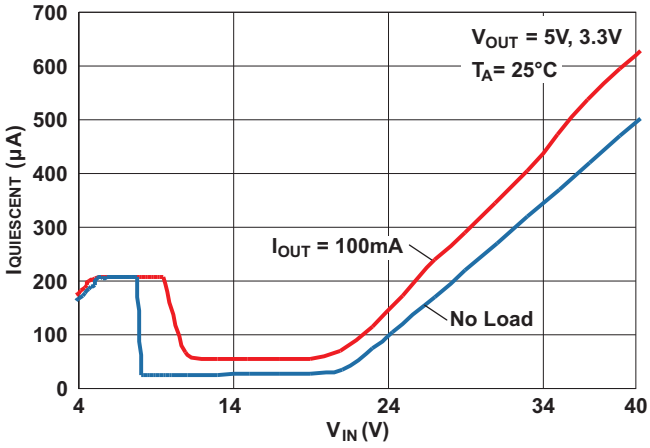
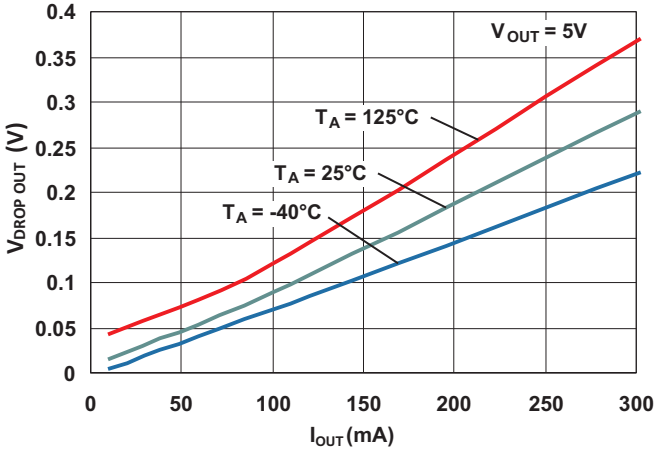
TYPICAL CHARACTERISTICS (continued)

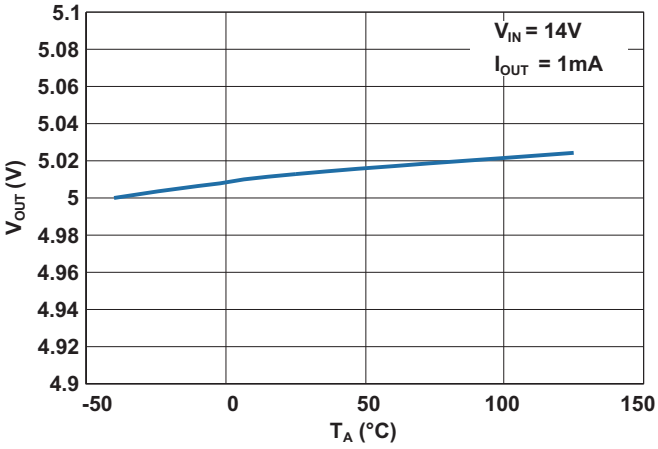
QUIESCENT CURRENT vs INPUT VOLTAGE



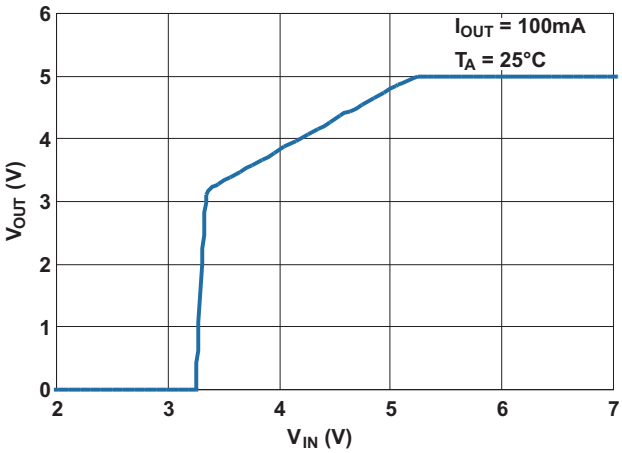
DROP OUT VOLTAGE(1) vs LOAD CURRENT



OUTPUT VOLTAGE vs AMBIENT AIR TEMPERATURE



OUTPUT VOLTAGE vs INPUT VOLTAGE



(1) Drop out voltage is measured when the output voltage drops by 100mV from the regulated output voltage level. (For example, the drop out voltage for TPS7A6550 is measured when the output voltage drops down to 4.9V from 5V.)

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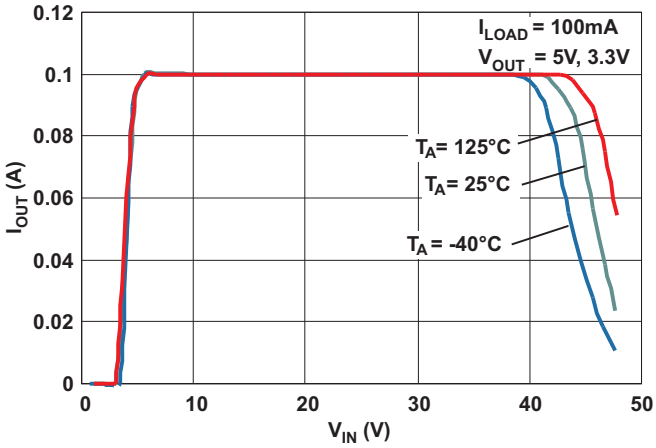
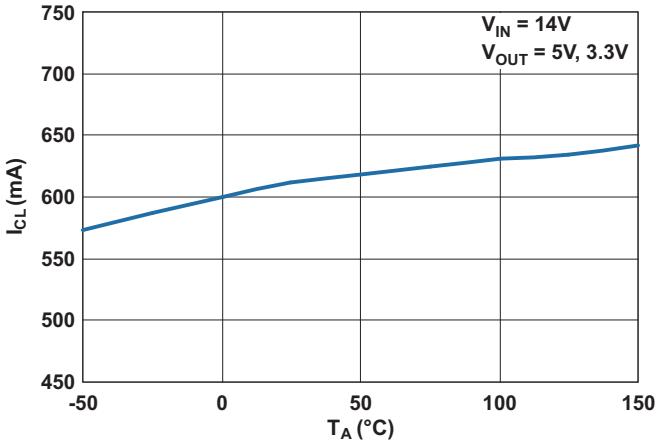
TYPICAL CHARACTERISTICS (continued)

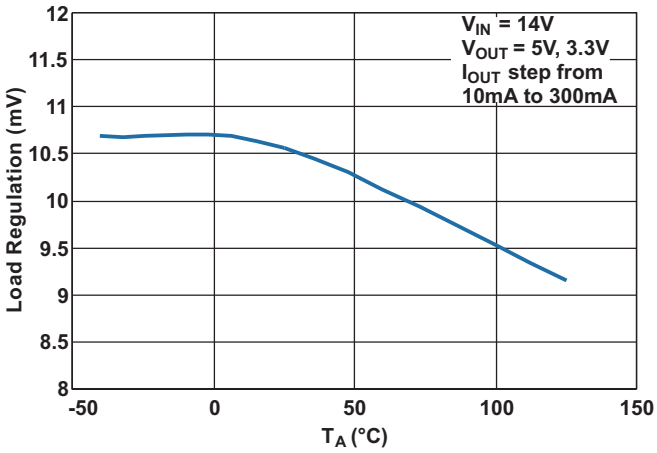
OUTPUT CURRENT vs INPUT VOLTAGE



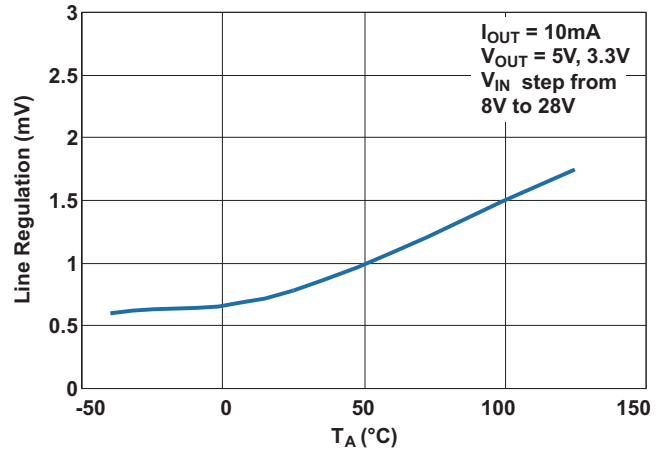
OUTPUT CURRENT LIMIT vs AMBIENT AIR TEMPERATURE



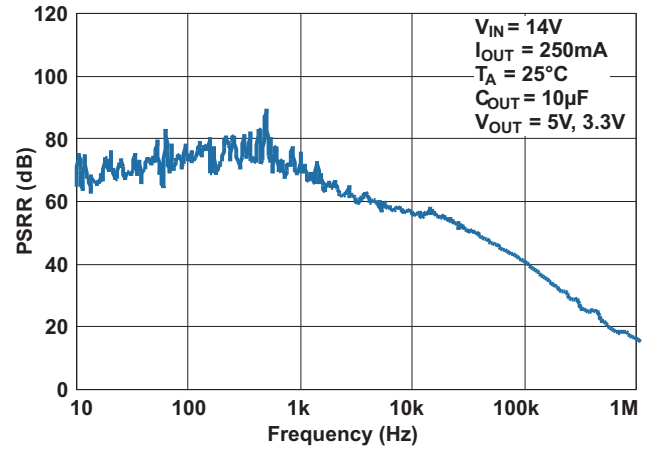
LOAD REGULATION vs AMBIENT AIR TEMPERATURE



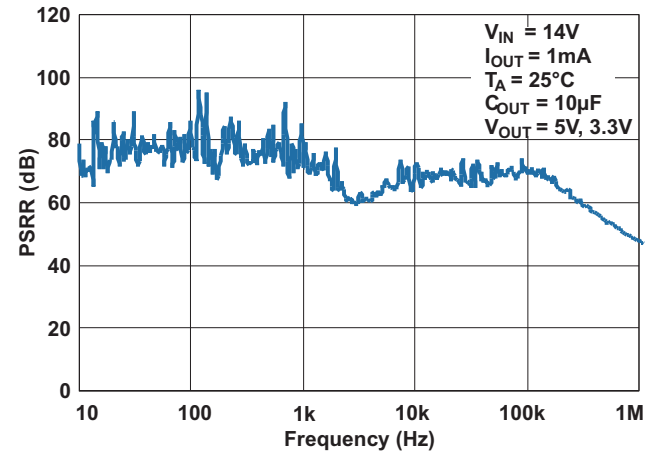
LINE REGULATION vs AMBIENT AIR TEMPERATURE



PSRR AT HEAVY LOAD CURRENT



PSRR AT LIGHT LOAD CURRENT



Note: Graphs shown in 'Typical Characteristics' section for unreleased devices are for preview only.

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DETAILED DESCRIPTION

TPS7A65xx is a series of monolithic low dropout linear voltage regulators designed for low power consumption and quiescent current less than 25µA in light load applications. Because of an integrated fault protection, these devices are well suited in power supplies for various automotive applications.

These devices are available in two fixed output voltage versions as follows:

- 5V Output version (TPS7A6550)
- 3.3V Output version (TPS7A6533)

The following section describes the features of TPS7A65xx voltage regulators in detail.

Power Up

During power up, the regulator incorporates a protection scheme to limit the current through pass element and output capacitor. When the input voltage exceeds a certain threshold ($V_{IN(POWERUP)}$) level, the output voltage begins to ramp up as shown in Figure 4.

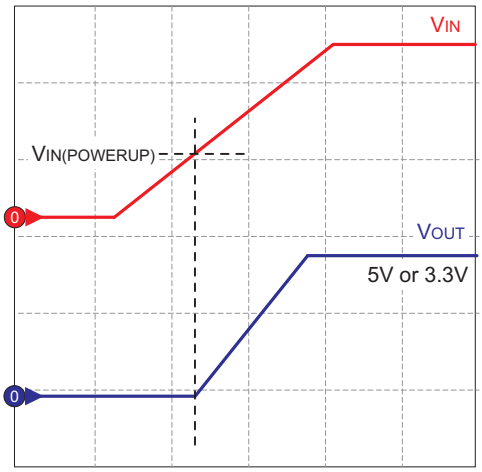

Figure 4. Power Up Sequence

Charge Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry shall not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. Figure 5 and Figure 6 shows typical switching thresholds for the charge pump at light (I_{OUT} < ~2mA) and heavy (I_{OUT} > ~2mA) loads respectively.

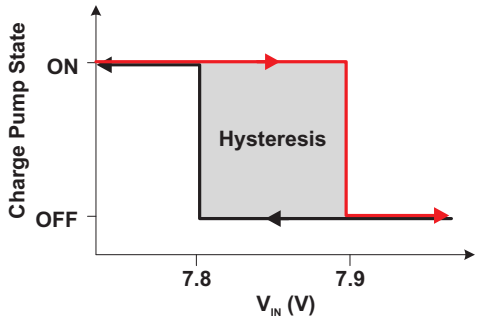

Figure 5. Charge Pump Operation at Light Loads

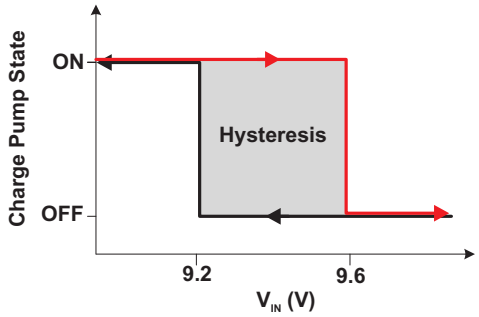

Figure 6. Charge Pump Operation at Heavy Loads

Low Power Mode

At light loads and high input voltages (V_{IN}>~8V such that charge pump is off) the device operates in Low Power Mode and the quiescent current consumption is reduced to 25µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < ~2mA (Light load)	250 µA	25 µA (Low Power Mode)
I_{OUT} > ~2mA (Heavy load)	280 µA	70 µA

Under Voltage Shutdown

These devices have an integrated under voltage lock out (UVLO) circuit to shutdown the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$) as shown in Figure 7. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will normally power up when the input voltage exceeds $V_{IN(POWERUP)}$ threshold.

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Low Voltage Tracking

At low input voltages the regulator drops out of regulation, the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}) as shown in Figure 7. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions.

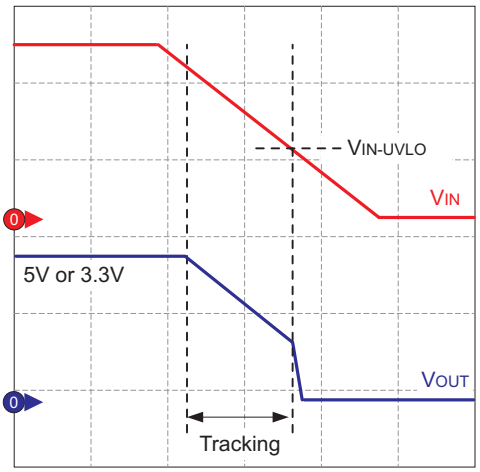

Figure 7. Under Voltage Shutdown and Low Voltage Tracking

Integrated Fault Protection

These devices feature an integrated fault protection to make them ideal for use in automotive applications. In order to keep them in safe area of operation during certain fault conditions, internal current limit protection and current limit fold back are used to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short circuit condition on the output; current through the pass element is limited to I_{CL} to protect the device from excessive power dissipation.

Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed TSD trip point. If the junction temperature exceeds TSD trip point, the output is turned off. When the junction temperature falls below TSD trip point, the output is turned on again. This is shown in Figure 8.

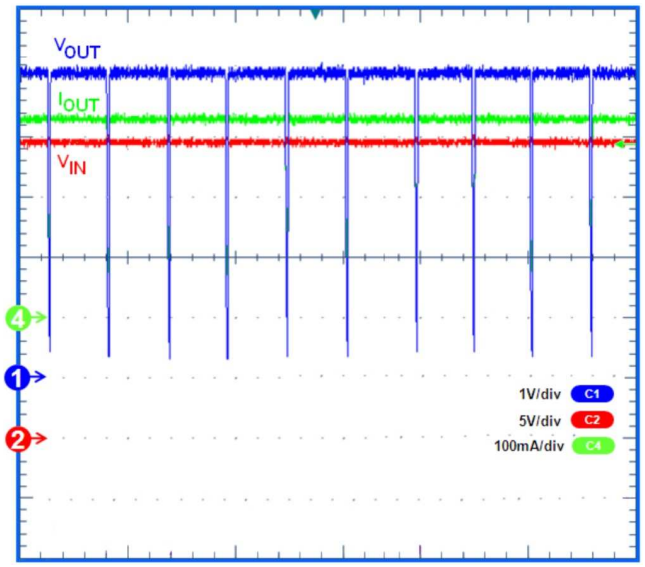

Figure 8. Thermal Cycling Waveform for TPS7A6550 (V_{IN} = 24 V, I_{OUT} = 300 mA, V_{OUT} = 5 V)

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APPLICATION INFORMATION

Typical application circuit for TPS7A65xx is shown in Figure 9. Depending upon an end application, different values of external components may be used. A larger output capacitor may be required during fast load steps to prevent output from temporarily dropping down. A low ESR ceramic capacitor with dielectric of type X5R or X7R is recommended. Additionally, a bypass capacitor can be connected at the output to decouple high frequency noise as per the end application.

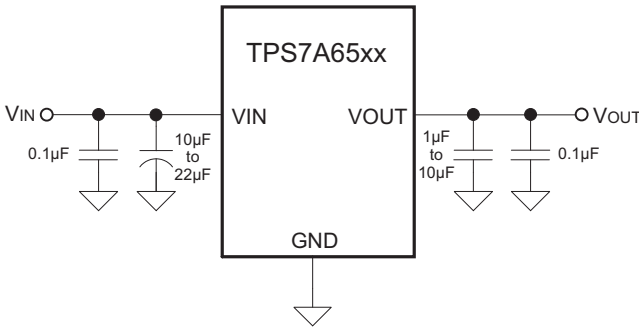

Figure 9. Typical Application Schematic

Power Dissipation and Thermal Considerations

Power dissipated in the device can be calculated using Equation 1.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN} \quad (1)$$

Where,

P_D = continuous power dissipation
I_{OUT} = output current
V_{IN} = input voltage
V_{OUT} = output voltage
$I_{QUIESCENT}$ = quiescent current

As $I_{QUIESCENT}$ << I_{OUT}, therefore, the term $I_{QUIESCENT} \times V_{IN}$ in Equation 1 can be ignored.

For device under operation at a given ambient air temperature (T_A), the junction temperature (T_J) can be calculated using Equation 2.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (2)$$

Where,

θ_{JA} = junction to ambient air thermal impedance

The rise in junction temperature due to power dissipation can be calculated using Equation 3.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate can be calculated using Equation 4.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (\theta_{JA} \times P_D) \quad (4)$$

Example

If I_{OUT} = 100mA, V_{OUT} = 5V, V_{IN} = 14V, $I_{QUIESCENT}$ = 250µA and θ_{JA}= 30˚C/W, the continuous power dissipated in the device is 0.9W. The rise in junction temperature due to power dissipation is 27˚C. For a maximum junction temperature of 150˚C, maximum ambient air temperature at which the device can operate is 123˚C.

For adequate heat dissipation, it is recommended to solder the power pad (exposed heat sink) to thermal land pad on the PCB. Doing this provides a heat conduction path from die to the PCB and reduces overall package thermal resistance. Power derating curves for TPS7A65xx series of devices in teh KVU(DPAK) package is shown in Figure 10.

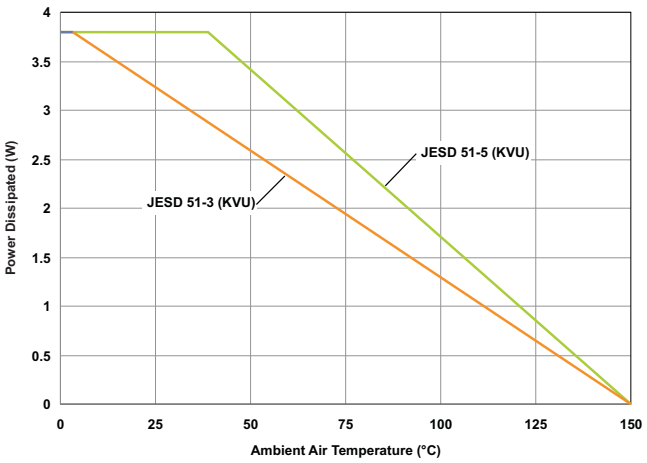

Figure 10. Power Derating Curves

For optimum thermal performance, it is recommended to use a high K PCB with thermal vias between ground plane and solder pad/ thermal land pad. This is shown in Figure 11 (a) and (b). Further, heat spreading capabilities of a PCB can be considerably improved by using a thicker ground plane and a thermal land pad with a larger surface area.

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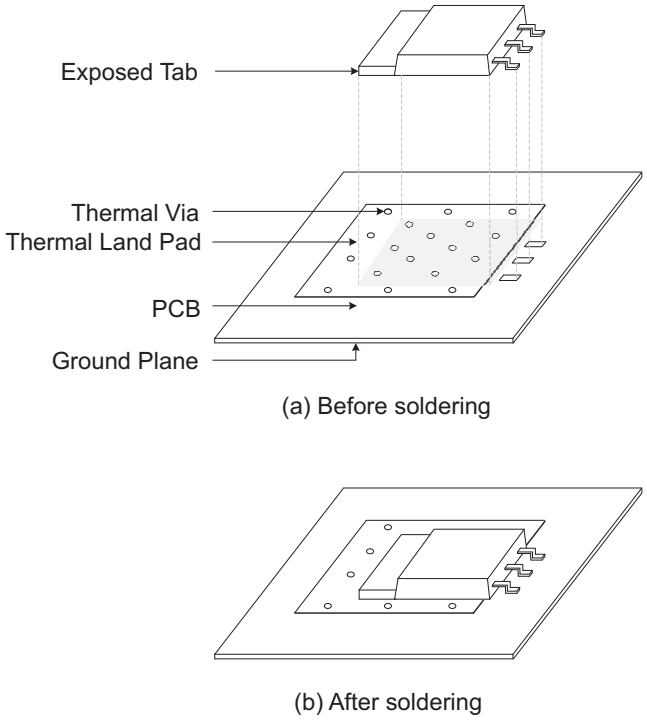

Figure 11. Using Multilayer PCB and Thermal Vias For Adequate Heat Dissipation

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 12 shows variation of θ_{JA} with surface area of the thermal land pad (soldered to the exposed pad) for the KVU package.

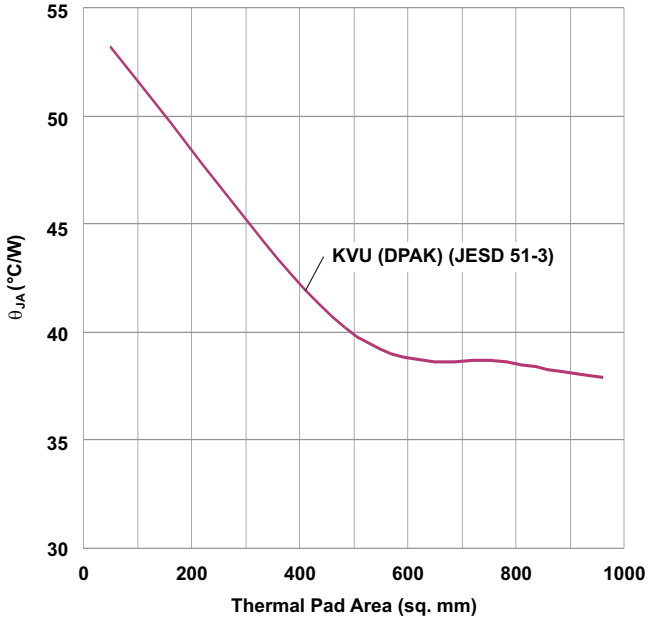

Figure 12. θ_{JA} vs Thermal Pad Area

REVISION HISTORY

Changes from Original (May 2010) to Revision A	Page
• Removed all KKT information.	2

Changes from Revision A (November 2011) to Revision B	Page
• Changed the θ_{JP} value in the Abs Max Table From: 12.7 To: 1.2°C/W	2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6533QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7A6533Q1	Samples
TPS7A6550QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7A6550Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION

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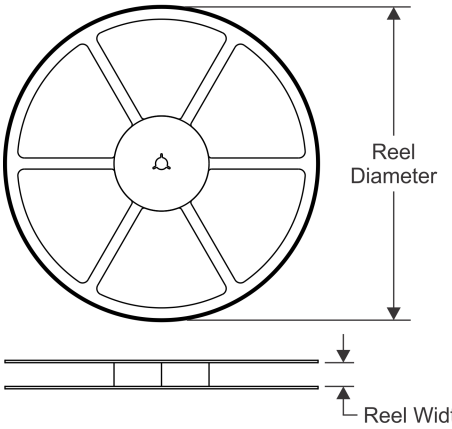
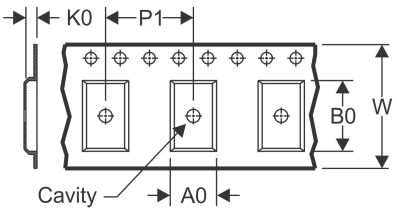
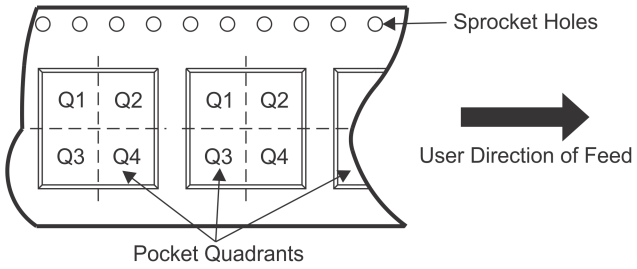


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

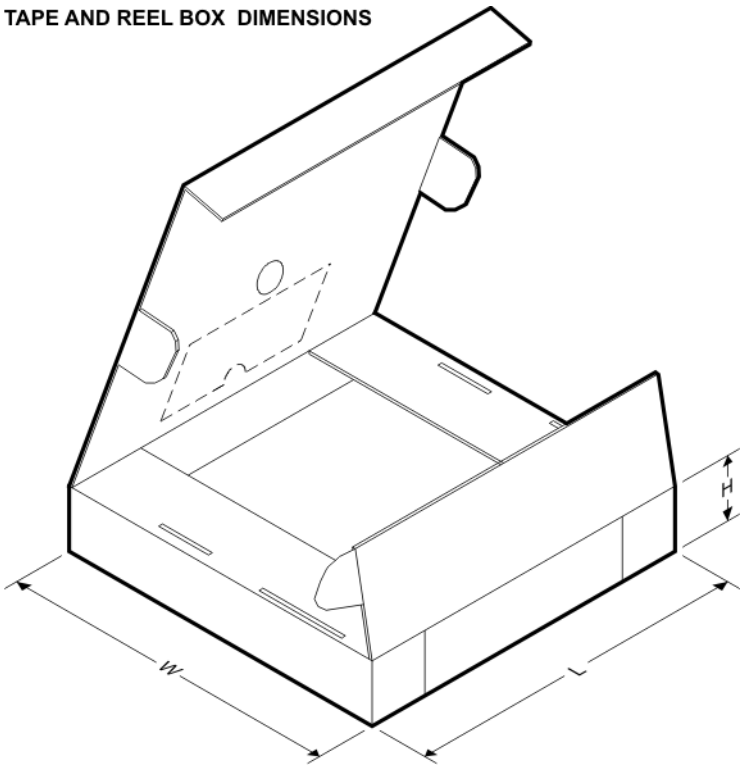
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

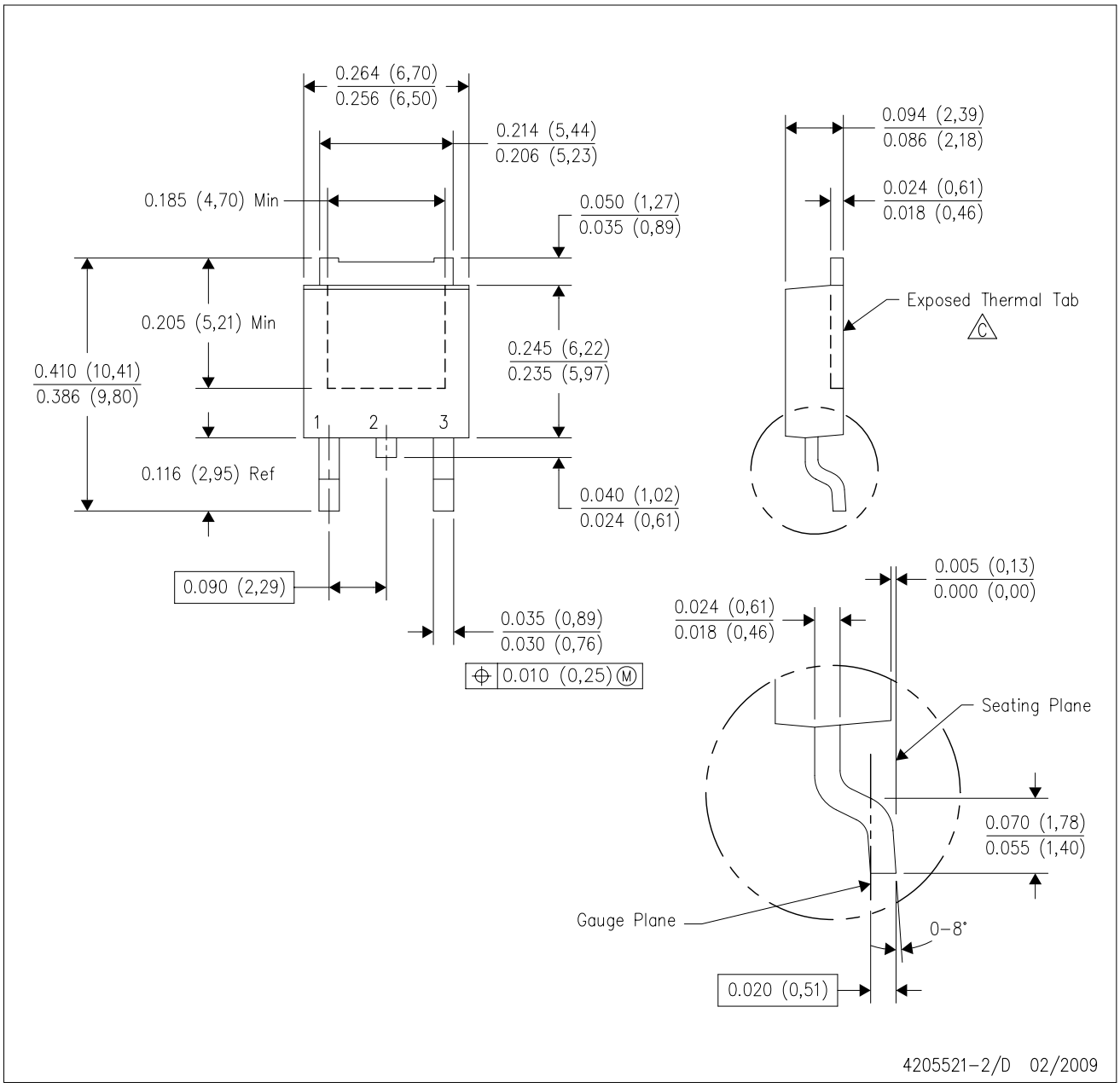
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

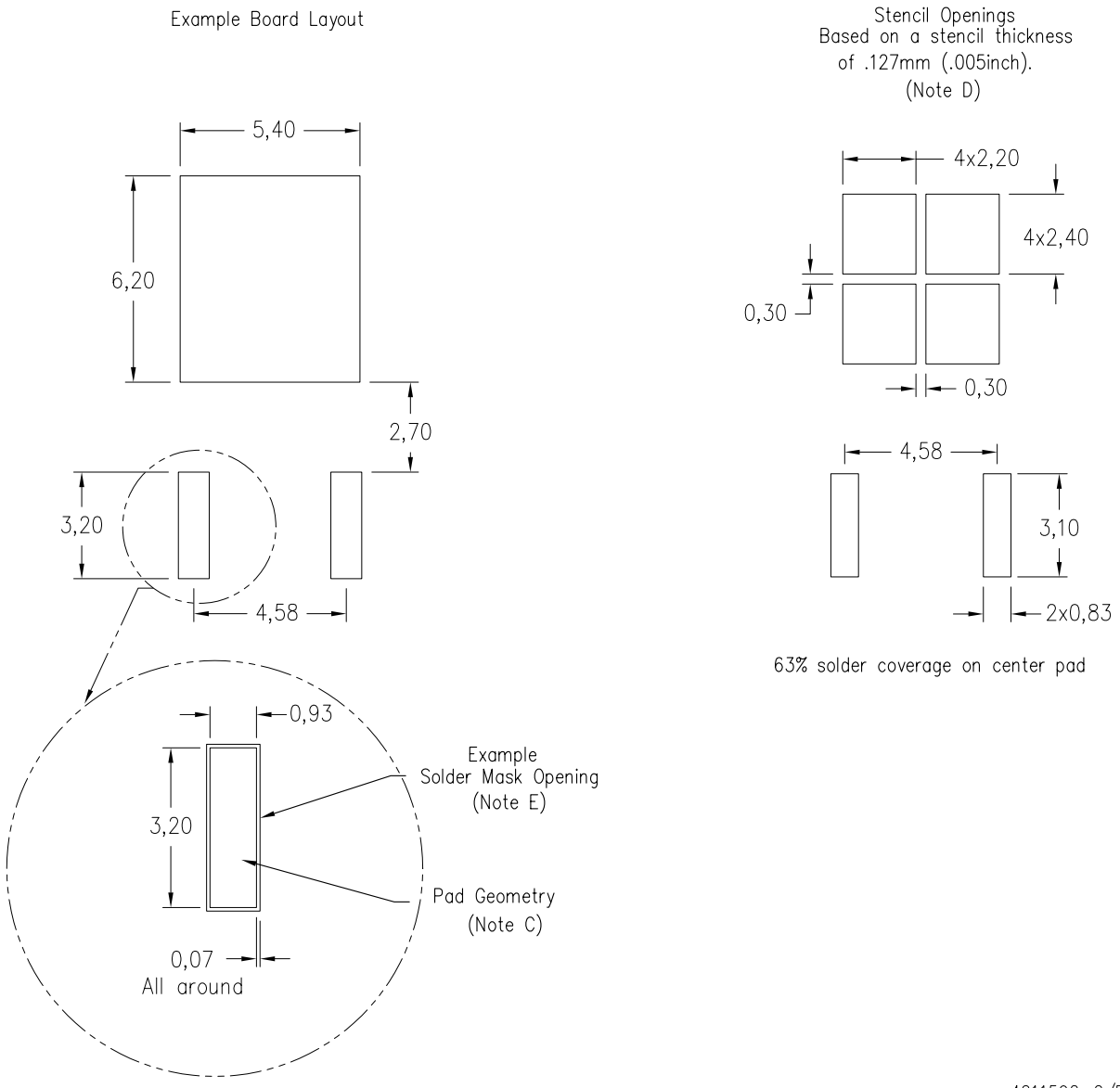
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0

KVU (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AA.

KVU (R–PSFM–G3) PLASTIC FLANGE MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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